Best Practices for Improving the PCB Supply Chain: Performing the Process Audit

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ABSTRACT
In the electronics industry, the quality and reliability of any product is highly dependent upon the capabilities of the manufacturing suppliers. Manufacturing defects are one of the top reasons why companies fail to meet warranty expectations. These problems can result in severe financial pain and eventual loss of market share. What a surprising number of engineers and managers fail to realize is that focusing on processes addresses only part of the issue. Supplier selection also plays a critical role in the success or failure of the final product.

Designing printed circuit boards today is more difficult than ever before due to significantly increased density, higher lead free processing temperatures and the associated changes required in manufacturing. The entire supply chain has also been impacted by requirements regarding the use of hazardous materials and recycling. The RoHS and REACH directives have caused suppliers throughout the industry to change both their materials and processes. So, everyone designing or producing electronics has been affected even if they've been part of categories designated as directive exempt.

Printed Circuit Boards (PCBs) should always be considered a critical commodity. Without stringent controls in place for PCB supplier selection, qualification, and management, long term product quality and reliability is neither achievable nor sustainable. This paper builds on the Part I paper and further expands it with auditing recommendations and case studies of defects [1].

Key Words: PCB, supply chain, PCB audit, PCB defects, PCB reliability, PCB fabrication

INTRODUCTION
A key recommendation from the initial paper concerned the need for an onsite audit of PCB suppliers. This recommendation arises due to the fact that there is no industry standard methodology for qualifying PCB suppliers. Standards do exist for lot-based PCB testing and acceptance within the IPC 6010 series but sourcing follows the "as agreed upon between user and supplier" (AABUS) approach. The IPC began discussing this gap in 2008 with a Blue Ribbon Committee but the effort has not yet resulted in a standard [2]. IPC has recently launched a Validation Business Unit with plans to eventually move towards an IPC Qualified Manufacturers List (QML) for suppliers, including PCBs [3]. In the meantime, however, onsite audits remain the best approach.

For an audit to be successful, it must be performed by people knowledgeable in the processes involved in fabricating a PCB. There more than 180 individual steps required in manufacturing a typical printed circuit board. The processes are complex, chemistry-intensive, and require tight process controls to guarantee acceptable results.

An audit encompasses all levels and types of PCB fabrication, from generic, multilayer rigid boards to complex rigid-flex configurations. Audits can be performed to assess the viability of a new supplier, to assure supplier compliance with customer requirements, or to resolve a problem that has resulted in product failure. Prior to performing an audit, the information outlined in the Part I article should be requested and reviewed. A formal report documenting the audit scope, contents, and results should be generated for all audits. The audit report should also identify the individuals who participated in the audit. As mentioned before, it is vital that people with process knowledge perform the audit. If a company lacks appropriate resources, they can partner with companies that provide PCB audit experts as a service.

MATERIALS & PROCESS AUDIT
This section provides insight into assessment of the process operations observed during a typical audit of a PCB fabrication facility.

Planning Engineering
The initial step in most PCB fabrication facility processes involves the Planning Engineering function. This is where an engineer verifies the customer data, the Quality Assurance codes, specifications, and any other special requirements. Commonly references industry standards include:

- IPC-1710 Printed Board Manufacturer's Qualification Profile
- IPC-2221 Generic Standard on Printed Board Design
- IPC-2222 Sectional Standard on Rigid Organic Printed Boards
- IPC-6011 Generic Performance Specification for Printed Boards
- IPC-6012 Qualification and Performance Specification for Rigid PCBs
- IPC-A-600 Acceptability of Printed Boards
- IPC-9151 Printed Board Process, Capability, Quality, and Relative Reliability Benchmark

There are numerous other IPC and industry standards available for both processes and test methods. If IPC standards are used, the customer must also specify the appropriate class. The IPC classes are defined as follows:

- Class 1 General Electronic Products (consumer products)
- Class 2 Dedicated Service Products (uninterrupted service is desired)
- Class 3 High Reliability (continued performance or performance on demand is critical)

The Planning Engineer normally constructs the in-house traveler and identifies the materials to be used for fabrication, the stackup needed to meet electrical requirements, and any impedance controls. Then, the lay-up sheet identifying the copper weights per layer, core thickness, and the laminate type is created. In addition, a net-list verification and review of the customer statement of work (SOW), Engineering Change Notices (ECNs), IPC-6012 requirements, panel size, and special codes are performed. If required, the Planning Engineer also incorporates highly accelerated thermal shock (HATS), interconnect stress test (IST) or other test coupons into the lay-up. Finally, Planning Engineering's work initiates the computer aided manufacturing/design (CAM/CAD) and Document Control activities. Verification of all of these functions occurs in the first stage a detailed audit.

CAM/CAD

The CAM activity usually establishes a customer part number and drawing for the project, creates a job number, links the input data from the customer, sets up the layers using internal naming structures, and performs any edits needed to match internal processes with the customer supplied data. CAM also checks the customer supplied data against the drill files and sets the lines and spaces necessary for each layer. A Design for Manufacturability (DFM) review and Design Rule Check (DRC) of gerber data for functional integrity and manufacturability are performed. Finally, the CAM operation generates a panelized layout for the project including the inclusion of specified test coupons. All of these actions must be verified during an audit.

Documentation and Configuration Control

Documentation packages are then prepared for each production run and are maintained for a defined period of time, typically 5 years, unless the customer requires a different retention period. All Standard Operating Procedures (SOPs) should be readily available for review in this area.

Certification & Training

An auditor should verify the internal certification and training programs in place for employees to ensure that they are all qualified to manufacture the customer's products to the appropriate specifications.

Change Management

The audit should also determine how changes in equipment, processes and materials are implemented, documented, and communicated, both internally and externally. Even supposedly "minor" changes can have a substantial impact on fabrication process results.

FABRICATION FLOW

The following sections describe a typical PCB fabrication flow and recommended assessment approach.

Incoming Receiving

The audit should check that the materials received are verified against the list of materials called out for in the project. Thickness of the cores, copper weight, laminate material, and layer identification are ascertained at this operation. Verify that the materials selected meet the procurement requirements by picking a random lot for assessment.

How prepreg is handled and transferred is a critical operation. Prepreg should be stored in a temperature and humidity controlled area at <23C and < 50% RH. Prepreg should not be folded and any opened packages should be resealed. If the storage temperature is significantly below room temperature, the prepreg should be allowed to acclimate to ambient conditions prior to use. Prepreg should only be handled by the edges and with gloves. Typically, prepreg should be moved into the fabrication process on a first in first out (FIFO) basis to properly control storage times. IPC 1601: Printed Board Handling and Storage Guidelines documents best handling practices throughout fabrication.

Inner Layer Processes

In the inner layer imaging process, the PCB laminate is coated with photoresist, a photosensitive polymer dry film material, and a positive image is transferred to it. In dry film development, imaged panels are placed in a conveyorized chamber of potassium carbonate and the unexposed dry film resist is chemically removed. This process results in a pattern formed in the resist on top of the copper surface (a positive image). Next, the developed internal layer panels are placed in a copper etchant chamber. In the developing process, the exposed copper is removed from the panel. The dry film resist covering or protecting the circuitry pattern is then stripped off.

The auditor should examine how the cores are cleaned and how the wet laboratory monitors samples. All processes analyzed should have process controls in place, checks for verification, planned maintenance, and calibration controls that are defined by the panel size.

Photo tool storage temperature and humidity levels should also be evaluated. The tools should be used and stored under conditions similar to the actual manufacturing conditions used to make them. The tools are moisture sensitive and grow or shrink due to changes in the storage condtions.

Next, audit the imaging process used to produce the artwork and the process used to perform the exposure operation to ensure that the set up and artwork match the panel structure.

Inner Layer Automated Optical Inspection (AOI) and Visual Inspection

The audit must examine the automated optical inspection (AOI) tools used and how they are linked to the CAD data. The AOI equipment is programmed using the gerber/CAD data to inspect the etched copper panels. Every panel is placed in the machine and inspected for defects as small as .001" in diameter. All identified defect locations are verified by operators using visual inspection under magnification.

Some type of data collection must be used to record defects found during the inspection of line widths and spacings that are listed on the traveler. All data should be recorded including information on the type of defect and its location.

Layer inspection is audited next. This should include the method used to monitor the materials being transferred into the operation. Good PCB fabricators perform transfers via an airlock to minimize oxidation.

Inner Layer Preparation

The bond film operation is next in the process and is usually fully automated. If necessary, the materials being prepared for lamination are baked and information is logged into a data collection system. Sets of lay-up materials are generated and are presented to the lamination presses as completed stackups or "books."

In lamination, the etched and inspected internal layers are sequenced and registered on large steel plates. Prepreg or B-stage material consisting of fiberglass and a semi-cured resin system is placed between the etched layers. The plates are then inserted into a heated press to bond the layers.

The process engineer establishes the recipes for the presses by linking the parameters to the specific job number. The engineer selects the correct recipe and logs it for verification purposes. A controller monitors the temperature, pressure and vacuum values to specified levels.

The laminated boards then go through a cleaning operation to remove excess material from the edges. The thickness of the stackup is verified using a laser thickness measurement system. All data should be recorded.

Next, each panel is typically serialized. Test coupons are cut out for microsectioning to confirm that inner copper layers are in the correct sequence and that the correct layers of pre-preg have been used.

If everything has been processed to specification, the process engineer gives the approval for the stackups to proceed to the drilling operation.

Drilling

Prior to the drilling operation, the stackups are X-ray inspected to set fiducials to estimate the center point for setting the tooling holes. Drilling is normally accomplished using automated drilling systems. The number of drill hits should be monitored through a drill list that defines replacement requirements based on size and speed. Drill bits are wearout items and need to be replaced per the directions on the traveler or specifications.

An X-ray inspection system performs reference detection and measurement of the drill coordinates. It also calculates the optimized drill location and determines compensation factors for tooling holes.

The laminated panels are registered to the drill machine. A drill program extracted from the gerber data is uploaded to the drill controller. Drill bits are automatically selected and the panels are drilled at the programmed locations.

X-ray inspection is again performed to verify the accuracy of internal layer alignment and to verify proper hole-pad positioning.

Hole Preparation and Hole Metallization

Hole preparation to accomplish deburring can be performed via several methods including a brushing technique or a plasma cleaning operation. The audit should verify that all holes are completely clear of debris. Desmear removes resin and drilling debris from the hole wall. Etchback is a controlled removal of resin to a specific depth in order to expose additional internal layer

connection surfaces. Etchback is typically used in high reliability applications.

Cross-sections are performed to verify numerous parameters including hole wall quality, desmear or etchback, plating thickness, and dielectrics. Physical cross sections of finished product or digital images are supplied to the customer per their specification. Ideally, each customer should discuss and specify desired cross-section locations and sampling plans. Many organizations understandably focus on the most challenging structures but lose sight of the variation that occurs across the diagonal of a panel or across varying hole sizes.

Copper Plating, External Layer Imaging & Developing

The electroless plating process deposits a thin layer of copper from an autocatalytic plating solution without the application of electrical current.

Audit all of the electroless processing tanks in the production area. At the control console, the operator should select from a list of materials and cycle times for each project and enter that data into a log to confirm correct selection.

The process engineer should be the only person who can change a recipe. Operators should only be able to select a recipe from the menu on the control computer. The sole action required by the operator at this point is to load and unload the panels since all other functions are typically automated. Figure 1 shows an example of plating process equipment.

Figure 1 Plating Process

At external layer imaging, the drilled panels are coated with photoresist and a negative image is transferred onto the dry film surface. The exposed panels are placed in the developer and the unexposed dry film resist is removed. The result is a pattern of exposed copper. This negative image is then ready for copper plating. Additional copper is added to the foil circuit pattern and drilled holes by an electrolytic copper plating process. A tank is electrically charged with current to activate the electroplate process. The copper plating line also includes several cleaning/etching baths, rinses and acid copper baths. All must be continuously controlled and monitored.

Copper Plating and Analysis

PCB fabricators have several pattern plate processes that can be utilized. They include:

- Nickel only
- Fused Sn/Pb
- Hot air solder leveling (HASL)
- Electroless Nickel / Immersion Gold (ENIG)
- Electroless Nickel / Electroless Palladium/ Immersion Gold (ENEPIG)
- Nickel with hard or soft gold

All process parameters for each of these variations should be monitored. TrueChem[1] software is highly recommended for this purpose.

Resist Strip, Outer Layer Etch, Tin Strip

The plasma etching process for etchback or desmear is the next process operation. The operator should log the film type, the exposure level, the age of the bath and the chart for day/day settings. To maintain control, etching is normally based on the starting copper weight versus the speed of the process. It is also at this point in the process that controlled impedances in the board are tested and verified.

The plated panels are removed from the copper bath and placed in a tin plate bath temporarily covering the copper circuitry and creating an etch resist. The dry film is stripped and the exposed copper is removed by the etching chemistry. The tin plate is chemically stripped. The etched external layers are laser inspected using AOI. All defective areas on the panel surface are then operator-inspected under magnification prior to solder mask coating. After these processes are complete, copper thickness and hole sizes are verified and the panels receive a 100% visual inspection. Figure 2 show an example of a cross section for a plated through hole (PTH).

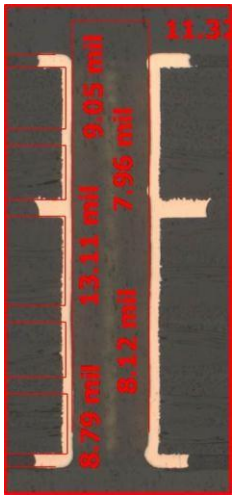

Figure 2 Plated Through Hole Cross-section

Solder Mask Processes
Resist is typically applied in a clean room environment per the requirements of the traveler which should also specify hold time and laminate type. This material is then photo-processed. The operator selects the resist height and logs the data into the collection system or tally sheet and shop order. A Laser Direct Imaging (LDI) process for this function is recommended.

Most soldermask processes use a Liquid Photo Imageable (LPI) material, with a 100% inspection of the images after processing. Dry or wet mask processes, if used, should also be audited. In LPI soldermask processing, the panel surface is coated with a polymer and partially cured. The soldermask image is applied to the panel. The unexposed solder mask is then removed in a developer. This exposes the holes and surface mount pads.

Legend/Silk Screening
The Legend/Silk Screening application is another highly automated process. The material must be properly applied and cured. A first article inspection is performed here to ensure complete, correct marking including date code and serial number. Legend ink should not cover solderable surfaces. Verifying controls for these processes is part of the audit.

Final Finish
Commonly available final surface finishes for PCBs include hot air solder level (HASL or Lead-Free HASL), ENIG, ENEPIG, Immersion Silver, and organic solderability preservatives, (OSP).

The surface finish influences the process yield, the amount of rework, field failure rate, the ability to test, the scrap rate, and the cost of a PCB.

The selection of a surface finish should be done with a holistic approach that considers all important aspects of the assembly. Companies can be lead astray by selecting the lowest cost surface finish only to find that the eventual total cost is much higher.

All process and highly accelerated thermal shock (HATS) or interconnect stress test (IST) coupons are removed after this operation and are sent to a cross-section laboratory for analysis or chambers for further testing.

PCB Cleanliness
Contamination is believed to be one of the primary drivers of field issues in electronics today. It induces corrosion and electrochemical migration (ECM). Several industry trends have converged to drive an increased risk of contamination failures. Decreased spacing of the components and circuitry used in electronics increases the impact from any contamination. The increased heat load per unit volume also drives higher air flow, which brings more particulates and gasses into contact with electronics. This has resulted in increased corrosion rates seen in the industry. In order to minimize this risk, PCBs must exit the fabrication processes as clean as possible. Cleanliness levels must be carefully measured and monitored.

Unpopulated PCB cleanliness guidelines and standards are available from IPC. They include:

- IPC-5701: Users Guide for Cleanliness of Unpopulated Printed Boards
- IPC-5702: Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards
- IPC-5703: Guidelines for Printed Board Fabricators in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards
- IPC-5704: Cleanliness Requirements for Unpopulated Printed Boards

Verify that the latest cleanliness standards are in use at the facility.

Ion Chromatography (IC) is the ‘gold standard’ method for measuring ionic cleanliness but very few PCB manufacturers qualify lots based on IC results. Most facilities use IC to baseline Resistivity of Solvent Extract (ROSE), Omegameter, or Ionograph (R/O/I) results. The recommended best practice is to perform lot qualification with R/O/I and periodically recalibrate with IC at some specified interval (every week, month, or quarter).

Electrical Testing
Flying probe and fixture or bed of nails probe testing are basic elements of PCB testing. Electrical measurements can be made at different levels using a sampling plan.

At electrical test, a test netlist, usually per IPC-D-356, is uploaded into the tester. Each board is placed on the tester and electrically tested for continuity and resistance. How tested PCBs are handled and segregated at test is critical. Due to the manual loading nature of the testing process, it can be easy to accidentally co-mingle passed and failed PCBs. Look closely at how tested material is identified and segregated. Auditors should also validate how the procedures for test yield are monitored and how aberrant or low yielding lots are handled.

Final Inspection and End Item Data Package
Certified inspectors should perform the final inspections of the circuit boards using stereo-zoom microscopes. On-site training should be provided to these inspectors for any and all specifications and standards required for the PCBs manufactured at the facility.

Not all product parameters require a 100% inspection. It is vital to establish an agreed upon sampling plan that considers product complexity and reliability needs.

IPC-A- 600 Acceptability of Printed Boards is widely used for final inspection; but, customers may require other standards or custom requirements. If defects are identified, they should be marked for touch up, if allowed, and then sent to a final inspection after rework. Coupons, cross sections, and full documentation should be prepared for delivery with the completed product as required by the customer. IPC-QL-653A Certification of Facilities that Inspect/Test Printed Boards, Components and Materials may also be used to verify inspection and test areas.

At final inspection, quality control personnel visually inspect 100% of the finished product and verify the product per fabrication drawing requirements for dimensional properties, board size, finished hole sizes, and other special customer specifications. If there are discrepancies, customer specifications always take precedence over referenced industry standards.

IPC-A-600 defines three levels for each inspected characteristic. They are:

- Target: Depicts the desired condition. May not be necessary to ensure reliability.
- Acceptable: Indicates that the condition depicted, while not necessarily perfect, will maintain the integrity and reliability of the board in its service environment.
- Nonconforming: Indicates that the condition depicted may be insufficient to ensure the reliability of the board in its service environment. Considered unacceptable for at least one class of product, but may be acceptable for other classes as specified by the acceptance criteria.

Characteristics are divided into two basic groups: externally visible or internally observable. Externally visible conditions are features or imperfections which can be seen and evaluated on or from the exterior surface of the board. These characteristics are candidates for visual inspection. Internally observable conditions are features or imperfections that require cross-sectioning of the specimen for detection and evaluation.

Laboratory Analysis: Wet & Cross-Section
As mentioned before, PCB fabrication involves complex, chemistry intensive processes which require tight process controls. The laboratory must validate that bath chemistries, processes, and product results meet all specifications. Requirements can originate from the customer, industry standards, or from equipment or chemistry suppliers. All requirements should be clearly documented and continuously monitored through the use of statistical process control (SPC). One recommended software tool is TrueChem which is designed specifically to control and automate the management of chemistries, coatings, and wet processes.

IPC provides a complete, free suite of test methods under IPC-TM-650. Many of these will be used in PCB fabrication. The methods encompass the following areas:

- Section 1.0 Reporting and Measurement Analysis Methods
- Section 2.1 Visual Test Methods
- Section 2.2 Dimensional Test Methods
- Section 2.3 Chemical Test Methods
- Section 2.4 Mechanical Test Methods
- Section 2.5 Electrical Test Methods
- Section 2.6 Environmental Test Methods

Cross sections for analysis of the processes should be performed at numerous steps throughout the process. A full laboratory report should be included with the customer's deliverables. These reports should be routinely read and verified by the customer for compliance to specifications. It is not uncommon to find reports showing conformance to IPC Class 2 requirements when Class 3 requirements have been specified. The customer can also specify whether digital images or actual cross-section samples should be provided with the report.

A basic understanding of common PCB defects is helpful. This knowledge can be used by an organization to monitor supplier performance over time. The following images illustrate defects that can be seen in cross-sections or microscopy.

Figure 3 Insufficient Plating

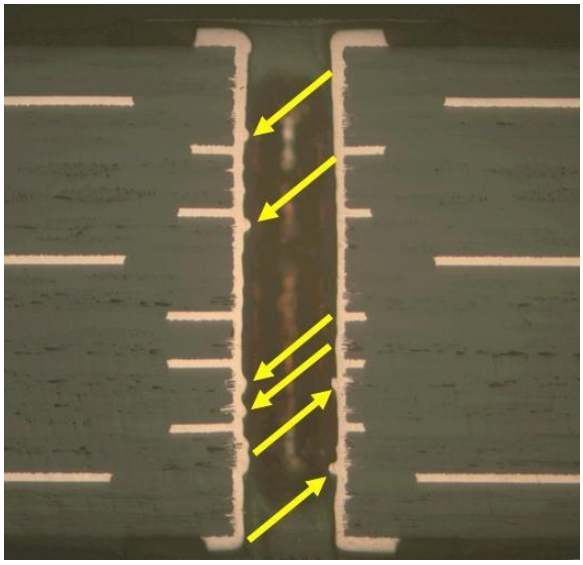

Figure 4 Plating Nodules

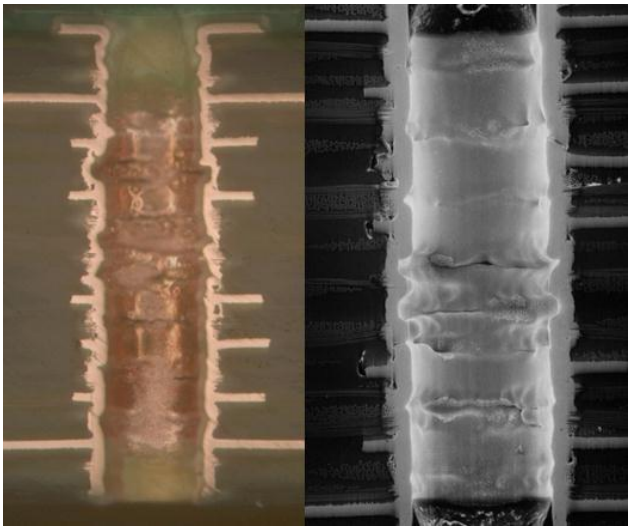

Figure 5 Plating Folds

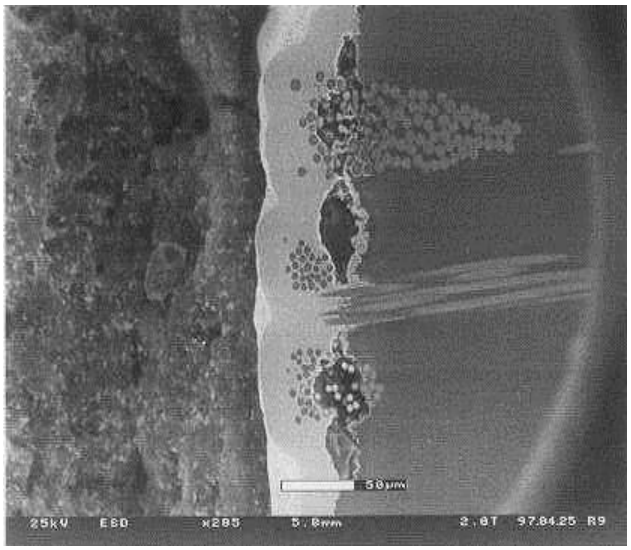

Figure 6 Plating Voids

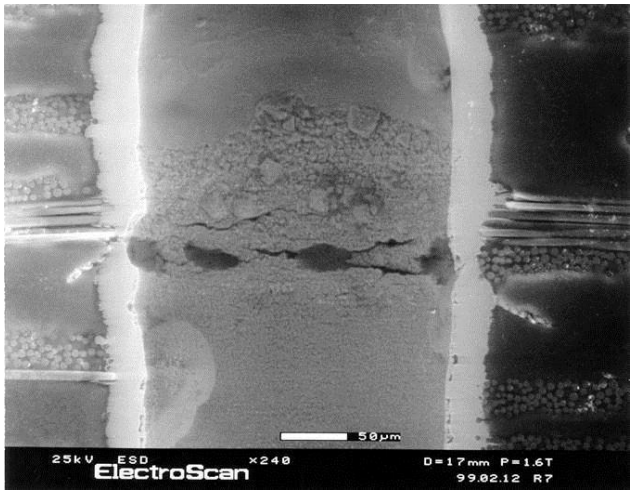

Figure 7 Etch Pits

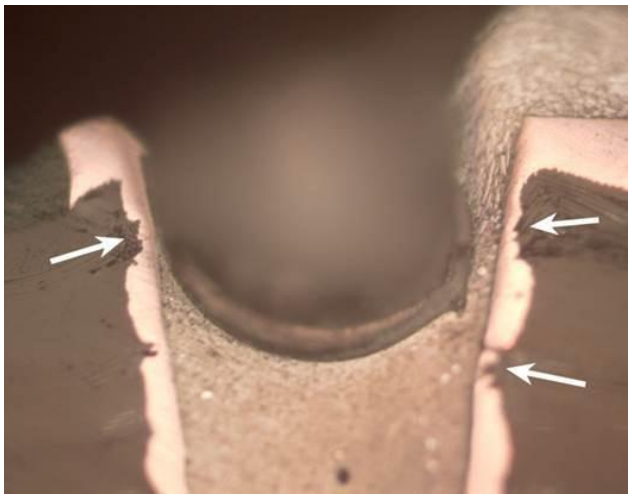

Figure 8 Glass Fiber Protrusions

Shipping

A Requirements Document should be used to summarize yield figures, start dates and date codes, along with special notes per customer requirements.

At shipping, PCBs are vacuum-sealed and packaged to ensure product integrity and to protect against moisture and contamination. Packaging should incorporate moisture barrier bags (MBB), desiccant, and humidity indicator cards (HIC). Bar codes and labels are applied per customer specifications. Certificates of Conformance, Test Certificates, RoHS Certificates, and any other customer requested documentation are provided for shipment. Transportation is usually based on customer requirements. As noted before, IPC 1601: Printed Board Handling and Storage Guidelines documents best practices.

Final Documentation Review

Audit a typical documentation package for completeness and accuracy. This stage can also be used to review and address any unique or special processes not covered elsewhere.

CONCLUSION

The audit process described addresses a typical printed circuit board fabrication process. Not all facilities have all of the operations described here. Regardless, the flow in the audit should encompass the unique processes to ensure compliance.

The foundation of a reliable product is a reliable PCB. Having a comprehensive strategy for selecting and qualifying PCB suppliers ensures that the foundation is strong. Performing effective on site audits is a critical component of that strategy.

REFERENCES

1. TrueChem Software, http://www.truelogiccompany.com/truechem/
2. McGuirk, Derek, “The Road to Qualification”, Circuitree Magazine, December 2008.
3. New Validation Services Unit Will Certify Global Suppliers, IPC Press Release, July 1, 2013.