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Keys to Successful ASIC Design: Part 2

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Introduction

There are multiple keys to having a successful ASIC design cycle. This paper will present Best Practices in design practices.

Design Implementation

Design work starts after the planning stage. A generic design implementation flow is shown in figure 2. The block specifications are determined by the architecture overview developed in the planning stage. The blocks are then entered into schematics and simulations are run to check functionality. Then the layout is completed and checked for correctness. Final simulations may show that it is necessary to go back and modify parts of the design to meet specifications.

Block Specifications, Design Entry and Simulation

Using the previously developed architecture overview the system is broken up into discrete building blocks for implementation. Simple parts are implemented and simulated as the lowest level blocks first. These small blocks are then used to build and simulate larger blocks representing more complex system parts. Once the top level blocks are completed they are assembled into a schematic of the whole system and simulated.

Depending on the type of design the schematic entry may be performed differently. Analog and digital building blocks can be implemented using a transistor level schematic editor. Purely digital building blocks can also be implemented using verilog or VHDL code to

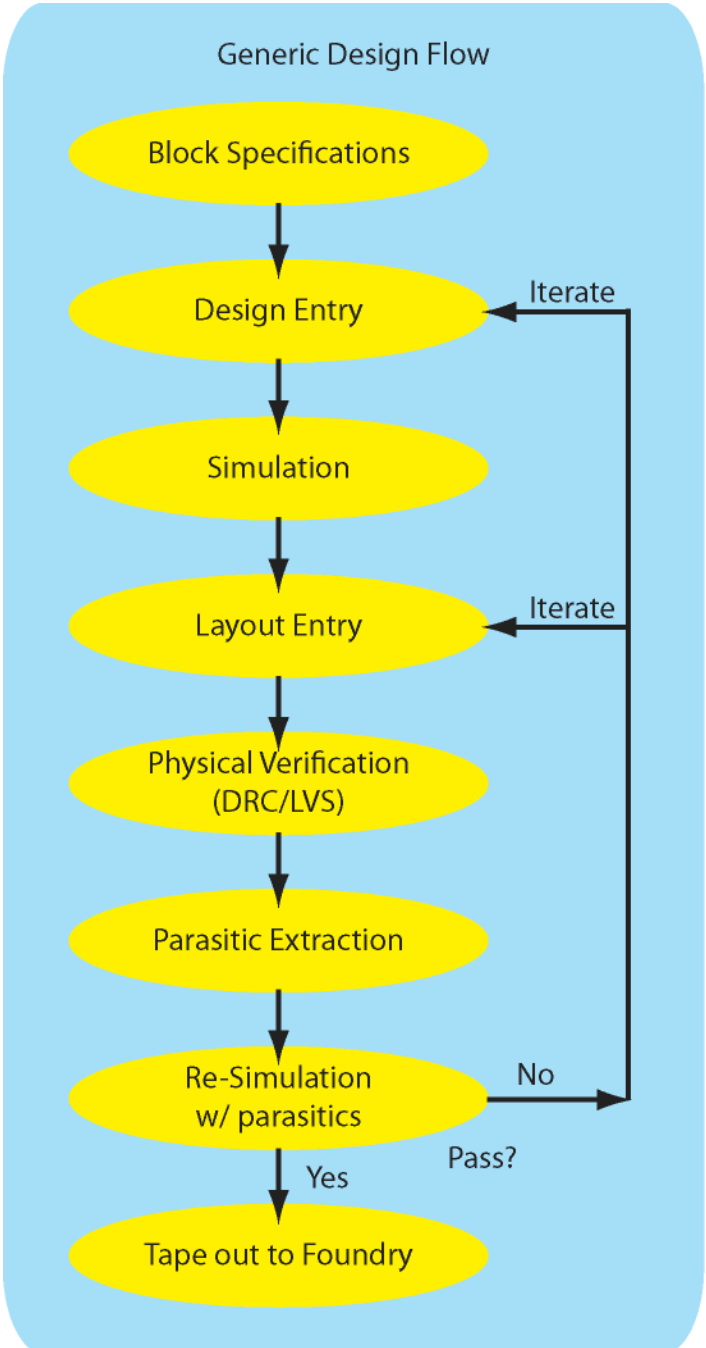

Figure 2 – ASIC Design Implementation Flow

describe the digital logic. Building blocks of either type can be turned into cells which are instanced to build more complex blocks. The hierarchical development continues until the whole design has been entered.

Simulation of the entire design is important but simulation should not wait until the whole design has been entered. It is best to simulate the individual blocks to confirm their functionality. The simulations are run on each level of hierarchy as they are assembled until the whole design can be simulated.

Simulation of both the blocks and the entire design is critical. These simulations should be performed at various temperatures and across the process corners. Process corners are models which add variation to the transistor characteristics based on the expected variations during fabrication. All functional modes of the design should be simulated, not just the expected usage with ideal inputs. Everything including the protection devices in the pads should be part of these simulations.

The type of simulator used is an important consideration. A purely analog type simulation is best. This type of simulation captures the complete behavior of the transistor. In a large, purely digital or mixed signal system these simulations can be very time consuming. This has led to the development of faster less accurate simulations. Many simulators now let the designer trade accuracy for speed. While these simulators can be helpful in cutting the time of a system simulation down from many hours or even days to an hour it is important that the designer understand what these simulations won't show. These types of simulators usually allow the designer to partition the system so that sensitive elements receive a more analog type simulation while other parts get treated as digital.

Layout Entry and Physical Verification

In general there is no correct way of doing layout so long as all of the layout rules are obeyed and the layout passes LVS. Digital circuits are usually very robust and hence the layout is not as critical, except to minimize area. However, for analog circuits layout becomes a very critical activity. Here shape, placement and interconnection of the circuit elements are important to the performance of the design.

Many books have been written about good layout practices for both analog and digital circuits. Thoroughly reviewing all of these practices is beyond the scope of this paper, but a few important considerations are outlined. The matching of both active and passive elements is dependant of their physical proximity and orientation in the layout. Capacitance between wiring can cause coupling between signals. Ground shielding should be used to isolate signals and blocks from one another. Analog and digital blocks should be separated to prevent noise coupling.

Along with standard good practice an additional layer of consideration may be needed for specialty designs. One example is radiation hardened (radhard) designs. Radhard designs require the designer to take into account threshold shifts that can occur in CMOS devices, leakage paths which can degrade performance and additional latch up conditions. There are several

techniques that can be employed to combat these issues so that radhard designs can be made successfully such as annular transistors and guard rings around individual transistors.

Every process will have a set of layout design rules which must be followed for a functional design. Some processes also have recommended rules that are more conservative than the required rules. For example the required minimum metal spacing on a layer may be 0.1 microns, but there may be a recommend rule of 0.2 microns. These recommended rules should be followed when possible. They will increase the yield of the design because the limits of the fabrication process will not be pushed.

The LVS comparison checks for any discrepancy between the layout and schematic. This confirms that the layout should implement the same functionality as the schematic. The LVS must return a 100% match to be certain that the circuitry the layout implements is the same as the circuitry the schematic implements.

Parasitic Extraction and Re-Simulation

The schematic is used to create a netlist for simulation. This netlist contains all of the circuit elements. When layout is extracted before LVS a netlist of the circuit is also created. Comparison of these two netlists is how the LVS checks that the implementations are matched. The extraction of the layout can go one step further by including parasitics in the extracted netlist. Parasitics are capacitances and resistances that arise between circuit elements and wiring due to the physical implementation of the layout. This extracted netlist with parasitics can be simulated to confirm the functionality of the layout. This is important because these parasitic capacitance and resistances can change the behavior of the circuit. They can cause excessive delay on clocked nodes in high speed circuits, cross talk between sensitive analog nodes, and voltage drops across high power wiring runs. These types of issues can not be found with the schematic simulations alone because they are a direct result of the layout implementation.

Fabrication, Packaging and Testing

Once the design has been completed submission to the foundry can proceed. The layout is sent to the foundry where DRC checks are usually run again. If the foundry finds any DRC violations it requests that they be fixed or that waivers be signed. Depending on the foundry the fabrication time can vary but it is usually around 3 months.

During these 3 months there is still work to be done to prepare for the testing of the part. Usually a test board is built that will allow for the new part to be thoroughly tested. This should be done while the part is in fabrication so that once the fabrication is complete everything is ready to begin testing.

Once received from the foundry the die needs to be packaged. While this step does not happen until after the fabrication is complete it should be considered from the beginning of the design process. Being sure that a suitable package is available and that the design fits in the package is often overlooked until later in the design flow which can results in difficulties and delays. The package needs to have the proper pin count and cavity size to accommodate the die.

Testing is necessary to prove the functionality of the fabricated device. The part needs to be subjected to all possible environments and input and output conditions.

Conclusions

The ASIC design flow is a complex process with many important details. Carefully and systematically going through the design process will help to ensure success. First pass success is desired but it is important to understand that some projects will require a few iterations to get all of the information needed to fully meet the specifications. Open channels of communication between the designer and customer will help ensure that both parties are pleased with the end result.