Predicting Package Level Failure Modes in Multi Layered Packages

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Abstract

Package technology is constantly improving in order to keep up with the advances in silicon technology. Multi layered packages exhibit several failure modes that can be predicted using modern software tools. This paper provides a methodology for creating a high-fidelity model of the interposer with all the conductor geometries. The two failure modes that are explored with this model are package warpage prediction due to actual copper imbalance and filled microvia delamination. Each layer can meshed based on the actual geometry in the layout design. Package warpage is caused by copper imbalance between the two sides of the interposer. The CTE mismatch between the two sides can bend the package to such a degree that it becomes impossible to assemble the solder interconnects. The filled microvias have copper structures that can delaminate from the copper traces in the conductor layers. The high-fidelity model provides the predictive tool to allow designers to adjust the layout before any manufacturing has taken place.

Key words

Package warpage, Trace modeling, Via fatigue failure, Via delamination, Substrate modeling

I. Introduction

The fabless semiconductor market is constantly searching for new innovation to tackle advanced silicon technology. Large ball grid arrays and QFNs are in development in various packaging companies. Substrates with complex copper traces and vias are constantly being pushed to tighter tolerances and smaller structures. The increased complexity is driving a decrease in reliability. R. Shukla, V. Murali and A. Bhansali of Intel corp. claim that “the most challenging aspect of the development was improving the reliability of the organic land grid array technology to meet the stringent reliability goals of CPU component packages” [7]. There is a distinct advantage to creating more robust substrates but it is quite difficult to figure out how to reduce problems that happen inside the package buildup without manufacturing and testing.

Tools for quickly predicting if a substrate design will meet reliability expectations are advancing as fast as the on chip architecture. Finite element methods have emerged as the forefront of prediction and prevention of various failure modes and manufacturing challenges. In the last few years the need for models with high-fidelity geometry has risen. Several schemes for refining meshes and smearing properties automatically are being used today. Creating high-fidelity models is still a labor intensive endeavor for most finite element modelers .Automatically generated full three dimensional models that include every geometrical feature are the next step.

In this paper, we chose a bare substrate to model, performed a warpage prediction and plotted the stresses in the vias. The warpage occurs mostly due to the copper imbalance between the two sides of the substrate. The via delamination occurs mostly due to the difference in coefficient of thermal expansion between the copper and the buildup material. Predictions for both phenomena are presented for the bare substrate model.

II. Creating The Substrate Model

The substrate model was created from the multi-chip module (MCM) files of a 25 by 25mm coreless substrate. A 15 by 15mm piece of the substrate was cut out for this investigation. A three dimensional model of the substrate was created using the Sherlock tool. Every segment of geometry is modeled for every trace and material properties are assigned automatically by the software. The drill holes for every layer are also created and the whole layered model

is exported to the Abaqus computer aided engineering tool. Boundary conditions are applied and the whole model is meshed inside Abaqus. The resulting model for the top and bottom layer of the substrate are shown in Fig. 1.

Trace Geometry

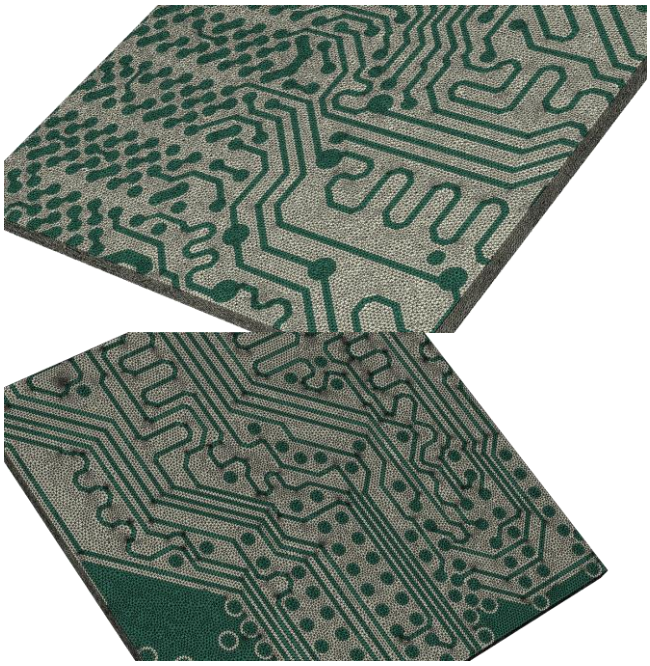

Figure 1: Top and bottom of the substrate model after the meshing operation.

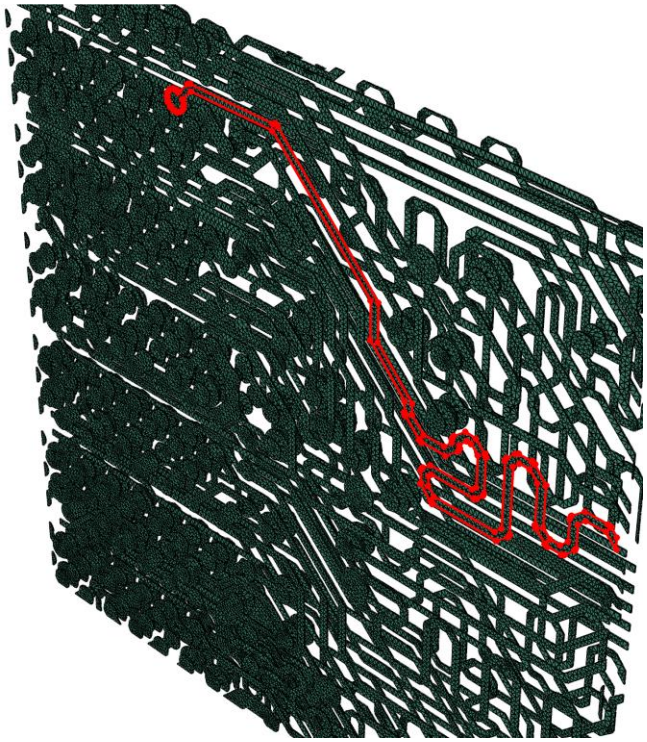

Figure 2: Detailed geometry and mesh of trace.

The model can be modified to perform predictions for several different phenomena because each trace and via has a selectable geometrical entity. Fig 2 shows a single trace in the model after it has been meshed. The analysis is this project is concentrated on predicting mechanical performance but the model can easily be converted to perform electromagnetic, thermal and multi-physics simulations.

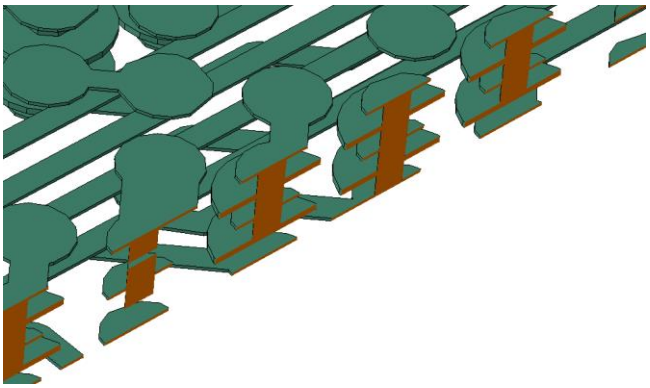

Figure 3: Detailed geometry of vias.

Fig 3 shows the detailed cross section of several vias. The level of detail is enough to capture the flanges in buried vias, different copper layer thicknesses and the correct via stacks. This substrate employs a stacked via structure without staggered vias. The level of detail and mesh density result in a large model size.

The model has 2,851,604 nodes and 2,044,465 elements. The model includes two materials. The copper material is isotropic and linear elastic and applied to the traces and vias. The buildup material is orthotropic.

III. Predicting package warpage

Package warpage is caused by copper imbalance between the two sides of the substrate stackup. Prediction of package warpage can be performed using effective properties and simpler models. An accurate model was useful for addressing the warpage issue successfully [4]. The detailed model can provide information about localized effects of each via. Excessive warpage can hinder the creation of solder joints when a die is attached to the pads. Malformed solder joints can lead to a higher probability of cracks forming in the joints. The plot of displacement magnitude is plotted in Fig 4.

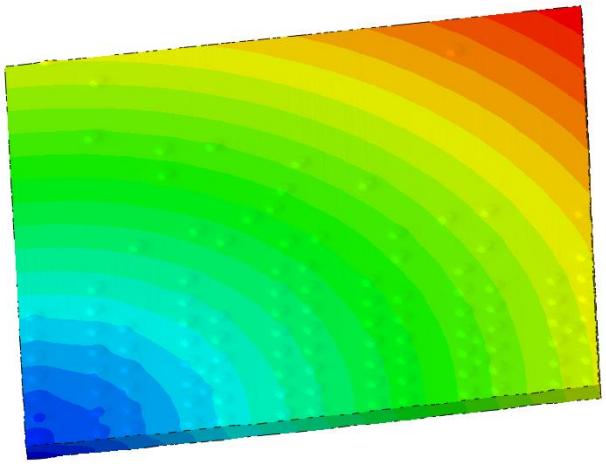

Figure 4: Warpage plot of the substrate

The warpage analysis is plotted for a temperature of (-55)°C and 260°C. The reference temperature is 25°C. At the high temperature, the diagonal warpage is predicted to be 55µm or 2.1 mils as shown in Fig 5.

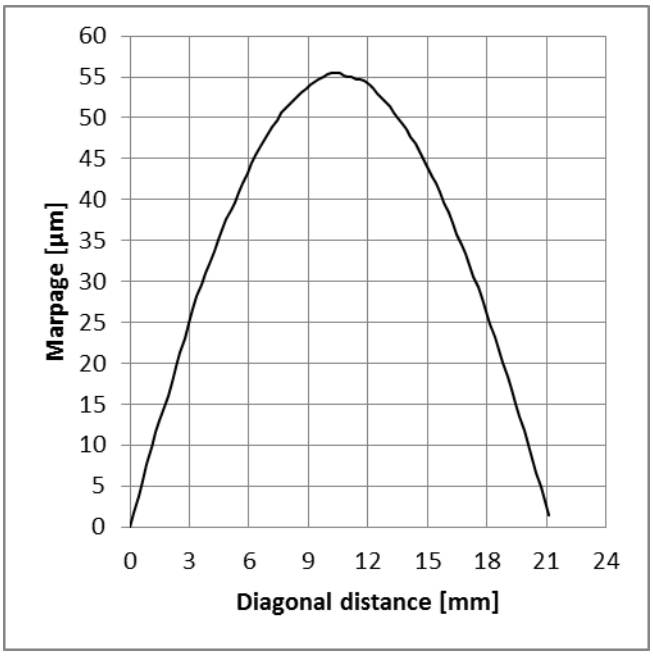

Figure 5: Predicted diagonal warpage

Wang, Jianjun, et al have shown that the deformation values of the package predicted from the finite element analysis are in a fair agreement with those obtained from the test [6] with a much coarser model. While this analysis could be performed using effective properties and layered models it is more challenging to obtain the warpage effect on individual vias. The plot in Fig 6 shows the out-of-plane direction deformation.

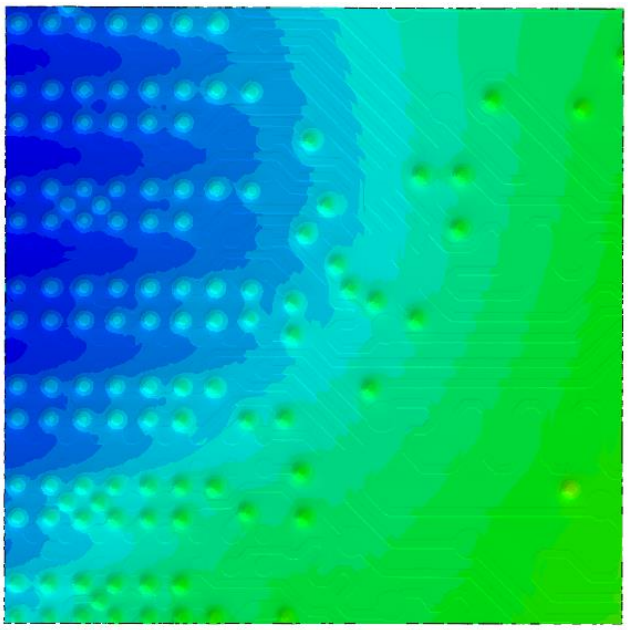

Figure 6: Out-of-plane direction deformation plot

This plot indicates that wherever there are plated vias, the out-of-plane CTE mismatch of the buildup and copper is causing a small difference in localized deformation. This finding would be difficult to obtain for a coreless substrate without using the high fidelity trace and via model.

IV. Microvia Delamination and Cracking Stresses

Microvias create the electrical connection between copper planes and pads in substrates. They are commonly used in packages with high input/output density and coreless substrates are no exception. They can be filled with copper and stacked. Fig. 7 shows a cracked via flange due to CTE mismatch between the copper and the buildup.

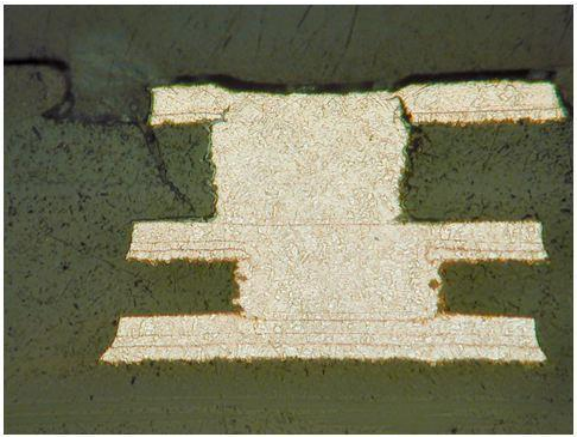

Figure 7: Copper filled microvia with corner crack. Source: Paul Reid [12]

The location of the microvias and the shape of the stack has been shown to have an effect on microvia reliability. Stress predictions using finite element models have been used to predict these stresses in simplified models [8].

Microvia Stresses at the Free Surfaces

The stresses predicted by the model will allow the substrate designer to highlight problematic areas before going in to production. This model only provides linear elastic stresses of the copper structures but it can easily be modified to capture fatigue effects.

The results show that the shape of the stack has an effect on the stresses in the copper. It is easier to concentrate on singular vias rather than using a design rule when a stress map exists for all the vias and pads. Fig. 8 shows the stresses in the vias for the top and bottom of the substrate The locations with the red areas are above the ultimate stress of electroplated copper and are predicted to have a higher probability of cracking. The traces are shown to have a higher stress than the substrate underneath. The pads that do not have a via underneath are at a relatively low stress and act as a stress redistribution layer for the solder attach.

This can be seen in the left side of the top image of Fig 8 and in the detailed view of Fig 9

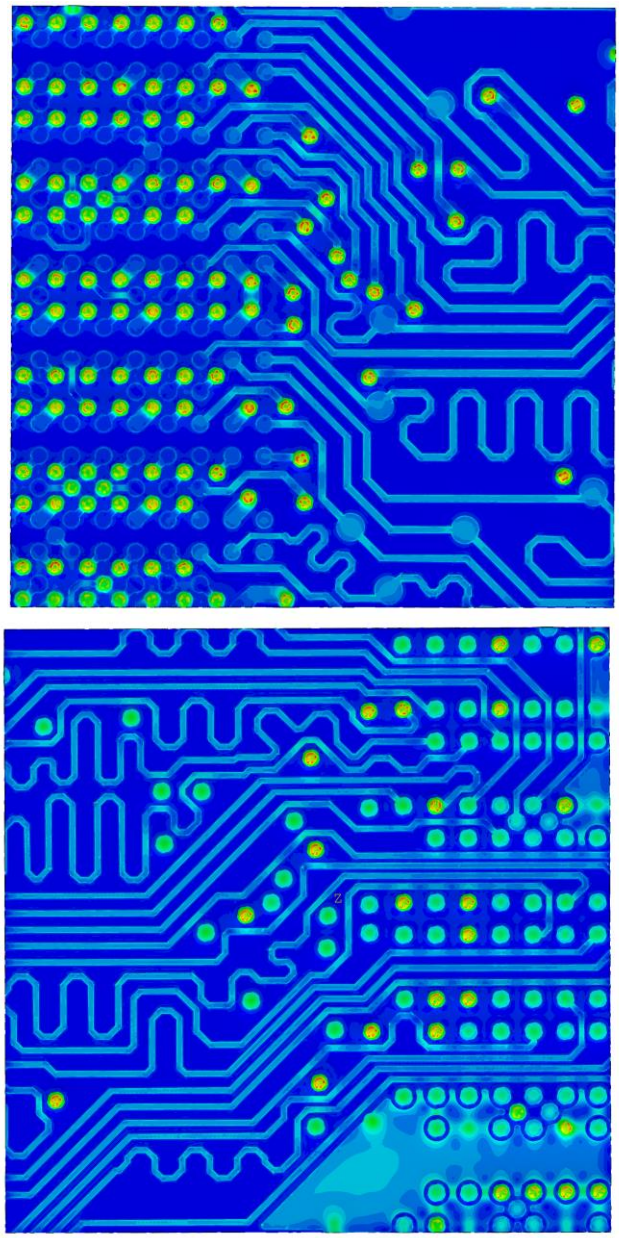

Figure 8: Von-Mises stress plotted for the both sides of the substrate

The other side of the substrate is shown in the bottom part of Fig 7. All of the pads on this side of the substrate are at a higher stress state. The microvia stack and pad design as shown in Fig 9 causes a lower stress state on one pad than the other. The dog-bone design is a standard routing pattern for high density substrates for this reason. The results show the added advantage for copper stress. A detailed model for all the vias is a good way to find these kinds of trends.

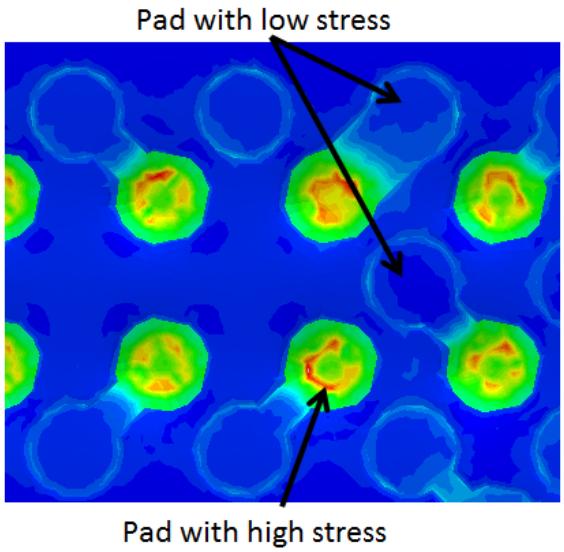

Figure 9: Detailed view of pads with high stresses and pads with low stresses

Stacked Microvia Stresses

The copper stress at the free surfaces are only one part of the stacked via. The vias have structures that go through the entire substrate and the stresses can be higher in the middle of the stack than the flanges. The stress field induced by differential thermal expansion in the via is three-dimensional in nature [1]. It is necessary to investigate the stresses in the stacked via to get the full picture.
We need to compare the Von-Mises stress with the first principal stress in order to look at the interfaces of the stacked vias. The Von-Mises stress is appropriate when looking at the ductile failure of copper at the flanges and barrel but the interfaces between vias are more susceptible to brittle fracture [3]. The Von-Mises stress plot in Fig 10 shows the stress distribution in a stacked via. The high stress regions are at the bottom interface, an inner interface and the flange.

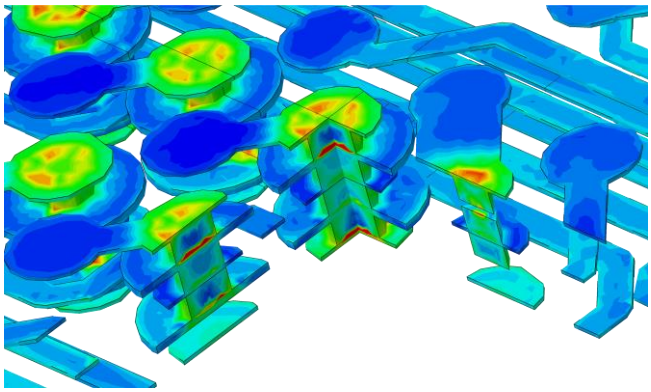

Figure 10: Von-Mises Stress plot for a stacked via

Myers, Alan M., et al disclose that "As a result of different thermal expansion coefficients of the metal interconnects, vias, and insulating layers, the via connections are subjected to large amounts of stress as the device is temperature cycled. Additionally, various residues consisting of fluorides and oxides, formed during the via etch process, are generally left at the interface prior to via metallization. These fluorides and oxides are generally brittle materials and when subjected to large amounts of thermal stress, crack and cause via delamination." [9]. Fig 11 shows the first principle stress in the same stacked via as Fig 10. The two plots can be compared to show that the high stress in the via to pad interface is of greater concern for causing brittle fracture. Failure analysis performed at Intel corp. (ADT) claims that "via delamination occurred at the interface between the first electrolytic Cu and electroless Cu" [11]. The first principal stress plot indicates that the interface is loaded in the tensile direction and predicts this failure mode. The Von-Mises plot indicates that while the flange is more susceptible to ductile modes of failure it is not at risk for brittle fracture.

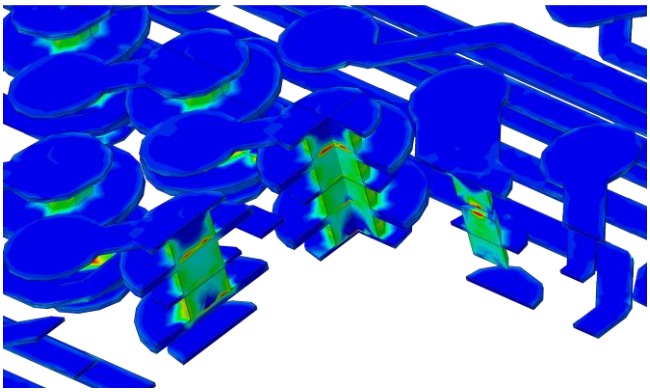

Figure 11: First principle stress (σ_1) plot for a stacked via

The stress plots for the substrate enable the board designers to predict many reliability issues. The high-fidelity model provides the predictive tool to allow designers to adjust the layout before any manufacturing has taken place.

V. Conclusion

Making a full three dimensional finite element model used to be a difficult and lengthy process. Detailed trace approach used to be prohibitively expensive for large packages and substrates with many metal levels [2]. Expert modelers spent many hours to create the models from layout files. It is more efficient to allow software to create the high fidelity substrate model automatically. Automation allows the reliability experts, who need not be modeling experts, to directly interact with the substrate model.
The high fidelity substrate model enables warpage predictions with a higher degree of accuracy. The diagonal

warpage plot of other modeling techniques is consistent with the high fidelity model. While this high fidelity is not always necessary the result in this project show that the out-of-plane deformation is affected by the presence of stacked vias.

The stresses in the filled microvias are shown to be affected by the stack properties. Both ductile and brittle failures can be predicted using this modeling method. The Von-Mises stresses at the flange of the vias are indicative of the ductile cracks. The first principal stress at the via and pad interfaces are predicting a high probability of delamination due to brittle fracture. The stresses in the traces are also helpful in designing substrates that can decrease localized stresses using different copper trace geometries. All three copper stress predictions were made possible by the high fidelity model.

This project highlights the advantages of using automation of model creation to improve modeling techniques. The constant demand for improved component packaging is driving the demand for improved modeling techniques. The advanced Sherlock software trace modeling capabilities improve the modeling capabilities while shortening the model creation time.

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