Case Study

Slow Body Diode Failures of Field Effect Transistors (FETs)

By the Staff of DfR Solutions

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Slow Body Diode Failures: Root-Cause and Corrective Actions

A telecommunications customer recently experienced field failures in a power supply. DfR initiated a root-cause investigation to determine the drivers for the failure and provide recommended corrective and preventative actions.

Introduction (Failure History)

The use of a power factor correction[1] (PFC) Boost with a zero voltage switching[2] (ZVS) full bridge is typical for high power applications. However, in this particular application, the customer was experiencing failures in field effect transistors (FETs) in either the PFC or the Full-bridge but never in both topologies at the same time.

The FETs in question were rated to 500V and were subjected to 400V bus voltages. In previous designs, failures had been eliminated through the substitution of 600V rated parts. This could imply that voltages spikes in excess of 500V were present in the electrical design. However, circuit simulation and electrical characterization did not identify voltage levels in excess of 500V.

This initial assessment seemed to effectively eliminate overvoltage as the cause of failure. To confirm this null hypothesis, an overvoltage breakdown experiment was conducted on functional FETs, both unused and from field return product, to determine their response to an overvoltage condition and how it compared to the datasheet.

Overvoltage Breakdown of FETs

Breakdown voltage at 125µA was recorded for the functional FETs. The results are displayed in Table 1. A lower current than the datasheet specified was initially used to reduce the chance of damaging the field returned devices. Based on these results the functional devices were within specification.

FET Source	Breakdown (Volts)	Build Year
Field	550	2006
Field	560	2006
Field	560	2006
Field	570	2006
Field	570	2006
Field	575	2006
Field	575	2005
Field	580	2006
Unused	575	2009

[1] A design that controls the amount of power drawn by a load to obtain a power factor (ratio of the real power flowing to the load to the apparent power) as close as possible to unity.
[2] The making or breaking of circuit timed such that the transition occurs when the voltage wave form crosses zero voltage

Electrical Characterization

As voltage breakdown, either through excessive voltage in application or insufficient resistance to breakdown, was not a driver in the FET failures, additional electrical characterization was performed. The specific focus of this activity was to benchmark the existing 500V FET that was failing to the 600V FET that was robust and identify parameters other than voltage rating that could explain the differences in failure rates. Electrical parameters that were characterized included

- Drain to source resistance
- Source to drain diode voltage drop
- Drain to source breakdown voltage

Drain to Source Resistance (RDS)

Testing was done to compare the on resistance of the FETs as a function of temperature. The experimental design included a cold plate, a high current power supply, and a digital multimeter to capture voltage and current measurements. The FETs were thermocoupled and the plate temperature was adjusted till a steady state condition was reached at the temperature of interest.

A comparison of the drain to source resistance between the 500V device and the 600V device is shown in Figure 1. This shows that RDS of the 600V device is lower and therefore better than the 500V FET.

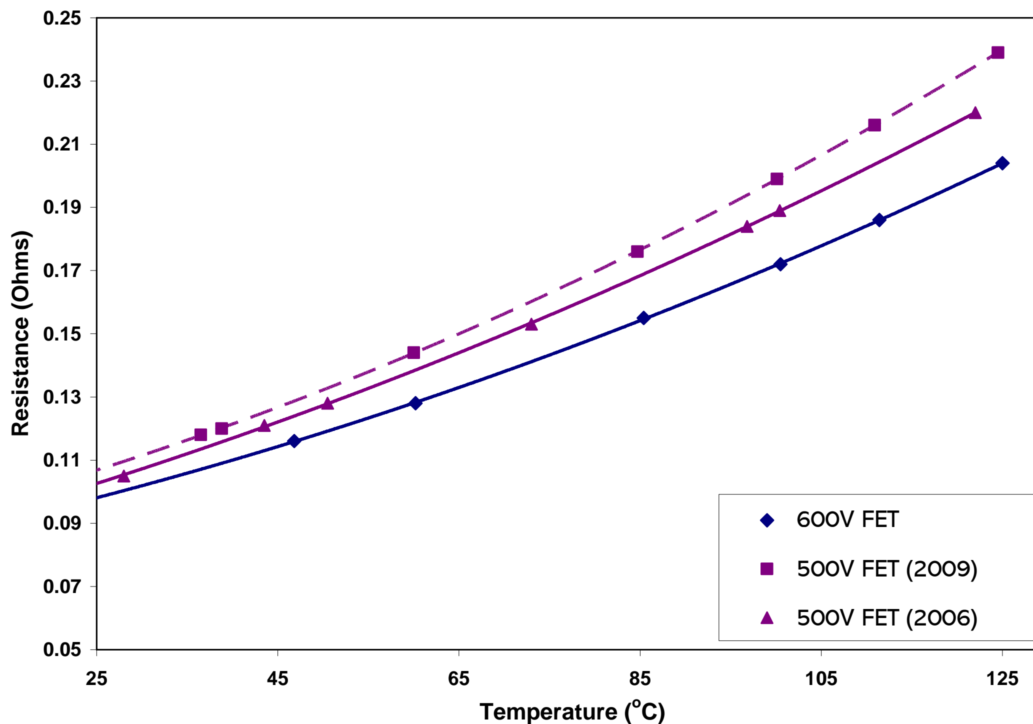

Figure 1

Source to Drain Diode Voltage Drop

The same experimental setup used to capture drain to source resistance was also used to characterize the diode voltage drop as a function of temperature. One new 500V FET and one new 600V FET were tested. The results are shown in Figure 2. The 500V FET was found to have a significantly lower diode voltage drop then the 600V FET.

This finding is significant as a typical slow reverse recovery diode will have a 0.6V to 0.8V forward drop. In FETs, these body diodes are normally slow and can be modified by doping the junction with gold or irradiating the device to damage the lattice which reduces the minority carrier life times and charge. This in turn reduces the reverse recovery time of the diode so that in can be used in faster circuit applications. However, the forward voltage is increased above 1V and as high as 2V for hyper-fast diodes used in PFC Boost applications. Therefore, this shows that 600V device had a much faster, lower charge body diode than the 500V device and is more suitable for the use in this power supply design.

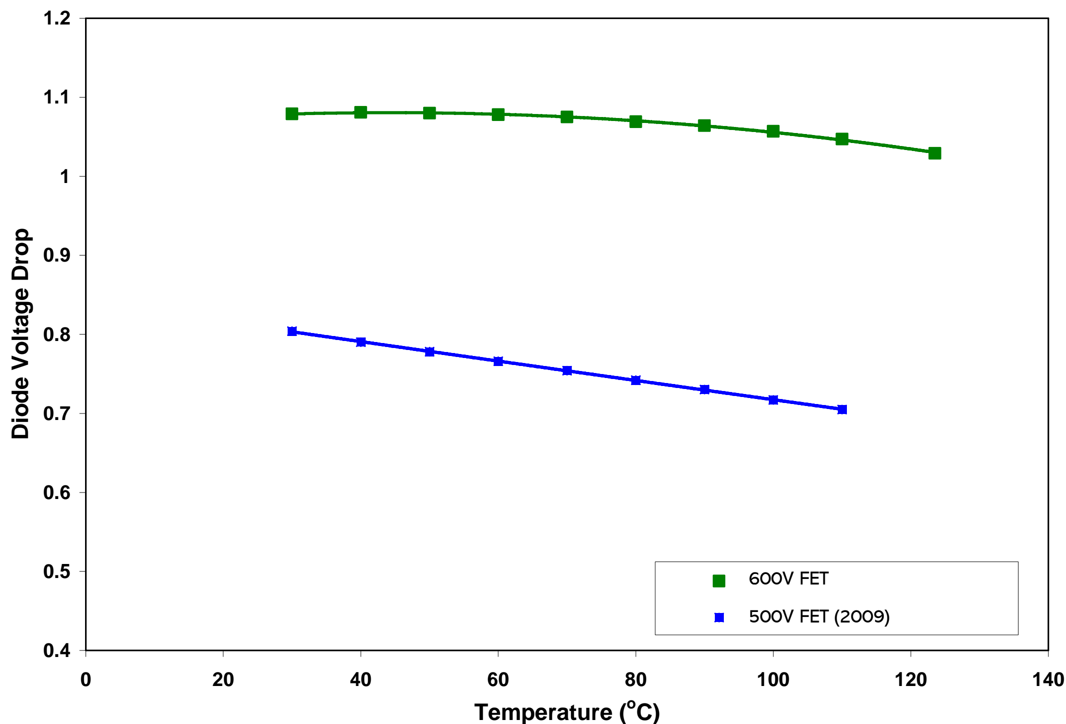

Figure 2

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Drain to Source Breakdown Voltage
Additional testing of the breakdown voltage at elevated temperatures was conducted to determine the effect of temperature on the breakdown voltage. Testing was done at 250µA per the 500V FET manufacturer's specification (note: the 600V FET manufacturer specified a much higher leakage current). The results for the breakdown voltages are shown in Figure 3.

The 500V devices had higher breakdown voltages at 250µA above 100°C junction than the 600V devices. This can be a problem with the 600V FETs because the power dissipation will be higher if the leakage current is increased. However, within the current application, the devices were running below 100°C junction. Given this operational condition, in combination with an applied voltage of 400V, this differentiation is not expected to be relevant to the failure mode.

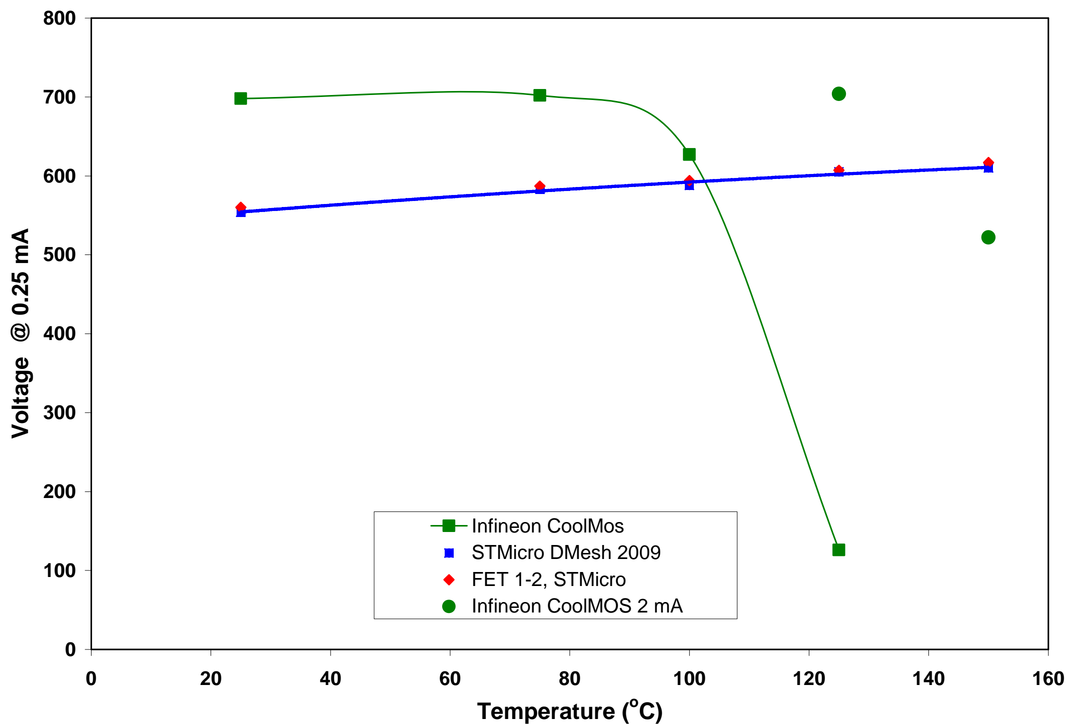

Figure 3

Discussion

There were no electrical design deficiencies that would cause the 500V rated device to fail due to voltage stresses. This was initially concerning to the customer, as it could indicate that the 600V devices may not solve the failure issue long-term. It is also strong justification for avoiding troubleshooting when attempting to resolve field failures.

Based on the knowledge gained in the failure investigation, the most likely theory for the cause of failure is related to the slow body diode characteristics of the 500V FET. As mentioned earlier, the 500V FET had a body diode with properties consistent with body diodes found in slower devices. A paper by International Rectifier titled "MOSFET Failure Modes in the Zero-Voltage-Switched Full-bridge Switching Mode Power Supply Applications," explains a failure mode using slow reverse recovery body diode devices. The failures result when a parasitic transistor turns on and allows high current to be drawn from drain to source when the FET is off. This results in overheating of the device similar to what was observed in the failed devices. The die and source bond connection showed high current yet there was no damage to the gate.

As a general rule, there are two mechanisms which can cause the parasitic transistor to turn on. One is when the FET transitions on in the forward direction with the body diode conducting, during which the FET will have limited dV/dt capability. This may explain the failures in the ZVS Full-bridge in the power unit. The particular type of ZVS Full-bridge used in this power supply design has a higher risk then some other ZVS Full-bridge designs. It is therefore recommend that fast reverse body diode FET's be used.

The other issue is the dV/dt when the FET turns off, which will be limited because of the parasitic transistor possibly turning on. In the Boost PFC, when the FET turns off, the inductor dumps energy into the FET causing the FET voltage to rise very quickly until the PFC diode conducts and the inductor charges the output capacitor. This rate of rise (dV/dt) on the drain-source of the FET is determined by the capacitance of the device and available inductor energy. In high current continuous mode PFC designs, such as this, the energy stored in the inductor is relatively high and the dV/dt on the FETs will be significantly high. As such, it is recommended that high dV/dt rated devices be used.

It should be noted that ZVS-Full-bridge can also experience failures due to high drain to source dV/dt. Most ZVS Full-bridges do not ZVS (zero voltage switch) below half load and will hard switch the FET which can result in high drain to source dV/dt. Testing the robustness of the FET under the above conditions is difficult. However, the datasheet of the FET devices can give some information in this area. For example, the industry has accepted the listing of a dV/dt rating as an important parameter when qualifying a device for Boost PFC applications.

Recommendations

DfR Solutions recommends two tests to compare the robustness of future FET devices for this application.

One is that a hot step stress test (HALT) be performed to determine the operating margin and destruct limits of the power supply. Ideally this should be performed starting at 55C and incrementally increasing the ambient operating temperature until the power supply no longer operates.

The second test is to measure the worst case drain to source slope dV/dt on the Boost PFC and ZVS Full-bridge. Compare this to the manufacturer's datasheet and contact the manufacturer if this information is not available. The recommendation is that the measured drain to dV/dt rating should not to exceed 50% of the rated drain to source dV/dt. The testing should be done at 4 corners, high/low line and high/low load.

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