Tutorial 16

DfR Solutions
reliability designed, reliability delivered

Design for Reliability & Sourcing of Printed Circuit Boards

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smthybridpackaging
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DfR Course Abstract

- Designing printed boards and assemblies today is more difficult than ever before because of the increased lead free process temperature requirements and associated changes required in manufacturing. Not only has the density of the electronic assembly increased, but many changes are taking place throughout the entire supply chain regarding the use of hazardous materials and the requirements for recycling. Much of the change is due to the European Union (EU) Directives regarding these issues. The RoHS and REACH directives have caused many suppliers to the industry to rethink their materials and processes. Thus, everyone designing or producing electronics has been or will be affected.

Instructor 1 Biography

- Cheryl Tulkoff has over 22 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She holds leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years and is also an ASQ Certified Reliability Engineer.

- She has a strong passion for pre-college STEM (Science, Technology, Engineering, and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.

Instructor 2 Biography

- Dr. Viktor Tiederle has over 29 years of experience in interconnection technology for microelectronic devices. He has worked in nearly all areas from development to production with the emphasis on quality and reliability. He started with his work in thick film technology and soldering techniques in SMD ceramics in the early 1980's. Later we worked in wire bonding technique as well as in adhesive technology and developing micromechanical devices for automotive applications. Since more than 10 years he is responsible for many projects within the automotive as well as other industrial segments, for example in photovoltaic.
- Viktor earned his Diploma of Physics at the Technical University of Munich and Stuttgart. After some years of industrial work he received his Dr.-Eng. degree with a studying Design of Experiments used for wire bonding technique in several applications.
- Viktor works in several working groups in the automotive industry for qualifying components for the use in such hazard environments.

Course Outline

MODULE 1: INTRODUCTIONS
- Intro to Design for Reliability
- DfR & Physics of Failure

MODULE 2: COMPONENTS
- Selection
- Critical Components
- Moisture Sensitivity Level
- Temperature Sensitivity Level
- Electrostatic Discharge
- Plating Material
- Miscellaneous
- Lifetime
- Derating & Uprating

MODULE 3: MECHANISMS & PHYSICS OF FAILURE

MODULE 4: PRINTED CIRCUIT BOARDS
- Surface Finishes
- Cracking & Delamination
- Laminate Selection
- PTH Barrel Cracking
- CAF
- Strain/Flexure Issues & Pad Cratering
- Cleanliness
- Electrochemical Migration

MODULE 5: Printed Circuit Board Sourcing

MODULE 6: Focus on DfR in Manufacturing

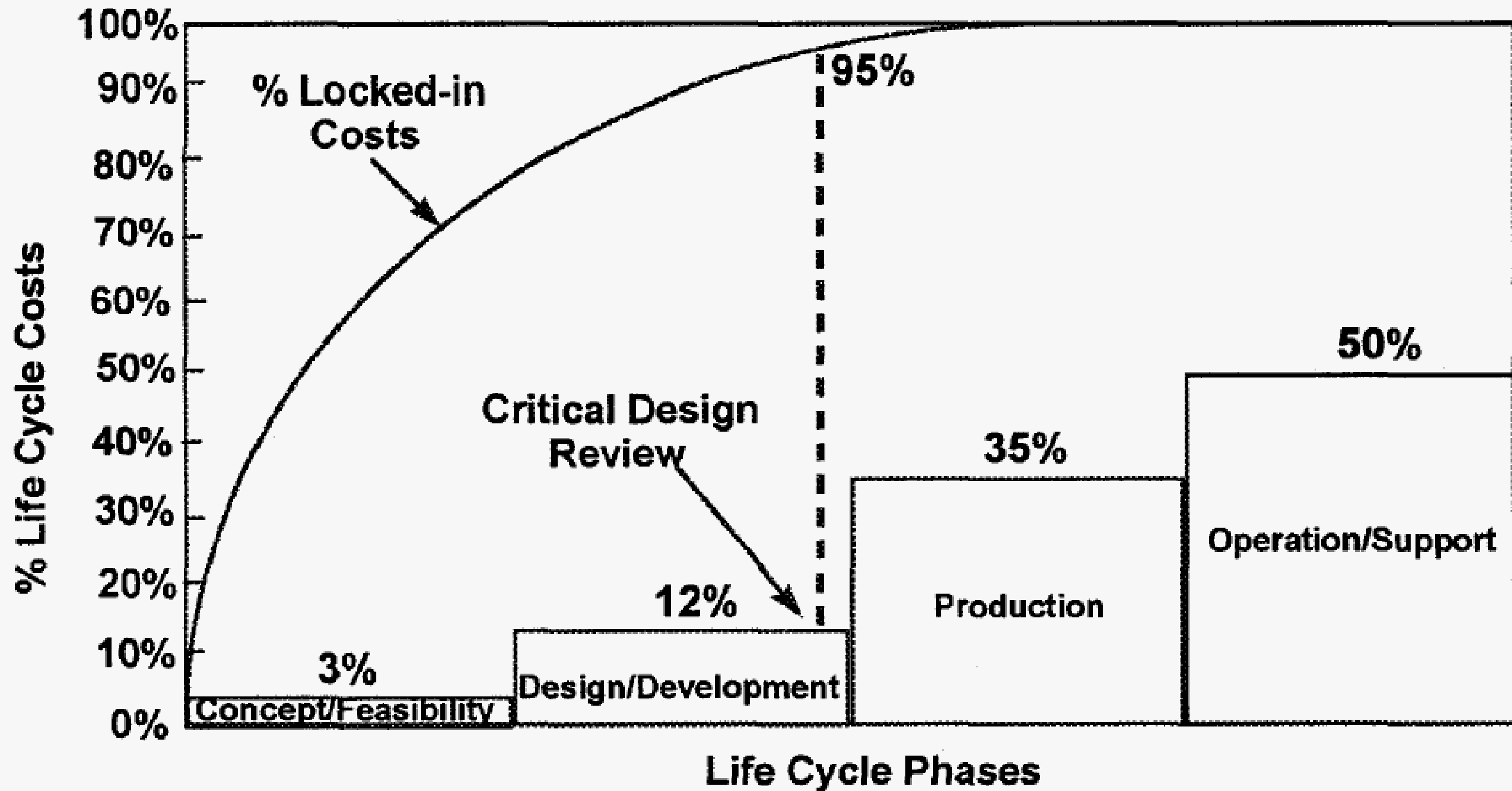
Design for Reliability (DfR) Defined

- DfR: A process for ensuring the reliability of a product or system during the design stage *before* physical prototype
- Reliability: The measure of a product's ability to
  - …perform the specified function
  - …at the customer (with their use environment)
  - …over the desired lifetime

Why Design for Reliability (DfR)?

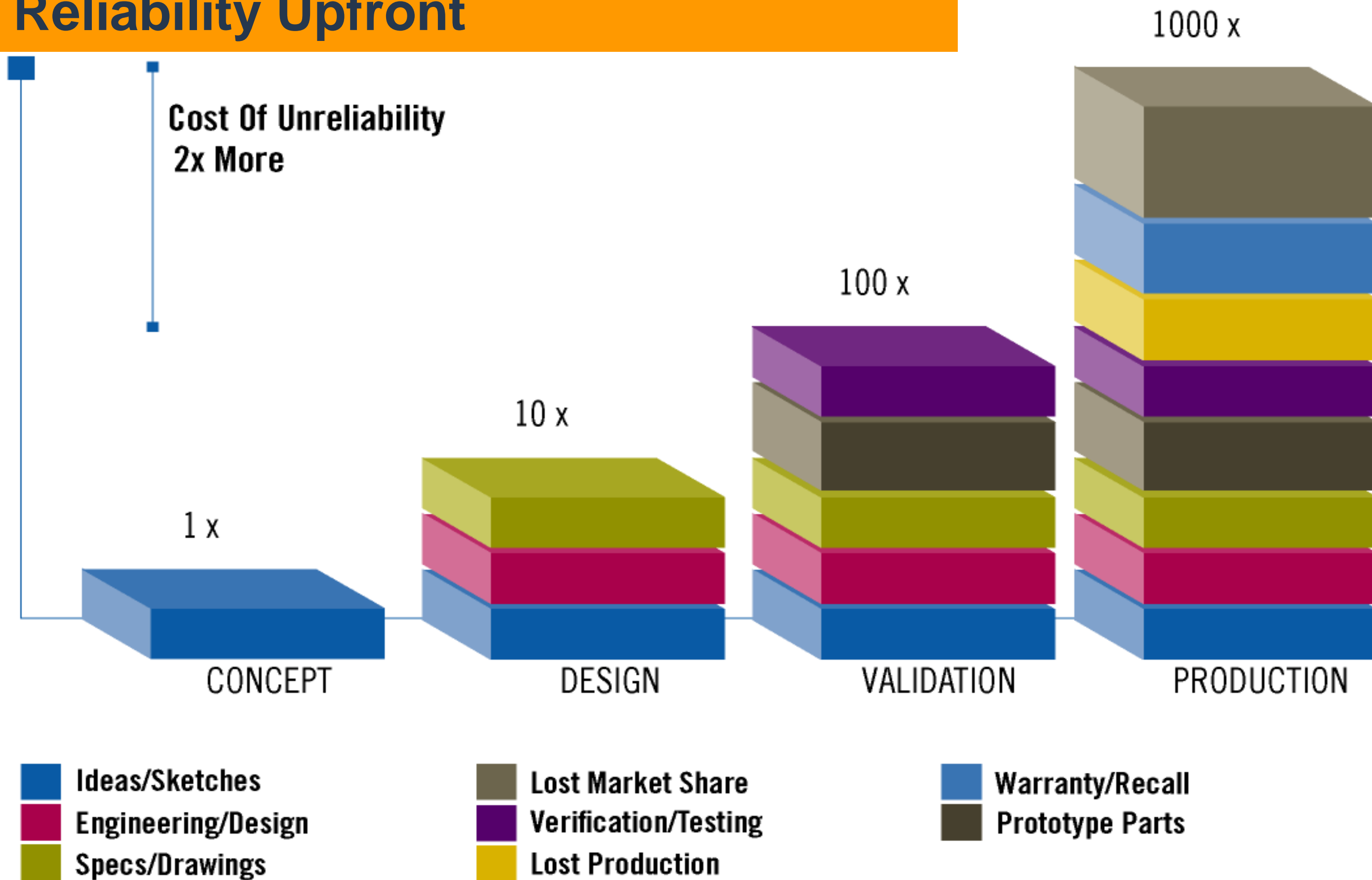
- The foundation of a reliable product is a robust design
  - Provides margin
  - Mitigates risk from defects
  - Satisfies the customer

Why DfR?



Architectural Design for Reliability, R. Cranwell and R. Hunter, Sandia Labs, 1997

Why DfR? (continued)



Who Controls Hardware Design?

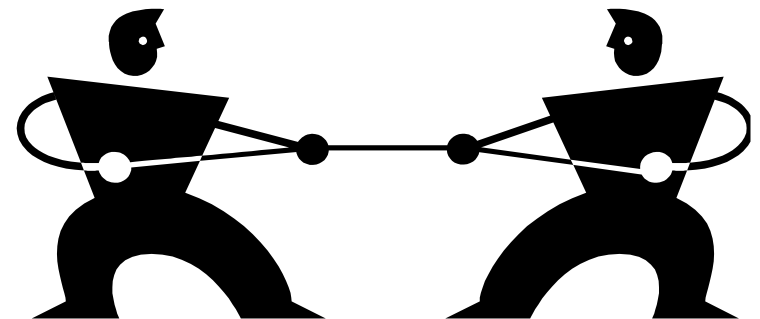
Electrical Designer

- Component selection
  - Bill of materials (BOM)
  - Approved vendor list (AVL)

Mechanical Designer

- PCB Layout
- Other aspects of electronic packaging

Both parties play a critical role in minimizing hardware mistakes during new product development.



When Do Mistakes Occur?

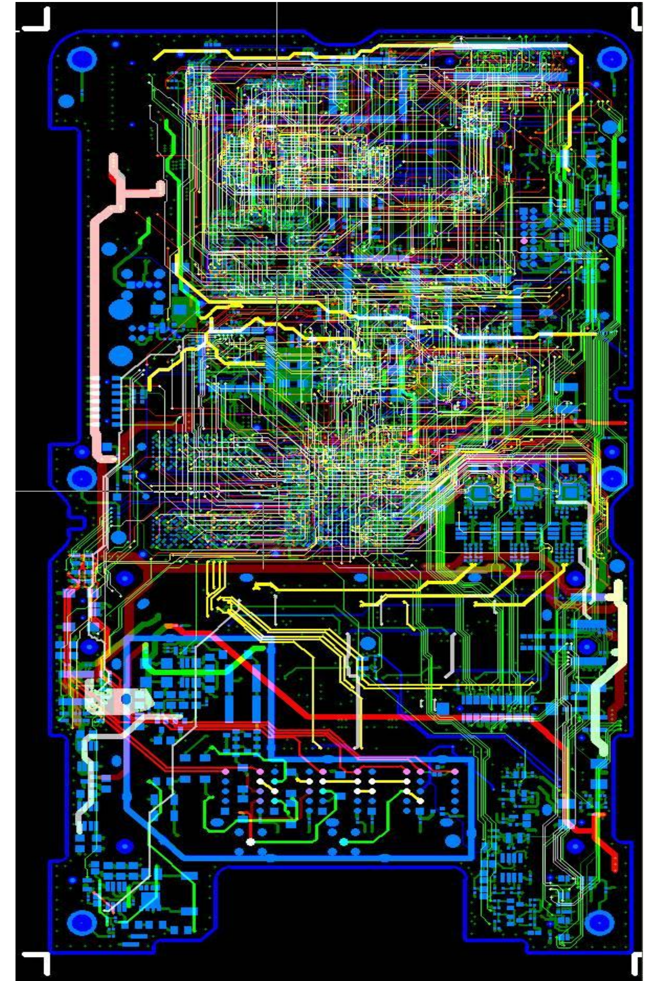
- Insufficient exchange of information between electrical design and mechanical design
- Poor understanding of supplier limitations
- Customer expectations (reliability, lifetime, use environment) are not incorporated into the new product development (NPD) process

"You don't know what you don't know"

Reality of Design for Reliability (DfR)

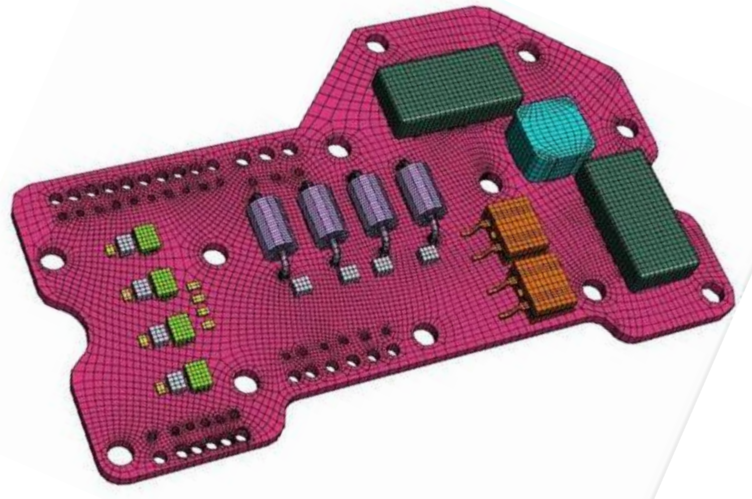
- Ensuring reliability of electronic designs is becoming increasingly difficult
  - Increasing complexity of electronic circuits
  - Increasing power requirements
  - Introduction of new component and material technologies
  - Introduction of less robust components

- Results in multiple potential drivers for failure



Reality (continued)

- Predicting reliability is becoming problematic
  - Standard MTBF calculations can tend to be inaccurate
  - A physics-of-failure (PoF) approach can be time-intensive and not always definitive (limited insight into performance during operating life)



Limitations of Current DfR

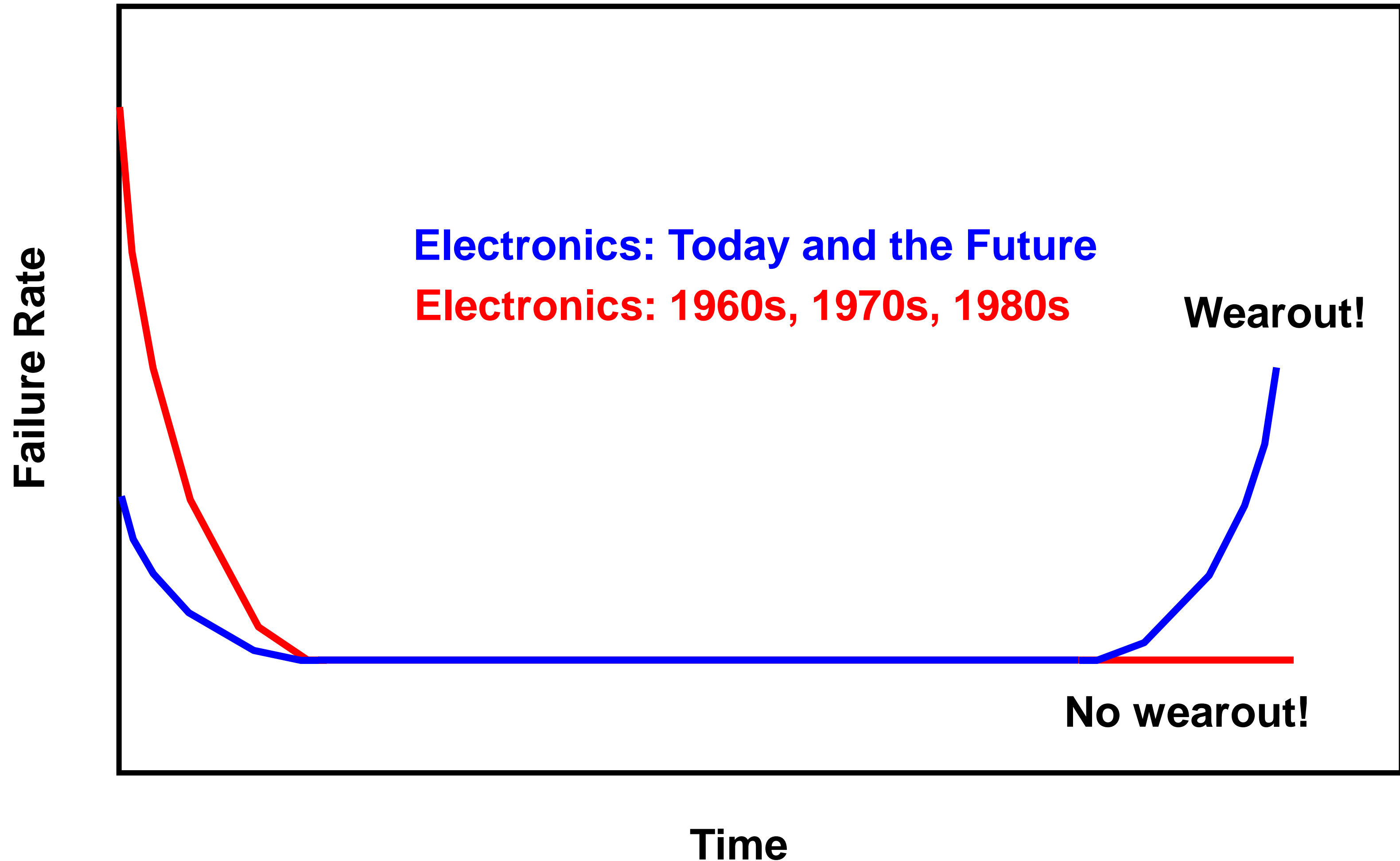
- Too broad in focus (not electronics focused)
- Too much emphasis on techniques (e.g., FMEA and FTA) and not answers
  - FMEA/FTA rarely identify DfR issues because of limited focus on the failure mechanism
- Overreliance on MTBF calculations and standardized product testing
- Incorporation of HALT and failure analysis (HALT is test, not DfR; failure analysis is too late)
  - Frustration with ‘test-in reliability’, even HALT, has been part of the recent focus on DfR

DfR and Physics of Failure (PoF)

- Due to some of the limitations of classic DfR, there has been an increasing interest in PoF (also known as: Reliability Physics)

- PoF Definition: The use of science (physics, chemistry, etc.) to capture an understanding of failure mechanisms and evaluate useful life under actual operating conditions

Why PoF is Now Important



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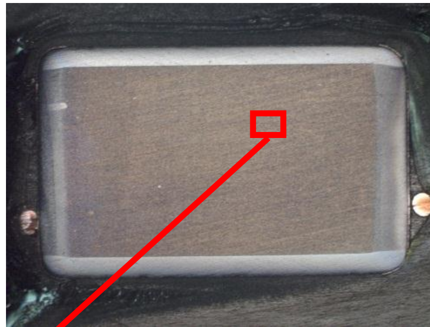
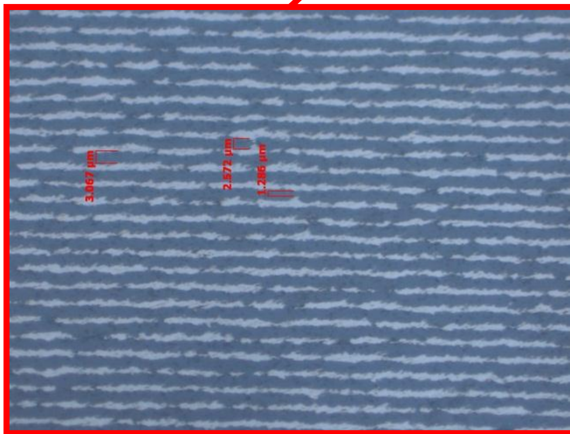
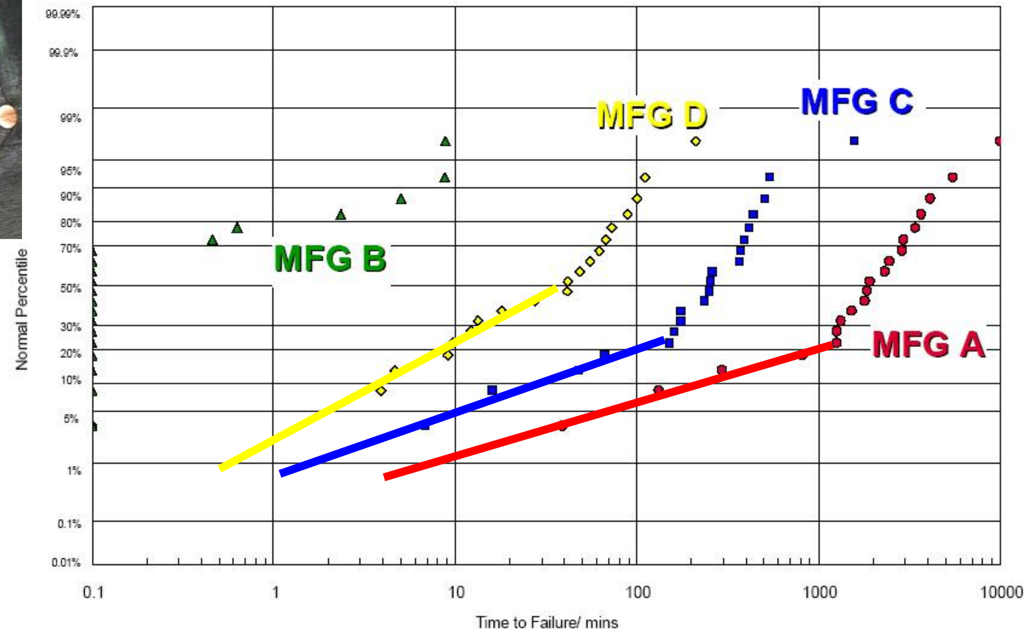
PoF and Wearout

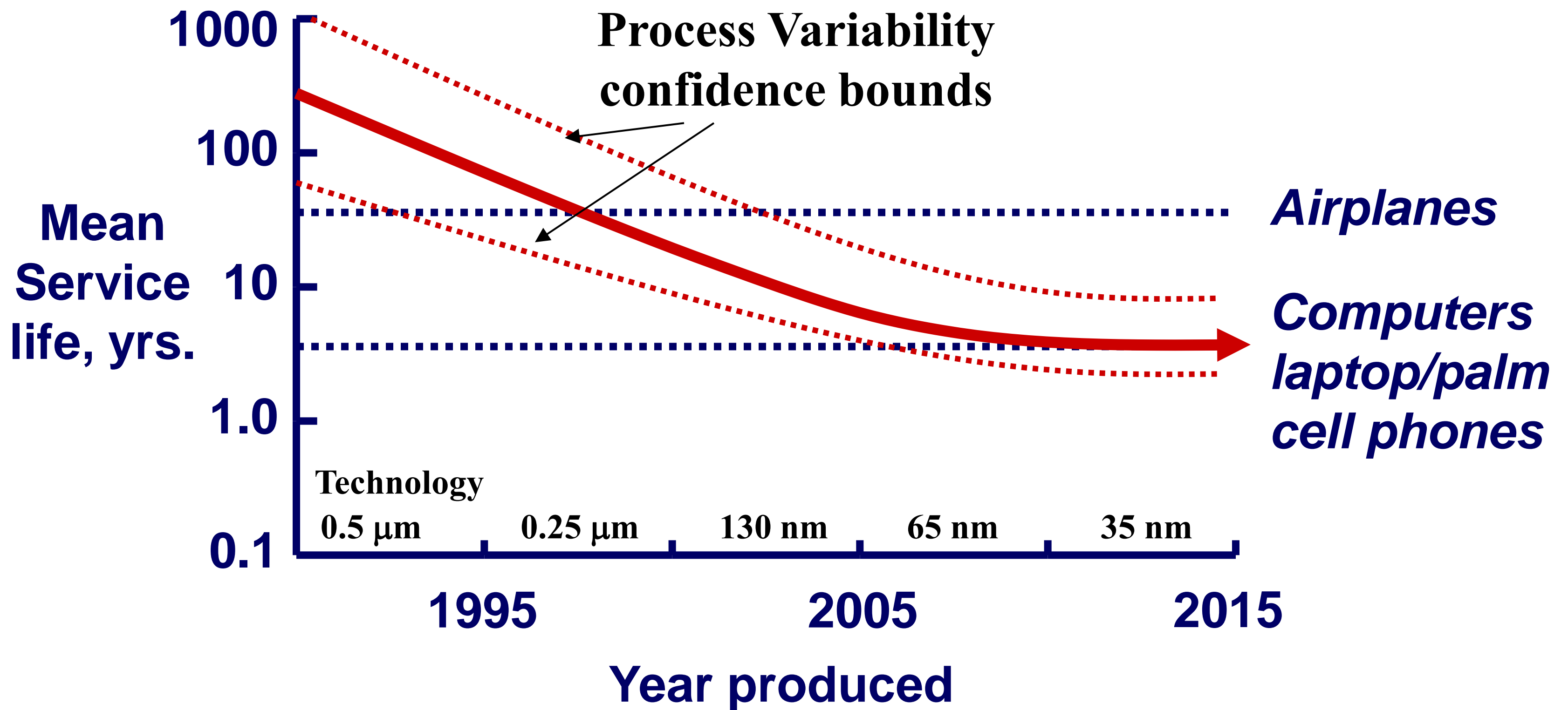
- What is susceptible to wearout in electronic designs?
  - Ceramic Capacitors (oxygen vacancy migration)
  - Memory Devices (limited write cycles, read times)
  - Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)
  - Resistors (if improperly derated)
  - Silver-Based Platings (if exposed to corrosive environments)
  - Relays and other Electromechanical Components
  - Light Emitting Diodes (LEDs) and Laser Diodes
  - Connectors (if improperly specified and designed)
  - Tin Whiskers
  - Integrated Circuits (EM, TDDB, HCI, NBTI)
  - Interconnects (Creep, Fatigue)
    - Plated through holes
    - Solder joints

Wearout (Ceramic Capacitors)

- Ceramic chip capacitors with high capacitance / volume (C/V) ratios
  - Can fail in **less than one year** when operated at rated voltage and temperature

Wearout (Integrated Circuits)



Known trends for TDDB, EM and HCI degradation

(ref: extrapolated from ITRS roadmap)

IC Wearout (continued)

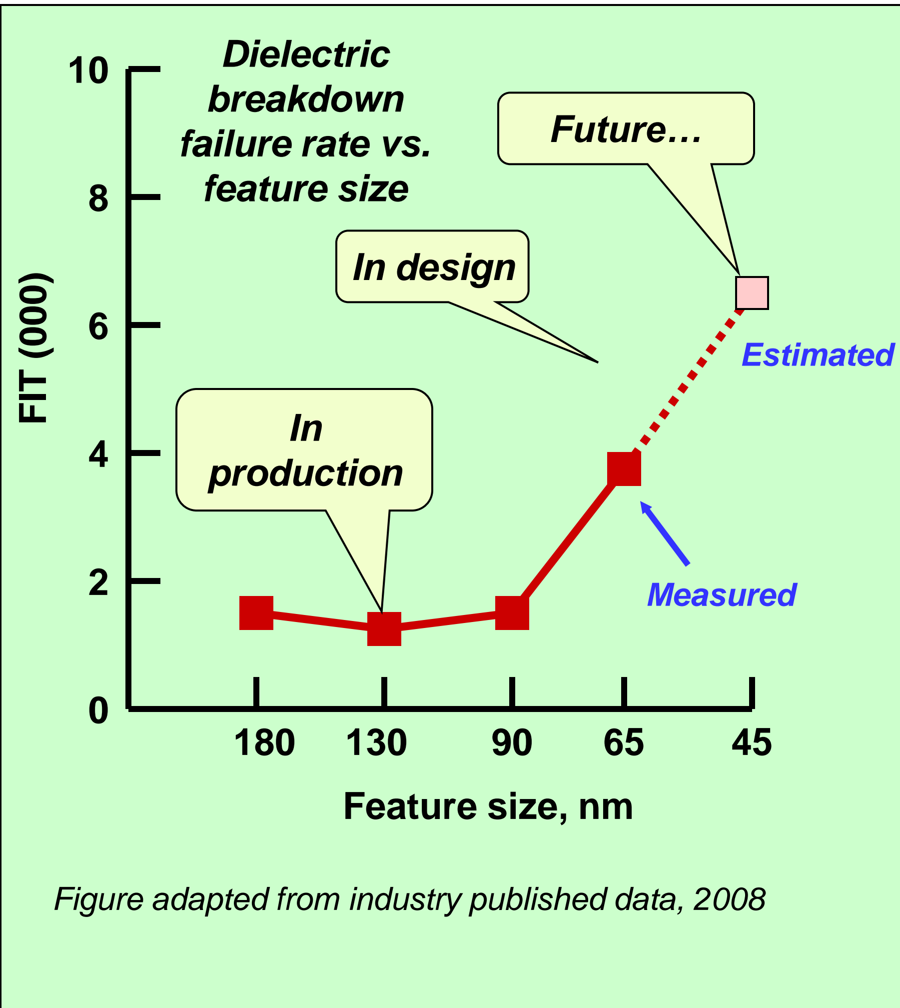


Figure adapted from industry published data, 2008

It is becoming more challenging to achieve very high reliability for products made with advanced technologies (90nm and smaller)

Phil Nigh, IBM Microelectronics

"failure rate increases as we scale to smaller technologies…hard failures will present a significant and increasing challenge in future technology generations."

Pradip Bose, Jude A. Rivers, et al., IBM T.J. Watson Research Center

Increasing need to predict failure behavior before incorporating new technology in long-life systems

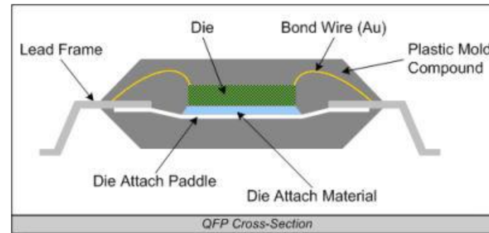
IC Testing Falls Short

- Limited degree of mechanism-appropriate testing
  - Only at transition to new technology nodes
  - Mechanism-specific coupons (not real devices)
  - Test data is hidden from end-users
- Questionable JEDEC tests are promoted to OEMs
  - Limited duration (1000 hrs) hides wearout behavior
  - Use of simple activation energy, with incorrect assumption that all mechanisms are thermally activated, can result in overestimation of FIT by 100X or more

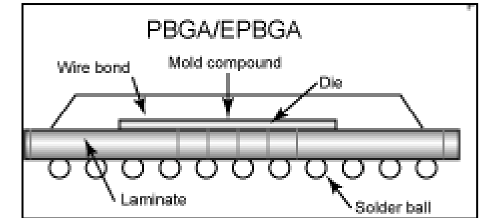
Solder Joint (SJ) Wearout

- Elimination of leaded devices
  - Provides lower RC and higher package densities
  - Reduces compliance

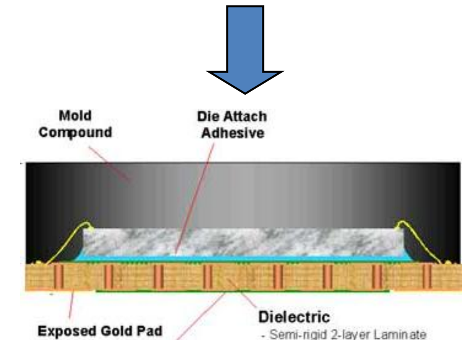
Cycles to failure
-40 to 125C



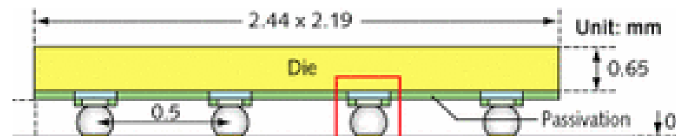
QFP: >10,000



BGA: 3,000 to 8,000



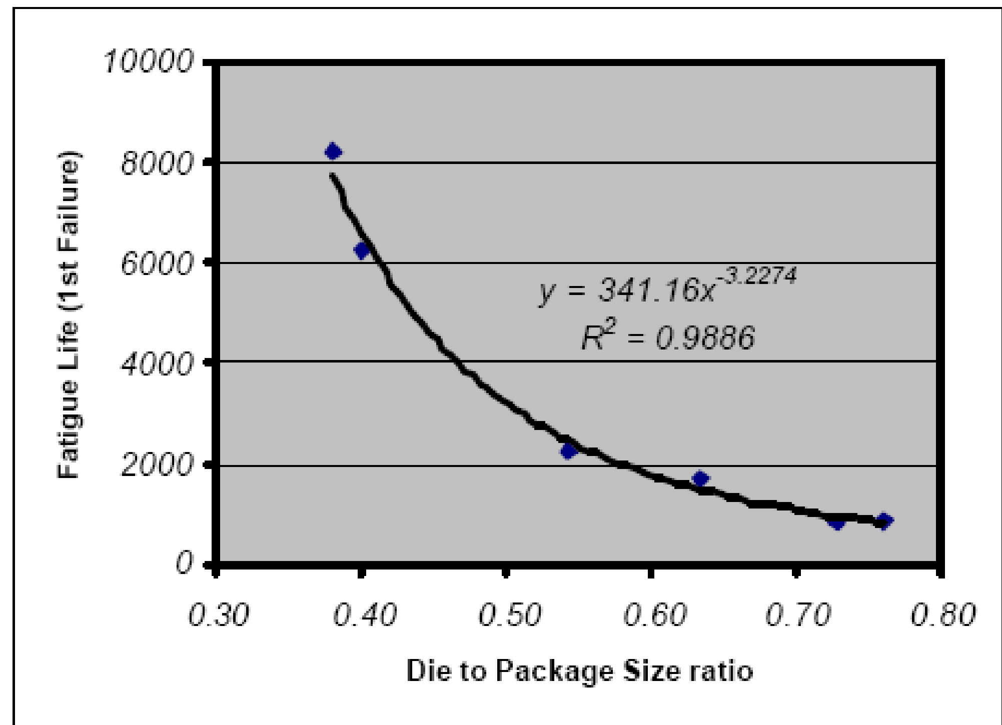
QFN: 1,000 to 3,000



CSP / Flip Chip: <1,000

SJ Wearout (cont.)

- Design change: More silicon, less plastic
- Increases mismatch in coefficient of thermal expansion (CTE)



BOARD LEVEL ASSEMBLY AND RELIABILITY CONSIDERATIONS FOR QFN TYPE PACKAGES, Ahmer Syed and WonJoon Kang, Amkor Technology.

Industry Testing of SJ Wearout

- JEDEC
  - Specification body for component manufacturers
- JEDEC JESD4747H, February 2011
  - Guidelines for new component qualification
  - Requires **2300** cycles of 0 to 100C
  - Testing is often done on **thin** boards

- IPC
  - Specification body for electronic OEMs
- IPC 9701A, February 2006
  - Recommends **6000** cycles of 0 to 100C
  - Test boards should be **similar thickness** as actual design

Industry and PoF

- VITA 51.2: Physics of Failure Reliability Predictions 2011
  - Established by the standard bodies responsible for VME technology (open system architecture of real-time, modular embedded computing)
  - VITA 51.2 provides rules and recommendations for the application of Physics of Failure (PoF) methods to reliability prediction of electronics at the board, packaging and component levels. It is a compilation in good faith, of existing physics of failure models selected by consensus of the working group of best practices in industry.
- IEC-TS-62239 2nd edition 2008: Process Management for Avionics
- FAA and Boeing expected to require PoF for IC wearout

Implementing DfR / PoF

- Many organizations have developed DfR Teams to speed implementation
  - Success is dependent upon team composition and gating functions

- Challenges: Classic design teams consist of electrical and mechanical engineers trained in the 'science of success'
  - PoF requires the right elements of personnel and tools

DfR / PoF Team

- Component engineer
- Mechanical / Materials engineer
- Electrical engineer
- Thermal engineer
  - Depending upon power requirements
- Reliability engineer?
  - Depends. Many classic reliability engineers provide **NO** value in the DfR / PoF process due to over-emphasis on statistical techniques and environmental testing

Component Selection

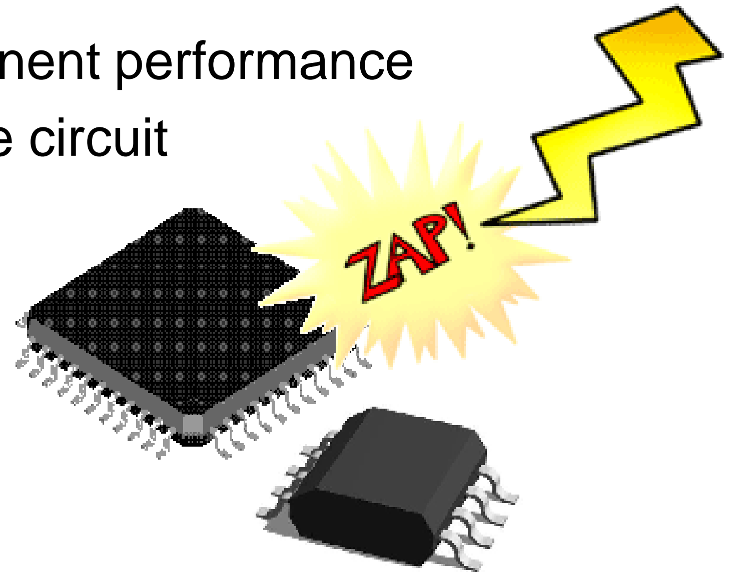
- The process of creating the bill of materials (BOM) during the ‘virtual’ design process
  - Before physical layout
- For some companies, this is during the creation of the approved vendor list (AVL)
  - Design-independent

Component Selection (continued)

- As technology progresses, functional performance has become a limited aspect of the part selection process
- Other concerns are increasingly taking center stage
  - Moisture sensitivity level (MSL)
  - Temperature sensitivity level
  - Electrostatic discharge (ESD) classification
  - Manufacturability (Design for Assembly)
  - Plating material
  - Lifetime / Long-term reliability
    - Sometimes Physics of Failure is required

Critical Components

- Most small to mid-size organizations do not have the resources to perform a thorough part selection assessment on every part
  - Does not excuse performing this activity
  - Requires focusing on components critical to the design
- Critical Components: A narrowed list of components of most concern to the OEM
  - Sensitivity of the circuit to component performance
  - Number of components within the circuit
  - Output from FMEA / FTA
  - Past experiences
  - Complexity of the component
  - Industry-wide experiences



Critical Components (Industry Experience)

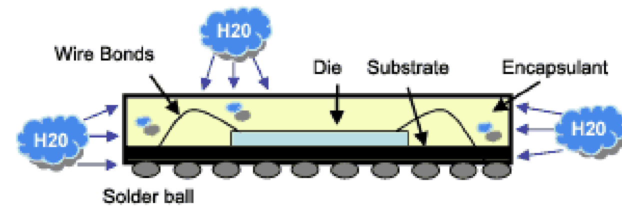
- Optoelectronics
  - High volume controls not always in place
  - Wearout can initiate far before 20 years
- Low volume or custom parts
  - Part is no longer a commodity item
- Memory devices
  - Non-volatile memory has limited data retention time and write cycles
- Parts with mechanical movements (switches, relays, potentiostats, fans)
  - Depending on environment, wear out can initiate far before 20 years
- Surface mount ceramic capacitors
  - Assembly issues

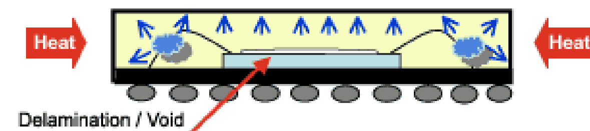
Critical Components (continued)

- New technologies or state-of-the-art
  - At the limit of the manufacturer's capabilities
  - MEMS, 45-nm technology, green materials, etc.
- Electronic modules
  - Part is a miniature assembly (no longer a commodity item)
- Power components
- Fuses
  - Susceptible to quality issues
- Electrolytic capacitors
  - Depending on environment, wear out can initiate far before 20 years

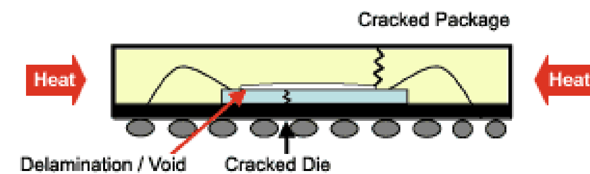
Popcorning

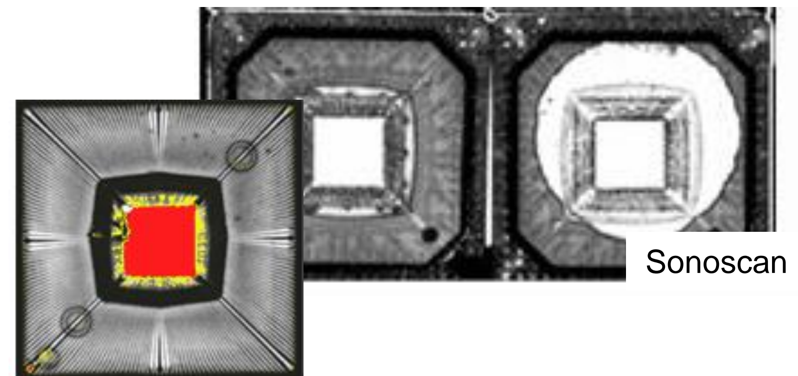
- Moisture can be absorbed by polymeric material during transportation, storage and handling
  - Epoxy encapsulant
  - Die attach
  - Printed substrate
- Trapped moisture can experience sudden liquid-gas phase transition during reflow
  - Sudden volume increase due to vaporization
- Cracking and delamination – sometimes accompanied by popping sound
- Driven by package design, materials, storage conditions and reflow parameters





Qualcomm

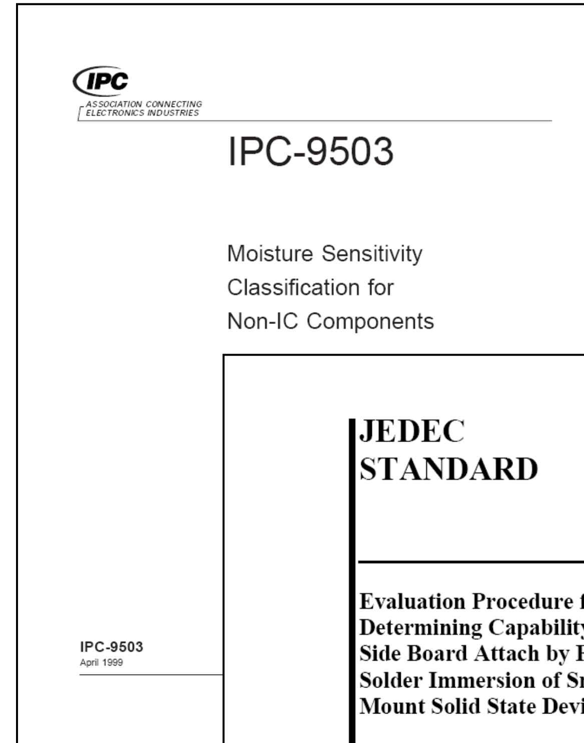


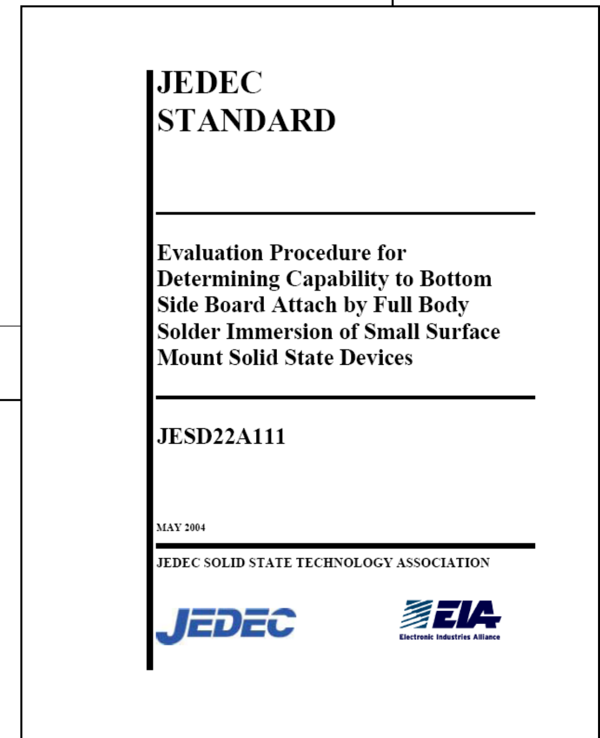


Sonoscan

MSL Issues and Actions (continued)

- Most 'standard' components have a maximum MSL 3
- Components with MSL 4 and higher
  - Large ball grid array (BGA) packages
  - Encapsulated magnetic components (chokes, transformers, etc.)
  - Optical components (transmitters, transceivers, sensors, etc.)
  - Modules (DC-DC converters, GPS, etc.)
- MSL classification scheme in J-STD-020D is only relevant to SMT packages with integrated circuits
  - Does not cover passives (IPC-9503) or wave soldering (JESD22A111)
  - If not defined by component manufacturer, requires additional characterization





Moisture Sensitivity Level (MSL)

- Popcorning controlled through moisture sensitivity levels (MSL)
  - Defined by IPC/JEDEC documents J-STD-020D and J-STD-033B
- Higher profile in the industry due to transition to Pb-free and more aggressive packaging
  - Higher die/package ratios
  - Multiple die (i.e., stacked die)
  - Larger components

LEVEL	FLOOR LIFE	
	TIME	CONDITIONS
1	Unlimited	≤30 °C/85% RH
2	1 year	≤30 °C/60% RH
2a	4 weeks	≤30 °C/60% RH
3	168 hours	≤30 °C/60% RH
4	72 hours	≤30 °C/60% RH
5	48 hours	≤30 °C/60% RH
5a	24 hours	≤30 °C/60% RH
6	Time on Label (TOL)	≤30 °C/60% RH

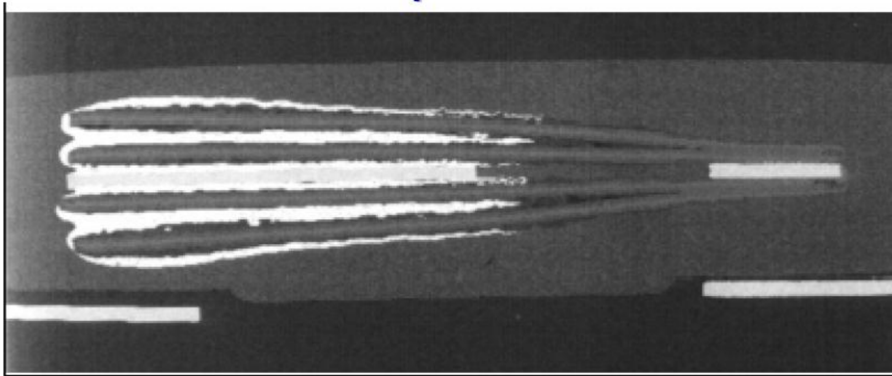
MSL: Typical Issues and Action Items

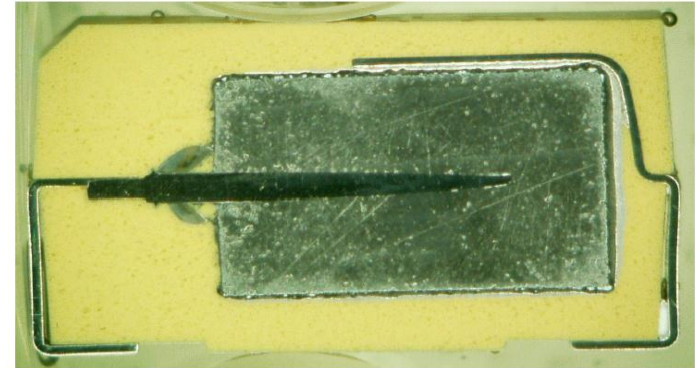
- Identify your maximum MSL
  - Driven by contract manufacturer (CM) capability and OEM risk aversion
  - Majority limit between MSL3 and MSL4 (survey of the MSD Council of SMTA, 2004)
  - High volume, low mix: tends towards MSL4
Low volume, high mix: tends towards MSL3
- Not all datasheets list MSL
  - Can be buried in reference or quality documents
- Ensure that listed MSL conforms to latest version of J-STD-020

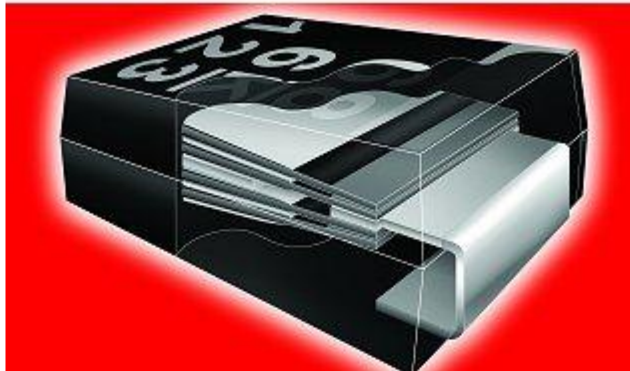
Highest Level Assembled :	
Don't know	26%
None used	4%
MSL 2A	4%
MSL 3	18%
MSL 4	18%
MSL 5	12%
MSL 5A	7%
MSL 6	10%

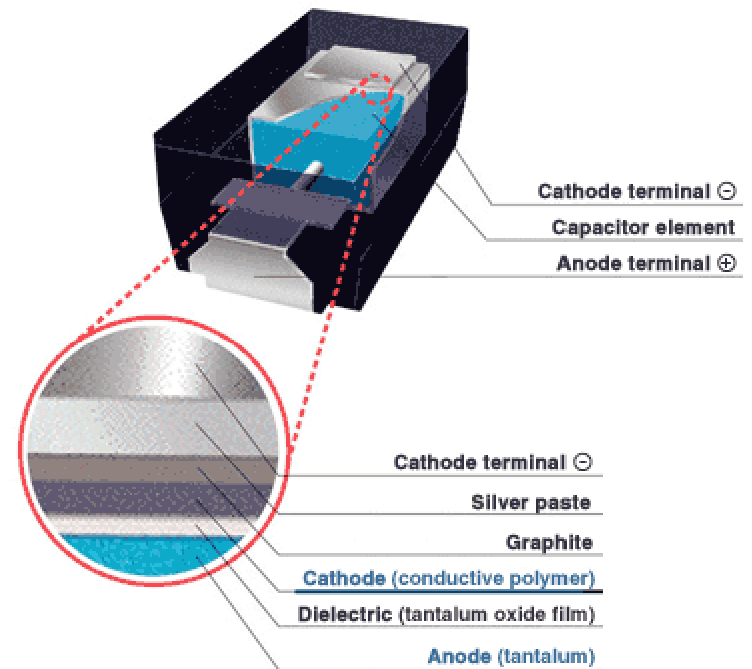
Cogiscan

Aluminum and Tantalum Polymer Capacitors







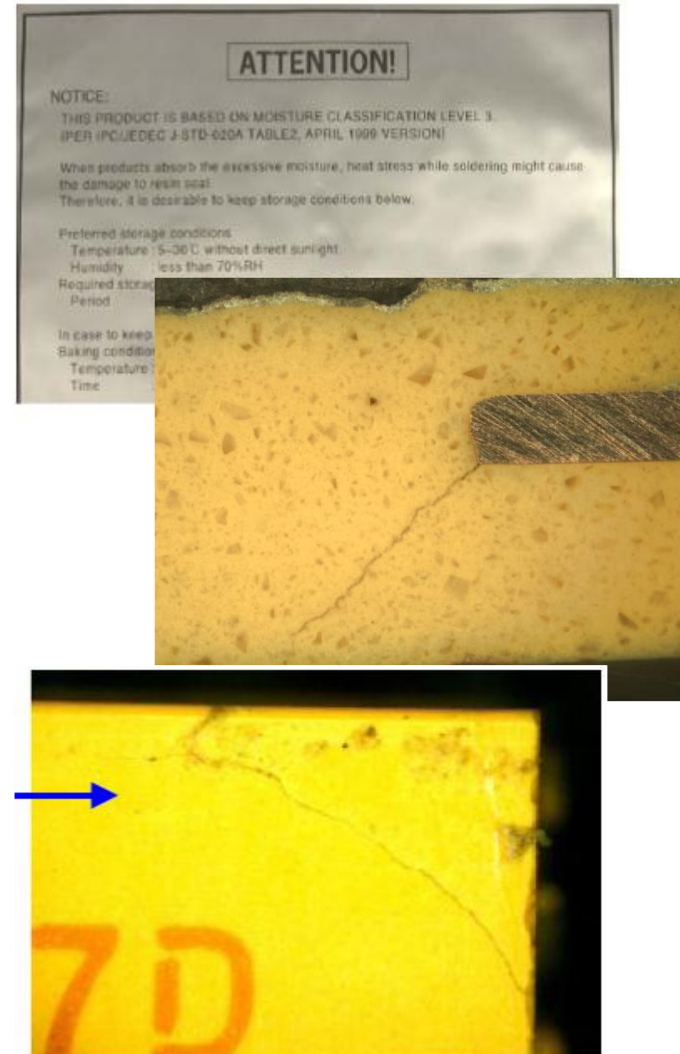


Aluminum Polymer Capacitor ↑

Tantalum Polymer Capacitor ↗

Popcorning in Tantalum/Polymer Capacitors

- Pb-free reflow is hotter
  - Increased susceptibility to popcorning
  - Tantalum/polymer capacitors are the primary risk
- Approach to labeling can be inconsistent
  - Aluminum Polymer are rated MSL 3 (SnPb)
  - Tantalum Polymer are stored in moisture proof bags (no MSL rating)
  - Approach to Tantalum is inconsistent (some packaged with dessicant; some not)
- Material issues
  - Aluminum Polymer are rated MSL 3 for eutectic (could be higher for Pb-free)
  - Sensitive conductive-polymer technology may prevent extensive changes
- Solutions
  - Confirm Pb-free MSL on incoming plastic encapsulated capacitors (PECs)
  - More rigorous inspection of PECs during initial build



Temperature Sensitivity

- Limits on process temperatures provided by component manufacturer
  - Components of concern with SnPb (220C peak) included RF devices and some optoelectronic components
- Broader issue due to introduction of Pb-free processes (260C peak)
  - Initially limited: SnPb reflow sensitive components, SMT connectors, ceramic capacitors, SMT electrolytic capacitors
- Primary issue for some OEMs
  - Current component packaging technology is insufficiently robust
  - Numerous components in a telecom / enterprise design now have peak temperatures below 260C

Component Selection for ESD

- Industry movement to decreasing feature sizes and high frequency technology
  - 90nm → 65nm → 45nm
  - GaAs / SiGe desirable at high GHz
- Increasing ESD risks
  - More parts are ESD susceptible
  - ESD sensitivity is increasing (is Class 0 still sufficient?)

Design for ESD Prevention: What Do You Need to Do?

- ESD Protection is necessary at the IC, component package and system level
  - Different approaches are needed to achieve reliable protection
- Designing for ESD impacts both the product design and the manufacturing process controls
- What technologies are available to assure a reliable ESD protected product?
  - At the IC level
  - At the component package level
  - At the system level

Good General Design Practices for ESD Prevention

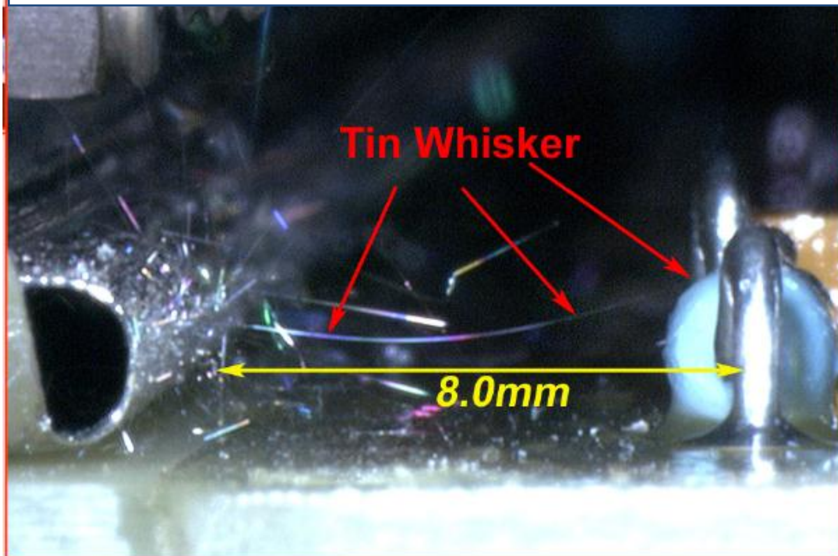
- Know the ESD rating for each part, and select parts (where possible) for the best ESD rating
  - Identify all ESD Sensitive Parts on drawings
  - Mark Locations of ESD Sensitive parts on the Board with the ESD symbol
- Consider the entire System (Design) as ESD Sensitive
- Use ESD Protection on all susceptible parts (not just System I/Os)
  - Box or System I/O
    - ESD Rating < Class 2 IEC 1000-4-2 (4000V) MANDATORY
  - Internal Components (not exposed to outside connectors)
    - ANSI/ESDA/JEDEC JS-001-2011, Human Body Model (HBM) - Component Level
      - ESD Rating <= Class 1 MANDATORY
      - ESD Rating < Class 2 WHEREVER POSSIBLE

DfR and Tin Whiskers

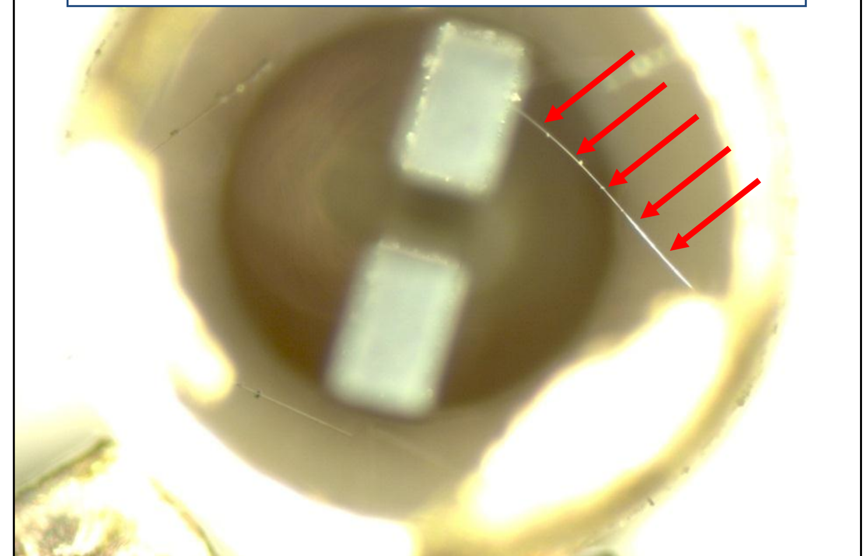
- The first step is to focus DfR on critical components
- Critical components are based upon three pieces of knowledge
  - The overwhelming majority of tin-plated electronic parts are matte tin over copper
  - Matte tin over copper produces whiskers of a finite length
  - Whiskers tend to only break off during handling

Where are the Scary Whiskers?

- When do really long whiskers occur?
  - Usually bright tin and/or plating over a substrate material other than copper (brass, bronze, steel, etc.)

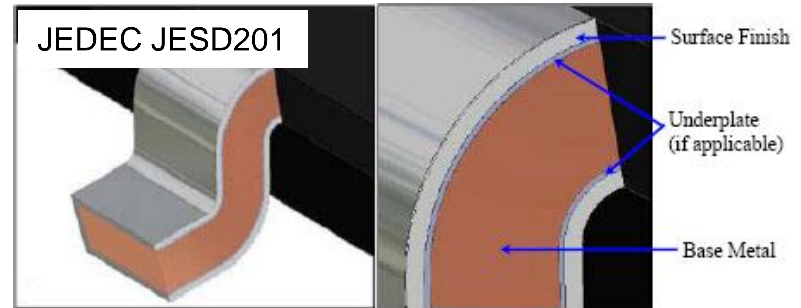


Tin (bright?) over steel

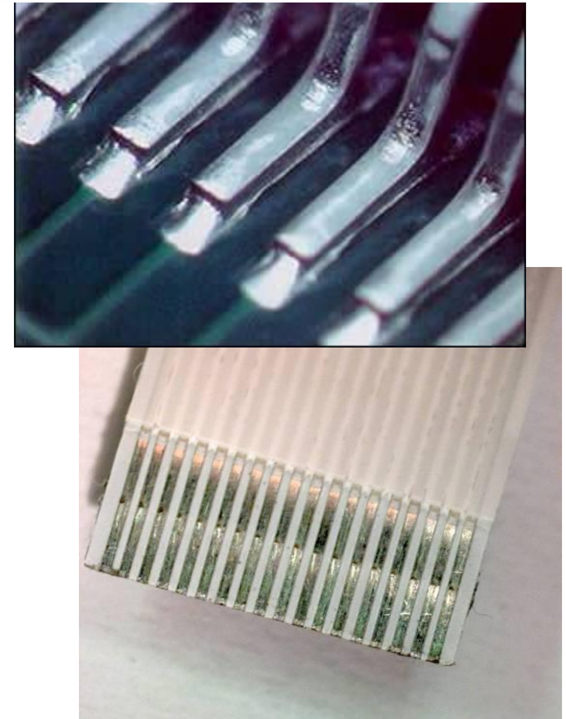


Tin (matte?) over brass

Critical Components



- Spacings of less than 500 microns
  - Parts with 0.8 mm lead pitch or less
  - 0201 chip components
  - Metal can housing
- Contact points (connector flex circuitry)
  - Stress gradients could change maximum length
- Welds (electrolytic capacitors)
  - Stress gradients could change maximum length



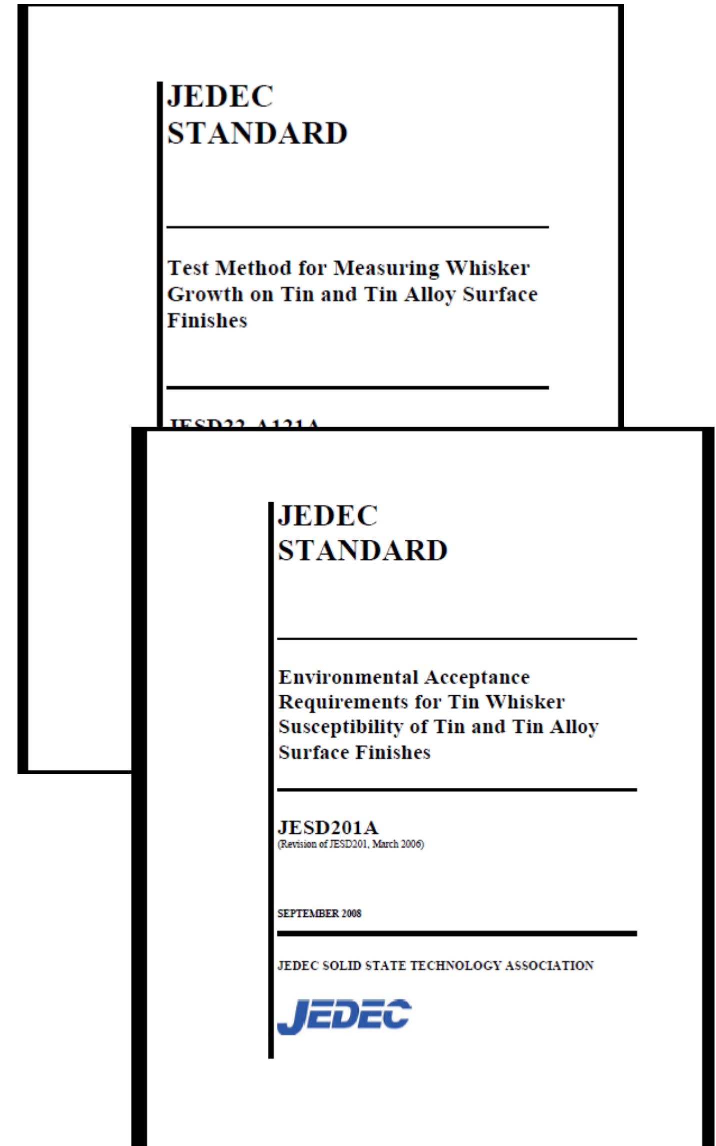
- Note: Some organizations specify the critical spacing as 350 microns
  - 0.65 mm pitch or less

How to Mitigate?

- There are three basic approaches to mitigation
- Data Gathering and Monitoring
- Part Manufacturer Mitigation
  - Steps offered by your suppliers
- Equipment Manufacturer (OEM) Mitigation
  - Steps you have to perform yourself

Data Gathering and Monitoring

- Driven by iNEMI and JEDEC (JESD22A121A, JESD201A, JP002)
- Industry recommended qualification tests
  - Ambient (30C/60%RH, 4000 hrs)
  - Elevated (55C/85%RH, 4000 hrs)
  - Cyclic (-40 to 85C, 1500 cycles)
  - Shorter test times for consumer products
- Use manufacturer's data, require third-party testing, or perform your own
  - Visual inspection should be performed properly
  - http://nepp.nasa.gov/whisker/background/index.htm#q6
- Few to no military/avionics manufacturers are using this approach



Part Manufacturer Mitigation

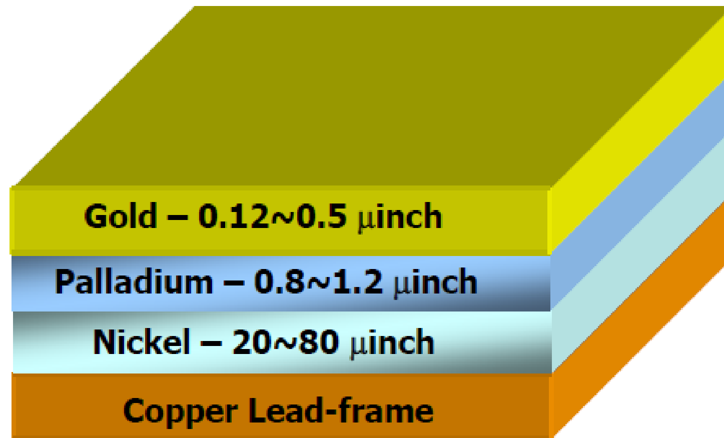
- Nickel underplate between the tin plating and the copper leadframe
  - Some question about effectiveness (IBM vs. TI)
  - Some question about minimum thickness
    - iNEMI (article) recommends 2 microns
    - ATIS requires 2 microns
    - PC manufacturer requires 1.2 microns
    - JP-002 March 2006 requires 0.5 microns
  - Might not help for ceramic substrate due to CTE mismatch
- Anneal for 1 hour at 150ºC within 24 hours of plating
  - This is the approach for Freescale
- Fusing (melting of tin through dipping in a hot oil bath)
  - Excellent field history; must be performed soon after plating
- Minimum plating thickness
  - Some question about minimum thickness
    - Telecom manufacturer requires 10 microns
    - JP-002 March 2006 recommends 7 microns minimum, 10 microns nominal

Part Manufacturer Mitigation (continued)

- Some component manufacturers claim proprietary whisker-free plating formulation
  - Be skeptical; require Statistical Process Control
- Tin bismuth alloy finishes
  - Mitigation not definitive
  - Low melting point of SnPbBi ternary might pose problems in mixed assemblies
    - Some experimental evidence suggests SnPb-plating and SnBi solder is a greater risk
- Request palladium (Pd) plating – NiPdAu
  - Increasingly offered as an option, even to low volume customers (medical, industrial controls, etc.)
  - Most manufacturers have moved to Pd as a standard plating for fine-pitch components

Leadframe Platings

Palladium and SnBi are seeing an increasing market share due to concerns with tin whiskering



Ni-Pd-Au Finish, Cypress Semiconductor

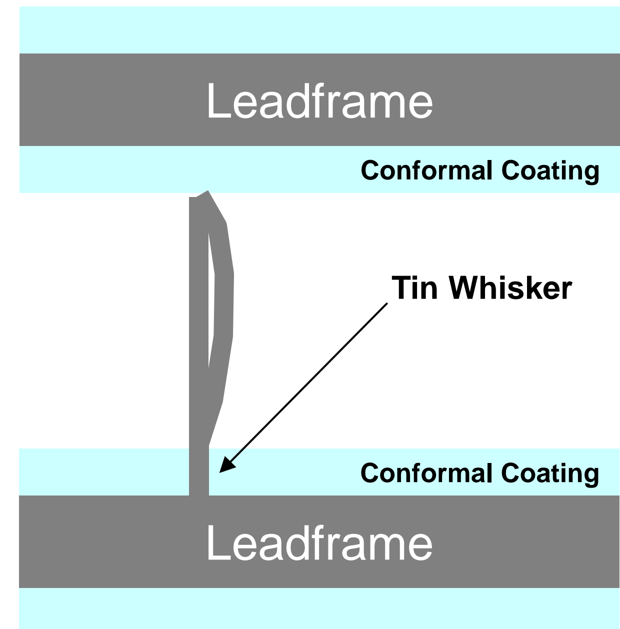
Company	Package	Plating
Intel	QFP / TSOP	Sn[1]
Samsung	QFP / TSOP	NiPdAu
Texas Instruments	QFP / TSOP	NiPdAu
Toshiba	TSOP (Discretes)	NiPdAu
	TSOP (Memory)	SnAg or SnCu
	TSOP (LSI)	NiPdAu or SnAg or SnBi
STMicroelectronics	QFP / TSOP	NiPdAu
Infineon	QFP	Sn or SnPb
	TSOP	NiPdAu
Renesas Technology	QFP	Mostly Sn-Cu, Sn-Bi; some NiPdAu
	TSOP	Mostly NiPdAu, with some Sn-Cu, Sn-Bi
Sony	QFP / TSOP	Pd or SnPb
Philips/NXP	QFP	Sn
	TSOP	NiPdAu
Hynix	TSOP	SnBi
Freescale	QFP / TSOP	Sn
NEC	QFP / TSOP	Sn, SnBi, or NiPdAu
Micron	TSOP	Sn, SnPb
Matsushita/Panasonic	QFP	Pd
	TSOP	SnBi
AMD	QFP	Sn, SnCu, or SnPb
IBM	QFP	N/A
Qualcomm	N/A	N/A
Fujitsu	QFP	SnBi
	TSOP	SnBi
Sharp	QFP	SnBi, NiPdAu
	TSOP	SnBi

OEM Mitigation

- Four Options
  - Procurement, Re-packaging, Post-plate or dip, Conformal coat
- Procurement / Design
  - Select only components with SnPb or Pd plating
  - May require complete change in circuit design if alternative component required
  - Rarely performed (functionality trumps reliability)
- Subcontract packaging or Re-packaging
  - SnPb or Pd plated leadframes
  - Rarely performed (cost, risk of damage)

Tin Whiskering – Conformal Coating

- Potential to provide a dual barrier
- Prevention or delay of whiskering
  - Some indication of a delay in whiskering (Rollins / Minter)
  - Short tin whiskers will eventually penetrate all current conformal coatings
  - No definitive trend in regards to coating properties
- Buckling
  - Based on calculations (Leidecker, NASA)
  - Not experimentally proven
- Limitations
  - Insufficient coverage at leads (gravity)
  - Problems with conformal coat may outweigh possible risk avoidance
- Current status:
  - Development of whisker-resistant coating
  - Assessment of single vs. double coating
  - http://nepp.nasa.gov/WHISKER/experiment/index.html



Component Selection (Misc)

Ceramic Capacitors (Cyclic Voltage)

http://www.avxcorp.com/docs/techinfo/parasitc.pdf

- Reports of field failures of MLCC in AC or pulsed DC voltage
- Piezoelectric effect
  - Variant voltage will vary internal stresses, potentially inducing fatigue behavior
  - With high frequency ripple current, capacitor can vibrate (resonate).
- Fatigued specimens can contain scattered microcracks
  - Decrease in capacitance; increase in leakage current
- Concern at hundreds of kHz
  - Decreases with increasing capacitance, X7R -> Y5V
  - Avoid or use AC-rated capacitors

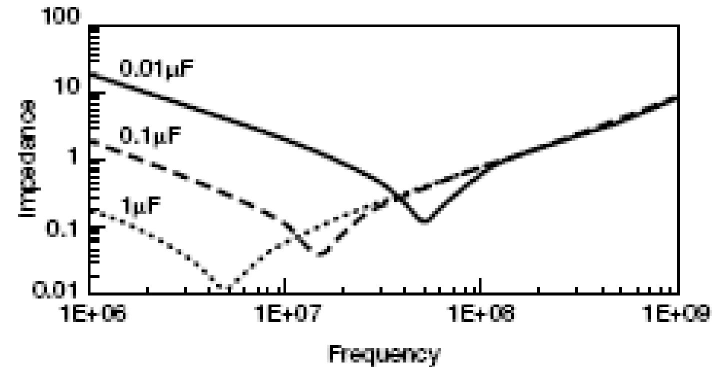


Figure 5. 1206, X7R impedance curves for a variety of capacitance values.

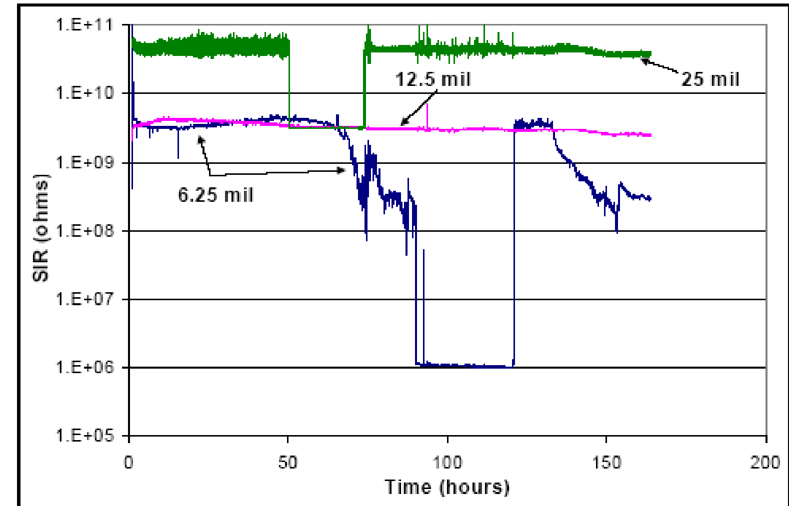
Case Size		Resonance Frequency
English	Metric	
3025	7563	250 - 750 kHz
2220	5750	300 - 900 kHz
1812	4532	400 - 1200 kHz
1210	3225	600 - 1200 kHz
1206	3216	600 - 1600 kHz
0805	2012	900 - 1800 kHz
0603	1608	N/A
0402	1005	N/A

Nippon Chemi-con, CAT.No.E1002I

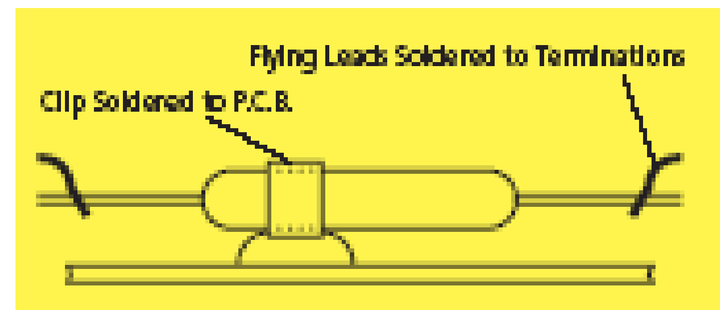
Sang-Joo Kim and Qing Jiangy, Microcracking and electric fatigue of polycrystalline ferroelectric ceramics, Smart Mater. Struct. 5 (1996)

Resistors (High Resistance)

- Board surfaces can be susceptible to periodic SIR drops
  - Especially with no-clean
  - Duration as short as 1 min
  - Down to 1 MegaOhm
  - Fine pitch, high voltage especially susceptible
- Can interfere with high resistance resistors
  - Especially chip resistors
  - Intermittent in nature
- Avoid values > 500 kOhms if used for sensing or calibration
  - Consider lower values in series
  - Use guard banding or cutouts

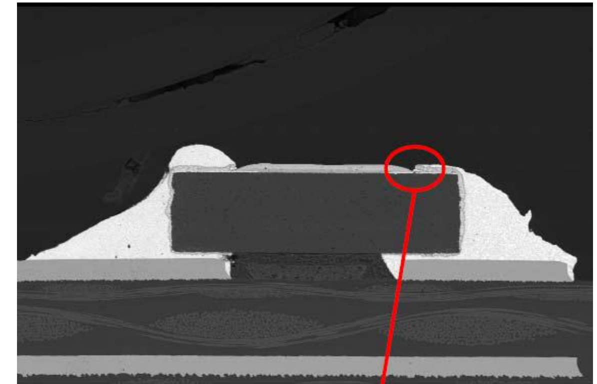


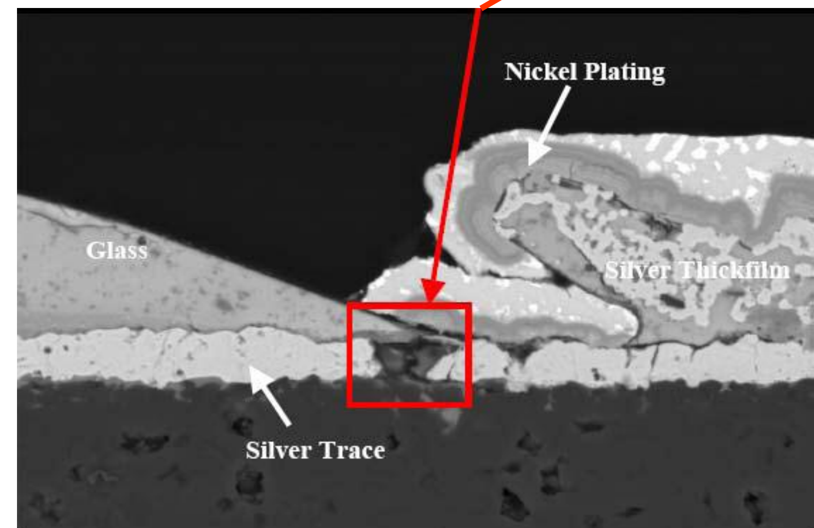
No-clean solder paste, 40/93 at 24 VDC



Sulfide Corrosion of Thick Film Resistors

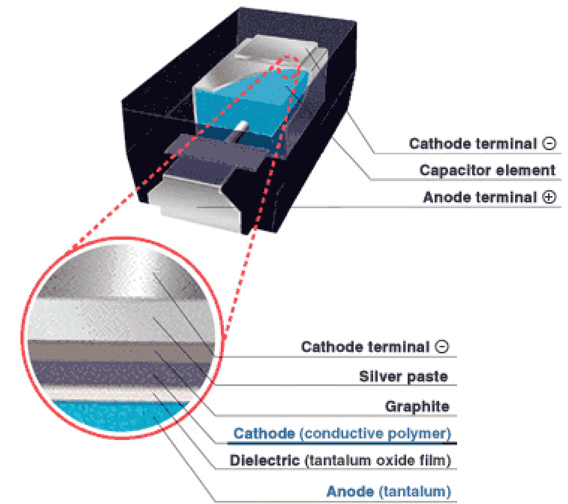
- Sulfur dioxide (SO_2) and hydrogen sulfide (H_2SO_4) in environment
  - Sources: Black rubber, industrial pollution
  - Attacks silver material under passivation/ termination
  - Creates nonconductive silver sulfide
- Drivers
  - Cracking/separation of coating/termination
    - Poor manufacturing
    - Thermal shock
  - Potting or conformal coating
    - Seems to act as a ‘sponge’
    - Holds SO_2 molecules in place
- Electrical opens within 1-4 years
- Avoidance
  - Orient parallel to solder wave
    - Entrance side can experience thermal shock
  - Avoid hand soldering/rework
  - Sulfur-resistant PdAg material (KOA)





Tantalum and Polymeric Capacitors

- Tantalum capacitors are selected for volumetric efficiency
- Older technology can be susceptible to ignition
  - Requires aggressive derating (50% or greater)
  - Sensitive to higher temperatures (>85C) and certain circuits
- Newer, polymeric capacitors are available
  - Significant reduction in ESR
  - Less derating
  - No risk of ignition



	MnO_2 (27Batches)	Ta-Poly KO (37 Batches)	Alum-Poly – AO (78 Batches)
100 PPM FR % V_{Rated}	68%	114%	235%
@50% V_{Rated} FR(PPM)	9	0	0
@80% V_{Rated} FR(PPM)	458	5	0
@90% V_{Rated} FR(PPM)	1,700	19	0
@100% V_{Rated} FR(PPM)	2,943	255	0

Electrolytic Capacitors

- Voltage
  - Maintain a minimum of 25-33% of rated voltage (maintains the dielectric)
- Temperature
  - Maintain adequate distance from 'hot' components
    - Power resistors, IGBTs, etc.
    - Seems to accelerate time to failure and can induce explosive rupturing
  - 105C rated capacitors can be an issue at lower temperatures (below -40C)
    - ESR increases 500X; capacitance decreases 80-90%
- Ripple Current
  - Up to 100% or greater of rated ripple current
  - Need to calculate/measure case temperature rise
  - Equivalency on bill of materials is often not maintained
- Equivalent Series Resistance (ESR)
  - Often not specified on the component data sheet

Separable Connectors

- Separable Connectors
  - One of the most common failure sites
  - First thing maintenance checks (plug / unplug)
- Hardware Design Rules
  - Blind insertion increases risk of damage or mismating (consider flex or rigid-flex)
  - All connectors should be keyed
    - Prevents reversal of I/O pins
  - Use positively retained connectors
  - Avoid use of sockets
- Specify material and thickness

Separable Connectors [Gold (Au)]

- Connections and environments
  - Hi-speed digital or critical connections
  - Low voltage (< 5V), low current (< 10mA)
  - Corrosive environment (gases such as H_2S, SO_2, Cl_2)
  - Risk of micromotion (< 2.5 µm)

- Material specifications
  - Be-Cu or P-bronze base pins
  - Nickel underplate (250 min)
  - Soft gold (Au) plating
  - 10 min (single insertion); 30 min (50 insertions); 70 min (hi-rel)
  - Porosity spec
  - No gold flash

- Contact specifications
  - 50-100 grams contact force
  - Minimum of 2 contacts; 4 preferred
  - Adequate contact wipe – 0.010” min.
  - No mating with tin plating

Separable Connectors [Tin (Sn)]

- Connections and environment
  - Power connections
  - Benign
- Tin plating design specification
  - 100 grams-force, 100 microinches (Tin Commandments)

DfR (Miscellaneous)

- Components taller then 1 inch
  - Use of staking compound to adhere to board

Component Selection
(Lifetime)

Component Lifetime

- What parts are susceptible to long-term degradation in electronic designs?
  - **Ceramic Capacitors (oxygen vacancy migration)**
  - Memory Devices (limited write cycles, read times)
  - **Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)**
  - Resistors (if improperly derated)
  - Silver-Based Platings (if exposed to corrosive environments)*
  - Relays and other Electromechanical Components
  - **Light Emitting Diodes (LEDs) and Laser Diodes**
  - Connectors (if improperly specified and designed)*
  - Tin Whiskers*
  - **Integrated Circuits (EM, TDDB, HCI, NBTI)**
  - **Interconnects (Creep, Fatigue)**
    - **Plated through holes**
    - **Solder joints**

Industry-accepted models exist
*Already discussed

Lifetime Example: Memory Devices

- Limited lifetime based on read-write cycles and retention time

Parameter	Minimum Guarantee	Units
Endurance	100,000	Data changes per bit
Store cycles	1,000,000	Store cycles
Data retention	100	Years

- Some memory devices provide data retention time for different operating temperatures (20 years at 125°C and 10 years at 150°C).

Light and Laser Diode Wearout

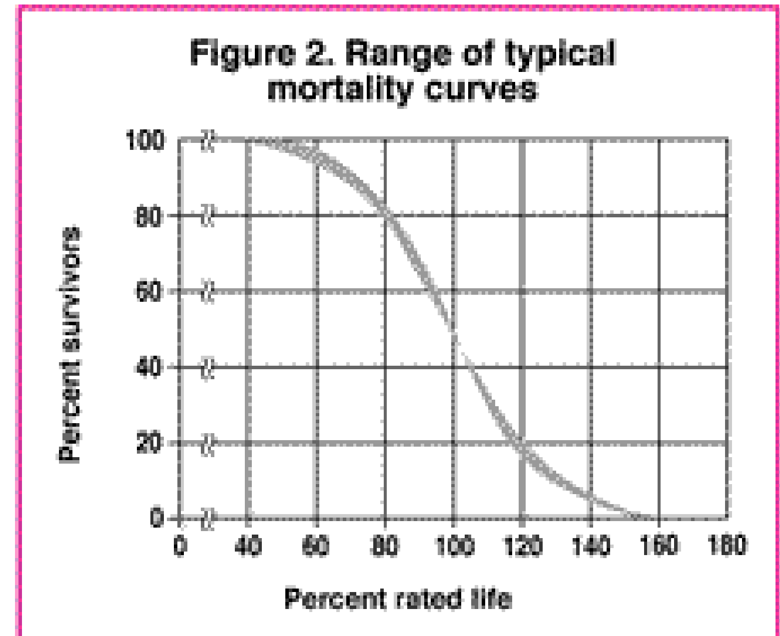
- Increasing importance with adoption of optical communications and LCD backlight
- Standard model for on-die wearout is:

$$t_f = A(J)^n \exp\left(\frac{E_a}{kT}\right)$$

- where A is a constant, J is the current density, n is an exponent
  - n =1.5 - 2 for a large number of different LED structures
  - n = 6 – 7 for laser diodes with facet passivation
- Expression applies for units run in automatic current control (ACC), or constant current.
  - Units run at constant output power (APC), power substitutes current density (n may be higher)
  - Some models will combine power and current density
- Note: Model does not apply to die attach fatigue
  - A risk in high power, cyclic applications

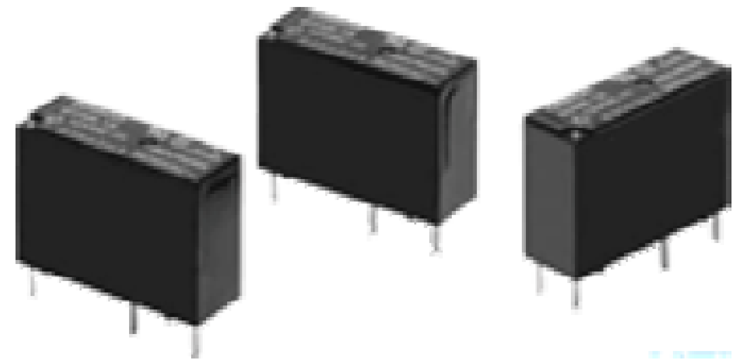
Light and Laser Diode Wearout

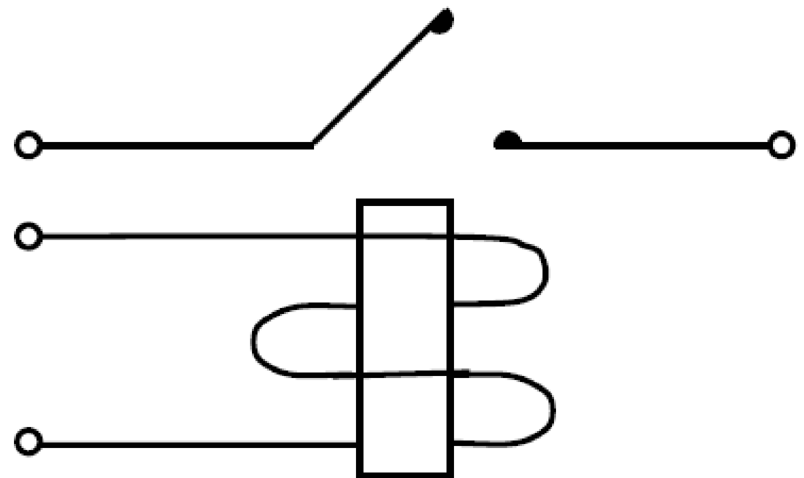
- Estimated lifetime is not always provided
- When lifetime is provided, it is MTBF at room temp.
  - Time to 5% failure can be half the time
  - Time to failure at 40C can be half the time
  - 50K hrs can turn into 12.5K hrs
- Lifetime is not always be equivalent to failure
  - 50% reduction in intensity



Lifetime Example: Relays/Switches

- Relays are an electromechanical switch
- Minimum of four I/Os
  - Control voltage
  - Signal voltage
- What are the major concerns in regards to relay reliability?
  - Number of cycles to failure
  - Long-term non-use
  - Power dissipation and contact resistance (heating and voltage drops)

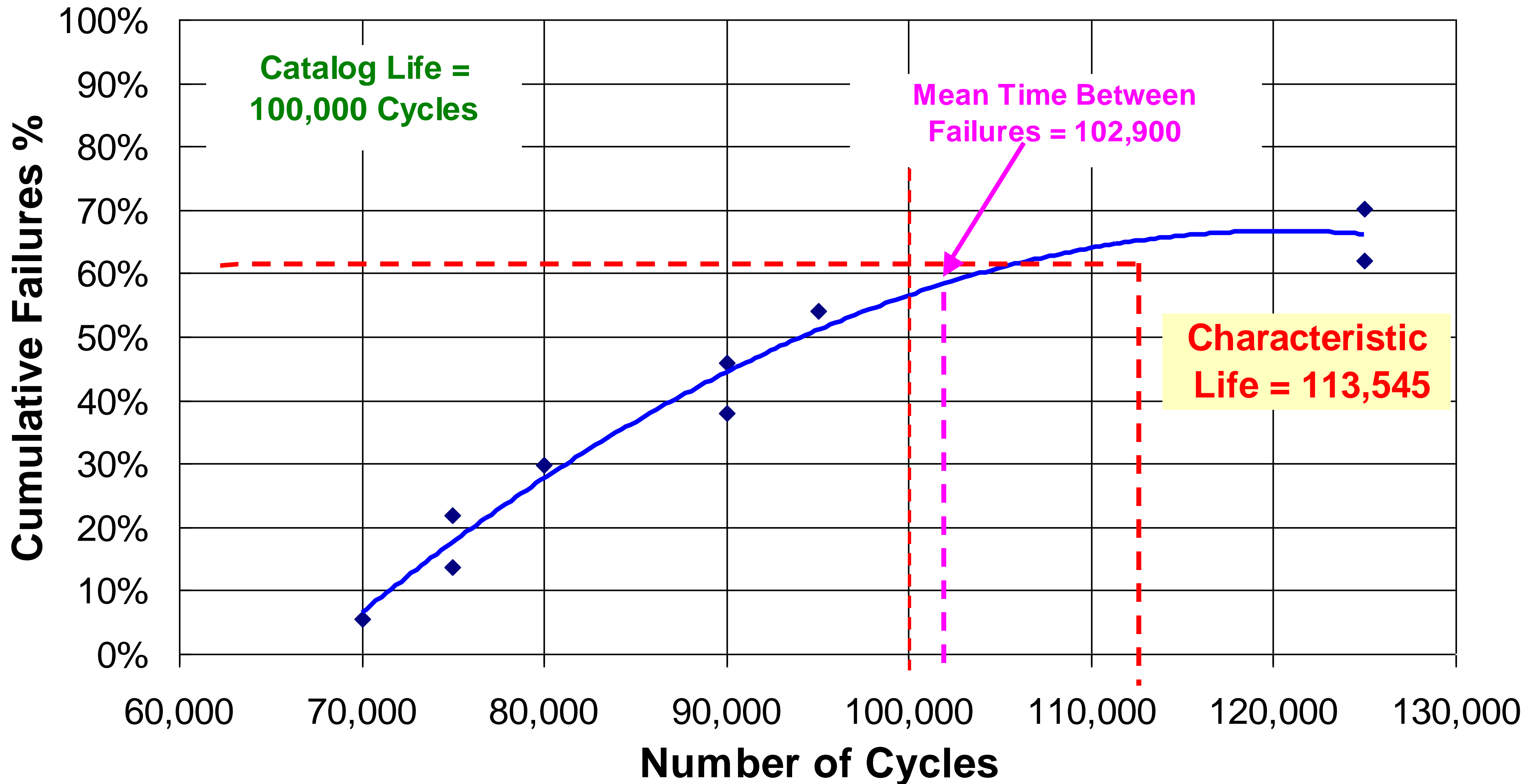




Relays/Switches (continued)

- Selection of appropriate plating
  - Idle for long periods of time: Gold contacts
  - Numerous cycles: AgCd contacts
- Sealed packages if cleaning operations
- Use of protective devices
  - Diode, resistor, capacitor, varistor, etc.
  - Prevents arcing during switching (accelerates degradation)
  - Must be nearby
- Temperature rise
  - Wide range of contact resistance in specifications
- Ensure margin between design life requirements and manufacturer's specifications

Wearout of Relays/Switches



Derating and Uprating

Component Ratings

- Definition
  - A specification provided by component manufacturers that guides the user as to the appropriate range of stresses over which the component is guaranteed to function
- Typical parameters
  - Voltage
  - Current
  - Power
  - Temperature

MSP430FG43x
MIXED SIGNAL MICROCONTROLLER

SLAS380B – APRIL 2004 – REVISED JUNE 2007

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} .... –0.3 V to 4.1 V
Voltage applied to any pin (see Note) .... –0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . ... ±2 mA
Storage temperature, T_{stg}: (unprogrammed device) .... –55°C to 150°C
(programmed device) .... –40°C to 85°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

	MIN	NOM	MAX	UNITS
Supply voltage during program execution (see Note 1), V_{CC} ($AV_{CC} = DV_{CC1/2} = V_{CC}$)	1.8		3.6	V
Supply voltage during program execution, SVS enabled, PORON=1 (see Note 1 and Note 2), V_{CC} ($AV_{CC} = DV_{CC1/2} = V_{CC}$)	2		3.6	V
Supply voltage during flash memory programming (see Note 1), V_{CC} ($AV_{CC} = DV_{CC1/2} = V_{CC}$)	2.7		3.6	V
Supply voltage, V_{SS} ($AV_{SS} = DV_{SS1/2} = V_{SS}$)	0		0	V
Operating free-air temperature range, T_A	–40		85	°C

IGBT MODULE (U series)
600V / 100A / PIM

■ **Features**
- Low $V_{CE(sat)}$
- Compact Package
- P.C. Board Mount Module
- Converter Diode Bridge Dynamic Brake Circuit

■ **Maximum ratings and characteristics**

● **Absolute maximum ratings (Tc=25°C unless otherwise specified)**

Item		Symbol	Condition	Rating	Unit
Inverter	Collector-Emitter voltage	V_{CES}		600	V
	Gate-Emitter voltage	V_{GES}		±20	V
	Collector current	I_C	Continuous	100	A
		I_{CP}	1ms	200	A
		$-I_C$		100	A
		$-I_C$ pulse	1ms	200	
	Collector power disspation	P_C	1 device	378	W
Brake	Collector-Emitter voltage	V_{CES}		600	V
	Gate-Emitter voltage	V_{GES}		±20	V
	Collector current	I_C	Continuous	50	A
		I_{CP}	1ms	100	A
	Collector power disspation	P_C	1 device	187	W
	Repetitive peak reverse voltage	V_{RRM}		600	V
Converter	Repetitive peak reverse voltage	V_{RRM}		800	V
	Average output current	I_O	50Hz/60Hz sine wave	100	A
	Surge current (Non-Repetitive)	I_{FSM}	Tj=150°C, 10ms half sine wave	700	A
	I^2t (Non-Repetitive)	I^2t		2450	A^2s
Operating junction temperature		T_j		+150	°C
Storage temperature		T_{stg}		-40 to +125	°C
Isolation voltage	between terminal and copper base *2	V_{iso}	AC : 1 minute	AC 2500	V
	between thermistor and others *3			AC 2500	V
Mounting screw torque				3.5 *1	N·m

smthybridpackaging

Derating

- Derating is the practice of limiting stress on electronic parts to levels below the manufacturer's specified ratings
  - Guidelines can vary based upon environment ("severe, protected, normal" or "space, aircraft, ground")
  - One of the most common design for reliability (DfR) methods
- Goals of derating
  - Maintain critical parameters during operation (i.e., functionality)
  - Provide a margin of safety from deviant lots
  - Achieve desired operating life (i.e., reliability)
- Sources of derating guidelines
  - Governmental organizations and 3rd parties
  - OEM's
  - Component manufacturers
- Derating is assessed through component stress analysis

Derating Guidelines (Examples)

Part Type	Derating parameters	Severe	Benign
Aluminium electrolytic caps	Voltage (% max rated)	70%	80%
	Temperature (°C)	T_{max} – 20°C	T_{max} – 20°C
Ceramic capacitors	Voltage (% max rated)	60%	70%
	Temperature (°C)	T_{max} – 10°C	T_{max} – 10°C
Solid tantalum capacitors	Voltage (% max rated)	70%	80%
	Temperature (°C)	T_{max} – 20°C	T_{max} – 20°C
	Reverse voltage (% max fwd)	2%	2%
Signal diodes	Forward current (% max rated)	90%	<100%
	Reverse voltage (% max rated)	70%	80%
	Max. junction temperature	95°C	115°C
Chip resistors	Power dissipation(% max rated)	50%	70%
Digital MOS and bipolar ICs	Fanout (% max rated)	90%	<100%
	Frequency (% max rated)	90%	<100%
	Output current (% max rated)	90%	<100%
	Max. junction temperature	95°C	115°C
Linear MOS and bipolar ICs	Frequency (% max rated)	90%	<100%
	Output current (% max rated)	90%	<100%
	Max. junction temperature	95°C	115°C

Criticality of Component Stress Analysis

- Failure to perform component stress analysis can result in higher warranty costs, potential recalls
  - Eventual costs can be in the millions of dollars
- Perspective from Chief Technologist at major Original Design Manufacturer (ODM)

"…based on our experience, we believe a significant number of field returns, and the majority of no-trouble-founds (NTFs), are related to overstressed components."

Derating Failures

- Where are the derating mistakes?
- Problem #1: Designers do not derate
  - Failure to perform component stress analysis
- Problem #2: Derating does not have a practical or scientific foundation
  - Extraordinary measures are taken when inappropriate
  - Derating is excessive: ‘The more, the better’ rule

Failure to Derate

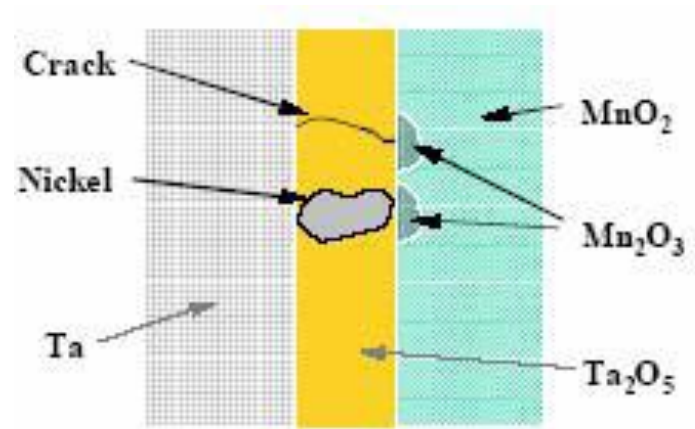
- Analog / Power Designs
  - Derating is typically overlooked during transient events
  - Especially turn-on, turn-off
- Digital
  - Excessive number of components and connections tends to limit attempts to perform component stress analysis

The Foundation of Derating

- To be effective, derating must have a practical and scientific foundation
  - Problem: Manufacturer's ratings are not always based on a practical and scientific foundation
- Manufacturers' viewpoint
  - Ratings are based on specific design rules based on materials, process, and reliability testing
- The reality
  - Ratings can be driven by tradition and market forces as much as science
- Best practice
  - Based on data from field returns
  - Based on test to failure qualification (especially for new suppliers)

Scientific Approach to Derating (Ta Caps)

High Impedance Circuits

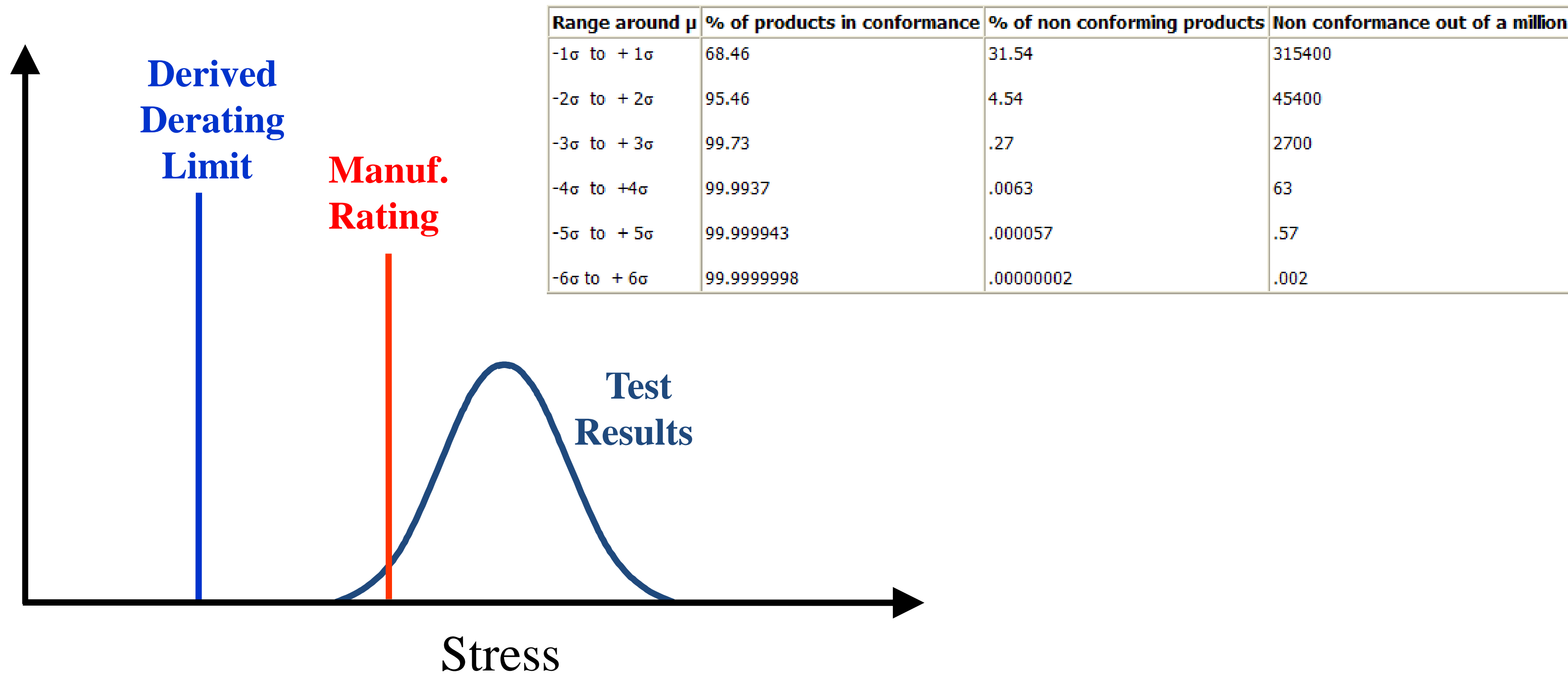


- Self healing in Ta capacitors involves leakage paths in the MnO_2 being healed by the transformation to the higher resistance compound Mn_2O_3
- Process requires enough current to allow internal temperatures to reach 500°C
- Small amounts of current (< 50 uA) will prevent self healing
  - Leads to degradation and potential component failure
- Avoid use in circuits with impedances greater than 100 kΩ

Derating Decision Tree

- Step 1: Derating guidelines should be based on component performance, not ratings
  - Test to failure approach (i.e., HALT of components)
  - Quantifies life cycle cost tradeoffs
  - For smaller OEMs, limit this practice to critical components

Derating based on Test to Failure



Range around μ	% of products in conformance	% of non conforming products	Non conformance out of a million
-1σ to +1σ	68.46	31.54	315400
-2σ to +2σ	95.46	4.54	45400
-3σ to +3σ	99.73	.27	2700
-4σ to +4σ	99.9937	.0063	63
-5σ to +5σ	99.999943	.000057	.57
-6σ to +6σ	99.9999998	.00000002	.002

- OEM was concerned with voltage rating of tantalum capacitors after 2 reflows and use on low resistance line
- Performed step stress surge test (SSST)
- Derived voltage derating based on a sub-ppm failure rate

Derating Decision Tree (continued)

- Step 2: Derating guidelines should be based on recommendations from the component manufacturer
  - They built it; they should know it
  - Don't trust the manufacturer? Use someone else
- Step 3: Derating guidelines should be based on customer requirements
- Step 4: Derating guidelines should be based industry-accepted specification/standard

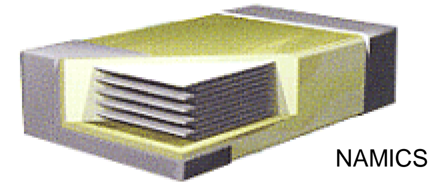
Be flexible, not absolute

Robustness - Components

- Concerns
  - Potential for latent defects after exposure to Pb-free reflow temperatures
  - 215°C - 220°C peak → 240°C - 260°C peak
- Drivers
  - Initial observations of deformed or damaged components
  - Failure of component manufacturers to update specifications
- Components of particular interest
  - Aluminum electrolytic capacitors
  - Ceramic chip capacitors
  - Surface mount connectors
  - Specialty components (RF, optoelectronic, etc.)

Ceramic Capacitors (Thermal Shock Cracks)

- Due to excessive change in temperature
  - Reflow, cleaning, wave solder, rework
  - Inability of capacitor to relieve stresses during transient conditions.
- Maximum tensile stress occurs near end of termination
  - Determined through transient thermal analyses
  - Model results validated through sectioning of ceramic capacitors exposed to thermal shock conditions
- Three manifestations
  - Visually detectable (rare)
  - Electrically detectable
  - Microcrack (worst-case)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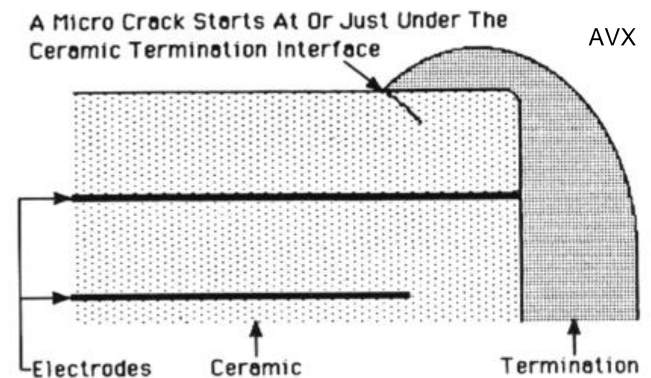
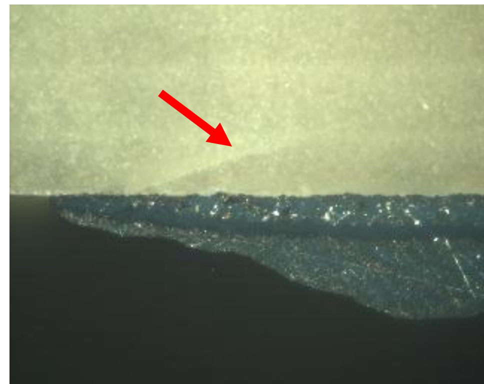
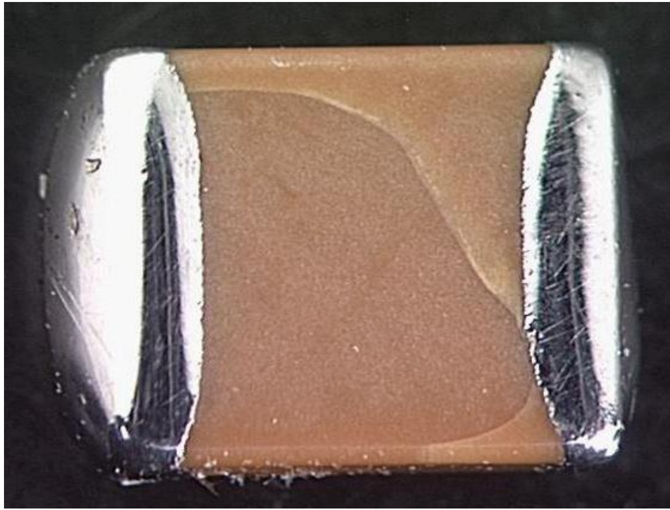
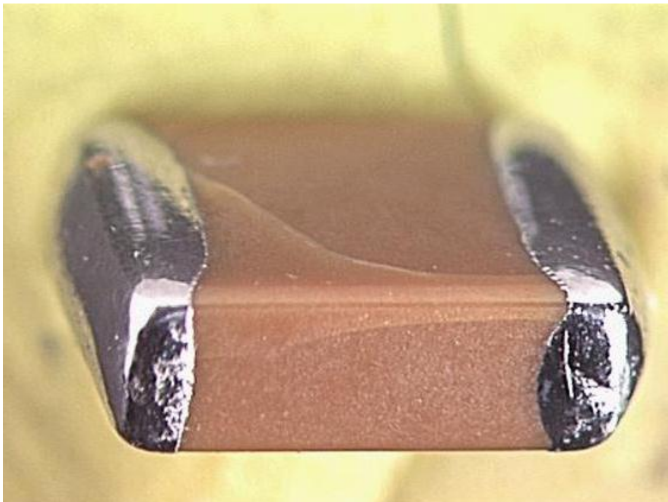


AVX



Thermal Shock Crack: Visually Detectable





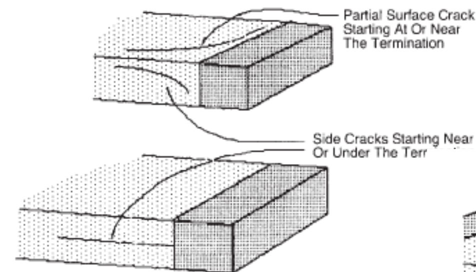


Figure 5. Extreme Thermal Shock Cracks in MLCs

AVX

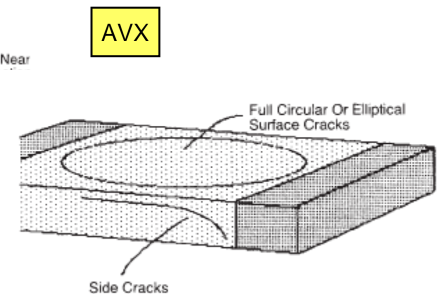
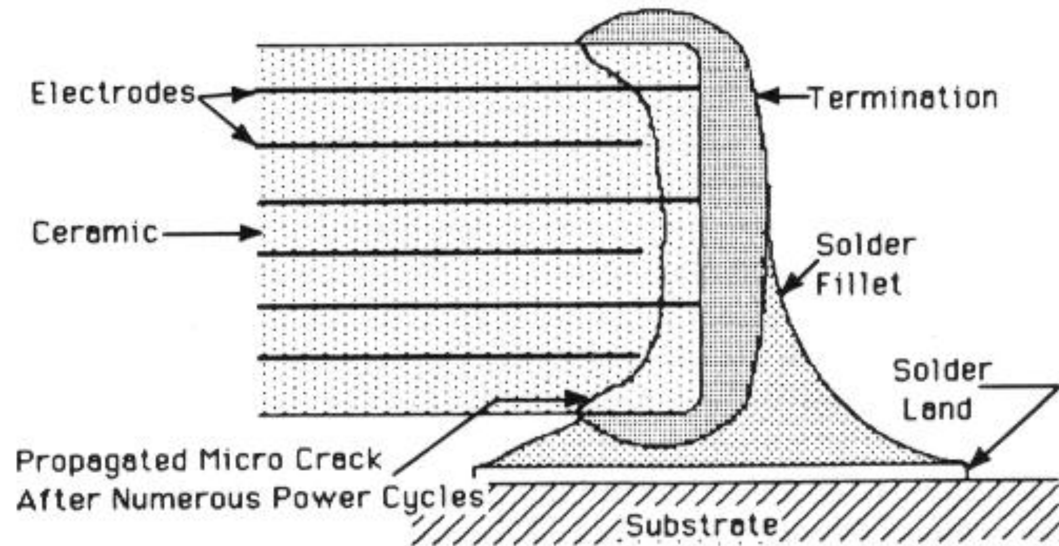
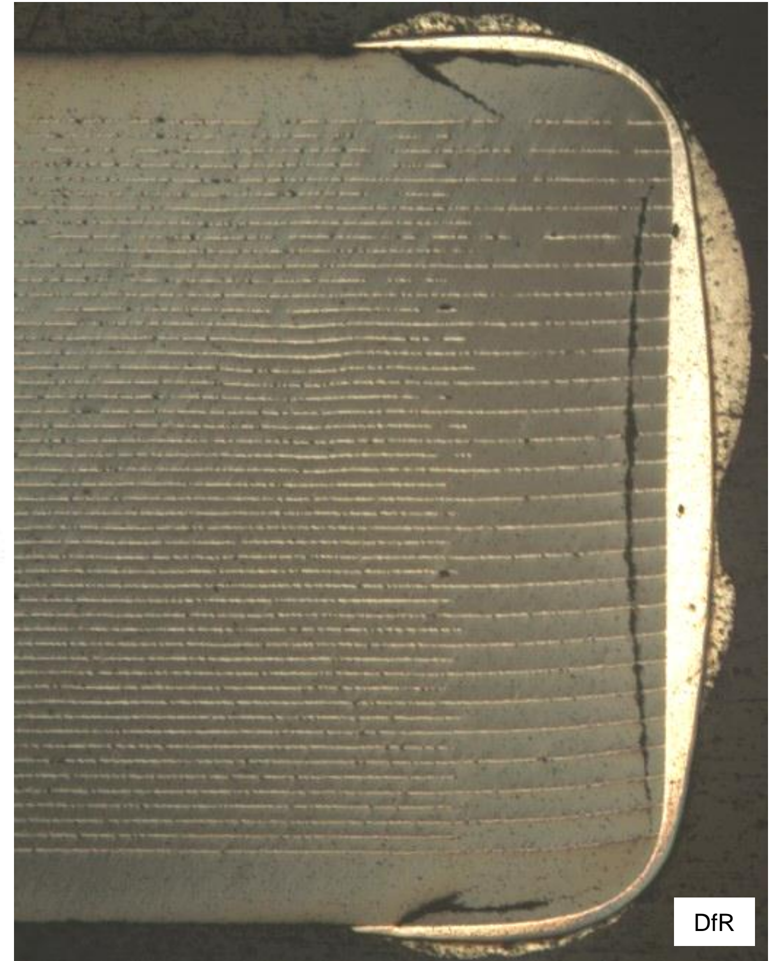


Figure 6. Severe Thermal Shock Cracks in Large MLCs

Thermal Shock Crack: Micro Crack





- Variations in voltage or temperature will drive crack propagation
- Induces a different failure mode
  - Increase in electrical resistance or decrease capacitance

Actions: Design

- Orient terminations parallel to wave solder
- Avoid certain dimensions and materials (wave soldering)
  - Maximum case size for SnPb: 1210
  - Maximum case size for SAC305: 0805
  - Maximum thickness: 1.2 mm
  - C0G, X7R preferred
- Adequate spacing from hand soldering operations
- Use manufacturer's recommended bond pad dimensions or smaller (wave soldering)
  - Smaller bond pads reduce rate of thermal transfer

Actions: Manufacturing

- Solder reflow
  - Room temperature to preheat (max 2-3oC/sec)
  - Preheat to at least 150oC
  - Preheat to maximum temperature (max 4-5oC/sec)
  - Cooling (max 2-3oC/sec)
    - In conflict with profile from J-STD-020C (6oC/sec)
  - Make sure assembly is less than 60oC before cleaning
- Wave soldering
  - Maintain belt speeds to a maximum of 1.2 to 1.5 meters/minute
- Touch up
  - Eliminate

Module 3: Mechanisms and Physics of Failure (PoF)

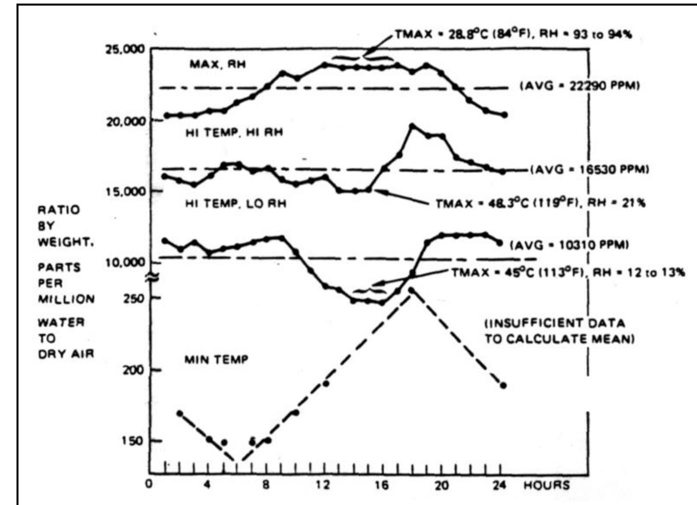
Examples: Desired Lifetime

- Low-End Consumer Products (Toys, etc.)
  - Do they ever work?
- Cell Phones: 18 to 36 months
- Laptop Computers: 24 to 36 months
- Desktop Computers: 24 to 60 months
- Medical (External): 5 to 10 years
- Medical (Internal): 7 years
- High-End Servers: 7 to 10 years
- Industrial Controls: 7 to 15 years
- Appliances: 7 to 15 years
- Automotive: 10 to 15 years (warranty)
- Avionics (Civil): 10 to 20 years
- Avionics (Military): 10 to 30 years
- Telecommunications: 10 to 30 years

Identify Field Environment

- Approach 1: Use of industry/military specifications
  - MIL-STD-810,
  - MIL-HDBK-310,
  - SAE J1211,
  - IPC-SM-785,
  - Telcordia GR3108,
  - IEC 60721-3, etc.
- Advantages
  - No additional cost!
  - Sometimes very comprehensive
  - Agreement throughout the industry
  - Missing information? Consider standards from other industries
- Disadvantages
  - Most more than 20 years old
  - Always less or greater than actual (by how much, unknown)

MIL HDBK310



USE CATEGORY	WORST-CASE USE ENVIRONMENT Tmin °C	Tmax °C	ΔT(1) °C	t_D hrs	Cycles/ year	Typical Years of Service	Approx. Accept. Failure Risk, %	ACCELERATED TESTING Tmin °C	Tmax °C	ΔT(2) °C	t_D min
1) CONSUMER	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) COMPUTERS	+15	+60	20	2	1460	5	0.1	+25	+100	75	15
3) TELECOM	- 40	+85	35	12	365	7-20	0.01	0	+100	100	15
4) COMMERCIAL AIRCRAFT	-55	+95	20	12	365	20	0.001	0	+100	100	15
5) INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1	0	+100	100 & COLD(3)	15
6) MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	10	0.1	0	+100	100 & COLD(3)	15
7) SPACE leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0.001	0	+100	100 & COLD(3)	15
8) MILITARY AVIONICS a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01	0	+100	100 & COLD(3)	15
9) AUTOMOTIVE UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0.1	0	+100	100	15

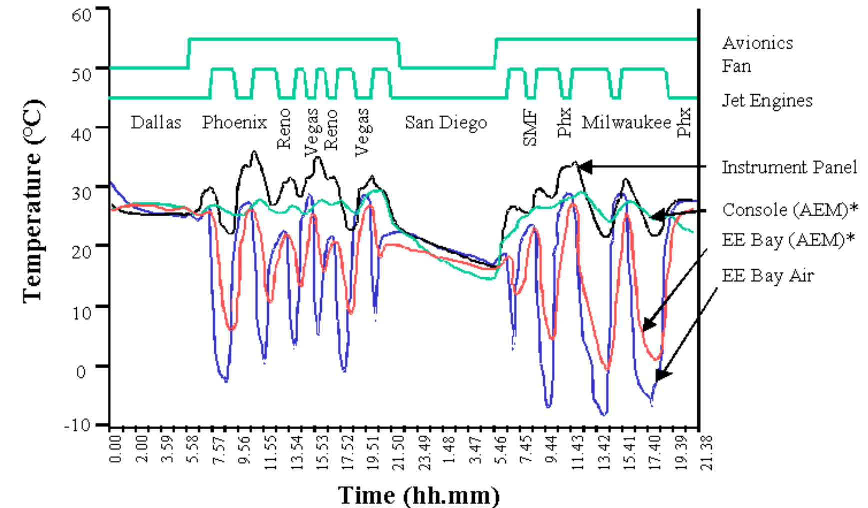
IPC SM785

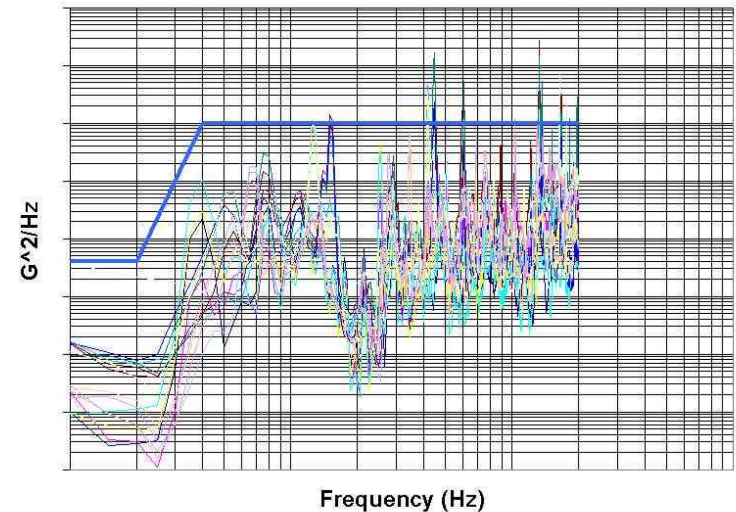
Field Environment (continued)

- Approach 2: Based on actual measurements of similar products in similar environments
  – Determine average and realistic worst-case
  – Identify all failure-inducing loads
  – Include <u>all</u> environments
    - Manufacturing
    - Transportation
    - Storage
    - Field

Failure Inducing Loads

- Temperature Cycling
  - Tmax, Tmin, dwell, ramp times
- Sustained Temperature
  - T and exposure time
- Humidity
  - Controlled, condensation
- Corrosion
  - Salt, corrosive gases (Cl_2, etc.)
- Power cycling
  - Duty cycles, power dissipation
- Electrical Loads
  - Voltage, current, current density
  - Static and transient
- Electrical Noise
- Mechanical Bending (Static and Cyclic)
  - Board-level strain
- Random Vibration
  - PSD, exposure time, kurtosis
- Harmonic Vibration
  - G and frequency
- Mechanical shock
  - G, wave form, # of events





Field Environment (Best Practice)

- Use standards when…
  - Certain aspects of your environment are common
  - No access to use environment
- Measure when…
  - Certain aspects of your environment are unique
  - Strong relationship with customer
- Do not mistake test specifications for the actual use environment
  - Common mistake with vibration loads

PoF and Wearout

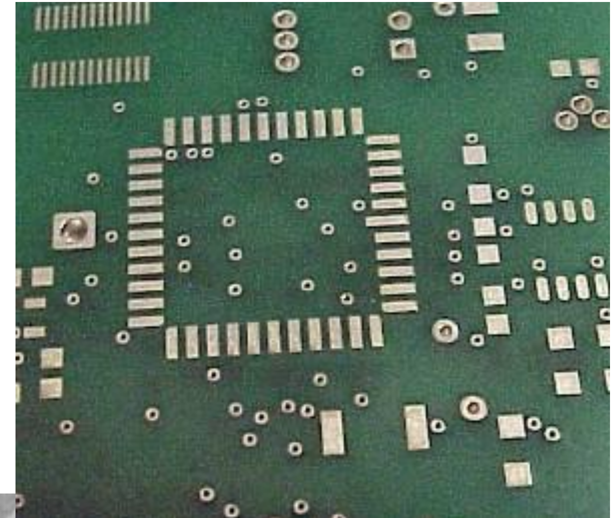
- What is susceptible to long-term degradation in electronic designs?
  - Ceramic Capacitors (dielectric breakdown)
  - Electrolytic Capacitors (electrolyte evaporation, dielectric dissolution)
  - Resistors (if improperly derated)
  - Silver-Based Platings (if exposed to corrosive environments)
  - Relays and other Electromechanical Components (wearout models not well developed)
  - Connectors (if improperly specified and designed)
  - Tin Whiskers
  - Integrated Circuits (next generation feature size)
  - Interconnects (Creep, Fatigue)
    - Plated through holes
    - Solder joints

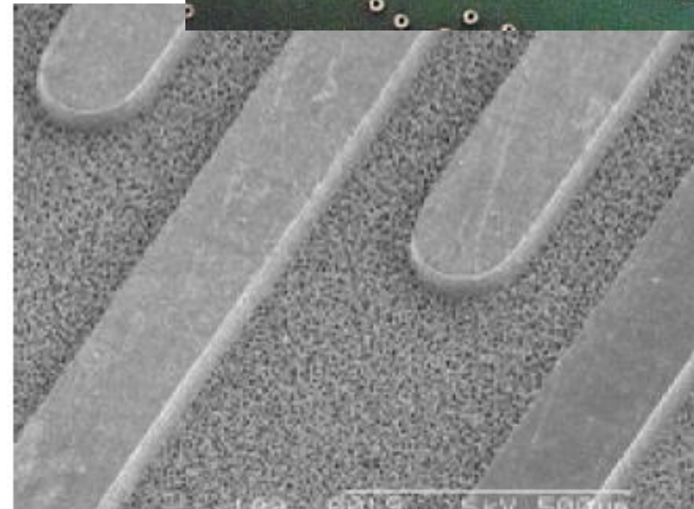
PoF Example: Silver and Sulfur

- Immersion silver (ImAg) introduced in the 1990's as the 'universal finish'

- Benefits
  - Excellent flatness, low cost, long-term storage

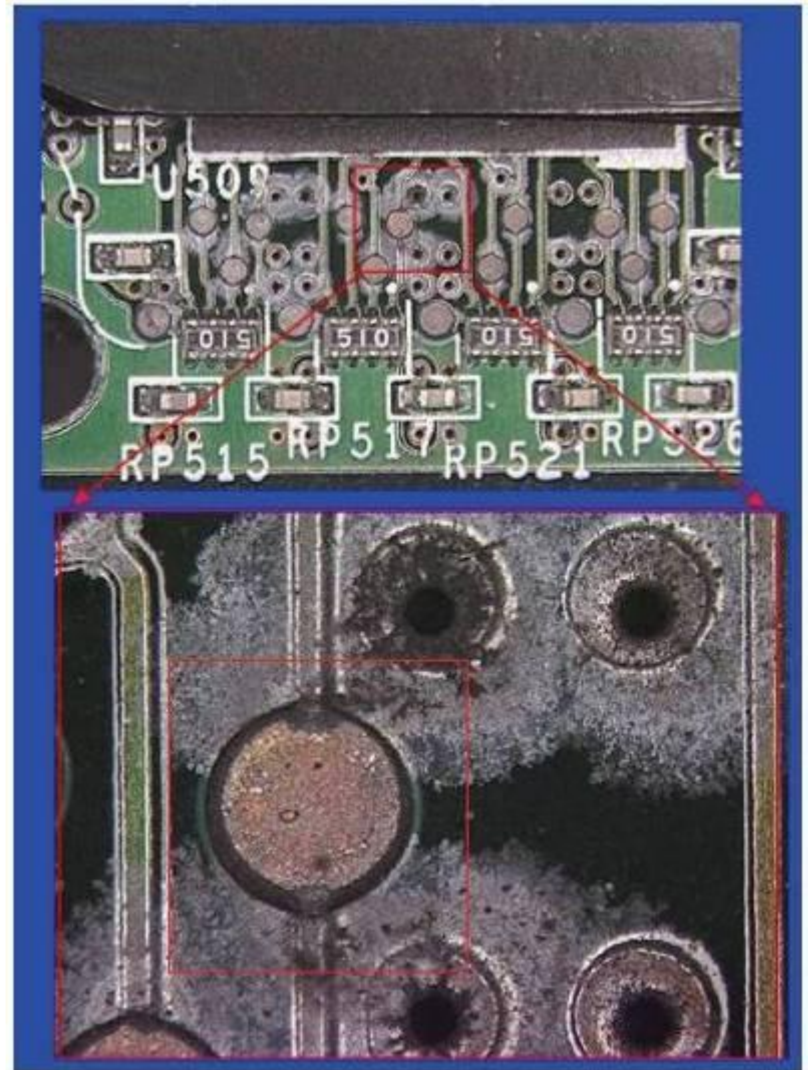
- Problem
  - Sulfur reacts with silver
  - Induces creeping corrosion





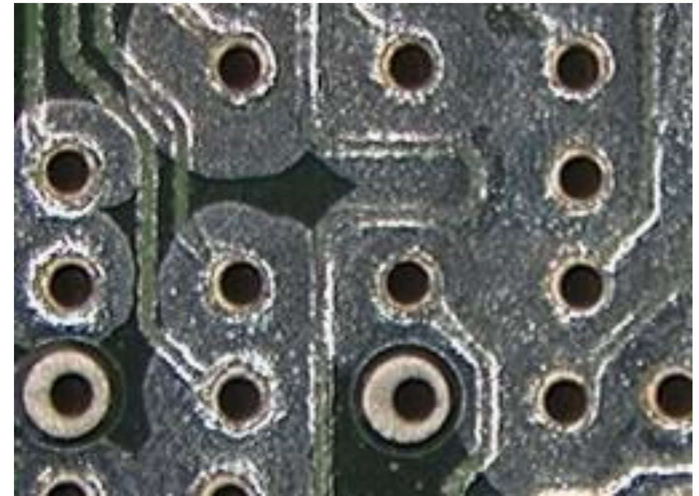
ImAg (Creeping Corrosion)

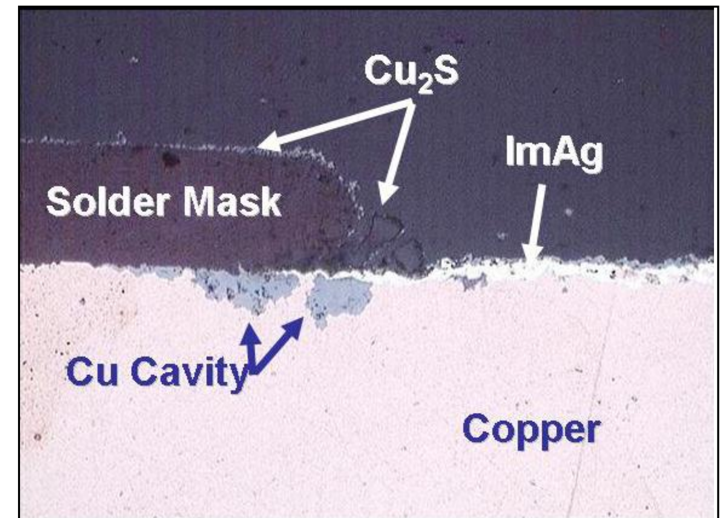
- Failures observed within months
  - Sulfur-based gases attacked exposed immersion silver
  - Non-directional migration (creeping corrosion)
- Occurred primarily in environments with high sulfur levels
  - Rubber manufacturing
  - Gasoline refineries
  - Waste treatment plants



Findings

- Analysis identified copper as the creeping element (not silver)
- Cross-sections identified corrosion sites near areas with no or minimal immersion silver
  - Galvanic reaction was initiating and accelerating corrosion behavior
- What went wrong?





PoF and Testing

- Failure #1
  - Test coupons were not representative of actual product
  - No solder mask defined pads, no plated through holes
- Failure #2
  - Industry test environments are limited to 70%RH (chamber limitations)
  - Actual use environment can be more severe

Conditions	Temp (°C)	RH (%)	H_2S (ppb)	Cl_2 (ppb)	NO_2 (ppb)	SO_2 (ppb)
Indoor	30±1	70±2	10±1.5	10±1.5	200±30	100±15
Outdoor	30±1	70±2	100±15	20±3	200±30	200±30

Telcordia

PoF and Immersion Silver

- The Final Failure?
- Acknowledging the reactivity of silver with sulfur and moving beyond 'test to spec' to truly capture potential risks
  - The 'physics' was not well enough understood before the new material was released

Alternatives to PoF

- Step 1: Rules of Thumb
- Step 2: Best Practice
  - Follow part selection guidelines
- Step 3: Norris-Landsberg

Rules of Thumb (Constant Temperature)

- Electrolytic Capacitor lifetime becomes an issue when ambient temperatures begin to exceed 40C on a constant basis
  - 85C/2000 hour ratings tend to be insufficient for more than 5 year life
- Many companies limit solder joint temperature to a maximum of 75°C – 85°C
  - Some limit IC junction temperature to a similar range

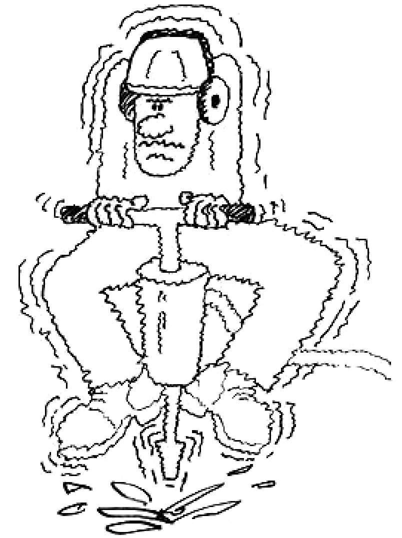
Rules of Thumb (Temperature Cycling)

- In nominal environments, solder joint wearout is unlikely
  - Low power, diurnal cycling
  - Δ25C, 1 cycle per day
  - Lifetime of less than 10 years
- Greater concerns in more severe environments
  - Diurnal heat sources with sufficient fluctuation (Δ40C)
  - Diurnal power dissipation of Δ40C and greater
  - Power cycling greater than 4 cycles/day (mini-cycling)

Rules of Thumb (Temp Cycling)(cont.)

- If a solder joint fatigue is a concern, manage package styles
  - MELF parts (SMA and SMB available)
  - Crystals on ceramic substrates (especially large ones)
  - Chip resistors greater than 1812 or capacitors greater than 2225
  - Large memory devices (44, 56, 66 I/O) with Alloy 42 leadframes
  - Large I/O (≥ 44) quad flat pack no-lead (QFN)

Rules of Thumb (Vibration)



- Maintain high board natural frequency
  - Two to three times greater than lo frequency peaks (>250-300 Hz)
  - Use of attachments, stiffer rail guides
- When peaks in the power spectral density (PSD) curve exceeds 0.01 G^2/Hz
  - Lower threshold for higher frequency peaks

Vibration (continued)

- Failures primarily occur when peak loads occur at similar frequencies as the natural frequency of the product / design
- Natural frequencies
  - Larger boards, simply supported: 60 – 150 Hz
  - Smaller boards, wedge locked: 200 – 500 Hz
  - Gold wire bonds: 2k – 4kHz
  - Aluminum wire bonds: >10kHz

Norris-Lanzberg (SnPb)

$$AF = \frac{N_o}{N_t} = \left(\frac{f_o}{f_t}\right)^{1/3} \left(\frac{\Delta T_t}{\Delta T_o}\right)^2 \exp\left[1414\left(\frac{1}{T_{\max,o}} - \frac{1}{T_{\max,t}}\right)\right]$$

- f is cycling frequency, DT is change in temperature, and T_{max} is the maximum temperature
  - "o" refers to operating environment and "t" refers to test environment
- Provides comparison of test results to field reliability
  - Usable if the component manufacturer provides accelerated life testing (ALT) results for 2nd level interconnects
  - Warning: Component manufacturers can cheat (use very thin boards)
- Can not provide an absolute prediction

Norris-Lanzberg (SAC)

$$AF = \frac{N_o}{N_t} = \left(\frac{\Delta T_t}{\Delta T_o}\right)^{2.65} \left(\frac{t_t}{t_o}\right)^{0.136} \exp\left\{2185\left(\frac{1}{T_{\max,o}} - \frac{1}{T_{\max,t}}\right)\right\}$$

- t is the hot-side dwell time, DT is change in temperature, and T_{max} is the maximum temperature
  - "o" refers to operating environment and "t" refers to test environment
- Not yet widely accepted
  - Found to be inaccurate within some datasets

[1] N. Pan et al, "An Acceleration Model For Sn-Ag-Cu Solder Joint Reliability Under Various Thermal Cycle Conditions". pp. 876-883, SMTAI, September 2005, Chicago, IL

Long-Term Reliability

- Rules of Thumb, Best Practices, and Norris-Landzberg are not always sufficient
  - Good first pass
- When the risk is too high, physics of failure (PoF) calculations are irreplaceable

PoF Example: SnAgCu Life Model

- Modified Engelmaier
  - Semi-empirical analytical approach
  - Energy based fatigue
- Determine the strain range (Dg)

$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T$$

- C is a correction factor that is a function of dwell time and temperature, L_D is diagonal distance, a is CTE, DT is temperature cycle, h is solder joint height

PoF Example – SAC Model (cont.)

- Determine the shear force applied to the solder joint

$$(\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \cdot \left(\frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2 - \nu}{9 \cdot G_b a} \right) \right)$$

  - F is shear force, L is length, E is elastic modulus, A is the area, h is thickness, G is shear modulus, and a is edge length of bond pad
  - Subscripts: 1 is component, 2 is board, s is solder joint, c is bond pad, and b is board
- Takes into consideration foundation stiffness and both shear and axial loads

PoF Example – SAC Model (cont.)

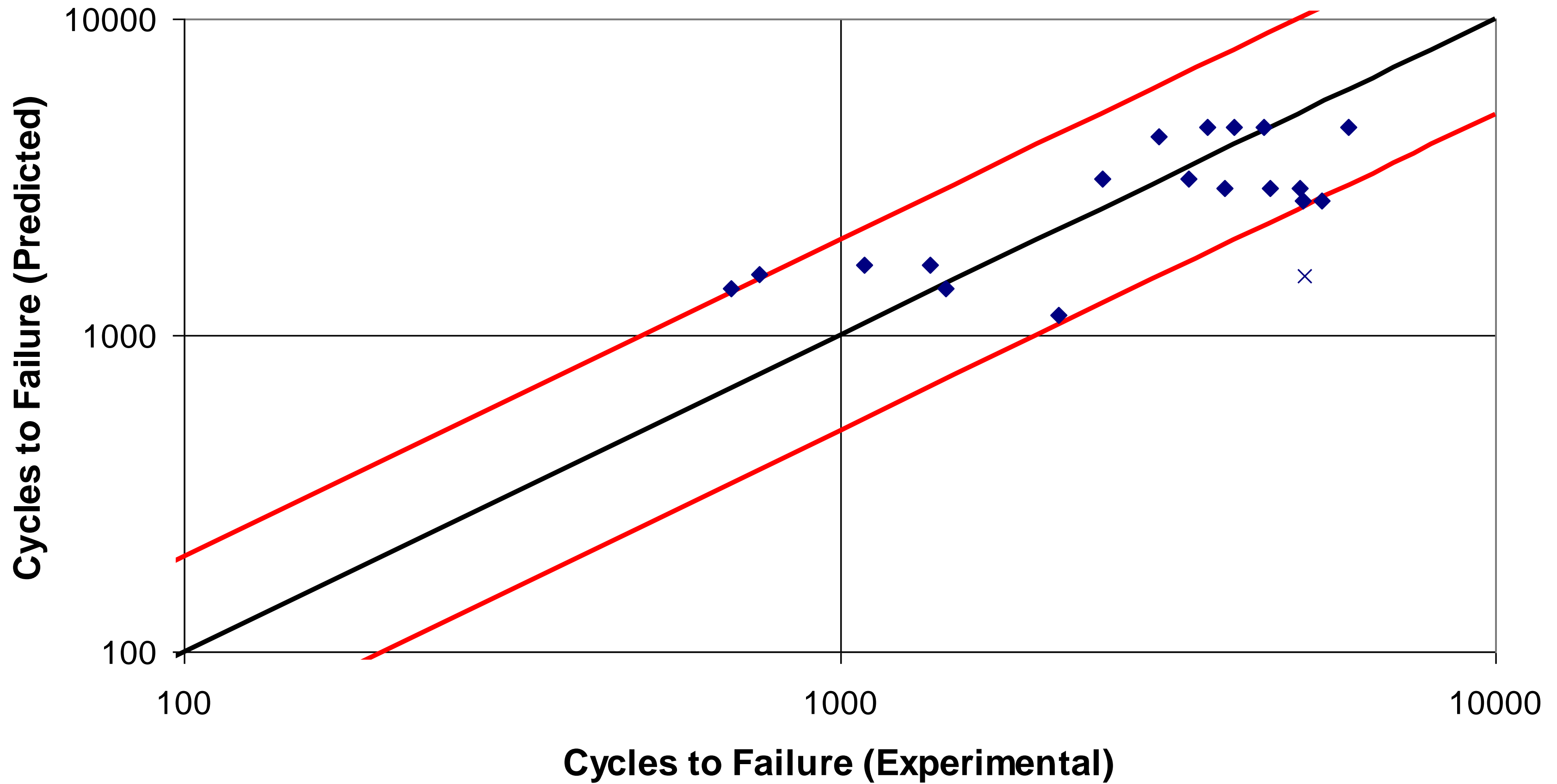
- Determine the strain energy dissipated by the solder joint

$$\Delta W = 0.5 \cdot \Delta\gamma \cdot \frac{F}{A_s}$$

- Calculate cycles-to-failure (N_{50}), using energy based fatigue models for SAC developed by Syed – Amkor

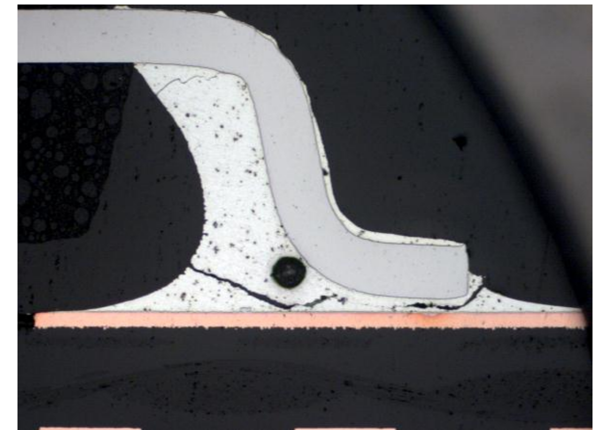
$$N_f = \left(0.0019 \cdot \Delta W\right)^{-1}$$

Validation – Chip Resistors



PoF Example – SAC Reliability (cont.)

- How to ensure 10 year life in a realistic worst-case field environment for industrial controls?
  - American Southwest (Phoenix)
  - Dominated by diurnal cycling



Month	Cycles/Year	Ramp	Dwell	Max. Temp (°C)	Min. Temp. (°C)
Jan.+Feb.+Dec.	90	6 hrs	6 hrs	20	5
March+November	60	6 hrs	6 hrs	25	10
April+October	60	6 hrs	6 hrs	30	15
May+September	60	6 hrs	6 hrs	35	20
June+July+August	90	6 hrs	6 hrs	40	25

+10C at max temperature due to solar loading

PoF Example – SAC Reliability (cont.)

- Total damage in desert environment over 10 years — 0.02604
- Total damage in one cycle of -40C to 85C test environment — 0.00012
- Total cycles at -40C to 85C to replicate 10 yrs in desert — 222 cycles

At 1 cycle/hour, approximately 1 day of test equals 1 year in the field

DfR Solutions
reliability designed, reliability delivered

Module 4: Printed Circuit Boards

Surface Finishes

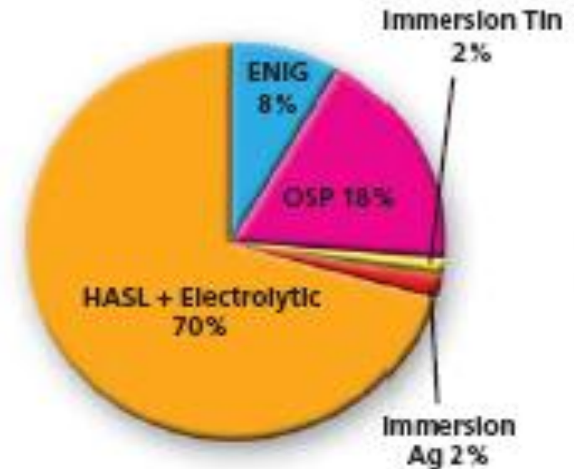
smthybridpackaging
Nuremberg, 8 - 10 May 2012

PCB Surface Finishes

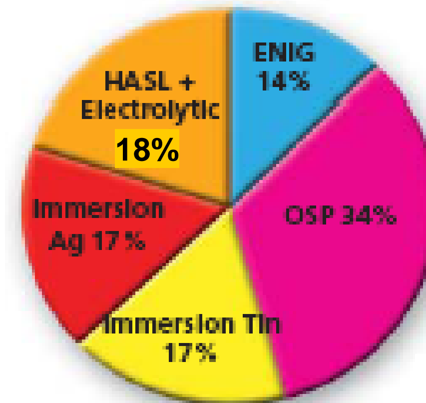
- Definition: A coating located at the outermost layer and exposed copper of a PCB.
  - Protects copper from oxidation that inhibits soldering
  - Dissolves into the solder upon reflow or wave soldering.
  - SnPb HASL (Hot Air Solder Leveling) being replaced by other finished due to technology and RoHS-Pb-free trends.
- Options (no clear winner)
  - Electroless nickel/immersion gold (ENIG)
  - Immersion tin (ImSn)
  - Immersion silver (ImAg)
  - Organic solderability preservative (OSP)
  - Pb-free HASL
  - Others (ENEPIG, other palladium, nano finishes etc.)
- Most platings, except for Pb-free HASL, has been around for several years

Surface Finishes, Worldwide

2003



2007



J. Beers
Gold Circuits

Pb-Free HASL

- Increasing Pb-free solderability plating of choice
- Primary material is Ni-modified SnCu (SN100CL)
  - Initial installations of SAC being replaced
  - Only Vicor recently identified as using SAC HASL (Electronic Design, Nov 2007)
  - Co-modified SnCu also being offered (claim of 80 installations [Metallic Resources])
- Selection driven by
  - Storage
  - Reliability
  - Solderability
  - Planarity
  - Copper Dissolution

Pb-Free HASL: Ni-modified SnCu

- Patented by Nihon Superior in March 1998
  - Claimed: Sn / 0.1-2.0% Cu / 0.002-1% Ni / 0-1% Ge
  - Actual: Sn / 0.7% Cu / 0.05% Ni / 0.006% Ge
- Role of constituents
  - **Cu** creates a eutectic alloy with lower melt temp (227C vs. 232C), forms intermetallics for strength, and reduces copper dissolution
  - **Ni** suppresses formation of b-Sn dendrites, controls intermetallic growth, grain refiner
  - **Ge** prevents oxide formation (dross inhibitor), grain refiner

Note: Current debate if Sn0.9Cu or Sn0.7Cu is eutectic

Pb-free HASL: Storage

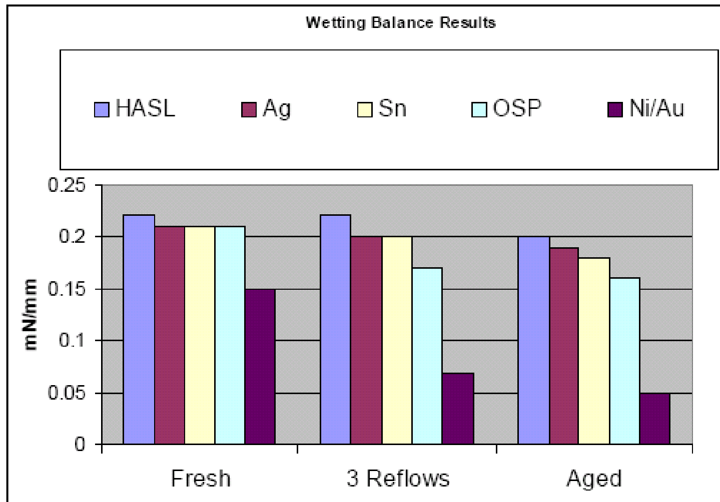
- PCBs with SnPb HASL have storage times of 1 to 4 years
  - Driven by intermetallic growth and oxide formation
- SN100CL demonstrates similar behavior
  - Intermetallic growth is suppressed through Ni-addition
  - Oxide formation process is dominated by Sn element (similar to SnPb)
- Limited storage times for alternative Pb-free platings (OSP, Immersion Tin, Immersion Silver)

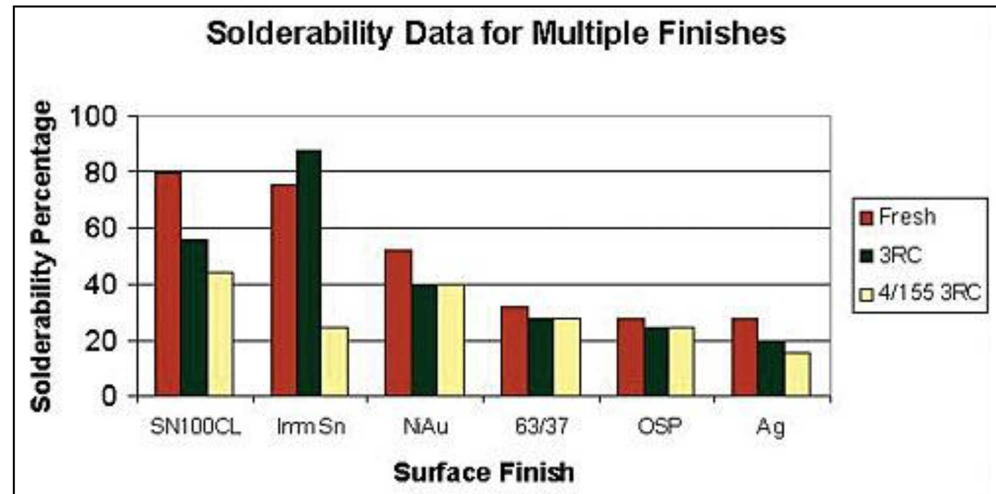
Pb-Free HASL: Reliability

- Contract manufacturers (CMs) and OEMs have reported issues with electrochemistry-based solderability platings
  - ENIG: Black Pad, Solder Embrittlement
  - ImAg: Sulfur Corrosion, Microvoiding
- Some OEMs have moved to OSP and Pb-free HASL due to their ‘simpler’ processes

Pb-Free HASL: Solderability

- Industry adage: Nothing solders like solder





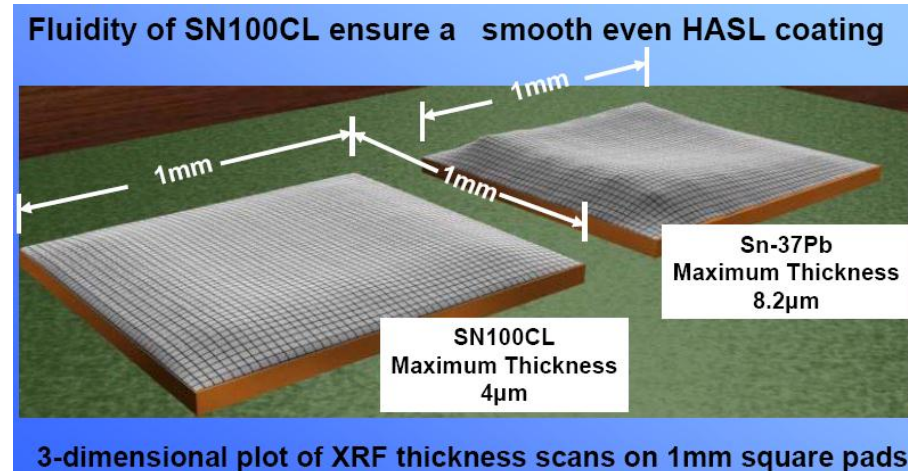
- Discussions with CMs and OEMs seem to indicate satisfaction with Pb-free HASL performance
  - Additional independent, quantitative data should be gathered
- Improved solderability could improve hole fill

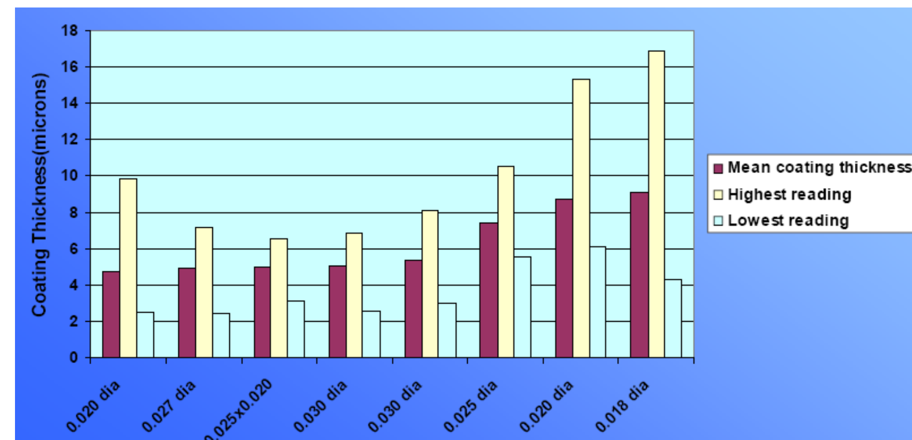
http://www.daleba.co.uk/download%20section%20-%20lead%20free.pdf

HASL and Flow: A Lead-Free Alternative, T. Lentz, et. al., Circuitree, Feb 2008, http://www.circuitree.com/Articles/Feature_Article/BNP_GUID_9-5-2006_A_10000000000000243033

Pb-Free HASL: Planarity

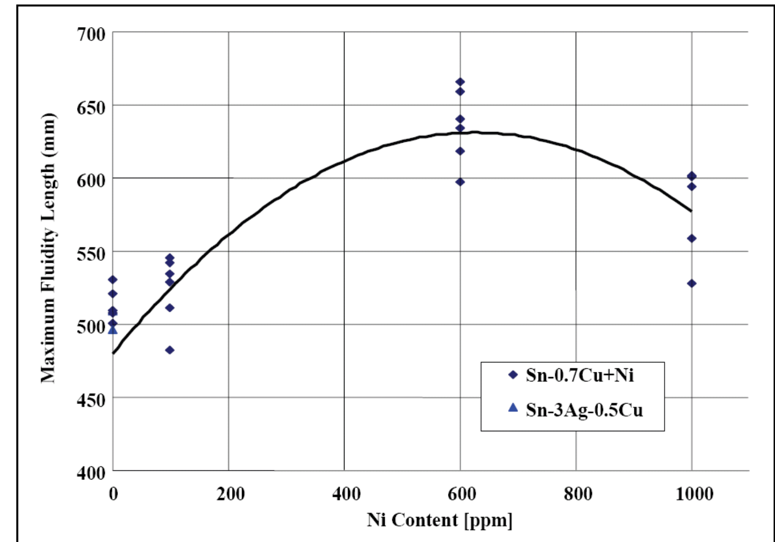
- Recommended minimum thickness
  - 100 min (4 microns)
  - Lower minimums can result in exposed intermetallic
- Primary issue is thickness variability
  - Greatest variation is among different pad designs
  - 100 min over small pads (BGA bond pads); over 1000 min over large pads
- Can be controlled through air knife pressure, pot temperatures, and nickel content





Pb-Free HASL: Planarity (cont.)

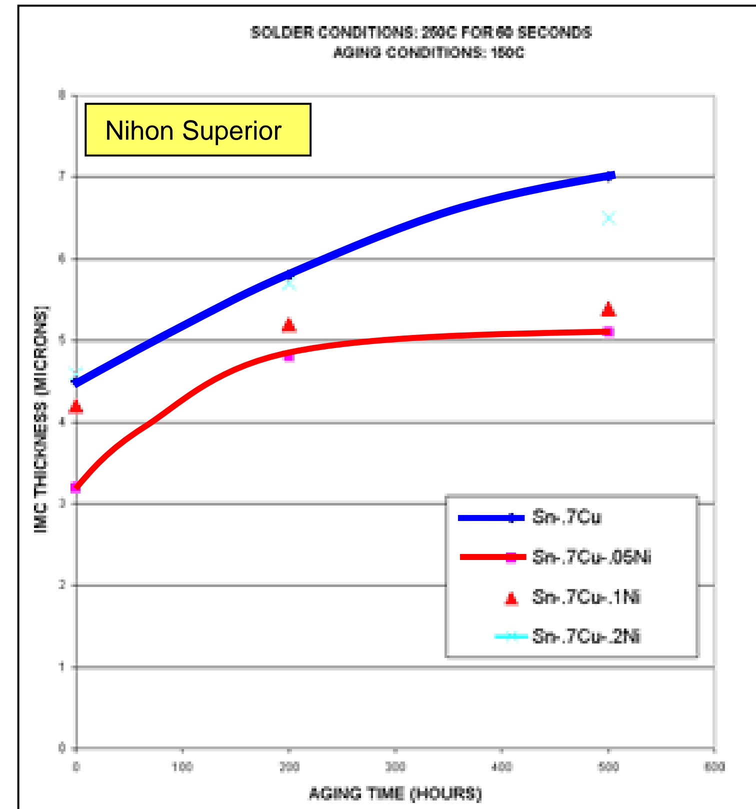
Sweatman and Nishimura (IPC APEX 2006)



- Air knives
  - Pb-free HASL requires lower air pressure to blow off excess solder
- Pot Temperatures
  - SnPb: 240C to 260C
  - SN100CL: 255C to 270C (air knife temp of 280C)
- Ni content
  - Variation can influence fluidity
    - Minimum levels critical for planarity
  - Some miscommunication as to critical concentrations

Pb-Free HASL: Copper Dissolution

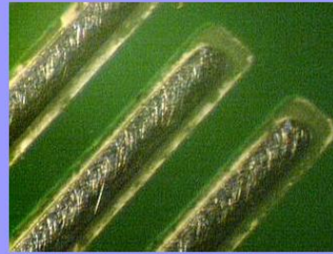
- To be discussed in detail in solder module
- Presence of nickel is believed to slow the copper dissolution process
  - SAC HASL removes ~5 um
  - SNC HASL removes ~1 um



After 6 Passes over Wave Soldering Machine
105°C Preheat, 256°C Solder Temperature, 4 seconds contact time

Sn-37Pb

Sn-3.0Ag-0.5Cu


Sn-0.7Cu+Ni

www.p-m-services.co.uk/rohs2007.htm

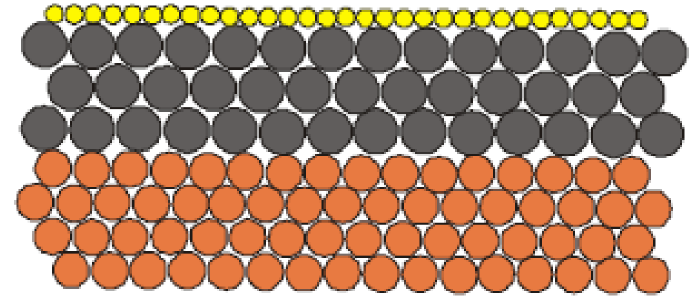
www.pb-free.org/02_G.Sikorcin.pdf

www.evertiq.com/news/read.do?news=3013&cat=8 (Conny Thomasson, Candor Sweden AB)

Pb-Free HASL: Additional Concerns

- Risk of thermal damage, including warpage and influence on long term reliability (PTH fatigue, CAF robustness)
  - No incidents of cracking / delamination / excessive warpage reported to DfR to date
  - Short exposure time (3 to 5 seconds) and minimal temp. differential (+5°C above SnPb) may limit this effect
- Compatibility with thick (>0.135”) boards
  - Limited experimental data (these products are not currently Pb-free)
- Mixing of SNC with SAC
  - Initial testing indicates no long-term reliability issues (JGPP)

Electroless Nickel/Immersion Gold (ENIG)

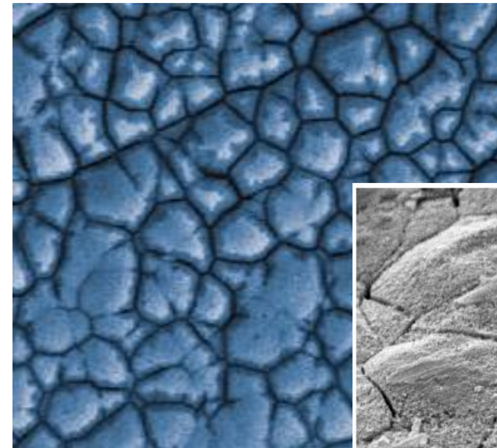


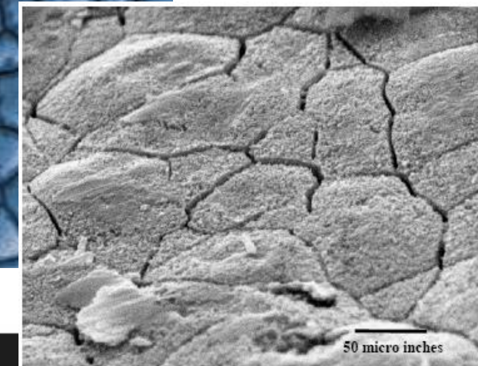
Saturn Electronics

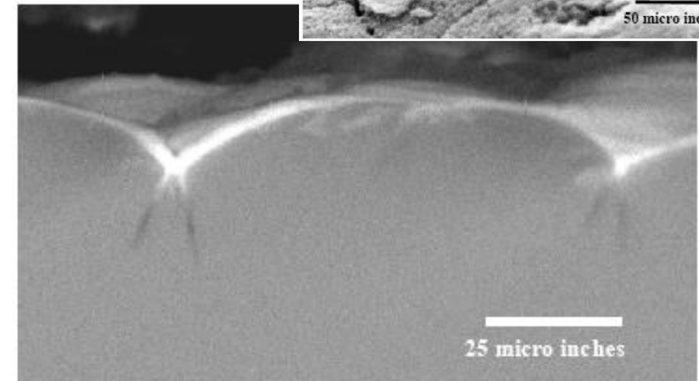
- Two material system
  - Specified by IPC-4552
- Electroless Nickel (w/P)
  - 3 – 6 microns (120 – 240 microinches)
  - Some companies spec a broader 1 – 8 microns
- Immersion Gold
  - Minimum of 0.05 microns (2 microinches)
  - Self-limiting (typically does not exceed 0.25 microns)
- Benefits
  - Excellent flatness, long-term storage, robust for multiple reflow cycles, alternate connections (wirebond, separable connector)

ENIG (Primary Issue)

- Solder Embrittlement
  - Not always black pad
- Not explained to the satisfaction of most OEMs
- Numerous drivers
  - Phosphorus content
    - High levels = weak, phosphorus-rich region after soldering
    - Low levels = hyper-corrosion (black pad)
  - Cleaning parameters
  - Gold plating parameters
  - Bond pad designs
  - Reflow parameters?
- Results in a severe drop in mechanical strength
  - Difficult to screen
  - Can be random (e.g., 1 pad out of 300)
- Board fabricators need to be on top of numerous quality procedures to prevent defects.

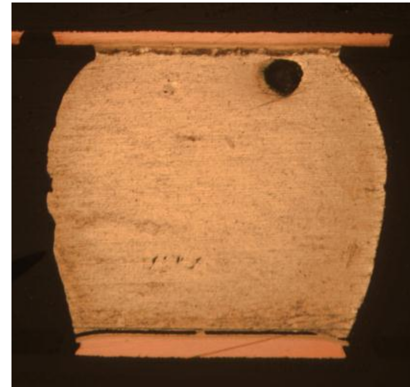


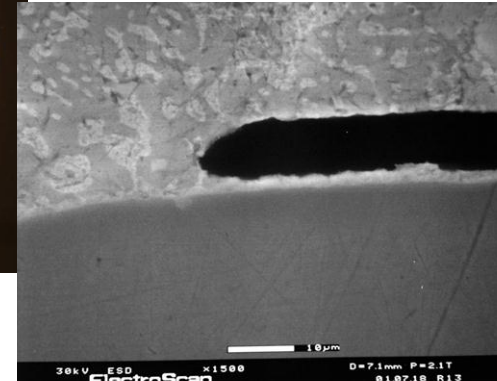




Other ENIG Failure Mechanisms

- Insufficient nickel thickness
  - Potential diffusion of copper through the nickel underplate
  - Can reduce storage time and number of reflow cycles
- Bond pad adhesion
  - Problem with corner balls on very large BGAs (>300 I/O)
- Reduced plated through hole reliability (stress concentrators)
- Dewetting
- Crevice corrosion (trapped residues)
- Poor performance under mechanical shock / drop

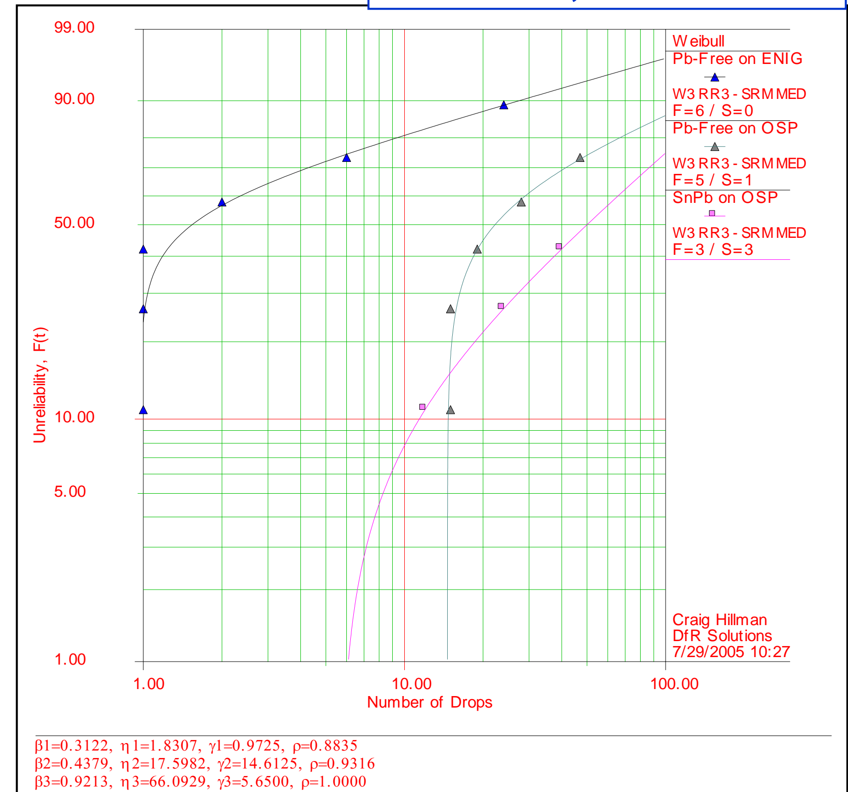


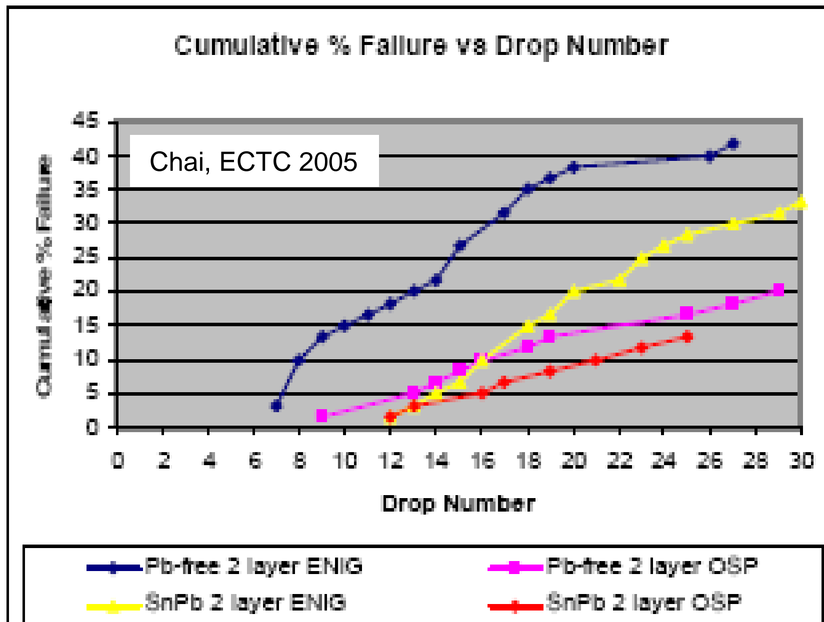


ENIG & Mechanical Shock

- Boards with ENIG finishes have less shock endurance.
  - Not always consistent
- Plating is an important driver
  - SnNi vs. SnCu intermetallics
- Crossover into board failure
  - Very strain-rate dependent

35x35mm, 312 I/O BGA





PQFP (28x28mm, 208 I/O)	Failures	
Pb-Free on ENIG	2/6	44/50, 45/50
Pb-Free on OSP	2/6	16/50, 29/50
SnPb on OSP	0/6	--

Chong, ECTC 2005

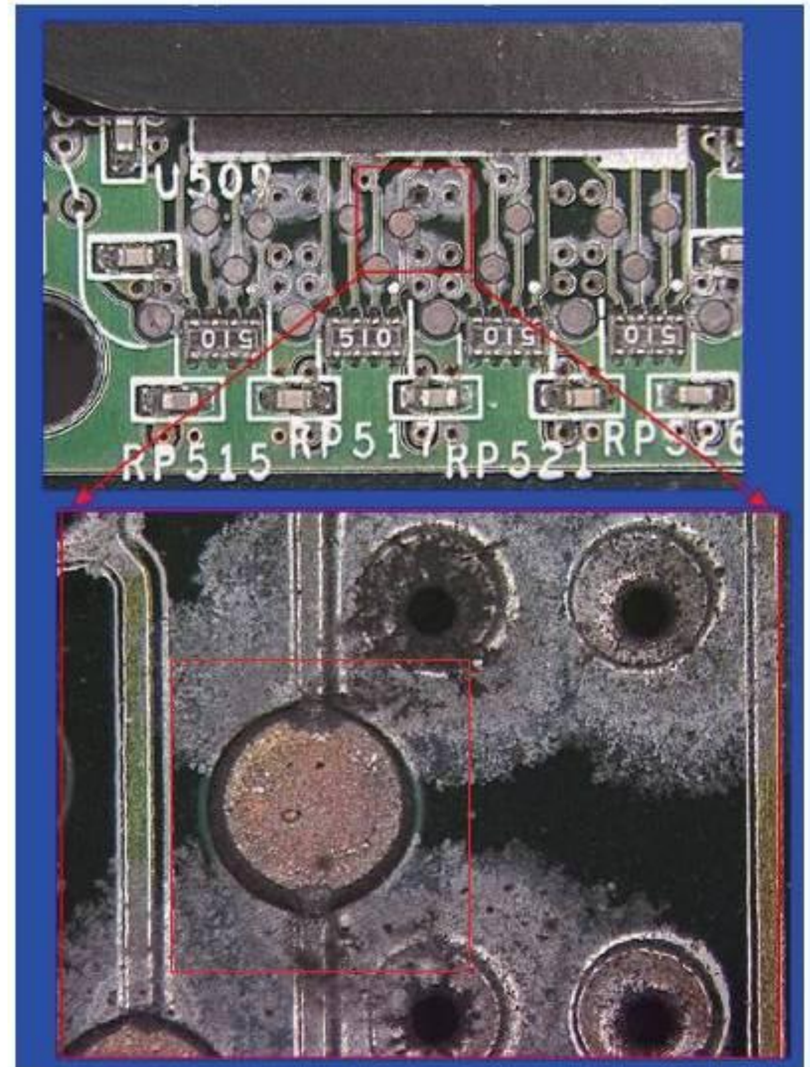
smthybridpackaging

Immersion Tin (ImSn)

- Single material system
  - Defined by IPC-4554
- Immersion Tin
  - Standard thickness: 1 micron (40 microinches)
  - Some companies spec up to 1.5 microns (65 microinches)
- Benefits
  - Excellent flatness, low cost, excellent bare test pad probing
- Not as popular a choice
  - Environmental and health concerns regarding thiourea (known carcinogen).
  - Not good for designs with small or micro vias – etchant gets entrapped during PCB processing and “erupts” during SMT soldering

Sulfide Corrosion and Migration of Immersion Silver

- Failures observed within months
  - Sulfur-based gases attack exposed immersion silver
  - Non-directional migration (creepage corrosion)
- Occurring primarily in environments with high sulfur levels. Not recommended for these applications.
  - Rubber manufacturing
  - Waste treatment plants
  - Petroleum refineries
  - Coal-generation power plants,
  - Paper mills
  - Sewage/waste-water treatment
  - Landfills
  - Large-scale farms
  - Modeling clay

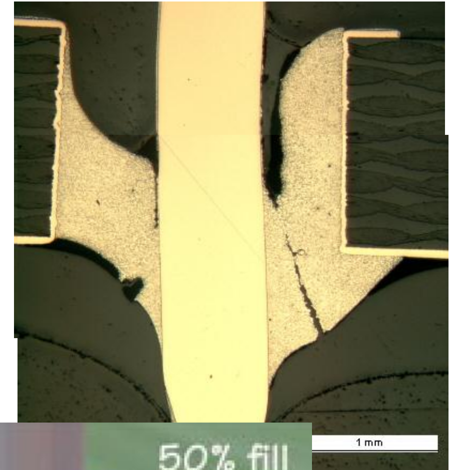


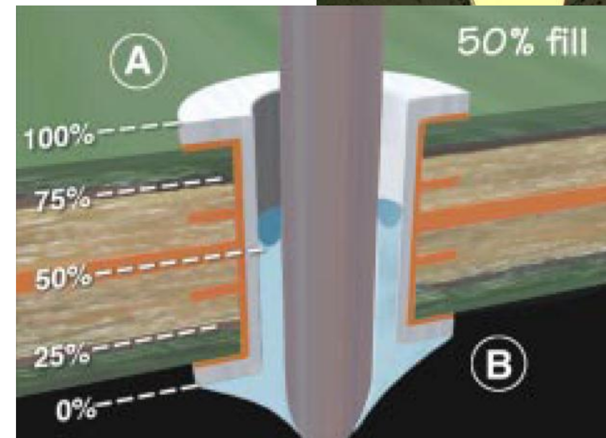
Organic Solderability Preservative (OSP)

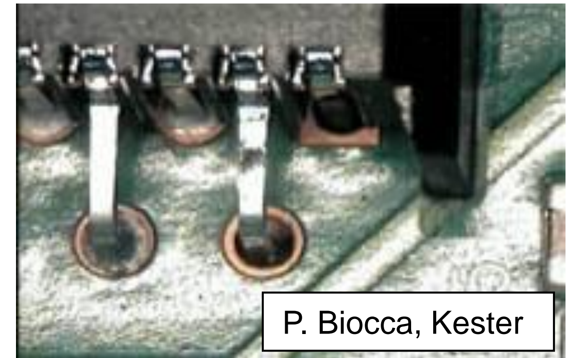
- Single material system
  - Specified by IPC-4555
- Thickness
- Benefits
  - Very low cost, flatness, reworkable
- Issues
  - Short shelf life (6-12 months)
  - Limited number of reflows
  - Some concerns about compatibility with low activity, no-clean fluxes
  - Transparency prevents visual inspection
  - Poor hole fill
  - Test pads must be soldered – prepare for probing through no clean materials if they are used.

OSP & Hole Fill

- Fill is driven by capillary action
- Important parameters
  - Hole diameter, hole aspect ratio, wetting force, thermal relief
  - Solder will only fill as along as its molten (key point)
- OSP has lower wetting force
  - Risk of insufficient hole fill
  - Can lead to single-sided architecture
- Solutions?
  - Changing board solderability plating
  - Increasing top-side preheat
  - Increasing solder pot temperature (some go as high as 280C)
  - Changing your wave solder alloy







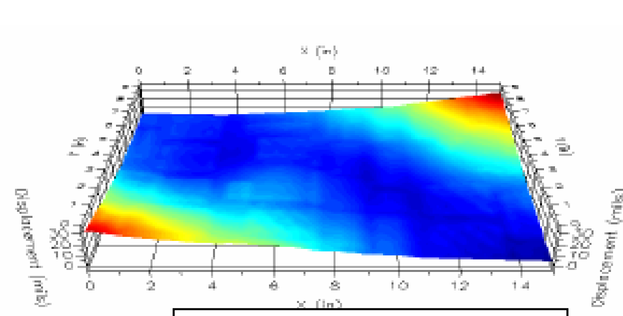
P. Biocca, Kester

DfR Solutions
reliability designed, reliability delivered

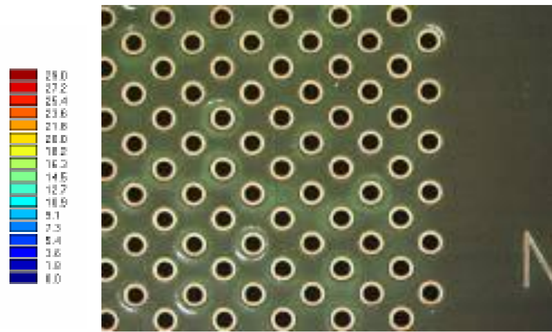
Module 4: Printed Circuit Boards

Robustness Concerns
Cracking and Delamination

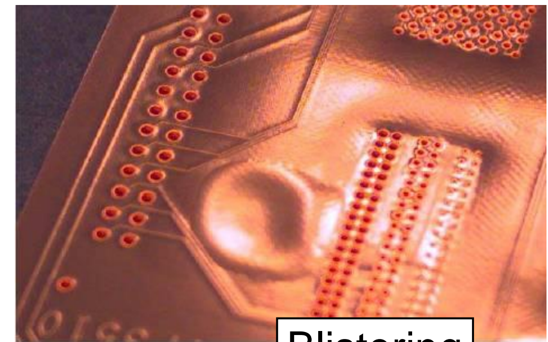
Printed Board Robustness Concerns



Increased Warpage

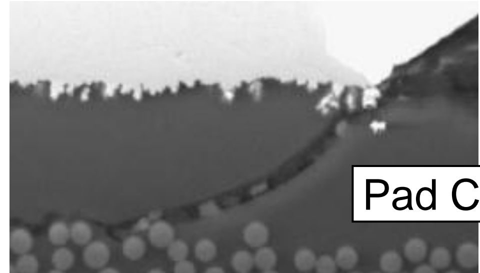


Solder Mask Discoloration

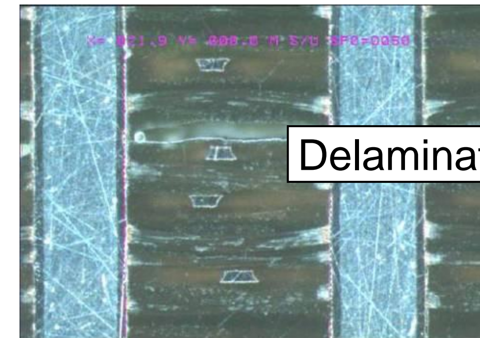


Blistering

Land Separation



Pad Cratering



Delamination

PTH Cracks

Printed Board Damage

- Predicting printed board damage can be difficult
  - Driven by size (larger boards tend to experience higher temperatures)
  - Driven by thickness (thicker boards experience more thermal stress)
  - Driven by material (lower Tg tends to be more susceptible)
  - Driven by design (higher density, higher aspect ratios)
  - Driven by number of reflows
- No universally accepted industry model

Printed Board Damage: Industry Response

- Concerns with printed board damage have almost entirely been addressed through material changes or process modifications
  - Not aware of any OEMs initiating design rules or restrictions
- Specific actions driven by board size and peak temperature requirements

PCB Robustness: Laminate Material Selection

Board thickness	IR-240~250℃	Board thickness	IR-260℃
≤60mil	Tg140 Dicy All HF materials OK	≤ 60mil	Tg150 Dicy HF- middle and high Tg materials OK
60~73mil	Tg150 Dicy NP150, TU622-5 All HF materials OK	60~73mil	Tg170 Dicy HF –middle and high Tg materials OK
73~93mil	Tg170 Dicy, NP150G-HF HF –middle and high Tg materials OK	73~93mil	Tg150 Phenolic + Filler IS400, IT150M, TU722-5, GA150 HF –middle and high Tg materials OK
93~120mil	Tg150 Phenolic + Filler IS400, IT150M, TU722-5 Tg 150 HF –middle and high Tg materials OK	93~130mil	Phenolic Tg170 IS410, IT180, PLC-FR-370 Turbo, TU722-7 HF –middle and high Tg materials OK
121~160mil	Phenolic Tg170 IS410, IT180, PLC-FR-370 Turbo TU722-7 HF –high Tg materials OK	≧131mil	Phenolic Tg170 + Filler IS415, 370 HR, 370 MOD, N4000-11 HF –high Tg materials OK
≧161mil	PhenolicTg170 + Filler IS415, 370 HR, 370 MOD, N4000-11 HF material - TBD	≧161mil	TBD – Consult Engineering for specific design review

1. Copper thickness = 2OZ use material listed on column 260 ℃
2. Copper thickness >= 3OZ use Phenolic base material or High Tg Halogen free materials only
3. **Twice lamination product use Phenolic material or High Tg Halogen free materials only (includes HDI)**
4. Follow customer requirement if customer has his own material requirement
5. DE people have to confirm the IR reflow Temperature profile

J. Beers, Gold Circuits

Printed Board Damage: Prevention

- Thermal properties of laminate material are primarily defined by four parameters
  - Out of plane coefficient of thermal expansion (Z-CTE)
  - Glass transition temperature (Tg)
  - Time to delamination (T260, T280, T288)
  - Temperature of decomposition (Td)
- Each parameter captures a different material behavior
  - Higher number slash sheets (> 100) within IPC-4101 define these parameters to specific material categories

Thermal Parameters of Laminate

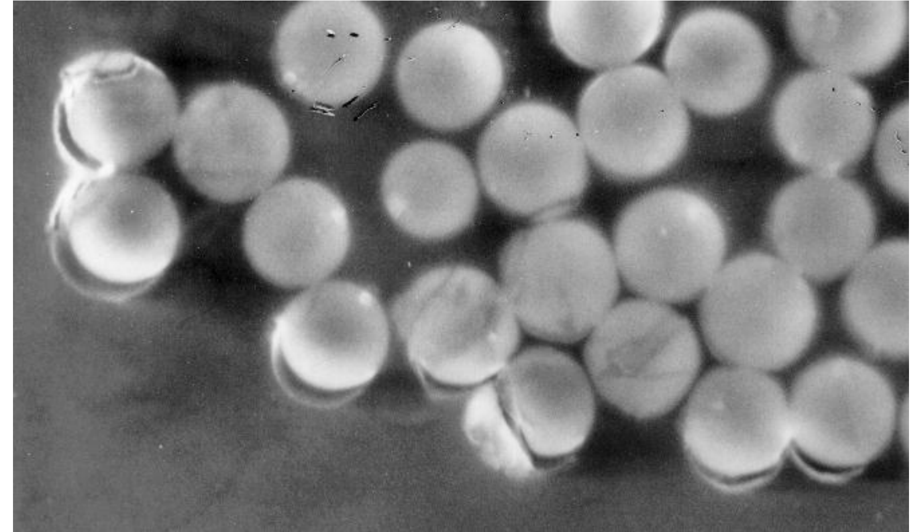
- Out of plane CTE (below Tg or Z-axis: 50ºC to 260ºC)
  - CTE for SnPb is 50ppm - 90ppm (50C to 260C rarely considered)
  - Pb-free: 30ppm - 65ppm or 2.5 – 3.5%
- Glass transition temperature (IPC-TM-650,)
  - Characterizes complex material transformation (increase in CTE, decrease in modulus)
  - Tg of 110ºC to 170ºC for SnPb
  - Pb-free: 150ºC to 190ºC
- Time to delamination (IPC-TM-650, 2.4.24.1)
  - Characterizes interfacial adhesion
  - T-260 for SnPb is 5-10 minutes
  - Pb-free: T-280 of 5-10 minutes or T-288 of 3-6 minutes
- Temperature of decomposition (IPC-TM-650, 2.3.40)
  - Characterizes breakdown of epoxy material
  - Td of 300ºC for SnPb
  - Pb-free: Td of 320ºC

PCB Robustness: Material Selection

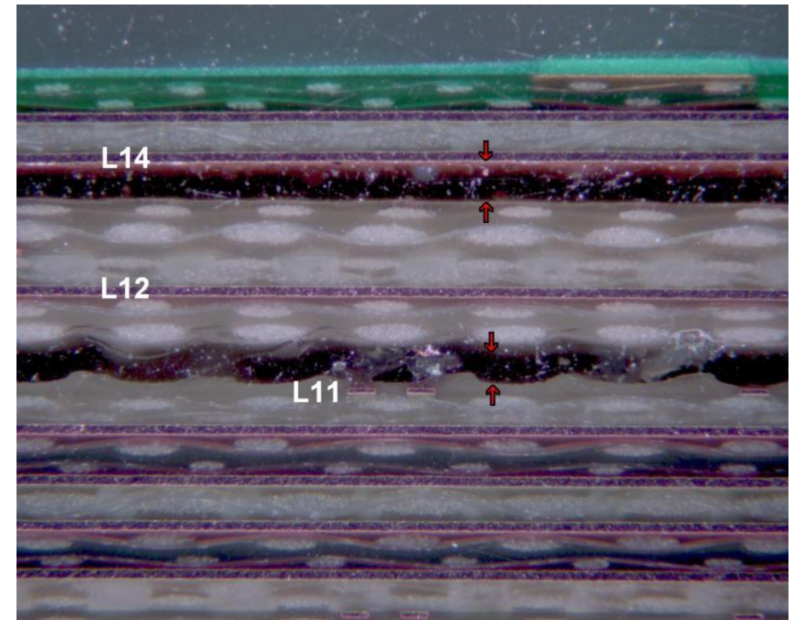
- The appropriate material selection is driven by the failure mechanism one is trying to prevent
  - Cracking and delamination
  - Plated through fatigue
  - Conductive anodic filament formation

PCB Delamination

- Fiber/resin interface delamination occurs as a result of stresses generated under thermal cycling due to a large CTE mismatch between the glass fiber and the epoxy resin (1 vs. 12 ppm/ºC)
- Delamination can be prevented/resisted by selecting resin with lower CTE's and optimizing the glass surface finish.
- Studies have shown that the bond between fiber and resin is strongly dependent upon the fiber finish



Delamination / Cracking: Observations

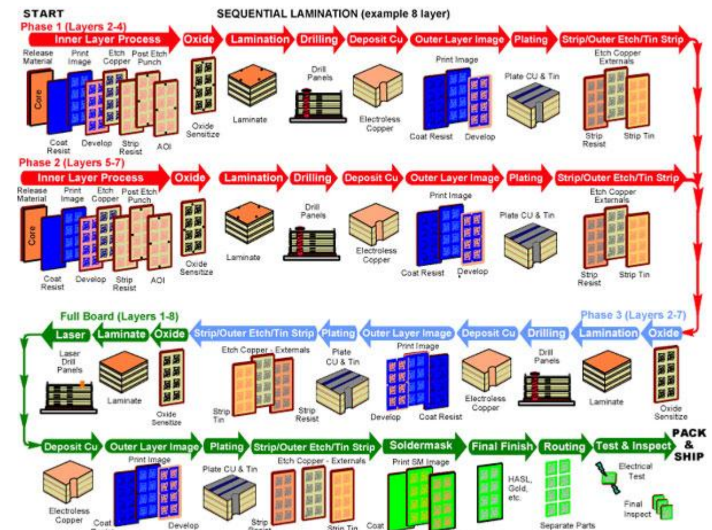


- Morphology and location of the cracking and delamination can vary
  - Even within the same board
- Failure morphology and locations
  - Within the middle and edge of the PCB
  - Within prepregs and/or laminate
  - Within the weave, along the weave, or at the copper/epoxy interface (adhesive and cohesive)

Additional Observations

- Drivers
  - Higher peak temperatures
  - Increasing PCB thickness
  - Decreasing via-to-via pitch
  - Increasing foil thickness (1-oz to 2-oz)
  - Presence of internal pads
  - Sequential lamination
- Limited information
  - Controlled depth drilling
- Extensive debate about root-cause
  - Non-optimized process
  - Intrinsic limit to PCB capability
  - Moisture absorption

Sequential Lamination

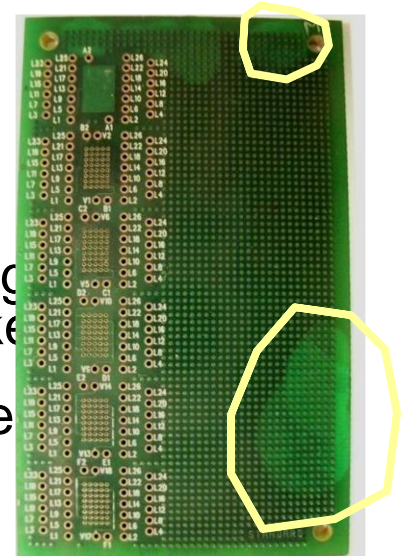


Rothschild, IPC APEX 2007

Delamination / Cracking: Root-Cause

- Non-Optimized Process
  - Some PCB suppliers have demonstrated improvement through modifications to lamination process or oxide chemistry
  - Some observations of lot-to-lot variability
- Limit to PCB Capability
  - Difficult to overcome adhesion vs. thermal performance tradeoff (dicy vs. phenolic)
  - High stresses developed during Pb-free exceed material strength of standard board material
- Moisture Absorption

Cracking and Moisture Absorption



- Does moisture play a role?
  - No
    - DfR found delamination primarily around the edge and away from PTH sites after MSL testing
    - IBM found minimal differences after a 24 hr bake of coupons with heavy copper (>2 oz)
    - Delamination / cracking observed in board store for short (<2 weeks) periods of time
  - Yes
    - DfR customer found improvement after 48 hrs at 125C
    - A number of companies now require 5 – 24 hour bake before reflow
    - IBM found improvement with coupons with nominal copper
    - DfR observed more rapid degradation of boards exposed to moisture, even after multiple reflows
    - Some customers specifying maximum moisture absorption
- Where does the moisture come from?

Cracking and Moisture (cont.)

- Storage of prepregs and laminates
- Drilling process
  - Moisture is absorbed by the side walls (microcracks?)
  - Trapped after plating
- Storage of PCBs at PCB manufacturer
- Storage of PCBs at CCA manufacturer

PCB Trace Peeling

- Delamination of trace from surface of the board
- Sources of increased stress
  - Excessive temperatures during high temperature processes
  - Insufficient curing of resin
  - Insufficient curing of solder mask
- Sources of decreased strength
  - Improper preparation of copper foil
  - Excessive undercut

PCB Robustness: Qualifying Printed Boards

- This activity may provide greatest return on investment
- Use appropriate number of reflows or wave
  - In-circuit testing (ICT) combined with construction analysis (cracks can be latent defect)
  - 6X Solder Float (at 288C) may not be directly applicable
- Note: higher Tg / phenolic is not necessarily better
  - Lower adhesion to copper (greater likelihood of delamination)
  - Greater risk of drilling issues
  - Potential for pad cratering
- Higher reflow and wave solder temperatures may induce solder mask delamination
  - Especially for marginal materials and processes
  - More aggressive flux formulations may also play a role
  - Need to re-emphasize IPC SM-840 qualification procedures

Material Selection - Laminate

- Higher reflow and wave solder temperatures may induce delamination
  - Especially for marginal materials and processes
    - Not all RoHS compliant laminates are Pb-free process capable!
    - Specify your laminate by name – not type or “equivalent”
  - Role of proper packaging and storage
    - PCBs should remain in sealed packaging until assembly
      - Reseal partially opened bricks
      - Package PCBs in brick counts which closely emulate run quantities
    - PCBs should be stored in temperature and humidity controlled conditions
    - Bake when needed
    - Packaging in MBB (moisture barrier bags) with HIC (humidity indicator cards) may be needed for some laminates
- Need to re-emphasize IPC SM-840 & other qualification procedures

DfR Solutions
reliability designed, reliability delivered

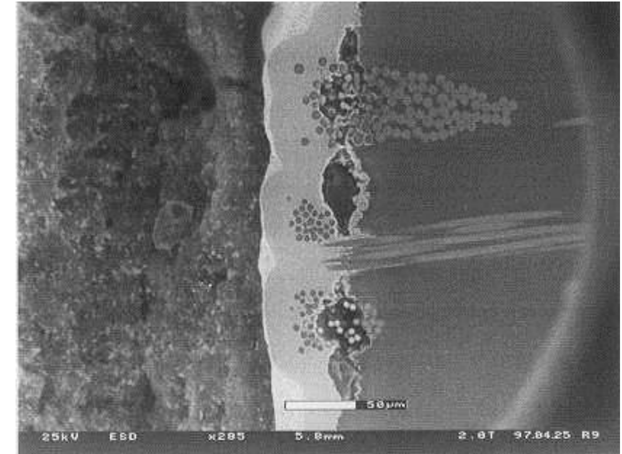
Module 4: PCB Robustness

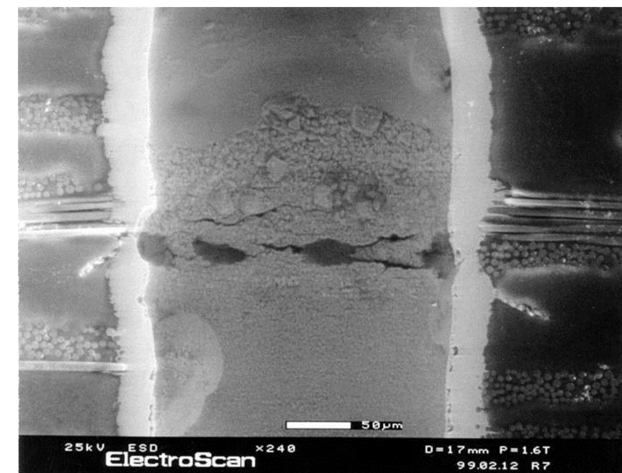
PTH Barrel Cracking

Conductive Anodic Filaments (CAF)

Plated Through Holes (PTH)

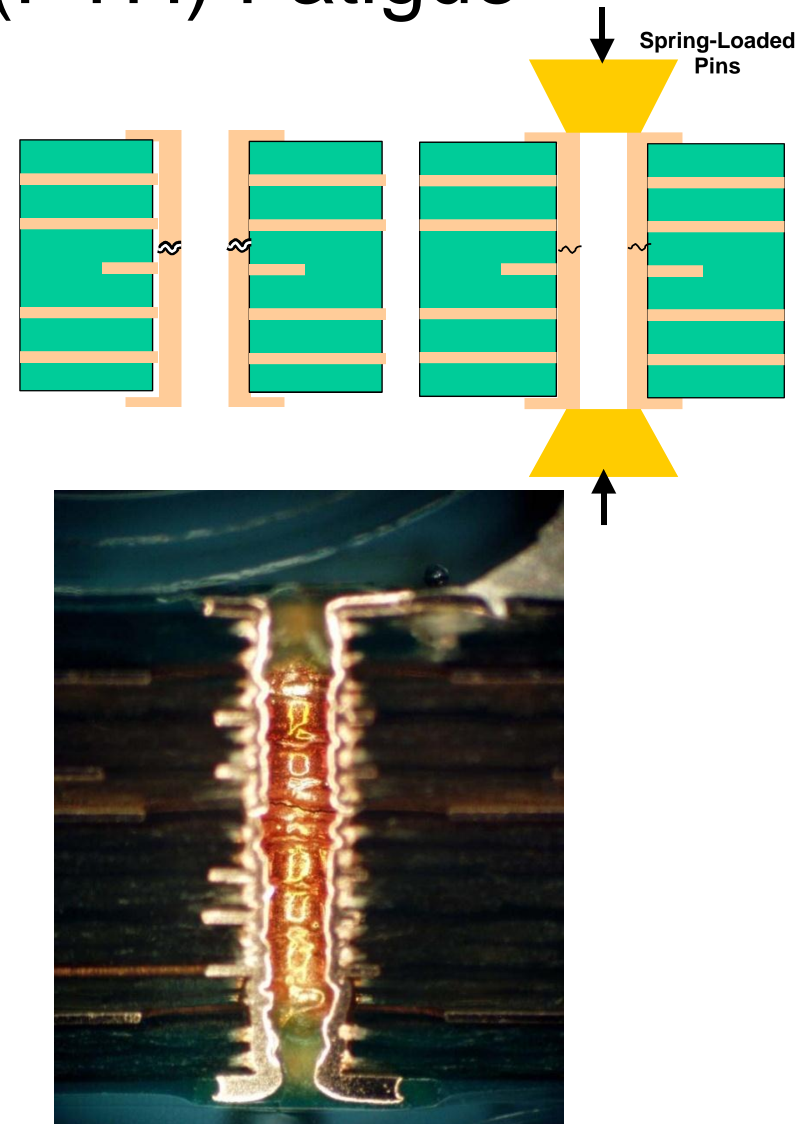
- Voids
  - Can cause large stress concentrations, resulting in crack initiation.
  - The location of the voids can provide crucial information in identifying the defective process
    - Around the glass bundles
    - In the area of the resin
    - At the inner layer interconnects (aka, wedge voids)
    - Center or edges of the PTH
- Etch pits
  - Due to either insufficient tin resist deposition or improper outer-layer etching process and rework.
  - Cause large stress concentrations locally, increasing likelihood of crack initiation
  - Large etch pits can result in a electrical open



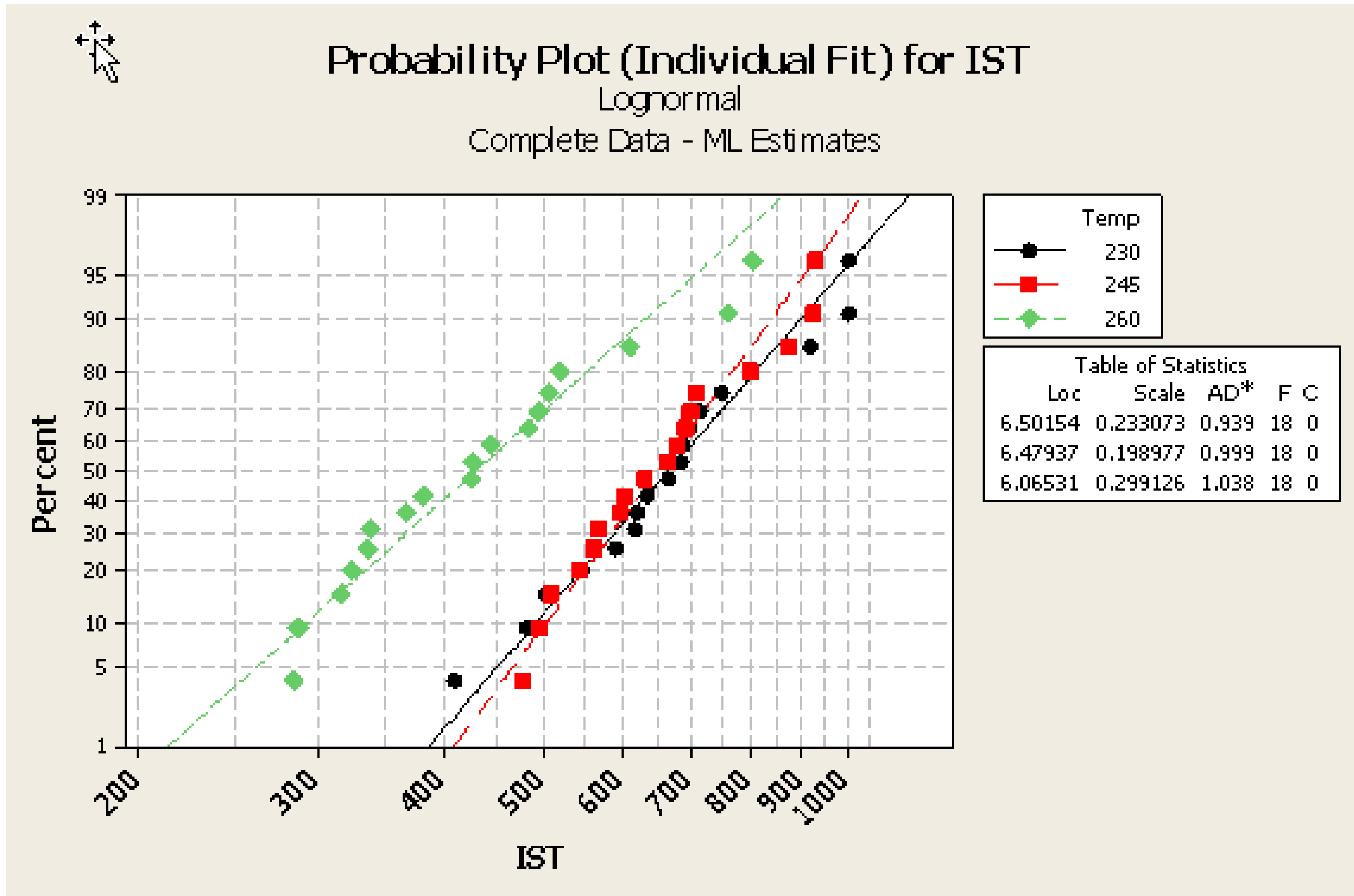


Plated Through Hole (PTH) Fatigue

- Overstress cracking
  - CTE mismatch places PTH in compression
  - Pressure applied during "bed-of-nails" can compress PTH
  - In-circuit testing (ICT) rarely performed at operating temperatures
- Fatigue
  - Circumferential cracking of the copper plating that forms the PTH wall
  - Driven by differential expansion between the copper plating (~17 ppm) and the out-of-plane CTE of the printed board (~70 ppm)
  - Industry-accepted failure model: IPC-TR-579



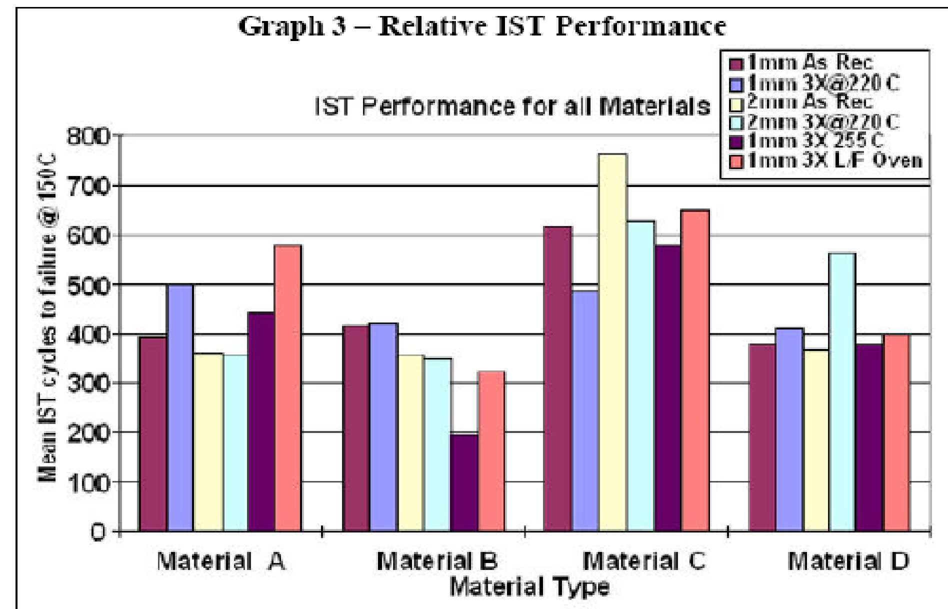
PTH Fatigue: Pb-Free



PTH and Pb-Free (continued)

- Findings
  - Limited Z-axis expansion and optimized copper plating prevents degradation

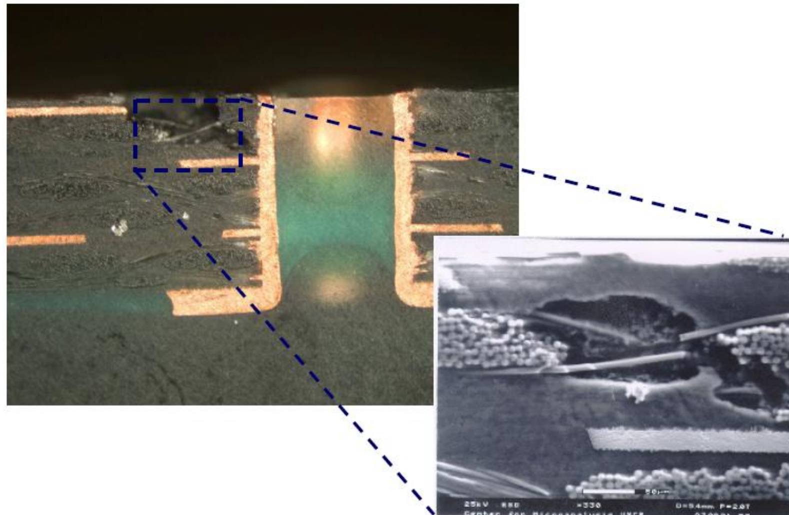
- Industry response
  - Movement to Tg of 150 - 170C
  - Z-axis expansion between 2.5 to 3.5%

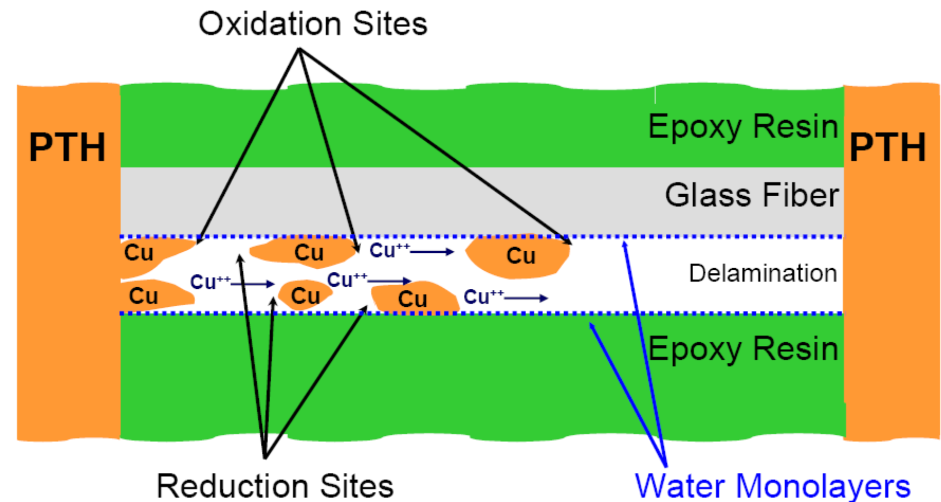


Property/Condition	Material A	Material B	Material C	Material D
Resin System	High Tg Epoxy	High Tg Enhanced	High Tg Epoxy	Mid Tg Epoxy
Tg (DSC)	175°C	210° C	175°C.	155°C.
Tg (TMA)	165°C	200° C	170°C.	150°C.
Tg (DMA)	195°C	240°C	180°C	160°C.
Degradation Temperature (TGA - 5% weight loss)	362°C	357°C	325°C	330°C.
Z axis expansion* (50 to 260°C in %)	3.20%	3.50%	3.70%	3.80%

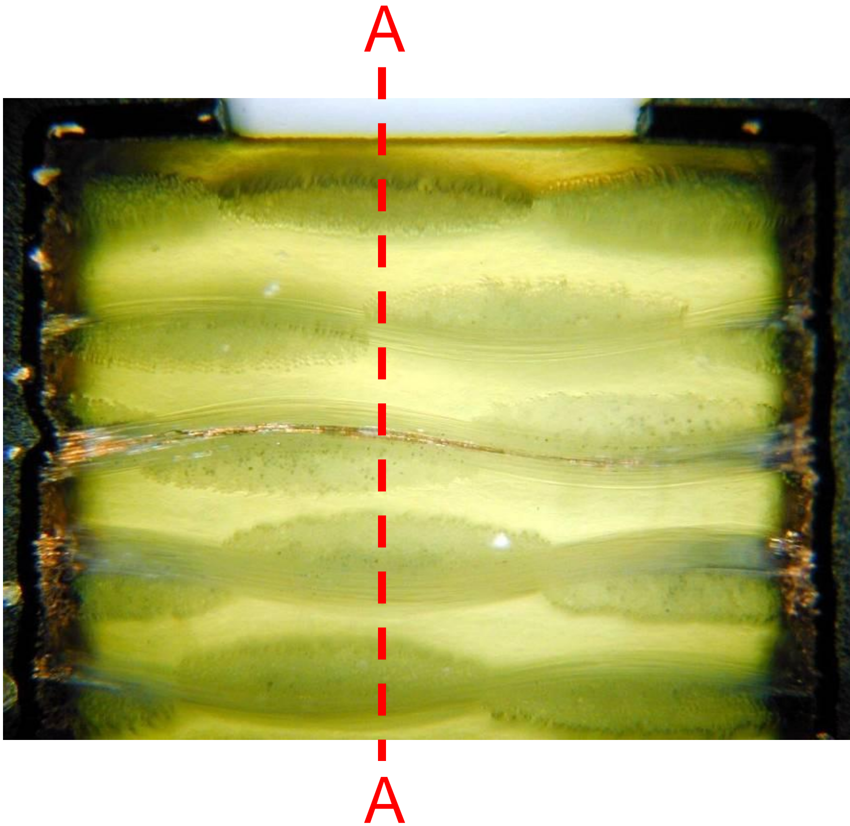
PCB Conductive Anodic Filaments (CAF)

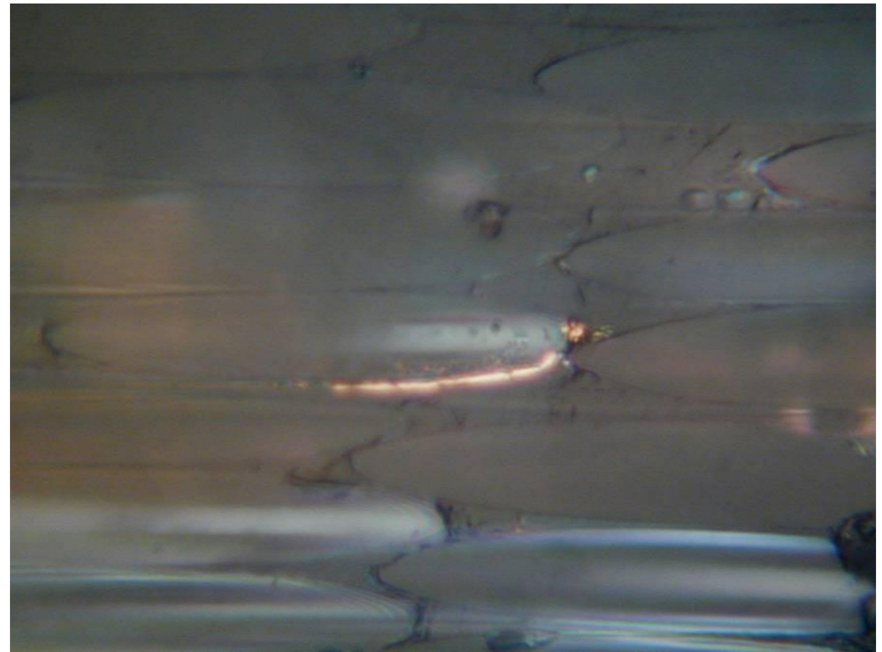
- CAF also referred to as metallic electro-migration
- Electro-chemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field
- CAF can cause current leakage, intermittent electrical shorts, and dielectric breakdown between conductors in printed wiring boards





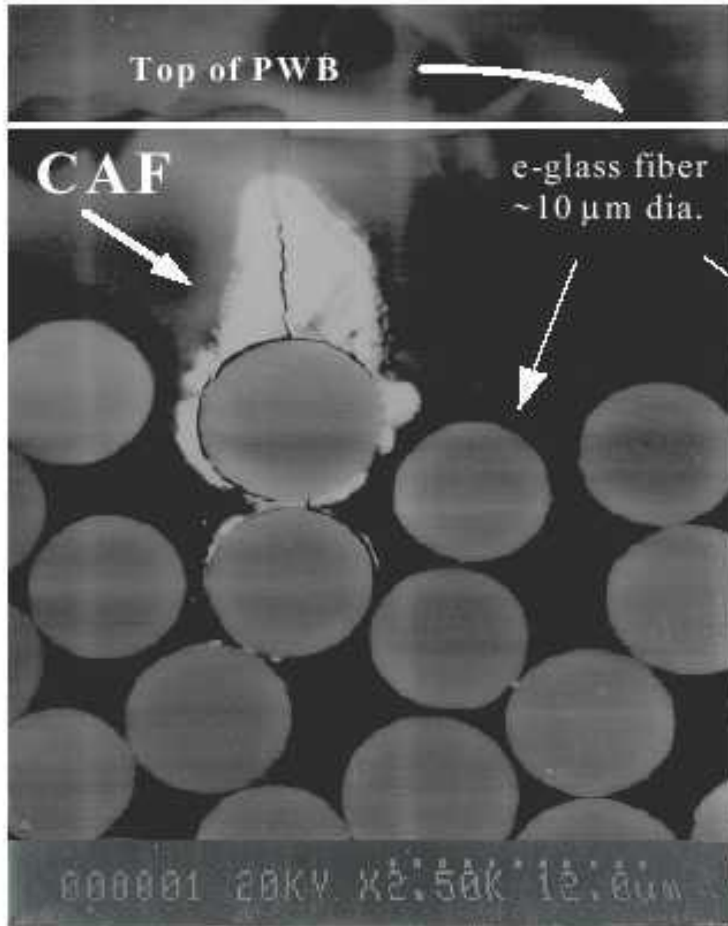
CAF: Examples

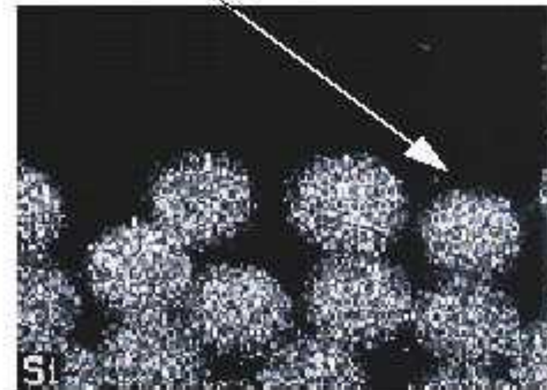




A:A Cross-Section

CAF: Examples





DfR Solutions
reliability designed, reliability delivered

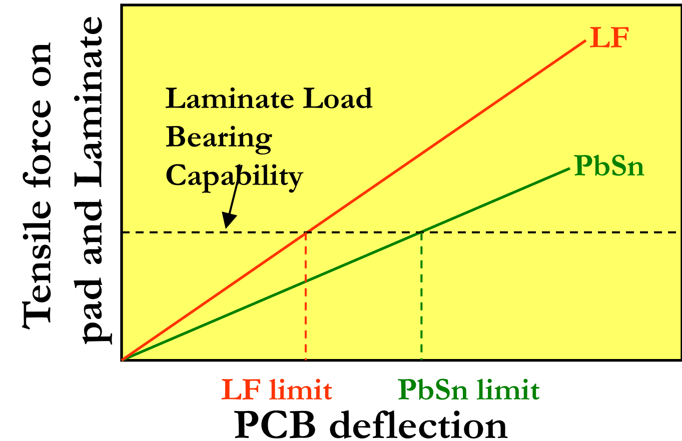
Module 4: PCB Robustness

Strain Flexure Issues & Pad Cratering
Electro-Chemical Migration (ECM)
Cleanliness

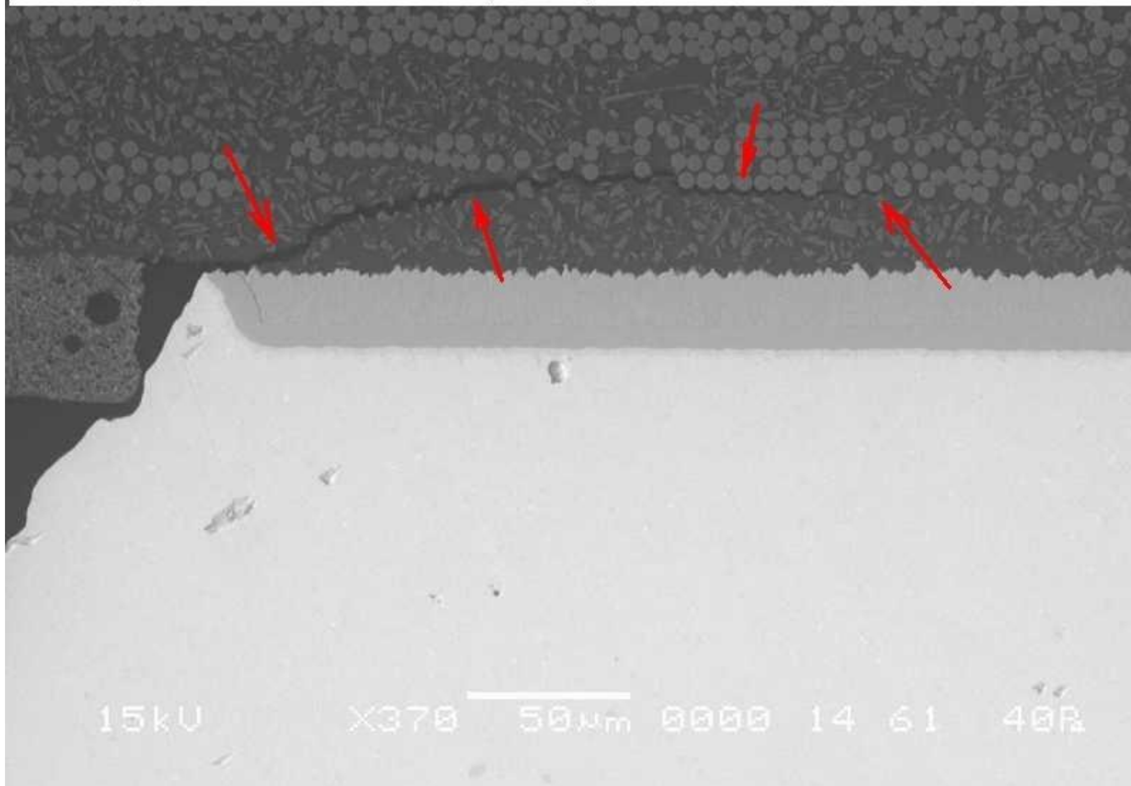
SAC Solder is More Vulnerable to Strain

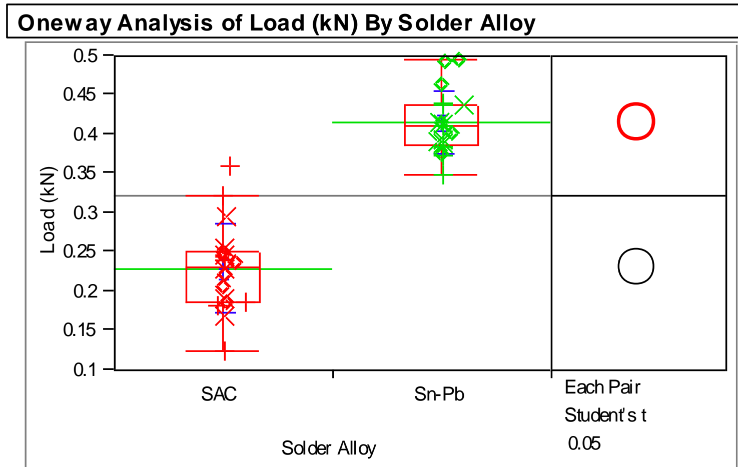
Sources of strain can be ICT, stuffing through-hole components, shipping/handling, mounting to a chassis, or shock events.

NEMI study showed SAC is more Sensitive to bend stress.



PICTURE 3476_4_IC_R1_s1a SHOWING A SEM PHOTO OF THE IC BGA FROM BOARD 4 LOCATION R1 (time T0 brd). NOTE LAMINATE FRACTURE (30 - 40%).



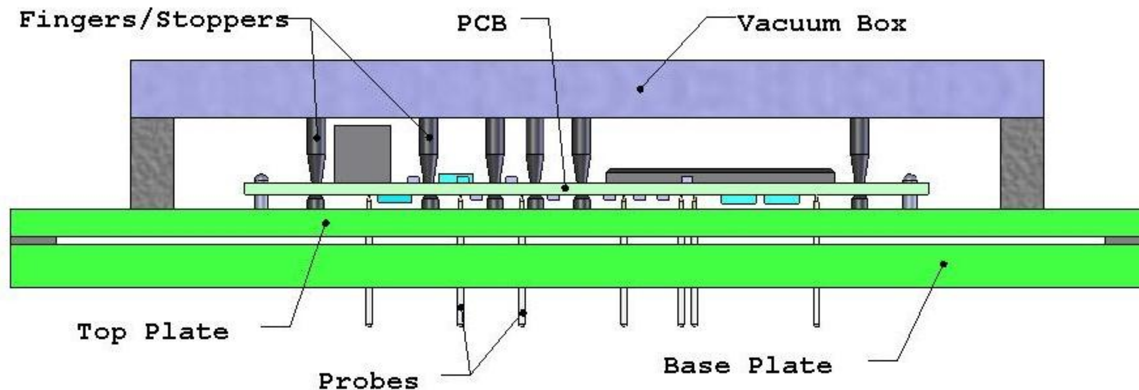


Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
SAC	18	0.230859	0.056591	0.01334	0.20272	0.25900
Sn-Pb	18	0.416101	0.040408	0.00952	0.39601	0.43620

ICT Strain: Fixture & Process Analysis

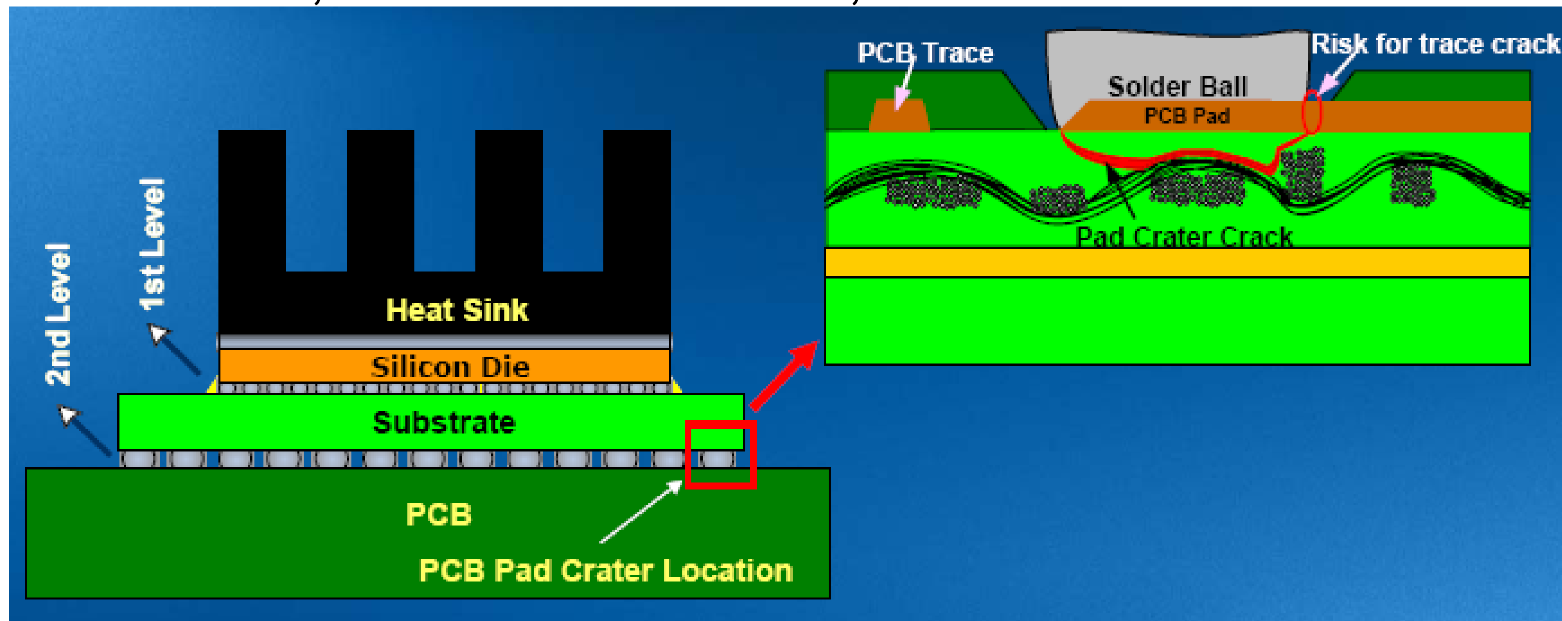
- Review/perform ICT strain evaluation at fixture mfg and in process: 500 us, IPC 9701 and 9704 specs, critical for QFN, CSP, and BGA
- http://www.rematek.com/download_center/board_stress_analysis.pdf



- To reduce the pressures exerted on a PCB, the first and simplest solution is to reduce the probes forces, when this is possible.
- Secondly, the positioning of the fingers/stoppers must be optimized to control the probe forces. But this is often very difficult to achieve. Mechanically, the stoppers must be located exactly under the pressure fingers to avoid the creation of shear points

Strain & Flexure: Pad Cratering

- Cracking initiating within the laminate during a dynamic mechanical event
  - In circuit testing (ICT), board depanelization, connector insertion, shock and vibration, etc.

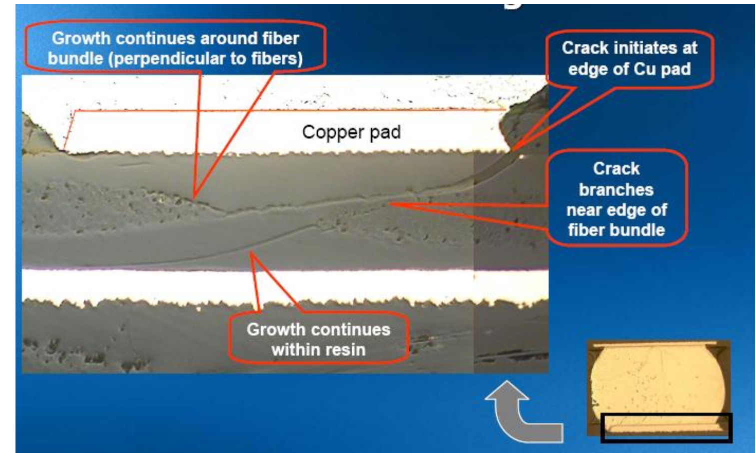


G. Shade, Intel (2006)

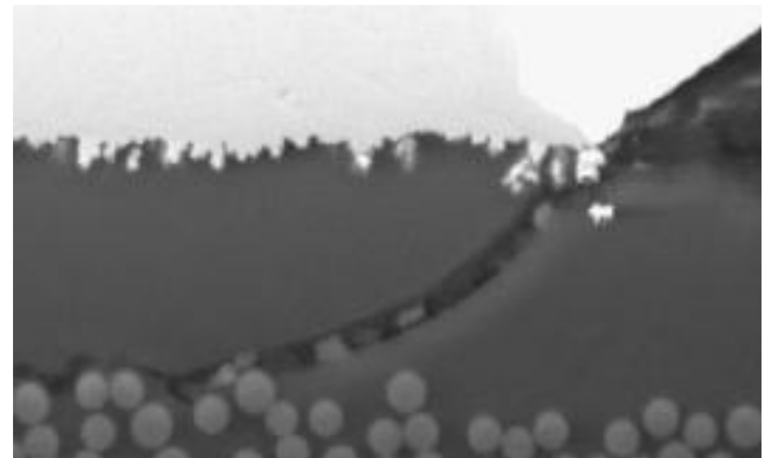
Pad Cratering

Intel (2006)

- Drivers
  - Finer pitch components
  - More brittle laminates
  - Stiffer solders (SAC vs. SnPb)
  - Presence of a large heat sink



- Difficult to detect using standard procedures
  - X-ray, dye-n-pry, ball shear, and ball pull



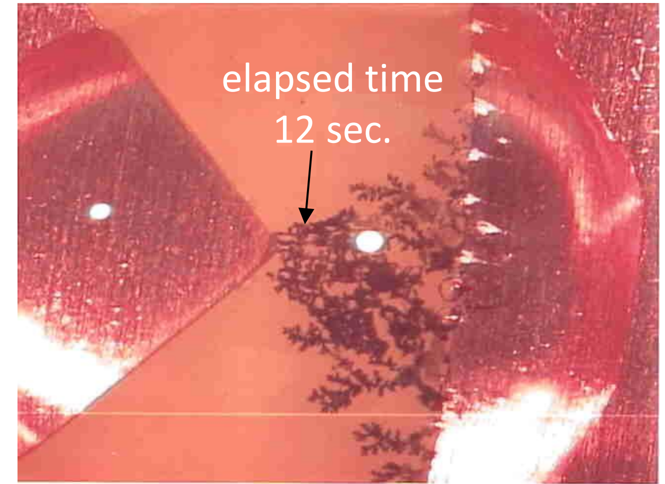
Solutions to Pad Cratering

- Board Redesign
  - Solder mask defined vs. non-solder mask defined
- Limitations on board flexure
  - 500 microstrain max, Component, location, and PCB thickness dependent
- More compliant solder
  - SAC305 is relatively rigid, SAC105 and SNC are possible alternatives
- New acceptance criteria for laminate materials
  - Intel-led industry effort
  - Attempting to characterize laminate material using high-speed ball pull and shear testing, Results inconclusive to-date

Laminate Acceptance Criteria

- Intel-led industry effort
  - Attempting to characterize laminate material using high-speed ball pull and shear testing
  - Results inconclusive to-date
- Alternative approach
  - Require reporting of fracture toughness and elastic modulus

Electro-Chemical Migration: Details



- Insidious failure mechanism
  - Self-healing: leads to large number of no-trouble-found (NTF)
  - Can occur at nominal voltages (5 V) and room conditions (25C, 60%RH)
- Due to the presence of contaminants on the surface of the board
  - Strongest drivers are halides (chlorides and bromides)
  - Weak organic acids (WOAs) and polyglycols can also lead to drops in the surface insulation resistance
- Primarily controlled through controls on cleanliness
  - Minimal differentiation between existing Pb-free solders, SAC and SnCu, and SnPb
  - Other Pb-free alloys may be more susceptible (e.g., SnZn)

PCB Cleanliness: Moving Forward

- Extensive effort to update PCB Cleanliness Standards
- IPC-5701: Users Guide for Cleanliness of Unpopulated Printed Boards (2003)
- IPC-5702: Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (2007)
- IPC-5703: Guidelines for Printed Board Fabricators in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (Draft)
- **IPC-5704: Cleanliness Requirements for Unpopulated Printed Boards (2010)**

Nominal Ionic Levels

- Bare printed circuit boards (PCBs)
  - Chloride: 0.2 to 1 $\mu g/inch^2$ (average of 0.5 to 1)
  - Bromide: 1.0 to 5 $\mu g/inch^2$ (average of 3 to 4)
- Assembled board (PCBA)
  - Chloride: 0.2 to 1 $\mu g/inch^2$ (average of 0.5 to 1)
  - Bromide: 2.5 to 7 $\mu g/inch^2$ (average of 5 to 7)
  - Weak organic acids: 50 to 150 $\mu g/inch^2$ (average of 120)
- Higher levels
  - Corrosion/ECM issues at levels above 2 (typically 5 to 10)
  - Corrosion/ECM issues at levels above 10 (typically 15 to 25)
  - Corrosion/ECM issues at levels above 200 (typically 400)
- General rule
  - Dependent upon board materials and complexity

Control Cleanliness Concerns

- Incoming PCB Cleanliness
  - Cleanliness testing performed using ROSE (resistivity of solvent extracted) or Omega-Meter method (ionic cleanliness, NaCl equivalent)
- Consider cleanliness requirements in terms of IC (ion chromatography) test for PCBs using WS flux
  - Don't use ROSE or Omegameter test as single option (at all? Risk from dirty IPA)
  - Inspection method with accept/reject limit
  - Sampling criteria
- Control cleanliness throughout the process from start to finish.

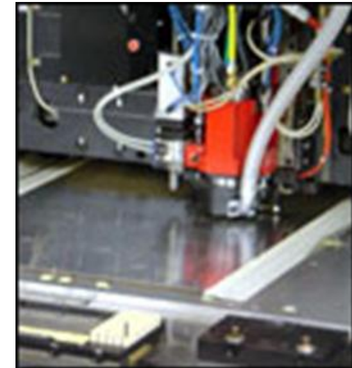
BTC, CSP & Low Profile Cleanliness Issues (Bottom Termination Components, Chip Scale Components)

- Low or no standoff parts are particularly vulnerable to cleanliness / residual flux problems
  - Difficult to clean under
  - Short paths from lead to lead or lead to via
  - Can result in leakage resistance, shorts, corrosion, electrochemical migration, dendritic growth

Recommendations – Process Qualification

- Validate compatibility of all new process materials using SIR testing.
- Continue spot check testing of cleanliness using ion chromatography under low profile SMT parts

PCB Sourcing & Supply Chain Best Practices



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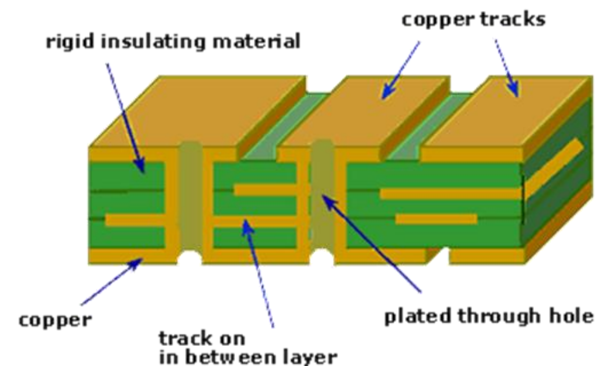
PCBs as Critical Components

- PCBs should be considered critical components or a critical commodity.
- Without stringent controls in place for PCB supplier selection, qualification, and management, long term product quality and reliability is simply not achievable.
- This section will cover some common best practices and recommendations for management of your PCB suppliers.



PCB Best Practices: Commodity Team

- Existence of a PCB Commodity Team with at least one representative from each of the following areas:
  - Design
  - Manufacturing
  - Purchasing
  - Quality/Reliability
- The team should meet on a monthly basis
  - Discuss new products and technology requirements in the development pipeline.
- Pricing, delivery, & quality performance issues with approved PCB suppliers should also be reviewed.
- The team also identifies new suppliers and creates supplier selection and monitoring criteria.

PCB Best Practices: Selection Criteria

- Established PCB supplier selection criteria in place. The criteria should be unique to your business, but some generally used criteria are:
  - Time in business
  - Revenue
  - Growth
  - Employee Turnover
  - Training Program
  - Certified to the standards you require (IPC, MIL-SPEC, ISO, etc.)
  - Capable of producing the technology you need as part of their mainstream capabilities (don't exist in their process "niches" where they claim capability but have less than ~ 15% of their volume built there.)
  - Have quality and problem solving methodologies in place
  - Have a technology roadmap
  - Have a continuous improvement program in place

PCB Best Practices: Qualification Criteria

- Rigorous qualification criteria including:
  - On site visits by someone knowledgeable in PCB fabrication techniques.
    - An onsite visit to the facility which will produce your PCBs is vital.
      - The site visit is your best opportunity to review process controls, quality monitoring and analytical techniques, storage and handling practices and conformance to generally acceptable manufacturing practices.
      - It is also the best way to meet and establish relationships with the people responsible for manufacturing your product.
  - Sample builds of an actual part you will produce which are evaluated by the PCB supplier
    - Also independently evaluated by you or a representative
    - To the standards that you require.

PCB Best Practices: Supplier Tiering

- Use supplier tiering (Low, Middle, High) strategies if you have a diverse product line with products that range from simpler to complex.
  - This allows for strategic tailoring to save cost and to maximize supplier quality to your product design. Match supplier qualifications to the complexity of your product. Typical criteria for tiering suppliers include:
    - Finest line width
    - Finest conductor spacing,
    - Smallest drilled hole and via size
    - Impedance control requirement
    - Specialty laminate needed (Rogers, flex, mixed)
    - Use of HDI, micro vias, blind or buried vias.
- Minimize use of suppliers who have to outsource critical areas of construction. Again, do not exist in the margins of their process capabilities.

PCB Best Practices: Relationships

- Relationship Management. Ideally, you choose a strategy that allows you to partner with your PCB suppliers for success. This is especially critical is you have low volumes, low spend, or high technology and reliability requirements for your PCBs. Some good practices include:
  - Monthly conference calls with your PCB commodity team and each PCB supplier. The PCB supplier team should members equivalent to your team members.
  - QBRs (quarterly business reviews) which review spend, quality, and performance metrics, and also include “state of the business updates” which address any known changes like factory expansion, move, or relocation, critical staffing changes, new equipment/capability installation etc.
    - The sharing is done from both sides with you sharing any data which you think would help strengthen the business relationship – business growth, new product and quoting opportunities, etc. At least twice per year, the QBRs should be joint onsite meetings which alternate between your site and the supplier factory site. The factory supplier site QBR visit can double as the annual on site visit and audit that you perform.
  - Semi-Annual “Lunch and Learns” or technical presentations performed onsite at your facility by your supplier. All suppliers perform education and outreach on their processes and capabilities. They can educate your technical community on PCB design for manufacturing, quality, reliability, and low cost factors. They can also educate your technical community on pitfalls, defects, and newly available technology. This is usually performed free of charge to you. They’ll often pay for lunch for attendees as well in order to encourage attendance.

PCB Best Practices: Supplier Scorecards

- Supplier Scorecards are in place and performed quarterly and yearly on a rolling basis. Typical metrics include:
  – On Time Delivery
  – PPM Defect Rates
  – Communication – speed, accuracy, channels, responsiveness to quotes
  – Quality Excursions / Root Cause Corrective Action Process Resolution
  – SCARs (Supplier Corrective Action Requests) Reporting
  – Discussion of any recalls, notifications, scrap events exceeding a certain dollar amount

Image courtesy ETQ

PCB Best Practices: Cont. Quality Monitoring

- Continuous Quality Monitoring is in place. Consider requiring and reviewing the following:
  - Top 3 PCB factory defects monitoring and reporting
  - Process control and improvement plans for the top 3 defects
  - Yield and scrap reporting for your products
  - Feedback on issues facing the industry
  - Reliability testing performed (HATS, IST, solder float, etc.)
    - As a starting point, consider the IPC-9151B, Printed Board Process Capability, Quality, and Relative Reliability (PCQR2) Benchmark Test Standard and Database at: http://www.ipc.org/html/IPC-9151B.pdf
    - Your PCB suppliers may be part of this activity already. Ask if they participate and if you can get a copy of their results.

PCB Best Practices: Prototype Development

- Prototype Development
  - Ideally, all of your PCBs for a given product should come from the same factory
    - from start to finish – prototype (feasibility), pre-release production (testability & reliability), to released production (manufacturability).
  - Each factory move introduces an element of risk
    - Product must go through setup and optimization specific to the factory and equipment contained there.
  - All PCBs intended for quality and reliability testing should come from the actual PCB production facility.

Summary

- To avoid design mistakes, be aware that functionality is just the beginning
- Be aware of industry best practices
- Maximize knowledge of your design as early in the product development process as possible
- Practice design for excellence (DfX)
  - Design for manufacturability
  - Design for sourcing
  - Design for reliability

Conclusion

- Design for Reliability is a valuable process for lowering cost, reducing time-to-market, and improving customer satisfaction
- PoF is a powerful tool that can leverage the value of DfR activities
- Successful DfR / PoF implementation requires the right combination of personnel and tools and time limitations

Partner for Reliability, Quality and Validation

DfR – Design for Reliability –

focus on production processes

Dr. Viktor Tiederle

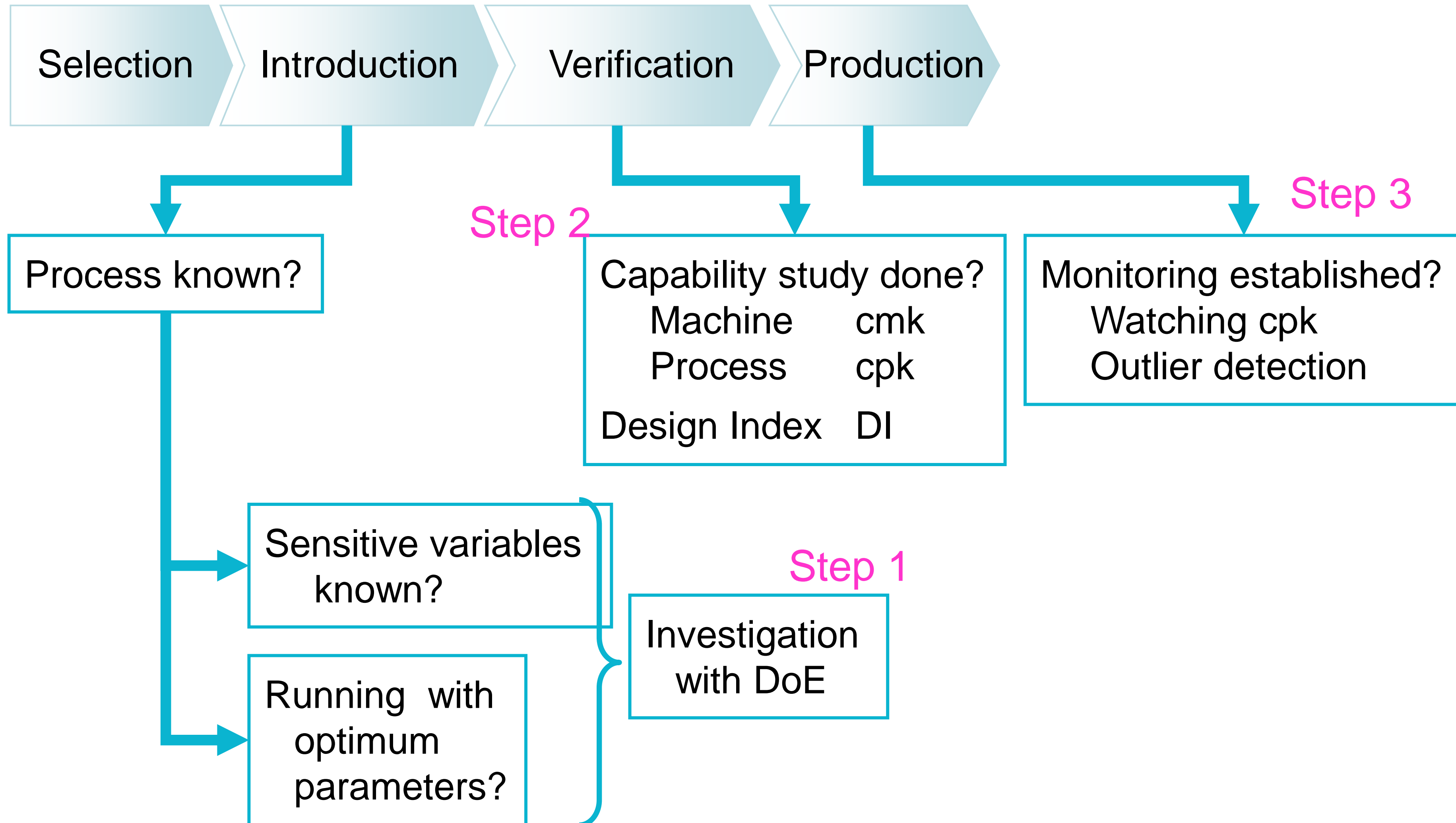
Instructor Biography

- Dr. Viktor Tiederle has over 29 years of experience in interconnection technology for microelectronic devices. He has worked in nearly all areas from development to production with the emphasis on quality and reliability. He started with his work in thick film technology and soldering techniques in SMD ceramics in the early 1980's. Later we worked in wire bonding technique as well as in adhesive technology and developing micromechanical devices for automotive applications. Since more than 10 years he is responsible for many projects within the automotive as well as other industrial segments, for example in photovoltaic.
- Viktor earned his Diploma of Physics at the Technical University of Munich and Stuttgart. After some years of industrial work he received his Dr.-Ing. degree with a studying Design of Experiments used for wire bonding technique in several applications.
- Viktor works in several working groups in the automotive industry for qualifying components for the use in such hazard environments.

Reliability in production processes – Content

- 0 – Frame conditions
- 1 – Establishing processes
- 2 – Design of experiments
- 3 – Monitoring
  - Capability
  - Design Index
  - Outlier

Reliable mass production – How?!



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Reliable mass production

Target

- High quality and high reliability
- During total production time
- Reaching low level of rejects during production and operation
- Successful start up of production processes

Procedure

Step 1: Design of Experiments (DoE[1])

Step 2: Process control including statistical calculation (SPC[2] / DI[3])

Step 3: Detecting potential field failures

[1] SPC: statistical process control

[2] DoE: Design of Experiments

[3] DI: Design index

Reliable mass production

Introduction of processes

Key questions

- How can the process be optimized?
- What are the key parameters?
- Which parameters should we use for SPC[1]?
- Are there any unknown parameters?
- What happens if quality in materials and components are changing?

Recommendation: Running design of experiments (DoE)

Constrains

- Well established processes — running with long time experience
- Time frame — need for rapid start of production
- Very complex approach approach — mostly not possible with “EXCEL”

[1] SPC: statistical process control

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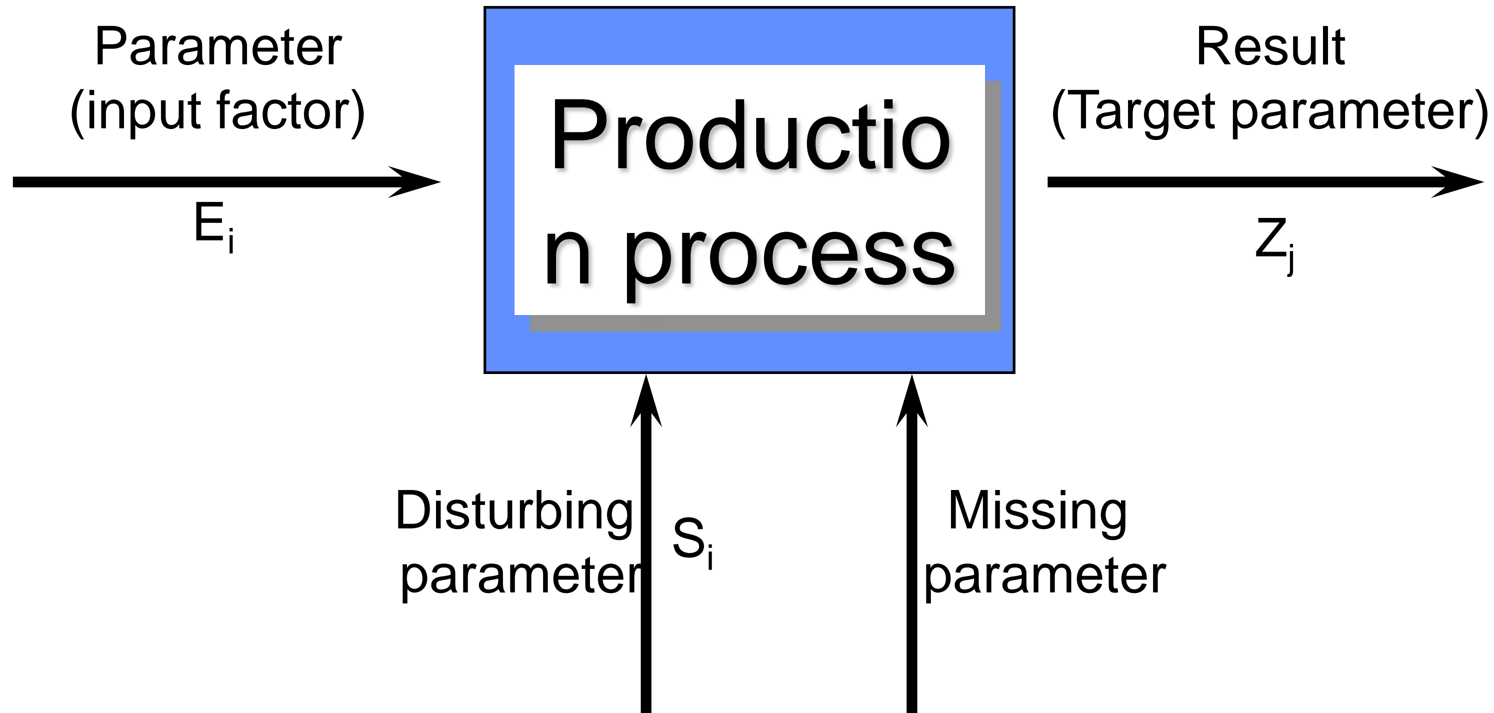
Step 1 / Abstract description of a process



Goal: description of process
knowing the best variable for optimization
despite of disturbing and missing parameters

i: input
j: output

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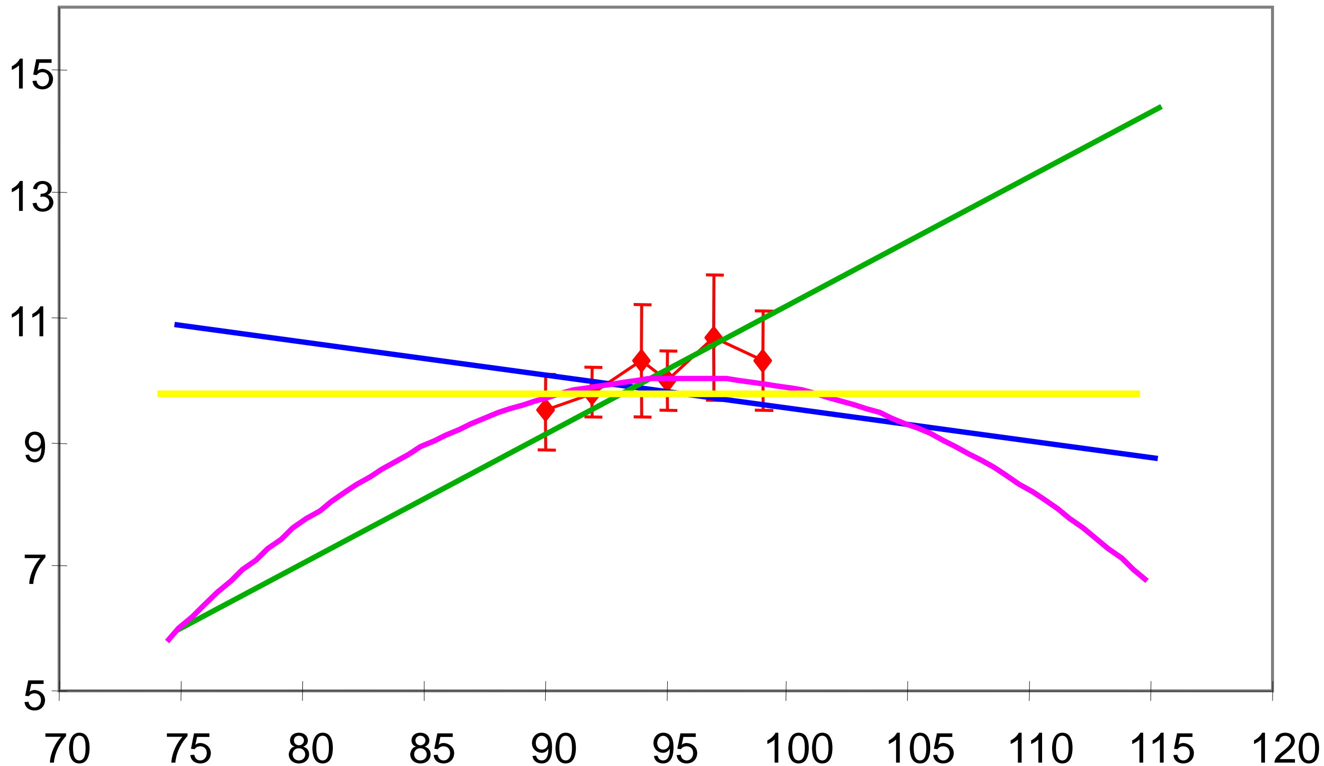
Step 1 / Task (example for 1 dimension)



Step 1 / Procedure

- Process to be investigated?
- Parameters (factors which are to be varied)
- Limits (go to edge of the process)
- Experimental plan (using algorithms to reduce quantity of parameters)
- Performing the experiment
- Calculation of results
  - Dependence of parameters
  - Results for optimized parameters
  - Prediction

Example

- Reflow soldering process
- Parameters:
  - Reflow Oven
    Atmosphere
    Profile
  - Solder paste
    Type
    Delivery
  - Mask type
- Given from running process
  (only for this example)

Step 1 / Example for use in process optimization

- Task: Introduction of new solder paste in PCB assembly process

- Parameters:

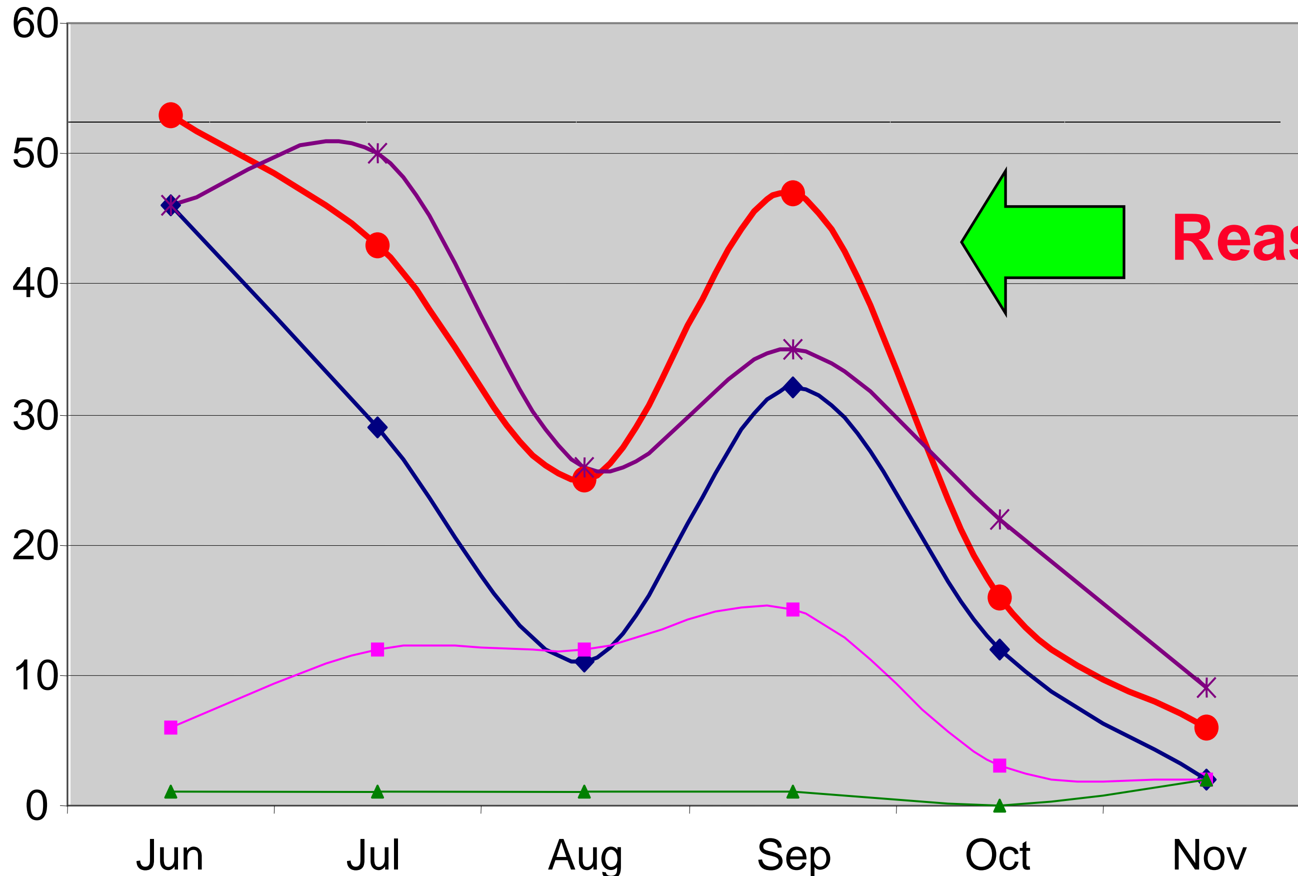
Reflow Oven	Atmosphere
	Profile
Solder paste	Type
	Delivery
Mask type	

- Limits and Experimental plan

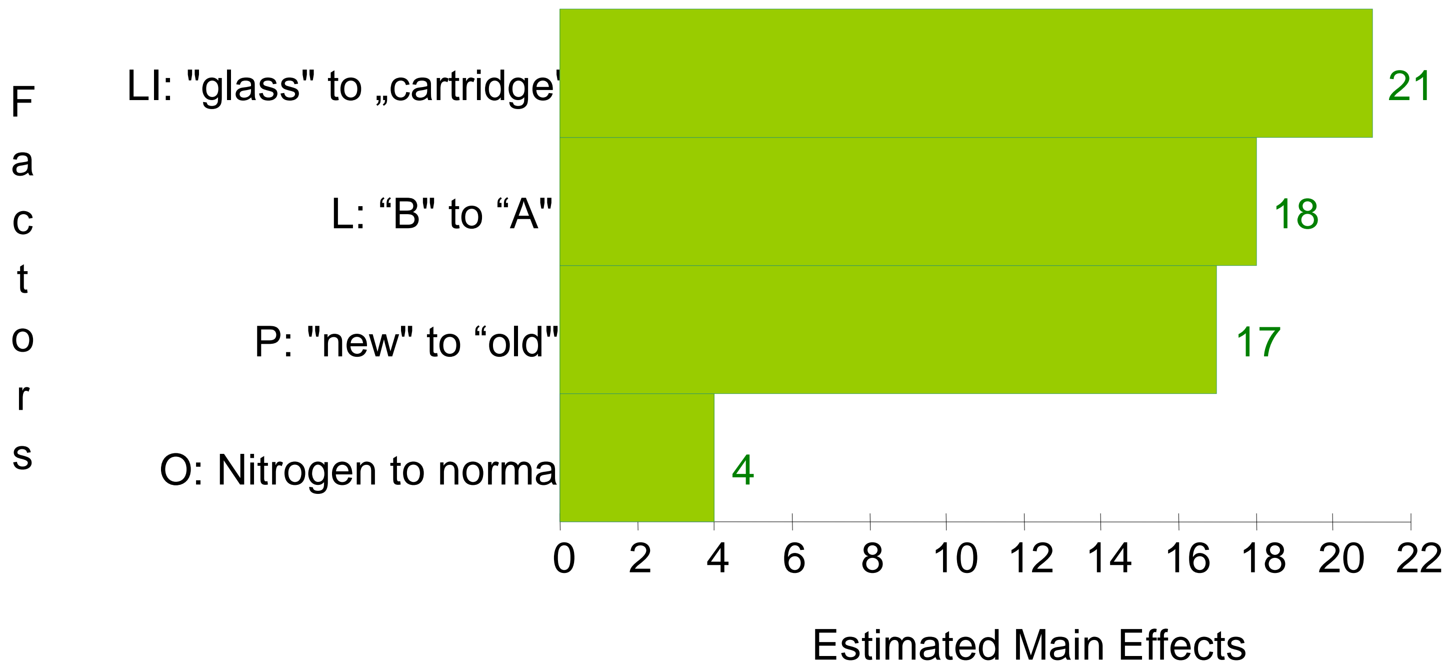
	Oven		Solder paste		
	Oven	Profile	Type	delivery	Mask type
Jun	Normal	old	A	glass	big
Jul	Normal	new	A	glass	big
Aug	Normal	new	B	glass	big
Sep	Normal	new	B	cartridge	small
Okt	Nitrogen	new	B	glass	small
Nov	Nitrogen	new	B	glass	small

Step 1 / Example for use in process optimization

- Results



Step 1 / Dependence for tombstone

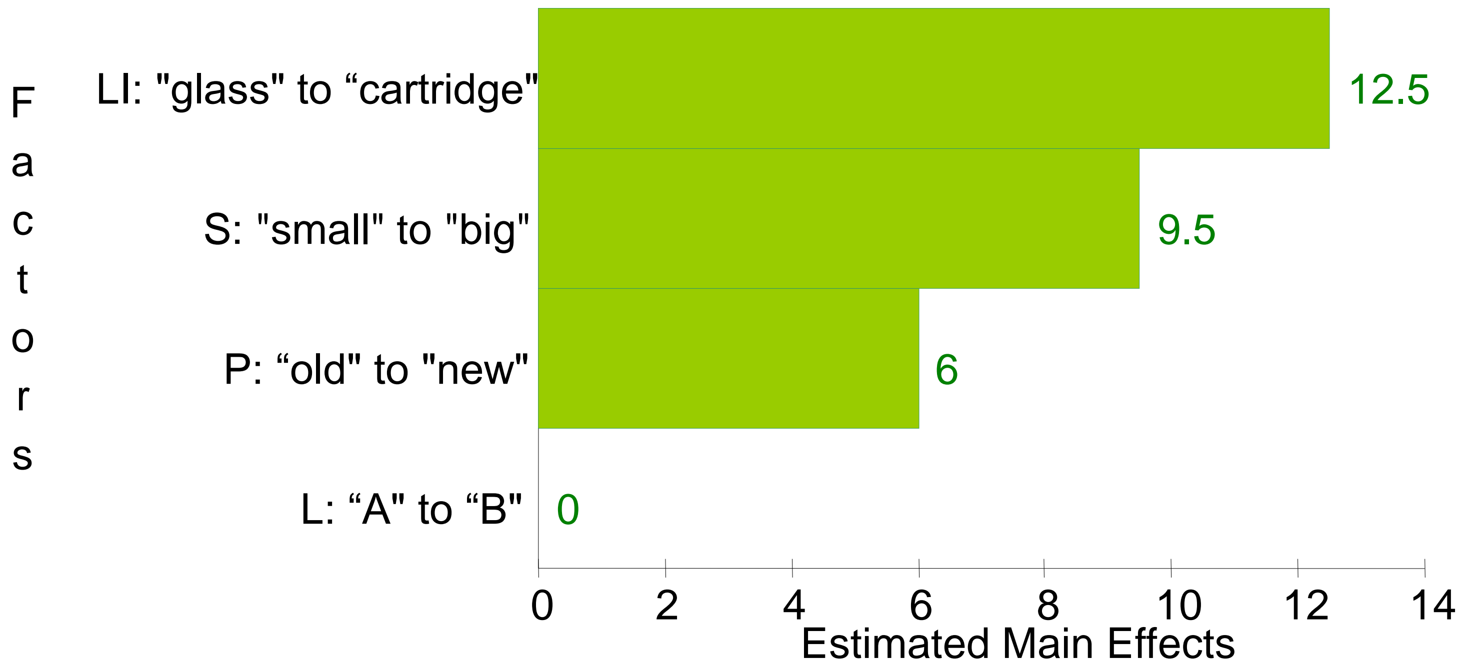


Additional information:

Data not complete

Model contains not all input factors

Step 1 / Dependence for solder bridge



Additional information:

Model describes the data nearly complete

that means: there are no other input factors

Step 1 / optimization and prediction

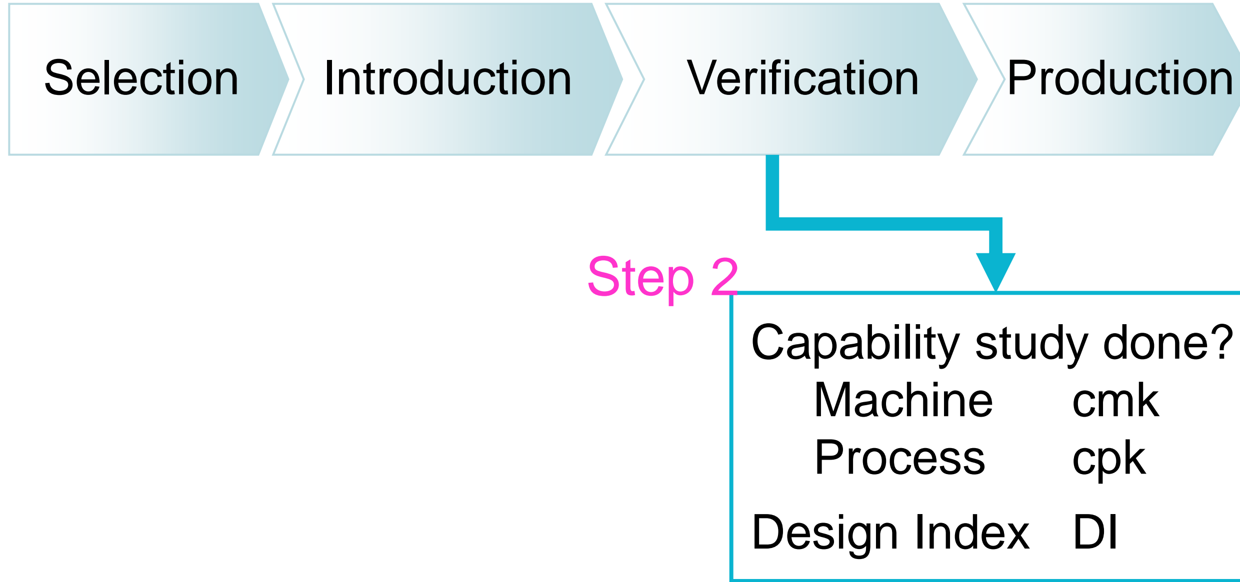
- Optimized
  - Parameter Delivery glass
  - Mask type small
  - Profile new

- Prediction separately for both types of solder paste

	Oven	
Solder paste	Nitrogen	Normal
A	29 ppm equals 3,8% PCB failure	43 ppm
B	11 ppm equals 1,4% PCB failure	25 ppm

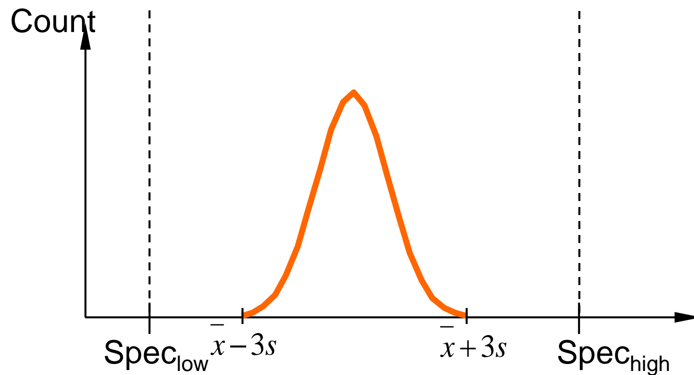
Reliable mass production – How?!

Definition of processes



Step 2 / Definition capability & design index

Capability Index

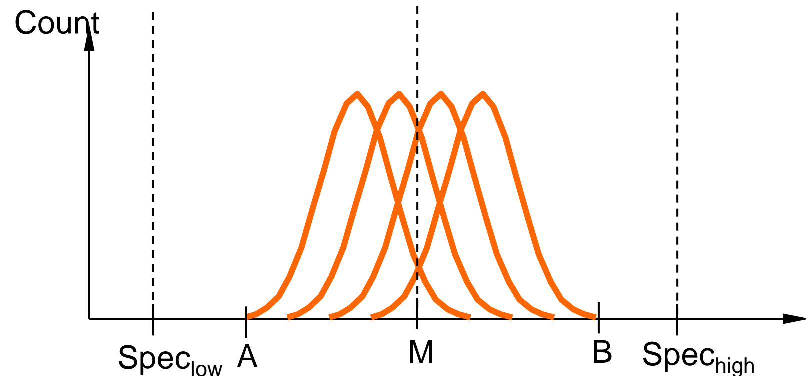


Assumption upper limit closer

$$c_{pk} = \left(\frac{USL - \bar{x}}{3s} \right) > 1{,}66$$

c_{pk}	Capability index
$\bar{x}$	Mean value
USL	Upper specification limit
s	Standard deviation

ex

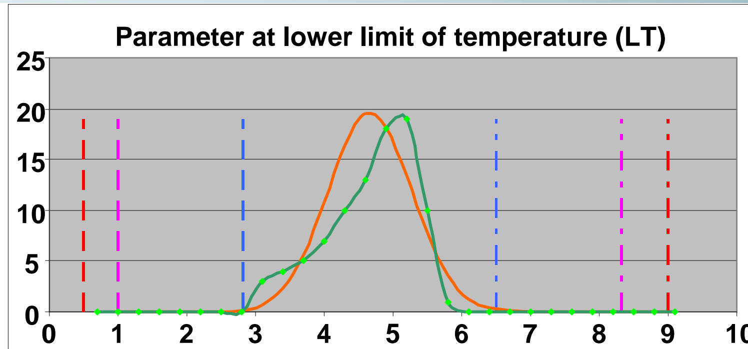


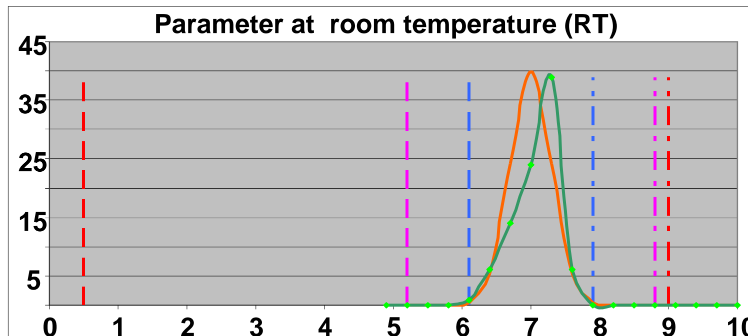
Assumption upper limit closer

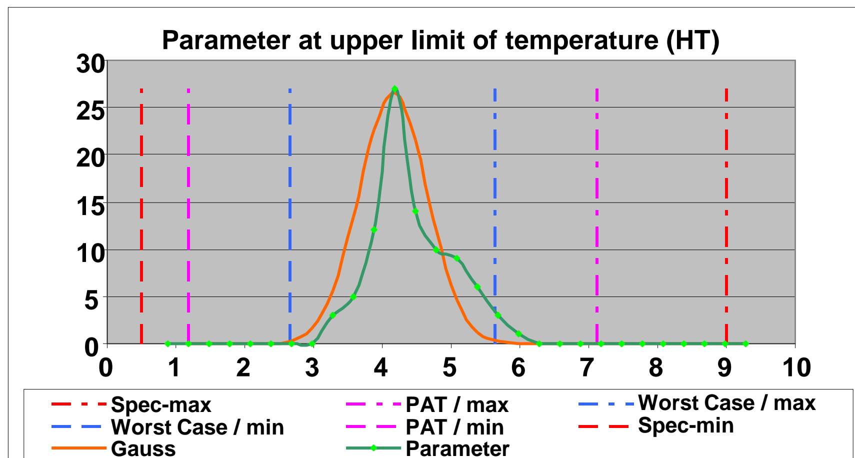
$$DI = \left(\frac{USL - M}{B - M} \right) > 1$$

DI	Design index	$M = ½ (A + B)$
x_{mi}	Mean value – single test	$A = min (x_{mi} + x_{iCL} + 3s)$
M	Mean value – single test	$B = max (x_{mi} + x_{iCL} + 3s)$
USL	Upper specification limit	
x_{iCL}	Confidence range of mean	

Step 2 / Example capability & design index







- Measurement at RT
- Different results at LT and HT

- C_{LT} = 2,27
- C_{RT} = 2,23 DI = 1,39
- C_{HT} = 2,45

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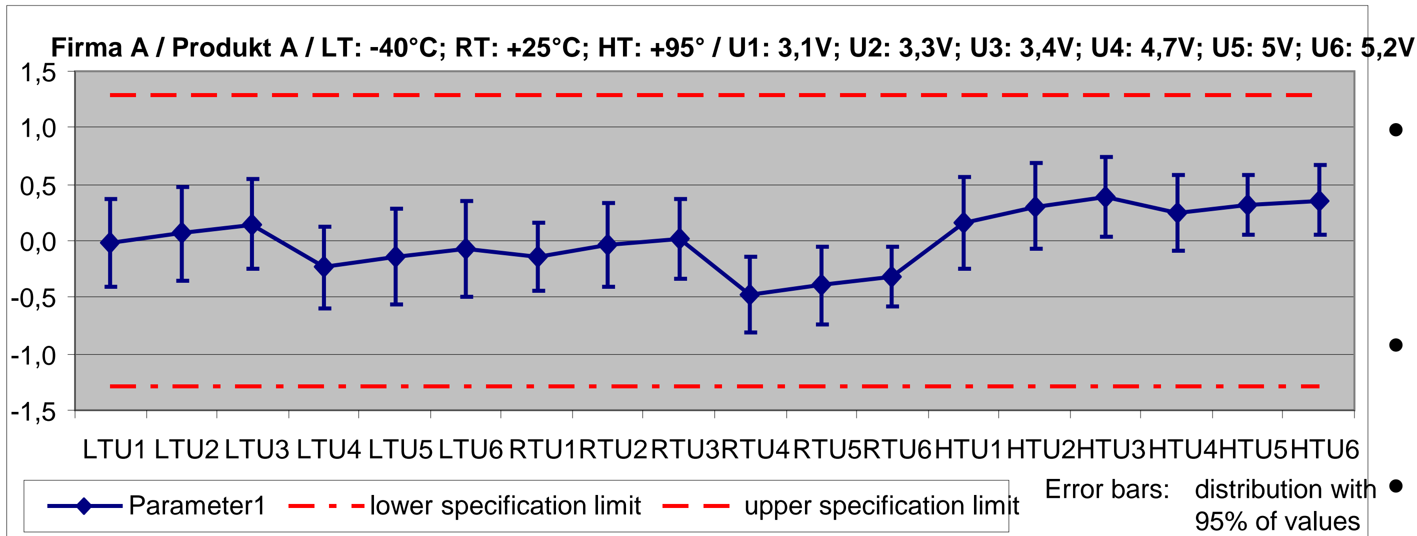
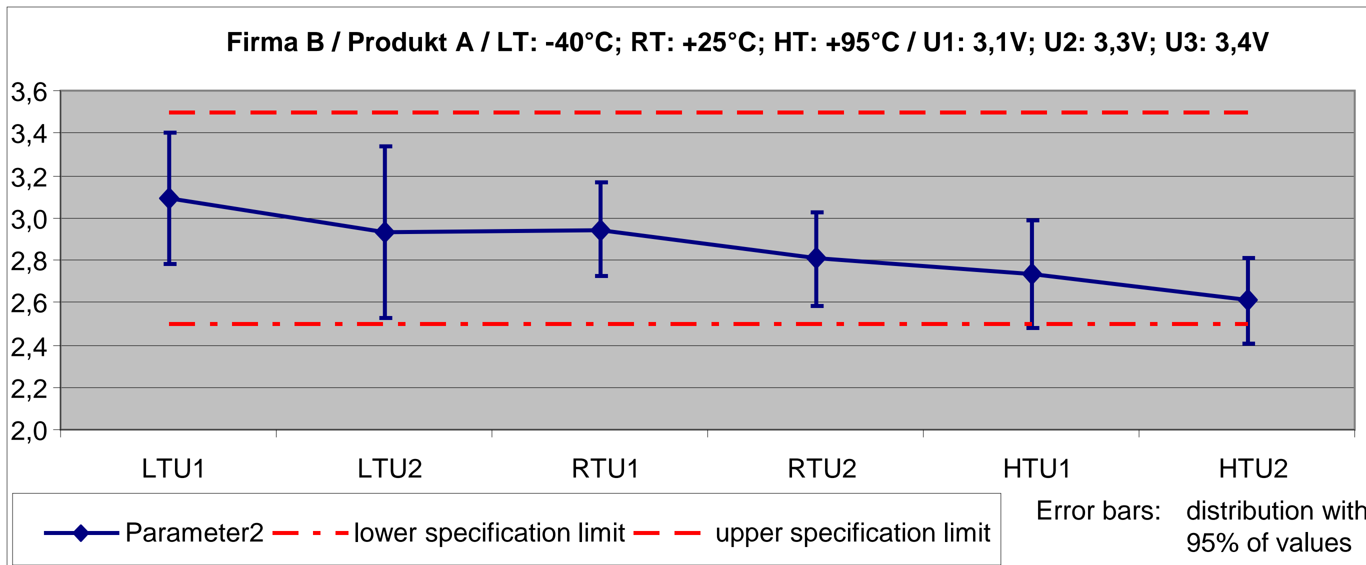
Step 2 / Example design index



- Variation
  - Temperature
  - Voltage
- Within the limits
- DI = 1,59



- Variation
  - Temperature
  - Voltage
- Partly outside of limits
- DI = 0,82

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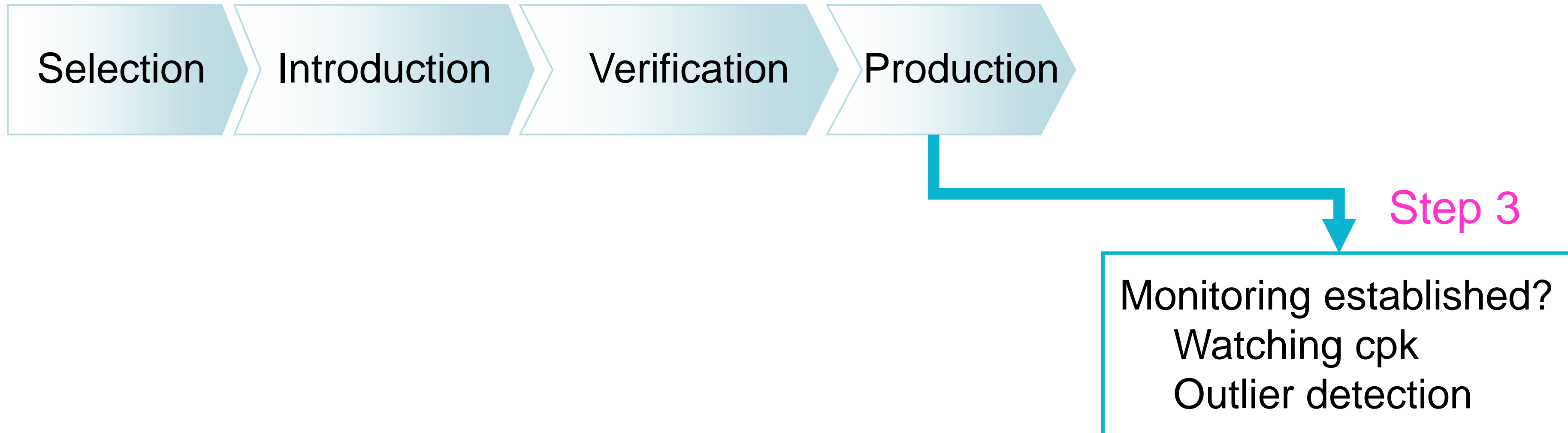
Reliable mass production – How?!



Step 3 / Identification potential field failure

- Method
  - Failures in the field are products with „not normal“ behavior
  - „Normal“ behavior: measurement with normal distribution
  - Measurements outside the normal distribution ➔ potential failures

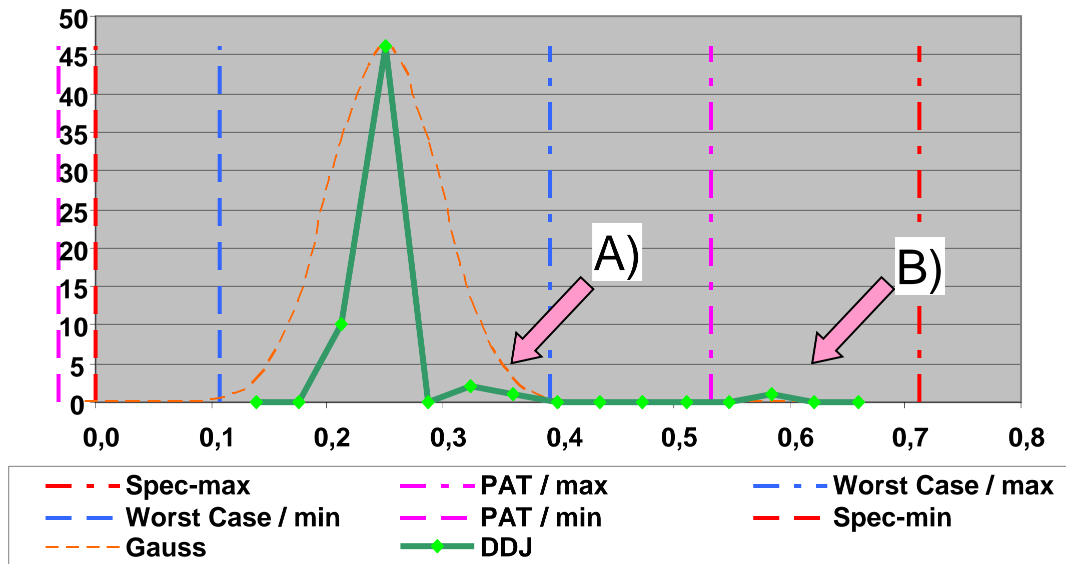
- Task
  - Search for outliers

- Procedure
  - Using data of testing within production (e.g. in-circuit test)
  - Statistical calculation using the data
  - Verification (checked by developing specialist)
  - Repair / scrap

Step 3 - Task

Judgment using standard data from mass production

▪ Distribution	process, product
▪ Drift behavior	product
▪ Identification of not normal properties	product



A) suspicious, but within distribution (2 & 1 value)

B) suspicious, outside of distribution ➔ outlier

Step 3 / Procedure

- Collecting data (from test, process, ...)
- Statistical calculation
  - robust mean
  - robust standard deviation

$$\bar{x}_{rob} = Median(Daten)$$

$$\sigma_{rob} = \left(\frac{Q3 - Q1}{1,35} \right) \quad \{61\}$$

$$Q1 = Quartile(Daten;1)$$

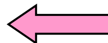
$$Q3 = Quartile(Daten;3)$$

- Identification of outlier
- Investigation of identified products
- During start-up better results with additional measurements at limits of temperature

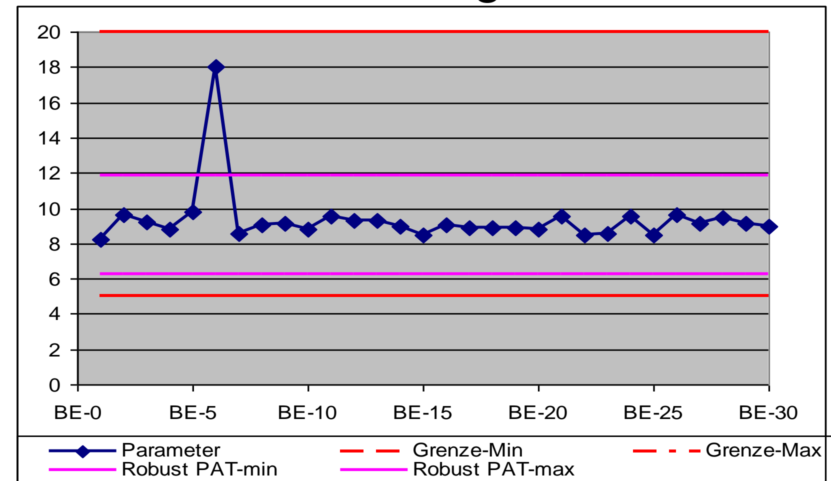
Step 3 – Robust mean / example

Data

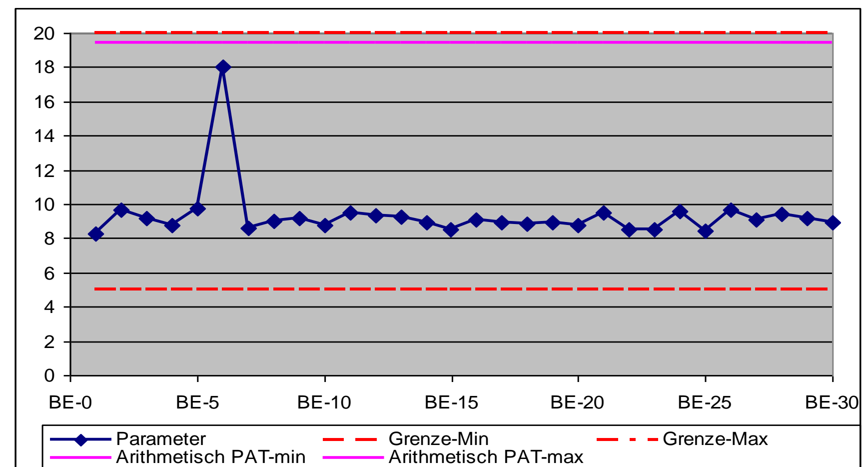
Bauelement	Parameter
BE-1	8,24
BE-2	9,67
BE-3	9,19
BE-4	8,81
BE-5	9,76
BE-6	**18,0**
BE-7	8,57
BE-8	9,04
BE-9	9,15
BE-10	8,79
BE-11	9,54
BE-12	9,33
BE-13	9,3
BE-14	8,97
BE-15	8,51
BE-16	9,08
BE-17	8,91
BE-18	8,87
BE-19	8,92
BE-20	8,79
BE-21	9,54
BE-22	8,5
BE-23	8,53
BE-24	9,55
BE-25	8,48
BE-26	9,66
BE-27	9,12
BE-28	9,46
BE-29	9,14
BE-30	8,97



Calculation with “robust” algorithm



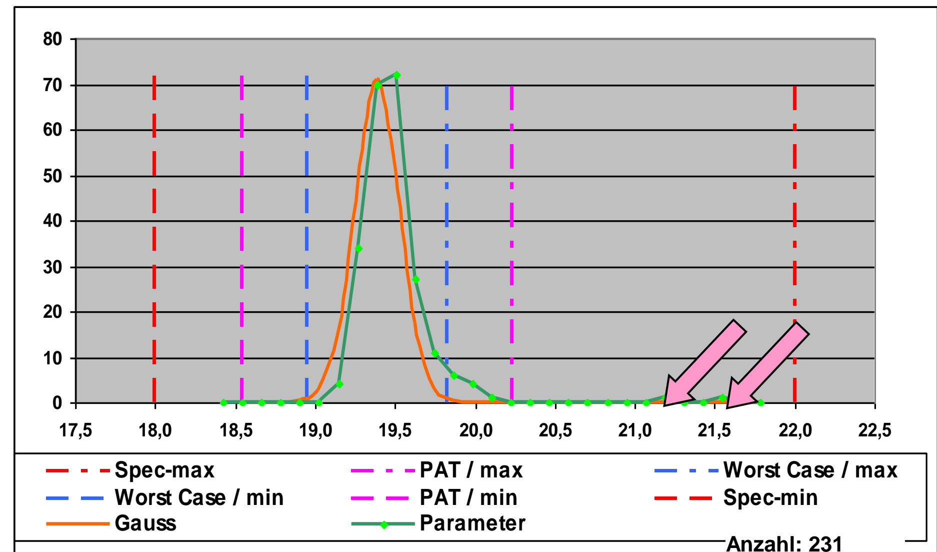
Calculation with “arithmetic” algorithm

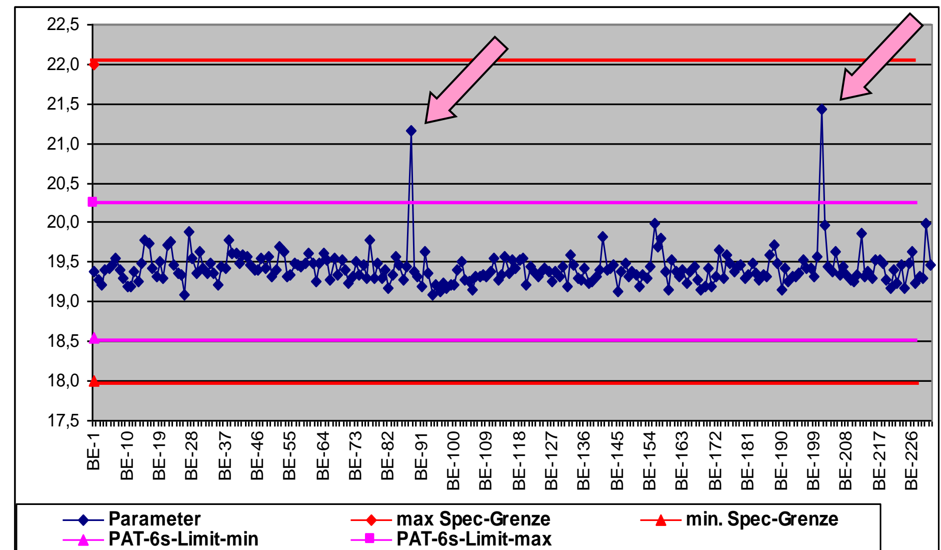


Step 3 – Example / Outlier

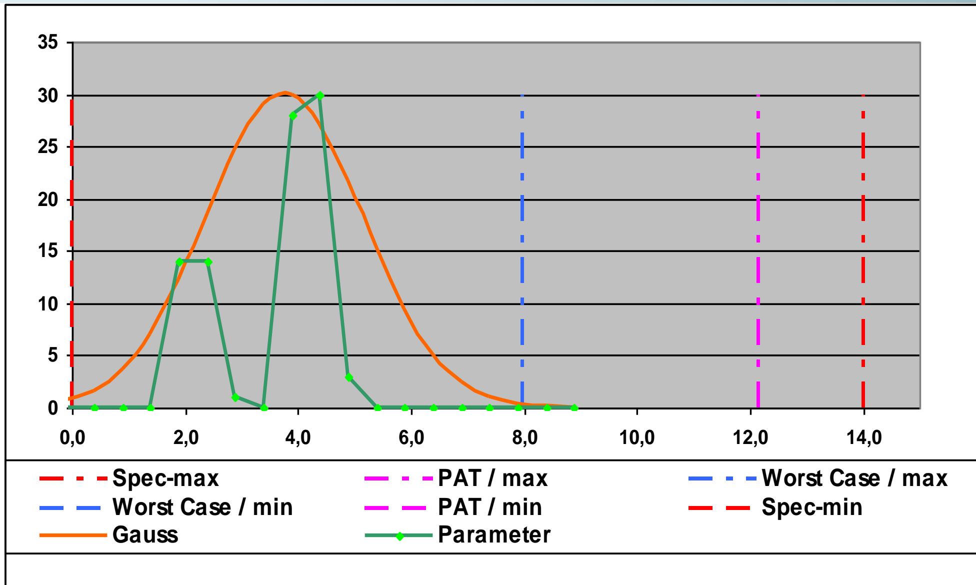
- Measurements with normal distribution (approximately)
- 2 measurements outside of calculated limits
- Special investigation necessary:
  high potential of failure?

  No delivery!

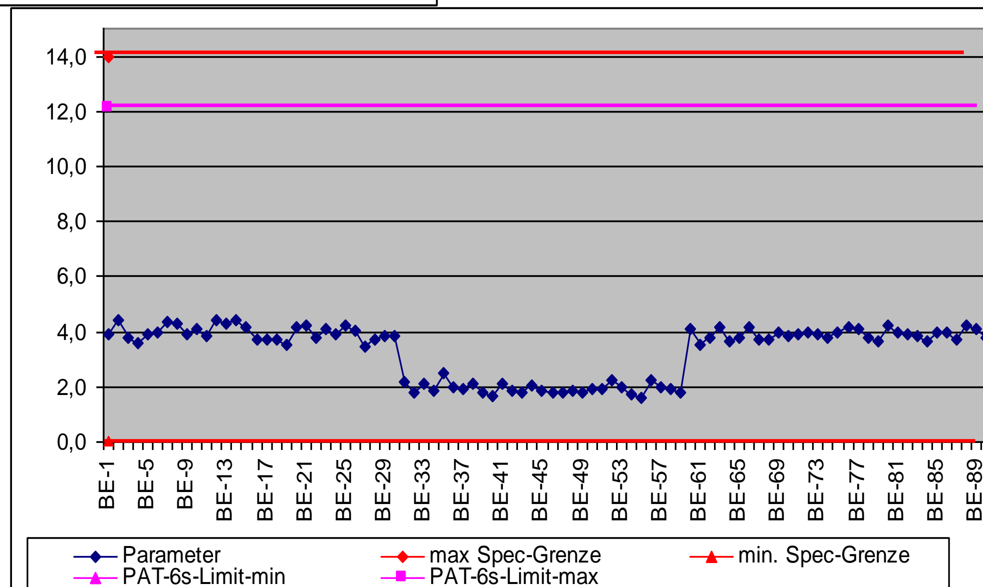




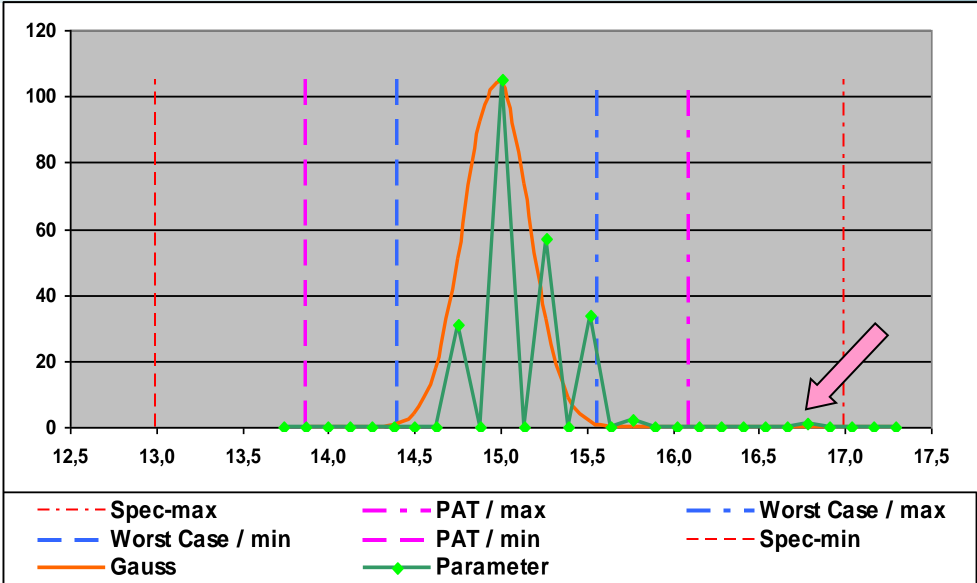
Step 3 – Example / local – global aspect of calculation



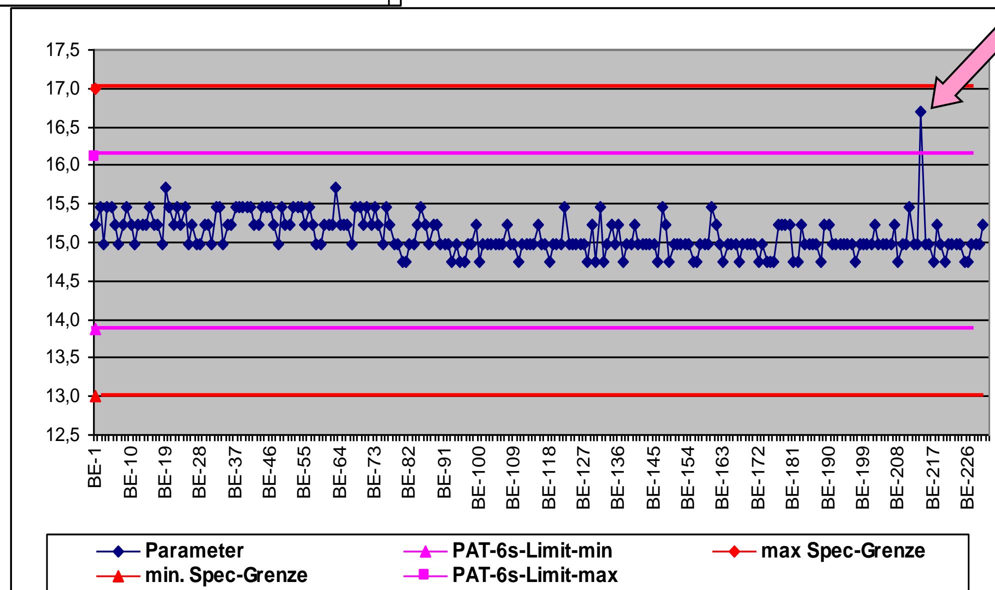
- Outlier not detectable with global approach
- Reason:
  Variation of different lots?



Step 3 – Strange behavior



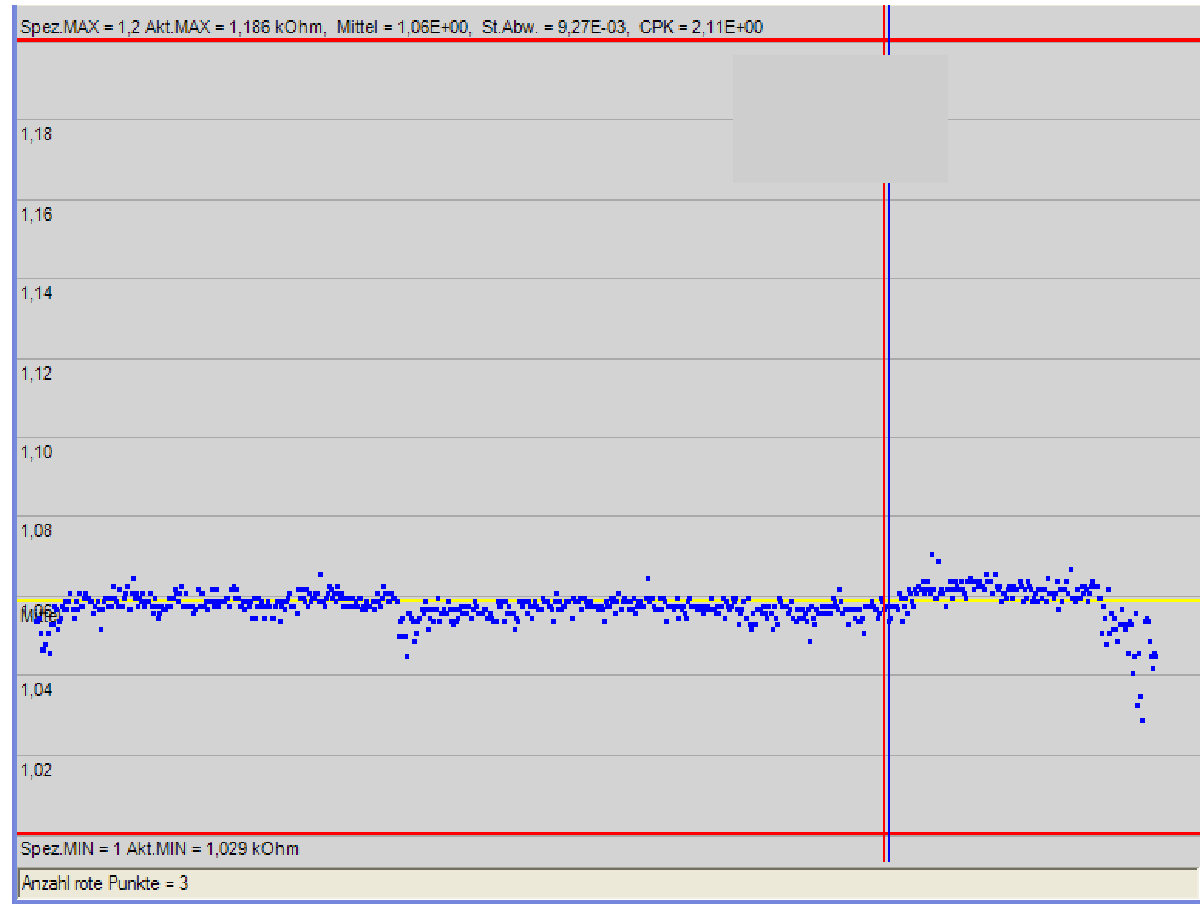
- Reason measurement at limit of resolution (quantification)
- Outlier



smthybridpackaging

Step 3 – Identification potential field failure / example

- All measurements within specification limits
- Capability index okay (2,11)
- 3 „not normal“ values



Conclusion

- Reliability is one of the key issues now and in the future
- Established tool are to improved to fulfill the further needs
- Knowledge of processes is the basis to have reliable products
- Existing data should be used more to improve the processes (as shown to detect outliers)

Contact information

Key Facts

- Founded in 2005 in College Park, MD
- 20+ Employees
  - Multiple US locations
- Offerings
  - Research, Lab Services, Consulting, Software
- 300+ customers, including:
  - Dell, HP, Apple, Microsoft, IBM, Ericsson, Cisco Systems, Verizon, Huawei, Polycom, AMD, and Nvidia

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