DfR Solutions

reliability designed, reliability delivered

Design for Reliability: PCBs

North Texas IPC Designers Council

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April 10, 2013

PCB DfR Abstract

- Designing printed boards today is more difficult than ever before because of the increased lead free process temperature requirements and associated changes required in manufacturing. Not only has the density of the electronic assembly increased, but many changes are taking place throughout the entire supply chain regarding the use of hazardous materials and the requirements for recycling.
- Much of the change is due to the European Union (EU) Directives regarding these issues. The RoHS and REACH directives have caused many suppliers to the industry to rethink their materials and processes. Thus, everyone designing or producing electronics has been or will be affected.

Course Outline

INTRODUCTIONS

- Intro to Design for Reliability (DfR)
- DfR & Physics of Failure (PoF)

PRINTED CIRCUIT BOARD ISSUES

- Laminate Selection
- Plated Through Vias (PTVs)
- PTH Barrel Cracking
- CAF
- Strain/Flexure Issues & Pad Cratering
- Cleanliness
- Electrochemical Migration
- Surface Finishes

Design for Reliability (DfR) Defined

- DfR: A process for ensuring the reliability of a product or system during the design stage *before* physical prototype

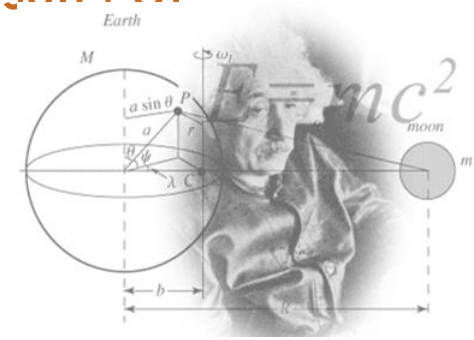
- Reliability: The measure of a product's ability to
  - …perform the specified function
  - …at the customer (with their use environment)
  - …over the desired lifetime

Why Design for Reliability (DfR)?

- The foundation of a reliable product is a robust design
  - Provides margin
  - Mitigates risk from defects
  - Satisfies the customer

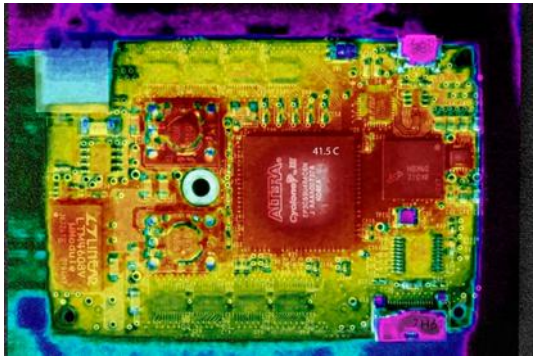
Physics of Failure (PoF)

- PoF Definition: The use of science (physics, chemistry, etc.) to capture an understanding of failure mechanisms and evaluate useful life under actual operating conditions
- Using PoF, design, perform, and interpret the results of *accelerated* life tests
  - Starting at design stage
  - Continuing throughout the lifecycle of the product
- Start with standard industry specifications
  - Modify or exceed them
  - Tailor test strategies specifically for the individual product design and materials, the use environment, and reliability needs



Physics of Failure Definitions

- Failure of a physical device or structure (i.e. hardware) can be attributed to the gradual or rapid degradation of the material(s) in the device in response to the stress or combination of stresses the device is exposed to, such as:
  - Thermal, Electrical, Chemical, Moisture, Vibration, Shock, Mechanical Loads . . .



- Failures May Occur:
  - Prematurely
  - Gradually
  - Erratically

Design for Reliability At Concept: Specifications

- Can DfR mistakes occur at this stage?
  - No……..and Yes
- Failure to capture and understand product specifications at this stage lays the groundwork for mistakes at schematic and layout
- Important specifications to capture at concept stage
  - Reliability expectations
  - Use environment
  - Dimensional constraints
- A perfectly designed & constructed PCB can still be unreliable if materials are chosen poorly – even if made to IPC Class 3!

A Word on Quality, Reliability & Class 2 versus Class 3

- Good quality is necessary but not SUFFICIENT to guarantee high reliability.
- Class 3 by itself does not guarantee high reliability
  - A PCB or PCBA can be perfectly built to IPC Class 3 standards and still be totally unreliable in its final application.
  - Consider two different PCB laminates both built to IPC Class 3 standards.
    - Both laminates are identical in all properties EXCEPT one laminate has a CTEz of 40 and the other has a CTEz of 60.
    - The vias in the laminate with the lower CTEz will be MORE reliable in a long term, aggressive thermal cycling environment than the CTEz 60 laminate.
    - A CTEz 40 laminate built to IPC class 2 could be MORE reliable than the CTEz 60 laminate built to Class 3.
    - Appropriate materials selection for the environment is key!

Laminate Selection

Plated Through Vias (PTVs)

PTH

Barrel Cracking

Conductive Anodic Filaments (CAF)

PCB Materials / Laminate Selection

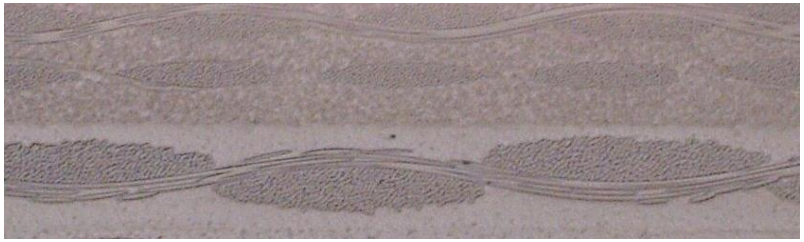
- Laminate selection is frequently under specified! Some common occurrences:
  - PCB supplier frequently allowed to select laminate material
  - No restrictions on laminate changes
  - Generic IPC slash sheet requirements used
  - Laminates called out by Tg only and with no measurement method specified (there is more than one)
  - No cleanliness requirements specified
  - Failure to specify stackup
- Not all laminates are created equal
  - Failure to put some controls in places opens the door to failure

PCB Materials and Plated Through Via Reliability

- Historically, two material properties of concern
  - Out-of-plane coefficient of thermal expansion (CTE_z)
  - Out-of-plane elastic modulus ('stiffness')(E_z)

- Key Assumption: No exposure to temperatures above the glass transition temperature (Tg)

- The two material properties (CTE and E) are driven by choices in resin, glass style, and filler



Laminate Datasheets

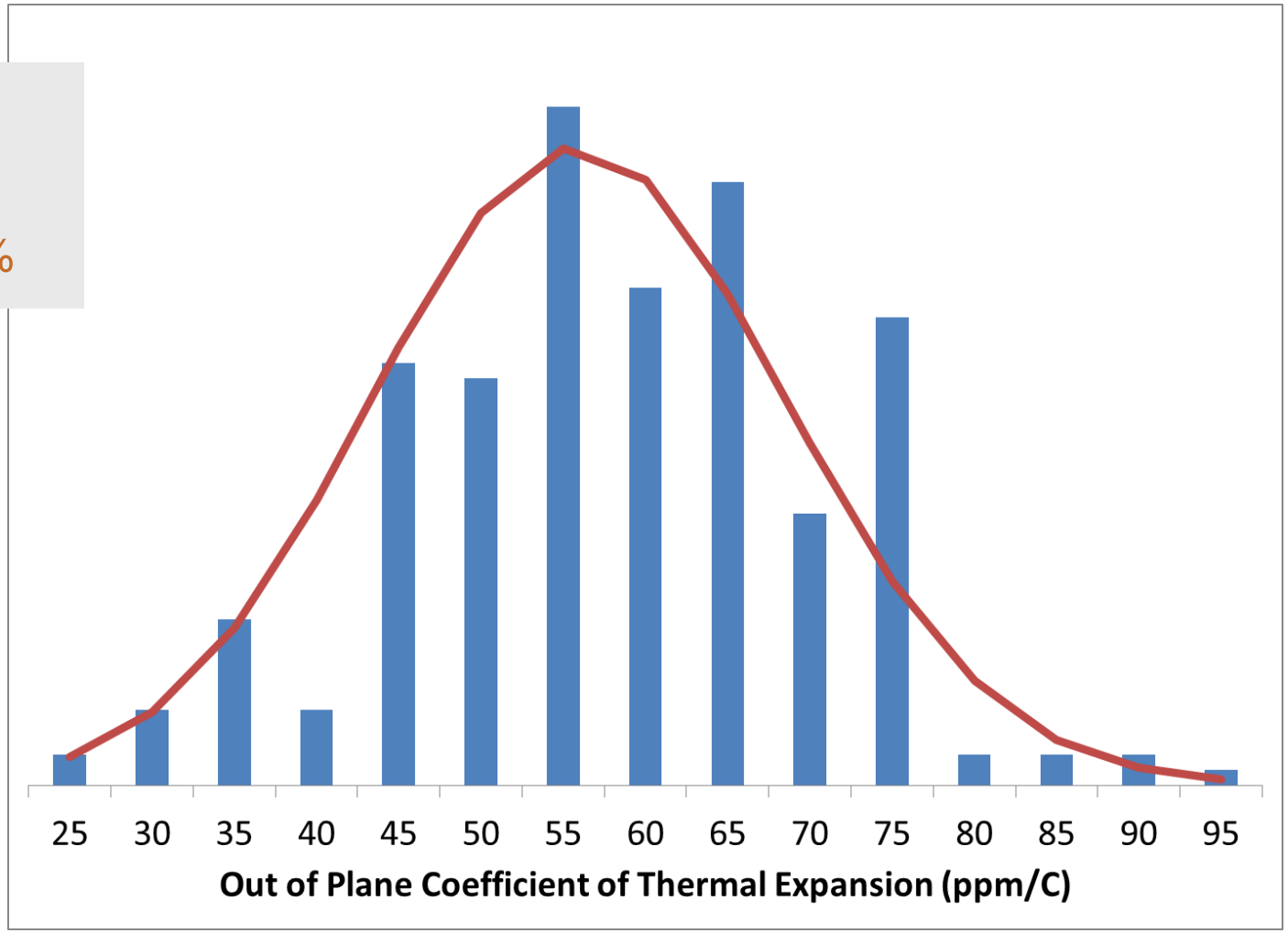
- Out-of-plane CTE (CTEz) is almost always provided on the laminate datasheet
  - Sometimes in ppm/C above and below the Tg
  - Sometimes in % between 50-260C

$$1/E_{laminate} = V_{epoxy}/E_{epoxy} + V_{fiber}/E_{fiber}$$

- Out-of-plane modulus (Ez) is almost never provided on the laminate datasheet
  - Requires calculation based on in-plane laminate properties, glass fiber properties, glass fiber volume fraction, and Rule-of-Mixtures / Halpin-Tsai models

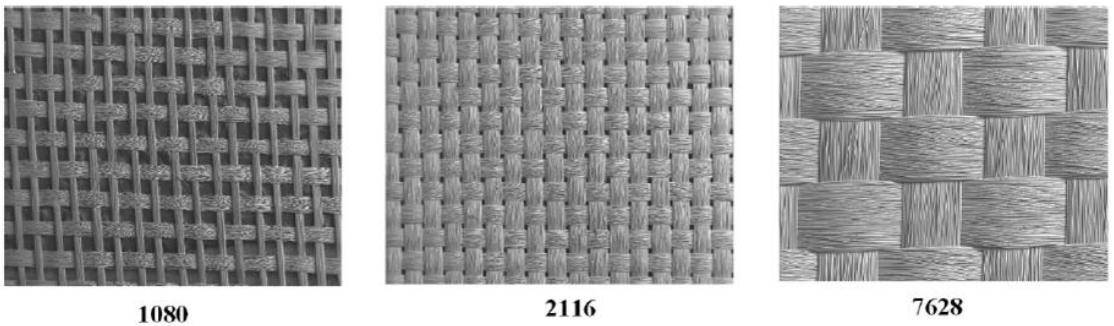
Survey of 300 Different FR-4 Datasheets

- Out-of-plane expansion ranged from 1.4% to 4.8%



Glass Style

- PCB laminates (and prepregs) are fabricated with a variety of glass styles



- Problem: All datasheet properties are for laminate with 7628 glass style

- Most laminate (and all prepreg) in complex PCBs have a low volume fraction of glass (i.e., 1080 or 106)

Glass Style	Resin Volume Content	Fiber Volume Content
1027	0.86	0.14
1037	0.86	0.14
106	0.84	0.16
1067	0.84	0.16
1035	0.83	0.17
1078	0.82	0.18
1080	0.79	0.21
1086	0.78	0.22
2313	0.74	0.26
2113	0.72	0.28
2116	0.71	0.29
3313	0.71	0.29
3070	0.68	0.32
1647	0.66	0.34
1651	0.66	0.34
2165	0.66	0.34
2157	0.66	0.34
7628	0.64	0.36

Glass Style and CTE

Glass Style	Modulus of Elasticity Ez (MPa)	CTEz (ppm)
1027	4380.4	73.9
1037	4380.4	73.9
106	4478.2	72.3
1067	4478.2	72.3
1035	4528.7	71.5
1078	4580.3	70.7
1080	4742.7	68.4
1086	4799.3	67.6
2313	5040.4	64.4
2113	5170.2	62.8
2116	5237.6	62.0
3313	5237.6	62.0
3070	5450.9	59.7
1647	5603.1	58.1
1651	5603.1	58.1
2165	5603.1	58.1
2157	5603.1	58.1
7628	5764.0	56.5

Laminate Properties (cont.)

- More recently, additional laminate properties of concern due to Pb-free assembly
  - Glass transition temperature (Tg)
  - Time to delamination (T260, T280, T288, T300)
  - Temperature of decomposition (Td)

- Each parameter 'supposedly' captures a different material behavior
  - Higher number slash sheets (> 100) within IPC-4101 define these parameters to specific material categories

Thermal Parameters of Laminate

- Glass transition temperature (Tg) (IPC-TM-650, 2.4.24/2.4.25c)
  - Characterizes complex material transformation (increase in CTE, decrease in modulus)
- Time to delamination (T-260/280/288/300) (IPC-TM-650, 2.4.24.1)
  - Characterizes interfacial adhesion
- Temperature of decomposition (Td) (IPC-TM-650, 2.3.40)
  - Characterizes breakdown of epoxy material

Thermal Parameters and IPC Slash Sheets

IPC-4101	99	101	102	103	121	122	124	125	126	127	128	129	130	131
ANSI	FR4	FR4	PPE	PPO	FR4	HF-FR4	FR4	HF-FR4	FR4	HF-FR4	HF-FR4	FR4	HF-FR4	HF-FR4
Fillers > 5%	Yes	Yes	Yes	Yes	N/A	N/A	N/A	N/A	Yes	Yes	Yes	N/A	Yes	N/A
Tg	>150° C	>110° C	>185° C	>150° C	>110° C	>110° C	>150° C	>150° C	>170° C	>110° C	>150° C	>170° C	>170° C	>170° C
Td	>325° C	>310° C	>340° C	>325° C	>310° C	>310° C	>325° C	>325° C	>340° C	>310° C	>325° C	>340° C	>340° C	>340° C
CTE 50-260°C	<3,5 %	<4%	<2,8 %	<3,5 %	<4%	<4%	<3,5 %	<3,5 %	<3,0 %	<4%	<3,5 %	<3,5 %	<3,0 %	<3,5 %
T260	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min	>30 min
T288	>5 min	>5 min	>15 min	>5 min	>5 min	>5 min	>5 min	>5 min	>15 min	>5 min	>5 min	>15 min	>15 min	>15 min
T300	---	---	>2 min	---	---	---	---	---	>2 min	---	---	>2 min	>2 min	>2 min

HDI Printed Circuit Boards, NCAB Group

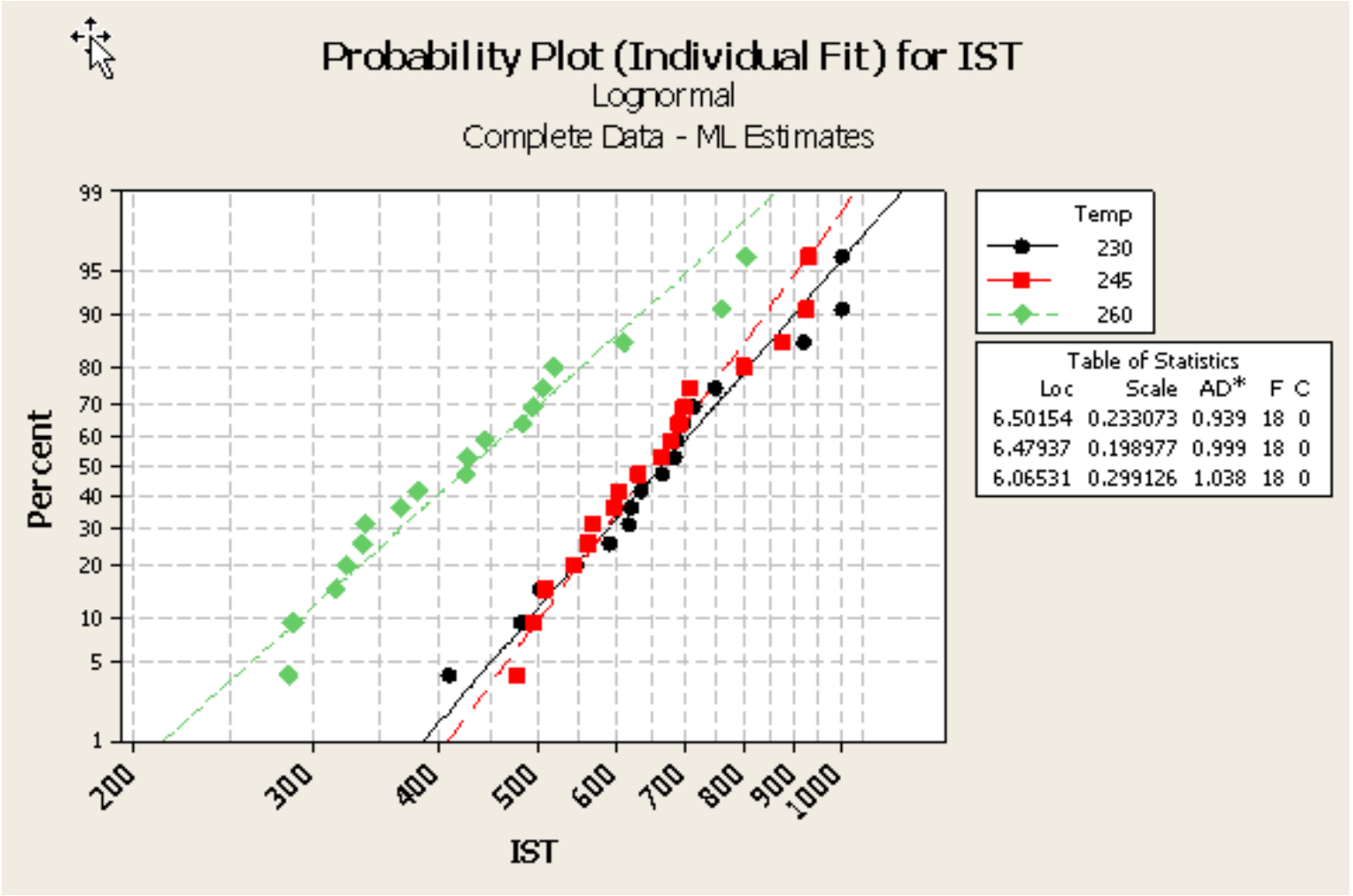
PCB Material Selection

Board thickness	IR-240~250℃	Board thickness	IR-260℃
≤60mil	Tg140 Dicy All HF materials OK	≤ 60mil	Tg150 Dicy HF- middle and high Tg materials OK
60~73mil	Tg150 Dicy NP150, TU622-5 All HF materials OK	60~73mil	Tg170 Dicy HF –middle and high Tg materials OK
73~93mil	Tg170 Dicy, NP150G-HF HF –middle and high Tg materials OK	73~93mil	Tg150 Phenolic + Filler IS400, IT150M, TU722-5, GA150 HF –middle and high Tg materials OK
93~120mil	Tg150 Phenolic + Filler IS400, IT150M, TU722-5 Tg 150 HF –middle and high Tg materials OK	93~130mil	Phenolic Tg170 IS410, IT180, PLC-FR-370 Turbo, TU722-7 HF –middle and high Tg materials OK
121~160mil	Phenolic Tg170 IS410, IT180, PLC-FR-370 Turbo TU722-7 HF –high Tg materials OK	≧131mil	Phenolic Tg170 + Filler IS415, 370 HR, 370 MOD, N4000-11 HF –high Tg materials OK
≧161mil	PhenolicTg170 + Filler IS415, 370 HR, 370 MOD, N4000-11 HF material - TBD	≧161mil	TBD – Consult Engineering for specific design review

1. Copper thickness = 2OZ use material listed on column 260 ℃
2. Copper thickness >= 3OZ use Phenolic base material or High Tg Halogen free materials only
3. **Twice lamination product use Phenolic material or High Tg Halogen free materials only (includes HDI)**
4. Follow customer requirement if customer has his own material requirement
5. DE people have to confirm the IR reflow Temperature profile

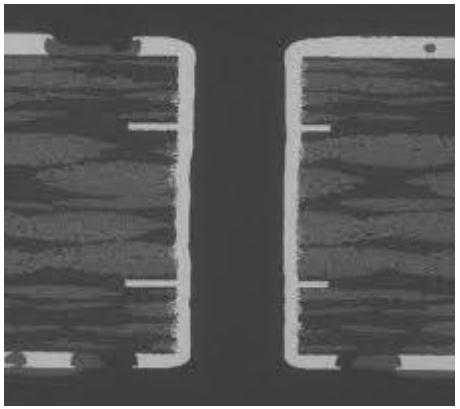
J. Beers, Gold Circuits

PTV Degradation due to Assembly

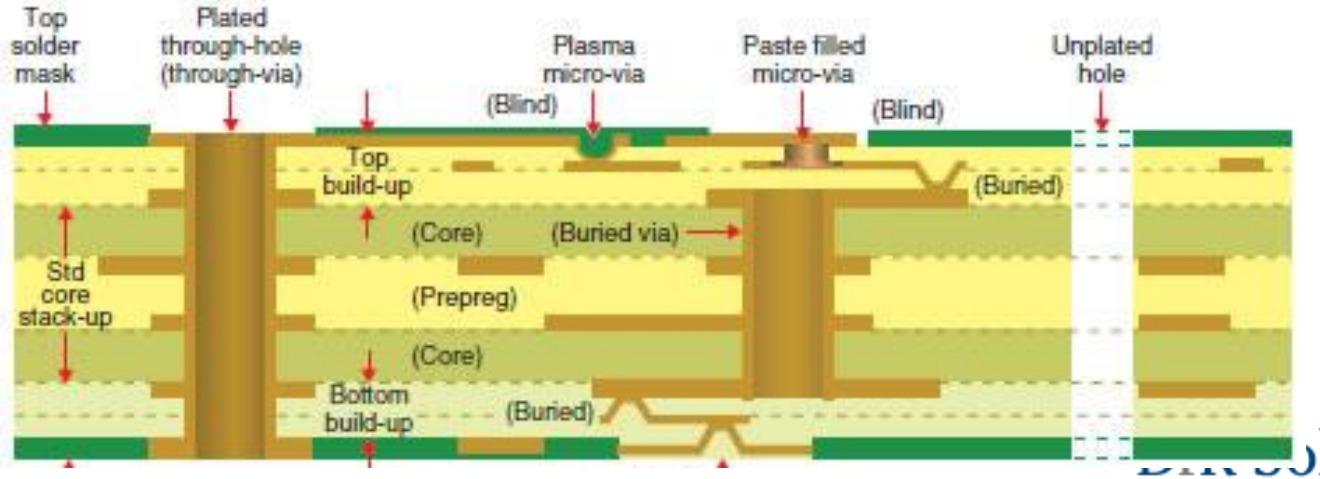


What is a Plated Through Via?

- A plated through via (PTV) is an interconnect within a printed circuit board (PCB) that electrically and/or thermally connects two or more layers

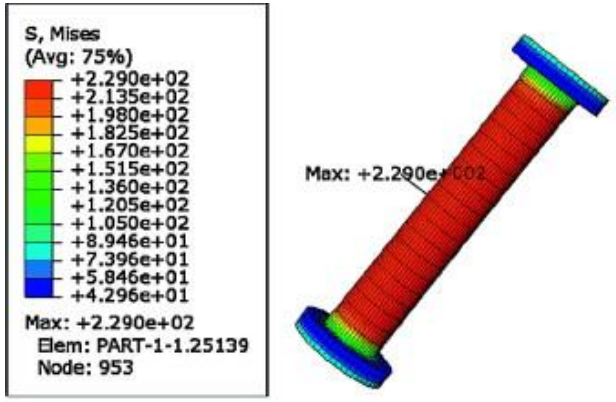


- PTV is part of a larger family of interconnects within PCBs

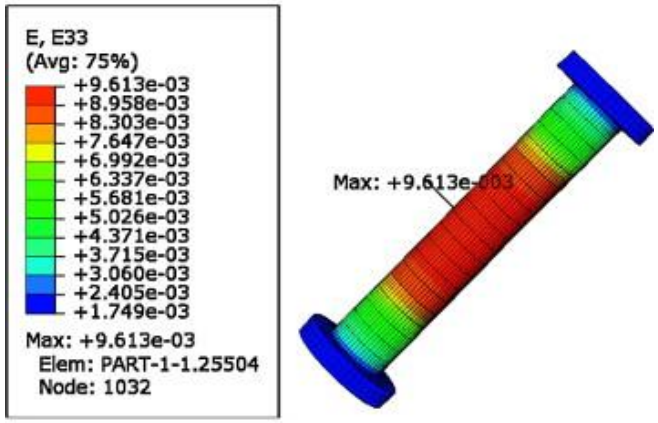


PCB Materials: Stackup

- Maximum stress in the PTV during thermal cycling tends to be in the middle of the barrel
- There is some concern that areas of high resin content in the middle of the barrel can be detrimental
- Non-functional pads (NFP)
  - Some debate as to their influence on barrel fatigue on higher aspect ratio PTV



(a) The Mises stress field of PTH at 150°C



(b) The residual strain field of PTH after 3 cycles

F. Su, et. al., Microelectronics Reliability, June 2012

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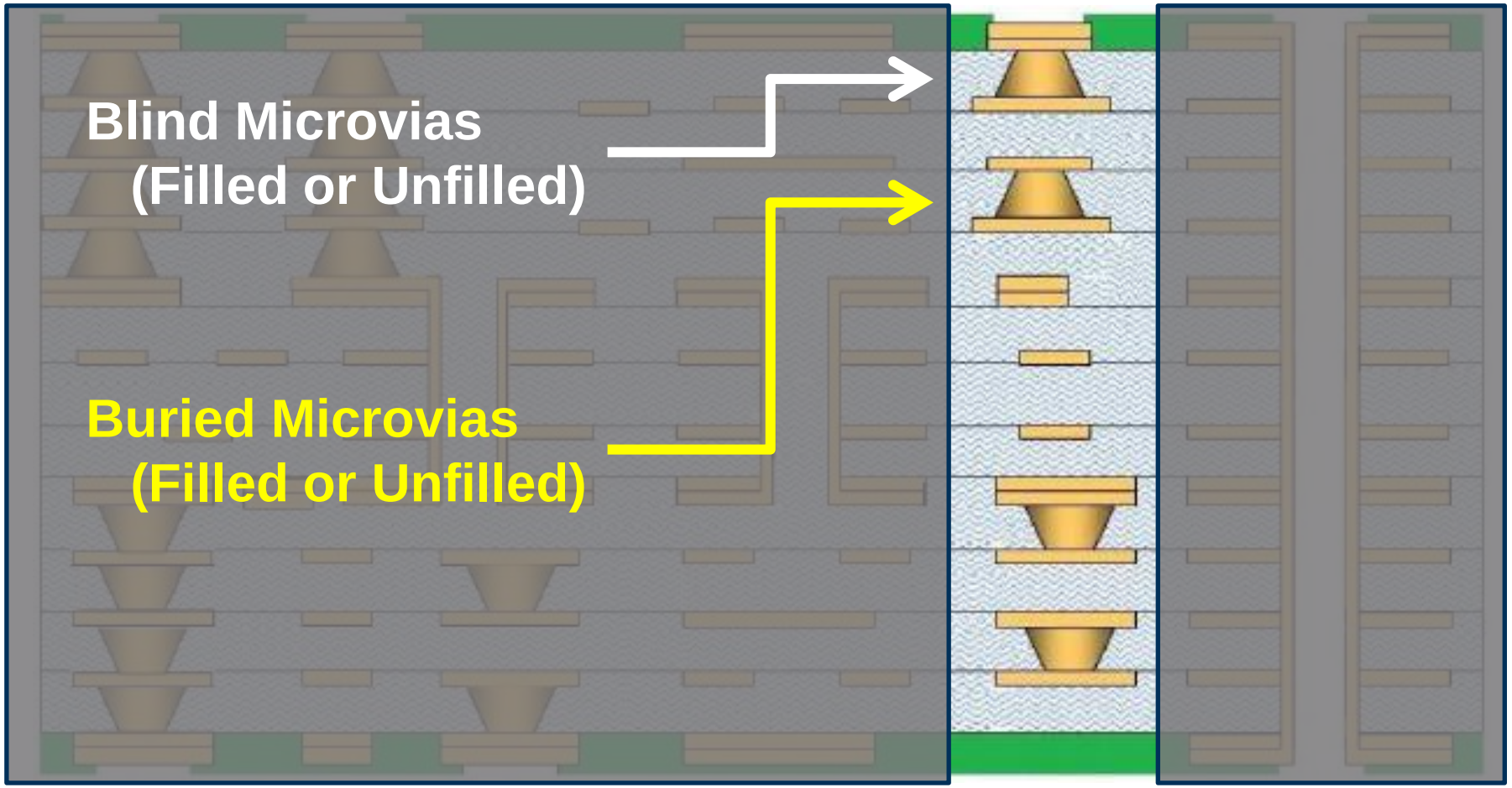
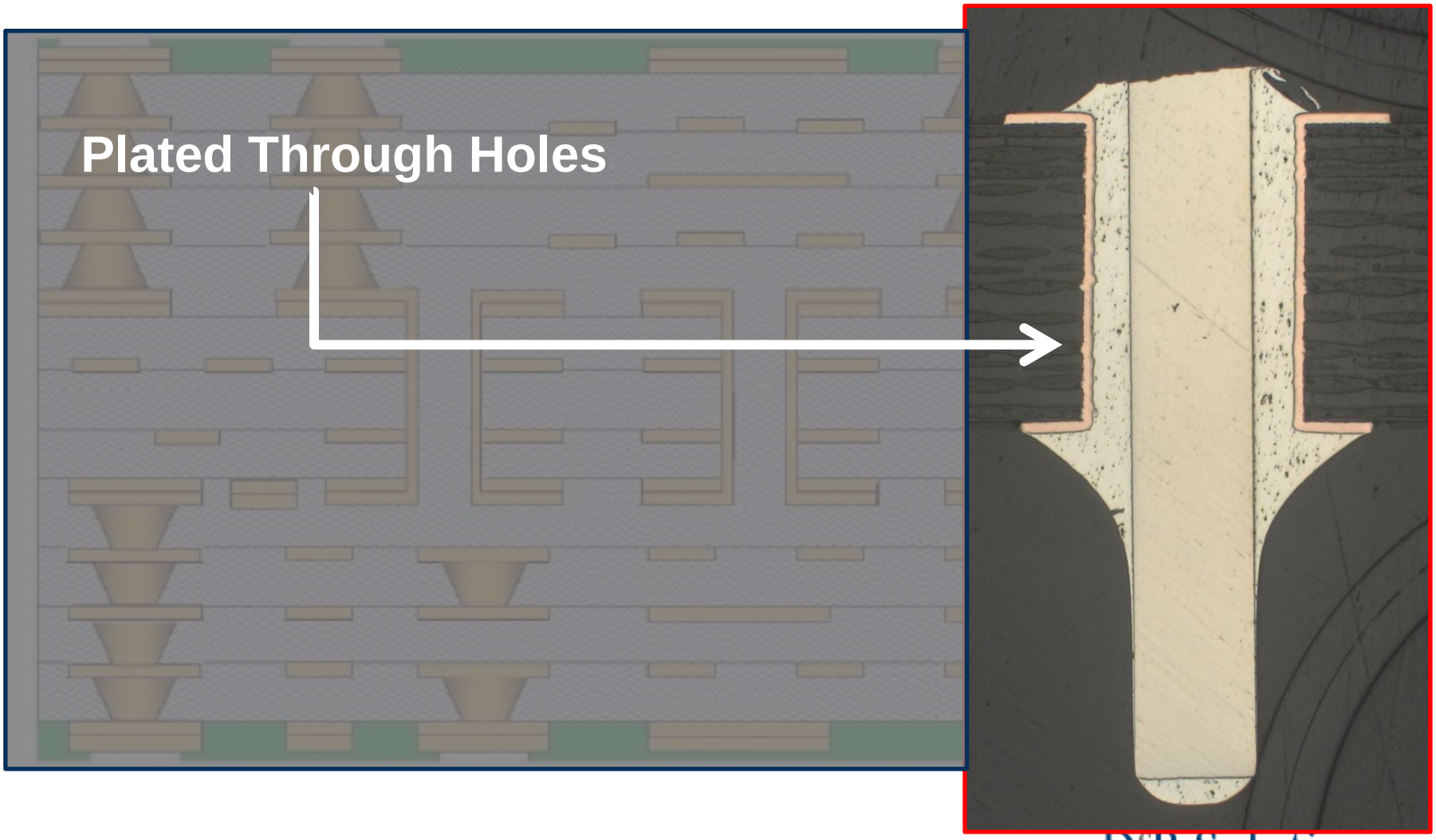
PCB Vias

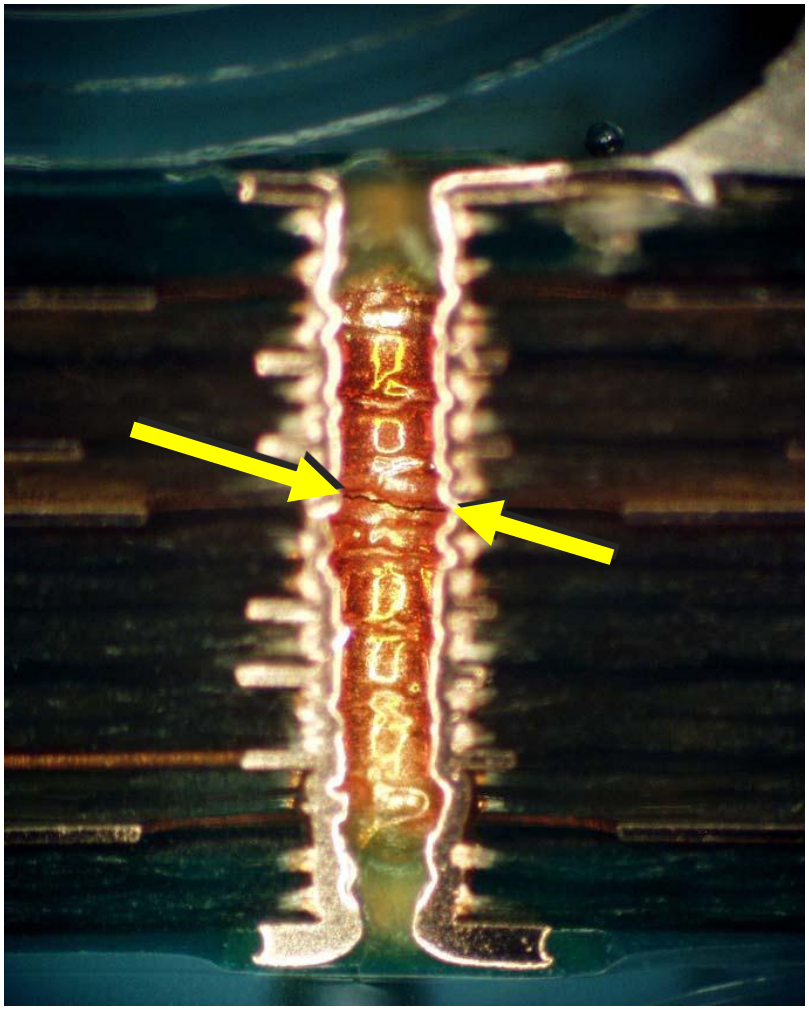

Blind Microvias
(Filled or Unfilled)
Buried Microvias
(Filled or Unfilled)

PCB Vias



How do PTV's Fail?

- The dominant failure mode in PTV tends to be barrel fatigue
- Barrel fatigue is the circumferential cracking of the copper plating that forms the PTV wall
- Driven by differential expansion between the copper plating (~17 ppm) and the out-of-plane CTE of the printed board (~70 ppm)



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How to Design a Reliable PTV?

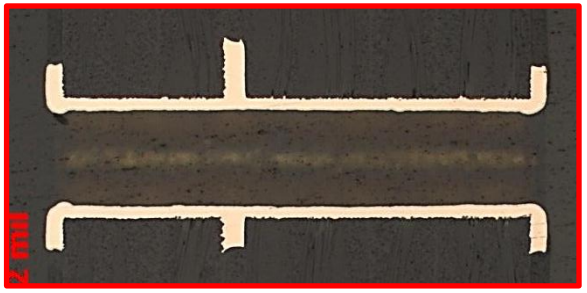
PTH Architecture
(height / diameter)

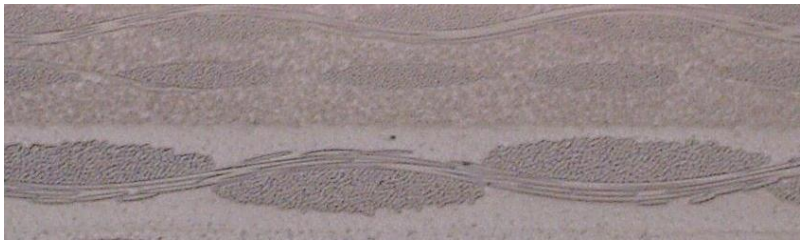
+

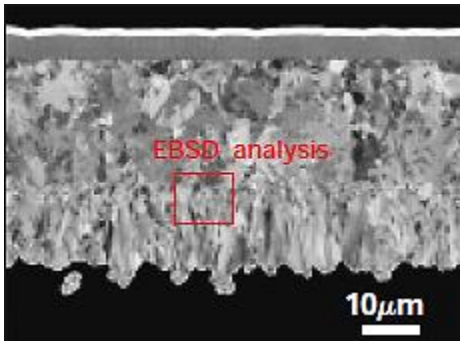
PCB Material
(modulus / CTE)

+

Plating
(thickness / material)







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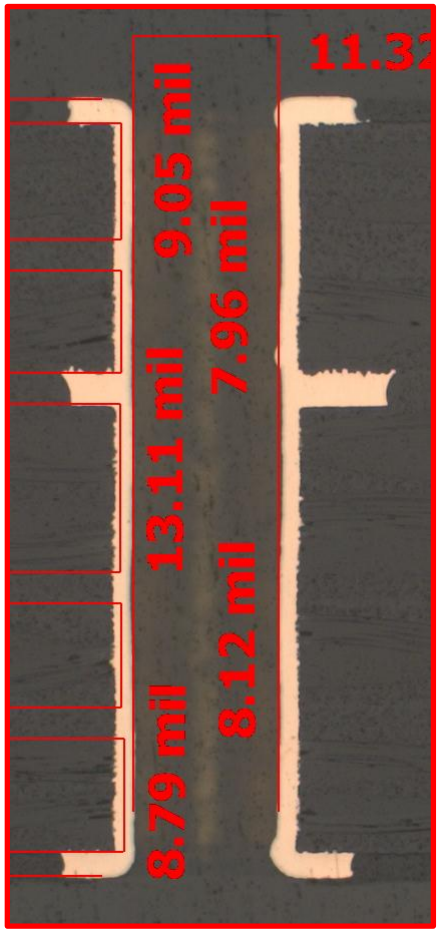
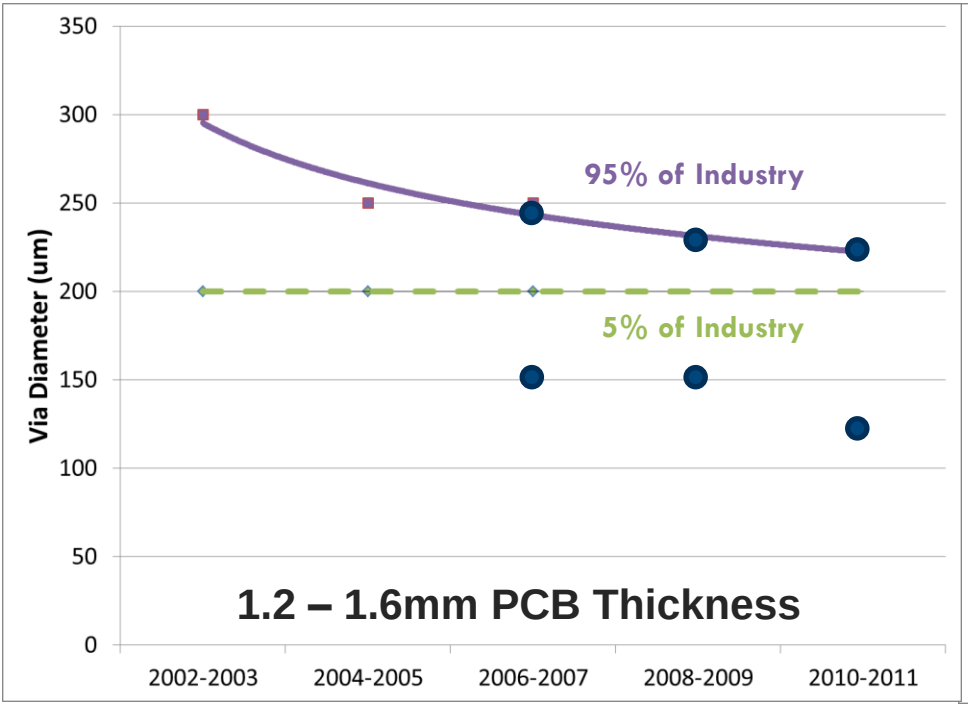
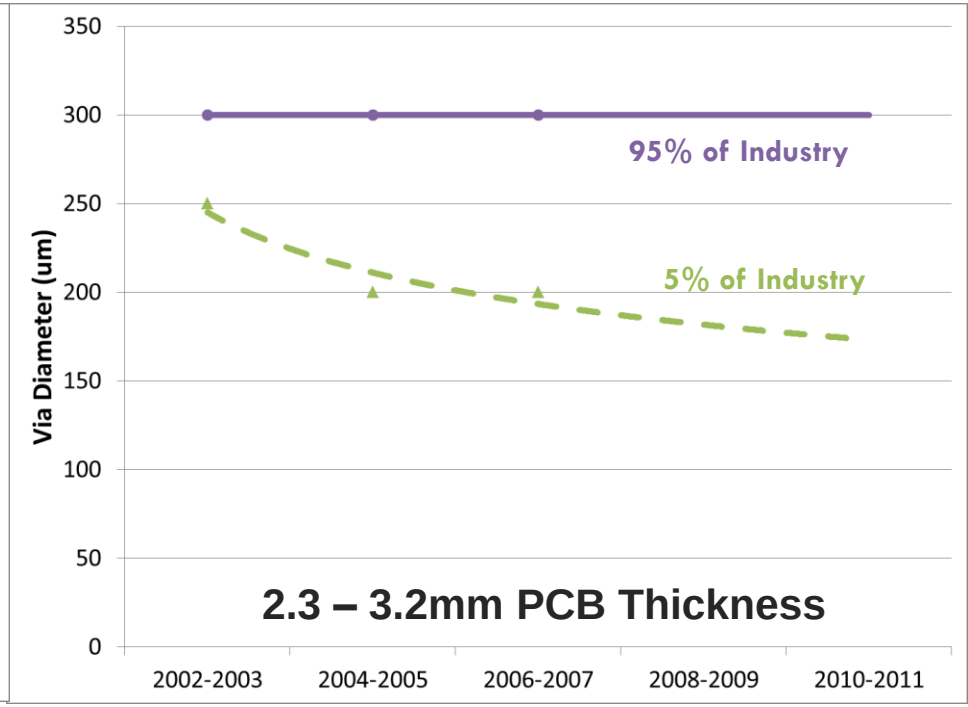
PTV Architecture

- PTV Height
  - Driven by the PCB thickness
  - 30 mil (0.75 mm) to 250 mil (6.25 mm)
- PTV Diameter
  - Driven by component pitch/spacing
  - 6 mil (150 micron) to 20 mil (500 micron)
- Key Issues
  - Be aware that PCB manufacturing has cliffs
  - Quantify effect of design parameters using IPC TR-579



PCB Industry PTV Capability





DDI Tech Roadmap 2011	PCB Thickness (mil / mm)		
Via Diameter (mil / um)	**Standard**	**Advanced**	**Engineering**
6 / 150	N/A	39 / 1.0	60 / 1.5
8 / 200	64 / 1.6	80 / 2	96 / 2.4
10 / 250	100 / 2.5	120 / 3	160 / 4

IBM PCB-OS Symposium 2007, Roadmap Technology Verification, Conductor Analysis Technologies (CAT)

- Minimal technological progress over past 10 years

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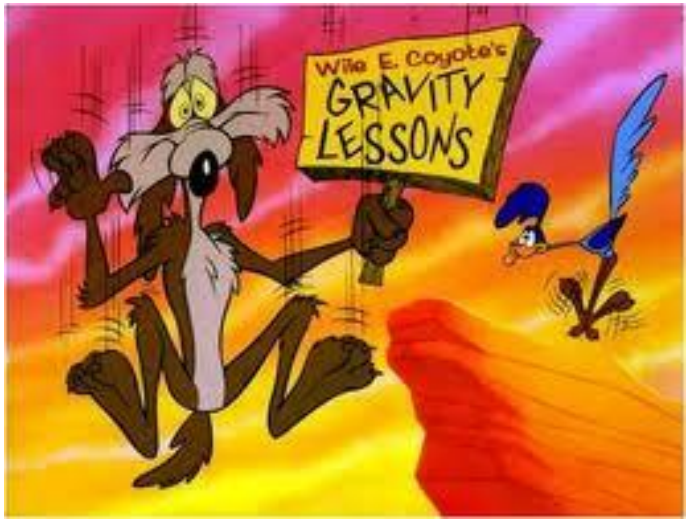
The PTV Cliff



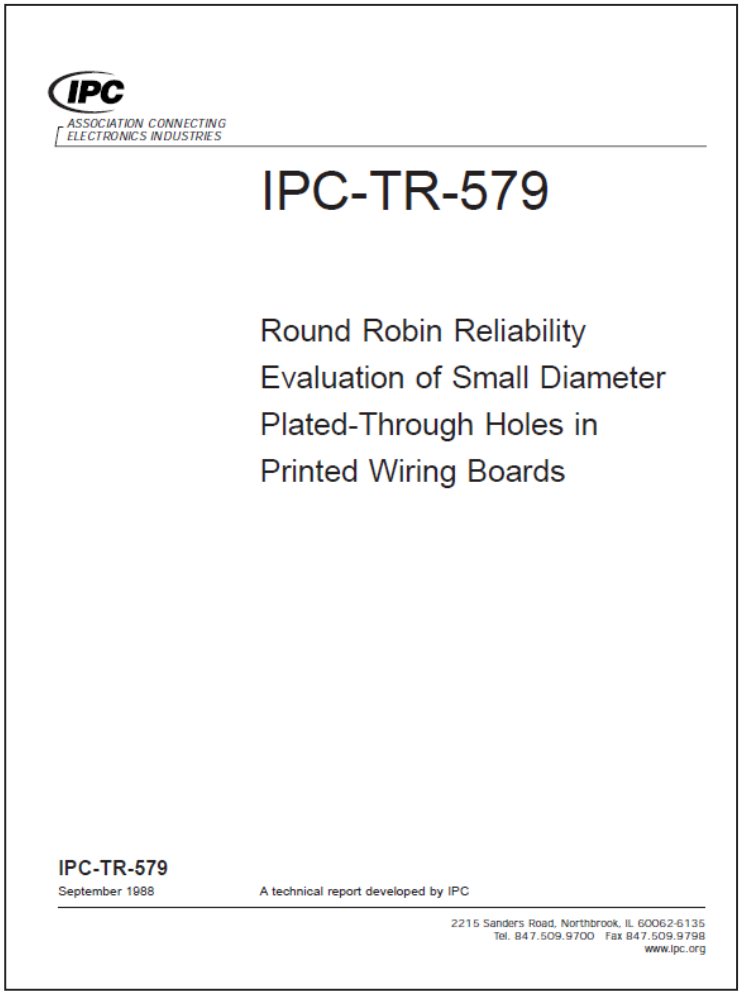
- Data from 26 PCB manufacturers
- Wide range of PCB designs
  - 6 to 24 layer
  - 62 to 125 mil thickness
- Results after six lead-free reflows
  - Initial defects segregated

Process Attribute	Hole/land (mils)	Count	Min	Q1	Median	Q3	Max
Yield Loss from Assembly Simulation (%) Threshold: Open	8 / 18	6	0.00	0.00	0.31	3.24	17.16
	10 / 20	15	0.00	0.00	0.00	1.13	4.60
	12 / 22	26	0.00	0.00	0.00	0.00	5.23
	13.5 / 23.5	26	0.00	0.00	0.00	0.00	4.09
	14.5 / 24.5	19	0.00	0.00	0.00	0.00	0.00
	16 / 26	11	0.00	0.00	0.00	0.00	0.00

Courtesy of CAT

IPC TR-579

- Round Robin Reliability Evaluation of Small Diameter (<20 mil) Plated Through Holes in PWBs
- Activity initiated by IPC and published in 1988
- Objectives
  - Confirm sufficient reliability
  - Benchmark different test procedures
  - Evaluate influence of PTH design and plating (develop a model)


IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

IPC-TR-579

Round Robin Reliability Evaluation of Small Diameter Plated-Through Holes in Printed Wiring Boards

IPC-TR-579
September 1988

A technical report developed by IPC

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org

IPC TR-579 (cont.)

- Determine stress applied (σ)
  - Assumes perfectly elastic deformation when below yield strength (Sy)
  - Linear stress-strain relationship above Sy

$$\sigma = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E E_{Cu}}{A_E E_E + A_{Cu} E_{Cu}}, \text{for } \sigma \le S_y$$

$$\sigma = \frac{\left[(\alpha_E - \alpha_{Cu})\Delta T + S_y \frac{E_{Cu} - E'_{Cu}}{E_{Cu} E'_{Cu}}\right] A_E E_E E'_{Cu}}{A_E E_E + A_{Cu} E'_{Cu}}, \text{for } \sigma > S_y$$

$$A_E = \frac{\pi}{4}\left[(h+d)^2 - d^2\right]$$

$$A_{Cu} = \frac{\pi}{4}\left[d^2 - (d-2t)^2\right]$$

h	PTV Height
d	PTV Diameter
t	Plating Thickness
E	Elastic Modululs
α	Coefficient of Thermal Expansion
T	Temperature (oC)

IPC TR-579 (cont.)

- Determine strain range ($\Delta\varepsilon$)

$$\Delta\varepsilon = \frac{\sigma}{E_{Cu}}, \text{ for } \sigma < S_y$$

$$\Delta\varepsilon = \frac{S_y}{E_{Cu}} + \frac{\sigma - S_y}{E'_{Cu}}, \text{ for } \sigma > S_y$$

IPC-TR-579 (Calibration Constants)

- Strain distribution factor, Kd (2.5 –5.0)
  - 2.5 recommended
- Quality index, K_Q (0 –10)
  - Extraordinary ($K_Q = 10$)
  - Superior ($K_Q = 8.7$)
  - Good ($K_Q = 6.7$)
  - Marginal ($K_Q = 4.8$)
  - Poor ($K_Q = 3.5$)
- Some companies assume $K_Q = 5$

$$\Delta\varepsilon_{eff} = \Delta\varepsilon\left(K_d \frac{10}{K_Q}\right)$$

IPC TR-579 (cont.)

- Iteratively calculate cycles-to-failure (Nf)

$$N_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E} \left[\frac{\exp(D_f)}{0.36} \right]^{0.1785 \log \frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

Two key plating properties

Df	Elongation (assumed ~30%)
Su	Tensile Strength (assumed ~40,000 psi)

Assessment of IPC-TR-579

- Advantages
  - Analytical (calculation straightforward)
  - Validated through testing
  - Provides guidance on relative influence of design/material parameters

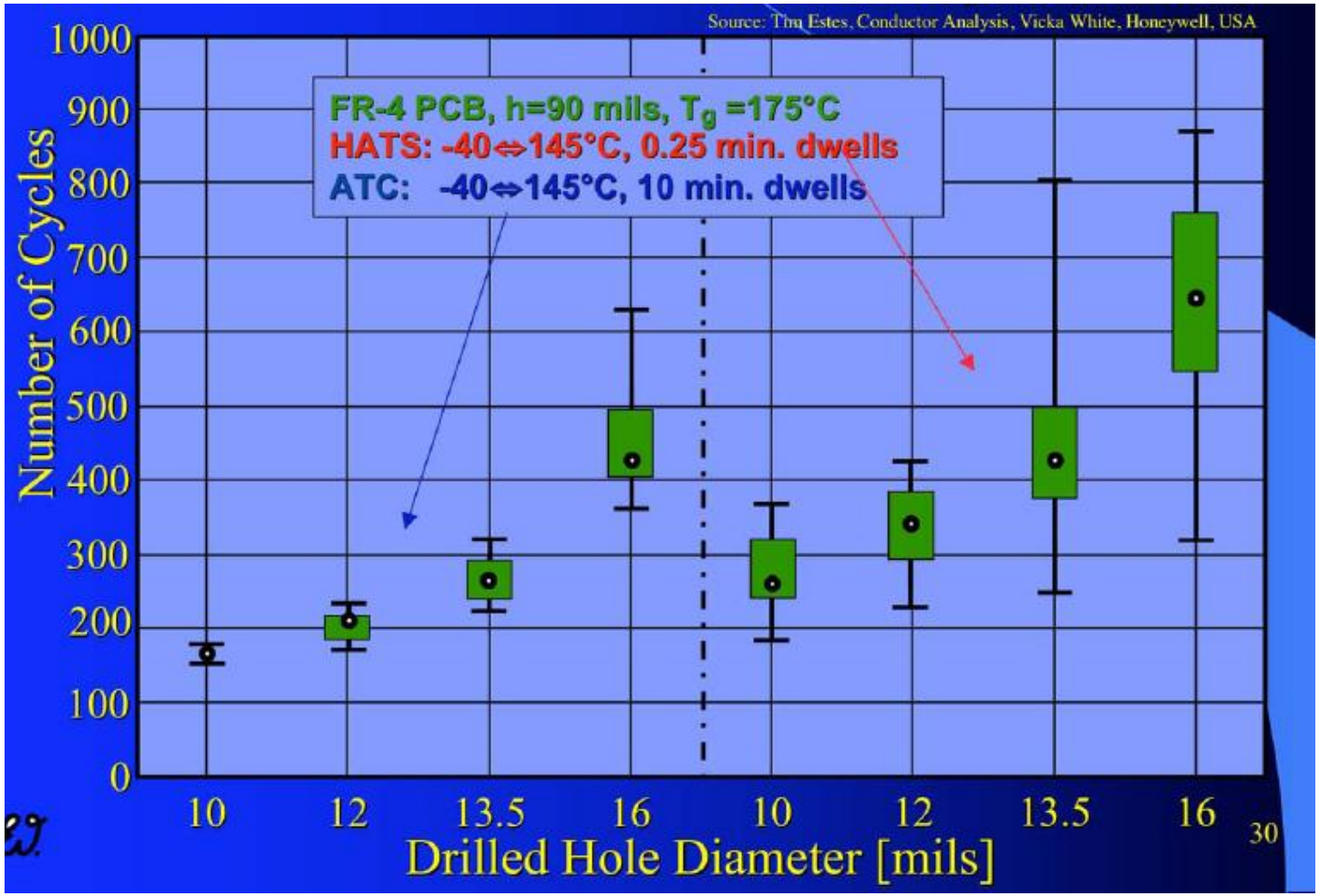
- Disadvantages
  - No ownership
  - Validation data is ~18 years old
  - Unable to assess complex geometries (PTH spacing, PTH pads)
    - Complex geometries tend to extend lifetime
  - Difficult to assess effect of multiple temperature cycles
    - Can be performed using Miner's Rule
  - Simplified assumptions (linear stress-strain above yield point)
  - How does one determine the quality index in the design phase?
  - Does not account for the effect of fill
  - Does not consider other failure modes (knee cracking, wall-pad separation, etc.)

The Effect of Design Parameters (Height / Diameter)

- Reduce the PTV Height (PCB Thickness)
  - Reduce laminate/prepreg thickness (2.7 to 4 mil is current limitation)
  - Results in minimal cost changes and minimal effect on design
  - Has the least effect on PTH reliability

- Increase PTV Diameter
  - Typically not an option due to spacing issues
  - An important, but significant effect (dependent on a number of other variables)
  - Example: Moving from 10 mil to 12 mil diameter on a 120 mil board, 50C temp cycle, will result in approximately 20% improvement

Effect of Design Parameters (cont.)



W. Engelmaier, Reliability Issues for Printed Circuit Boards in Lead-Free Soldering

Effect of Design Parameters (cont.)

Simulation
(PTV Height = 1.6mm)

Testing
(PTV Height = 1.6mm?)

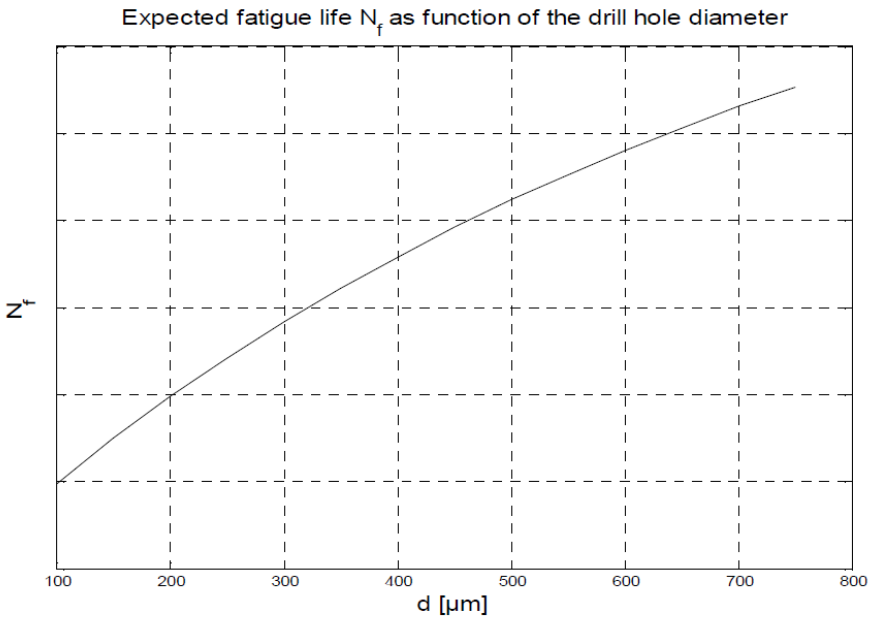
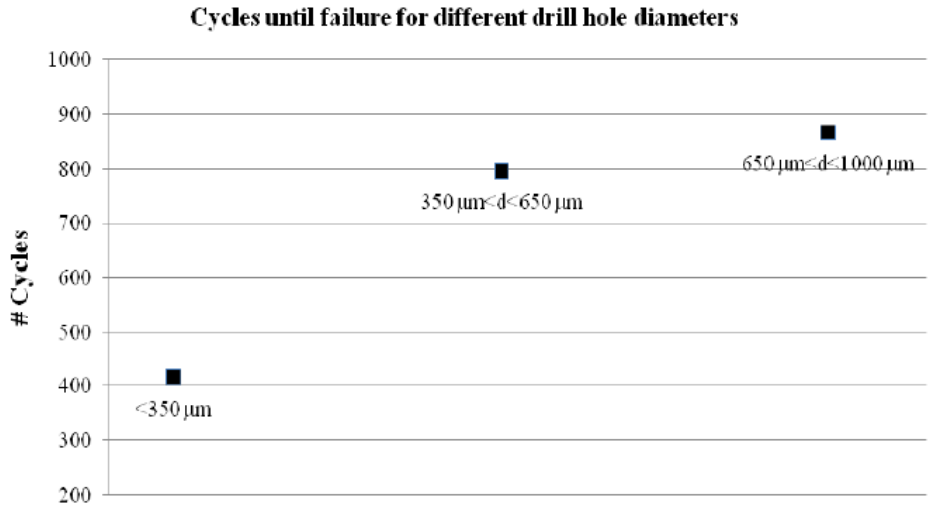
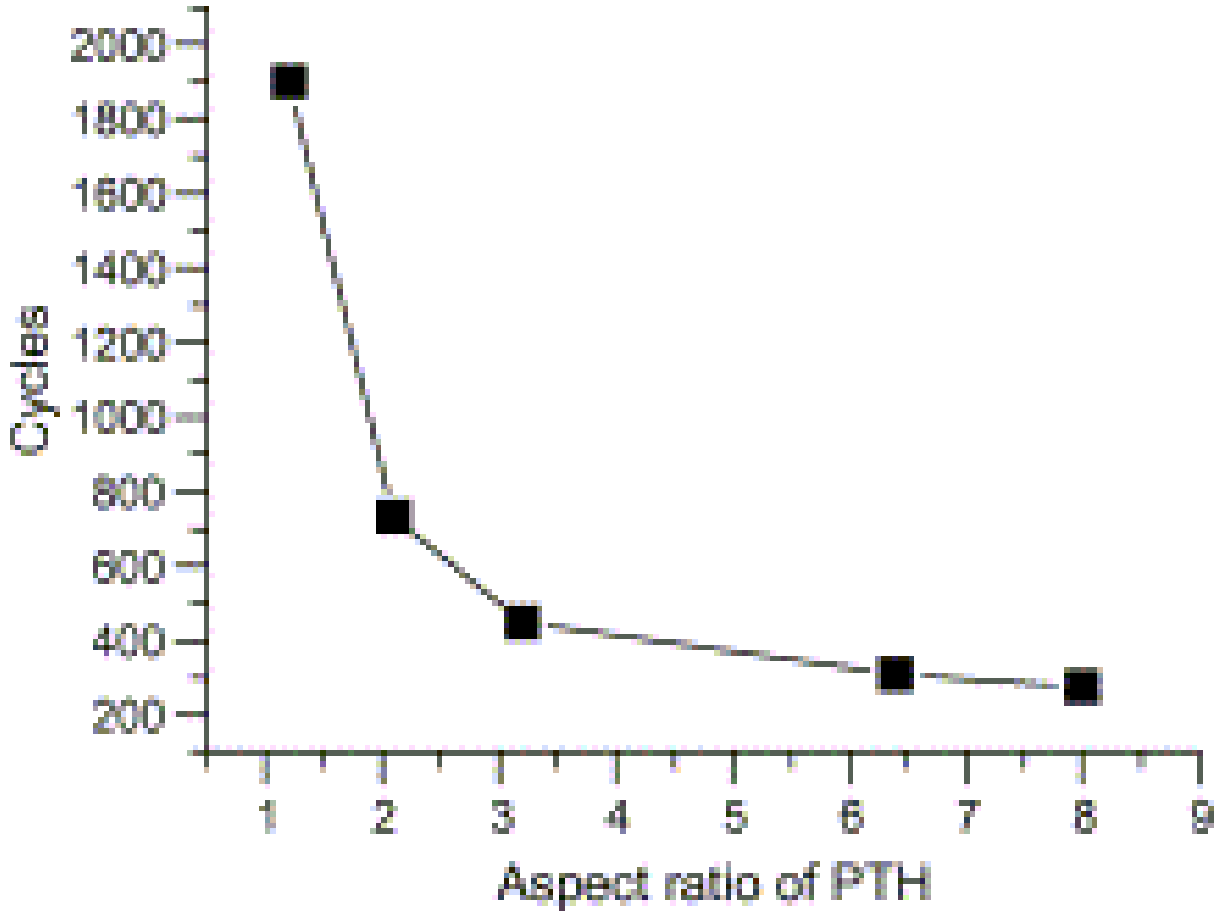


Figure 19: Number of stress cycles as function of d



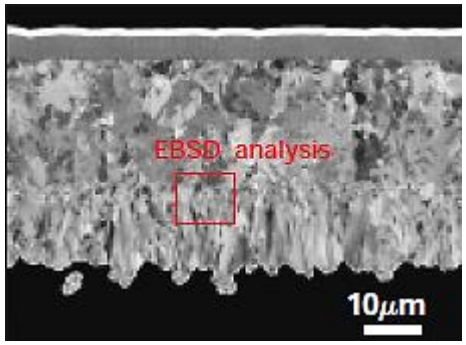
ɔ Mechanical Reliability in Printed Circuit Boards with Copper

Effect of Design Parameters (cont.)



F. Su, et. al., Microelectronics Reliability, June 2012

Plating (Thickness and Material Properties)



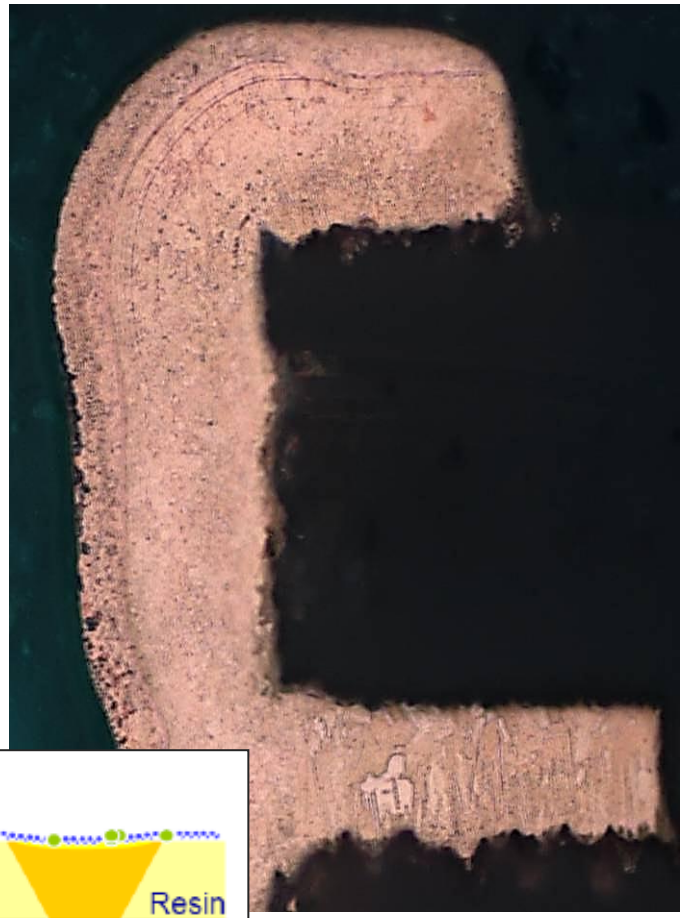
- Considered to be the number one driver for PTV barrel fatigue
- Classic engineering conflict
  - Better properties (greater thickness, higher plating strength, greater elongation) typically require longer time in the plating bath
  - Longer time in the plating bath reduces throughput, makes PCBs more expensive to fabricate
- PCB fabricators, low margin business, try to balance these conflicting requirements
  - Key parameters are thickness, strength, and elongation (ductility)

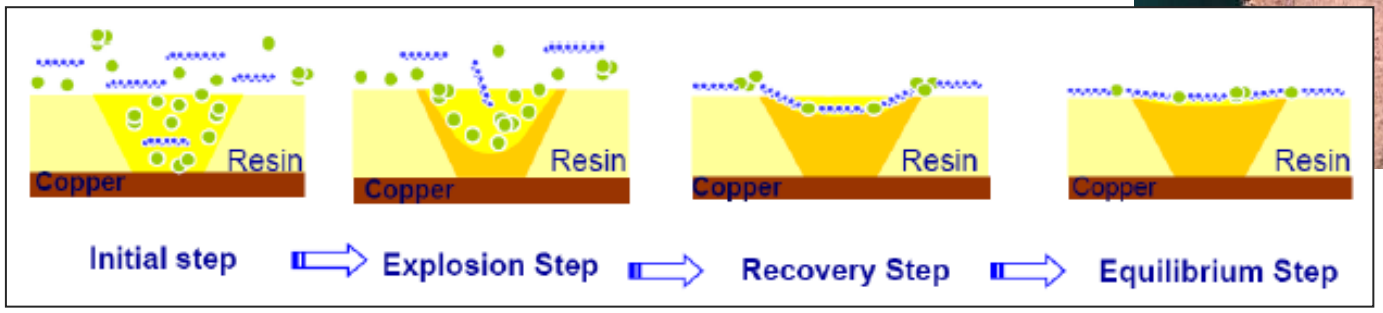
Plating Thickness

- Specifications tend to range from 0.8 mil (20 microns) to 1.0 mil (25 microns) to 1.2 mil (30 microns)
- Plating thickness can be less of an issue than seen in the past
- New formulations to fill microvias can drive an accelerated plating process
  - Some PCB manufacturers, depending on the design and production volume, will plate the PTV almost closed

Case Study: Microvia Fill and PTV Reliability

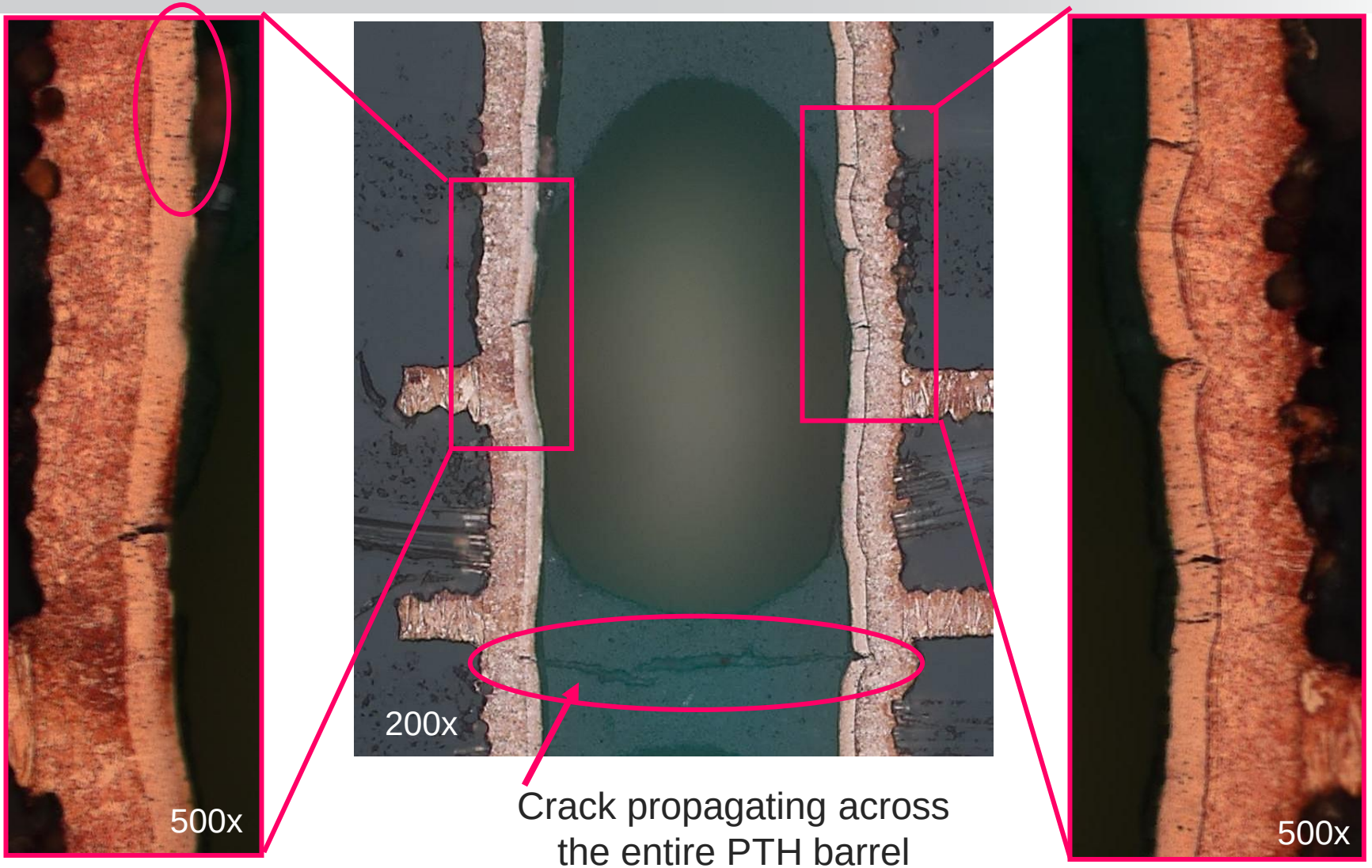
- OEM moved to microvias for first time
  - PCB manufacturer recommended via fill
- High plating rate process was not optimized, resulting in porous final plating layer
  - Once a crack is initiated, rapid failure





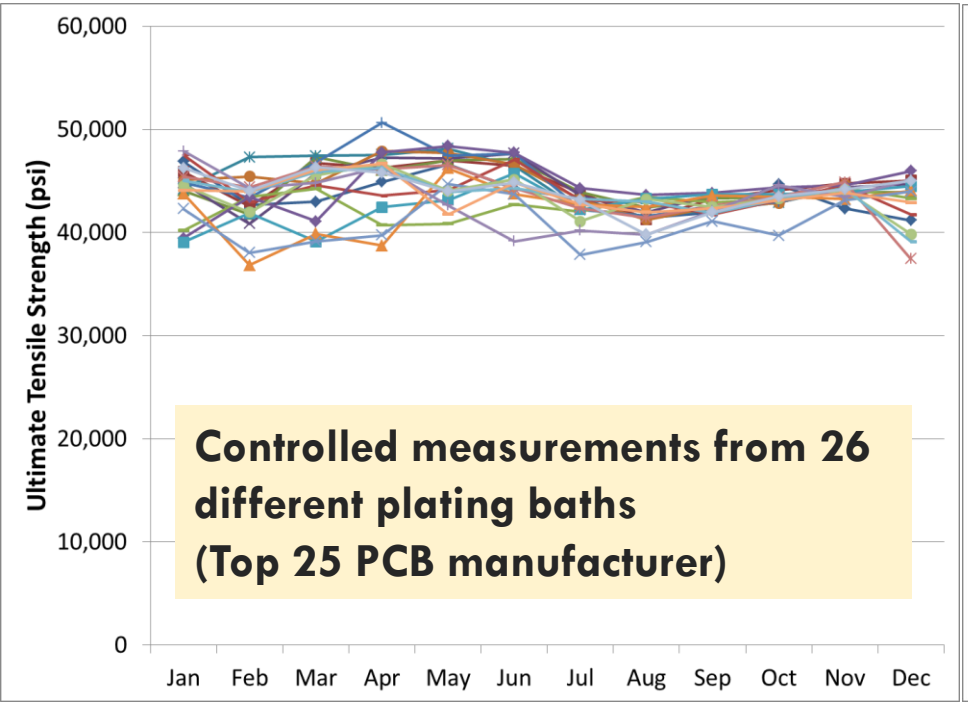
DfR Solutions

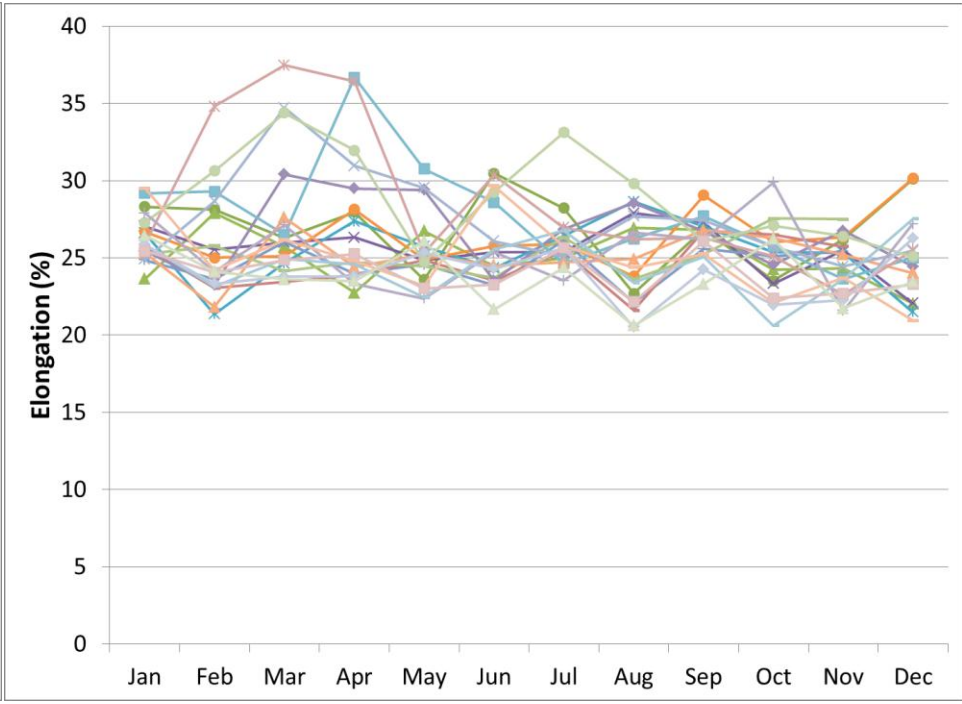
Case Study (cont.)



Plating Mechanical Properties

- Industry Requirements (IPC-6012C)
  - Ultimate Tensile Strength ≥ 36,000 psi (250 MPa)
  - Elongation ≥ 12%

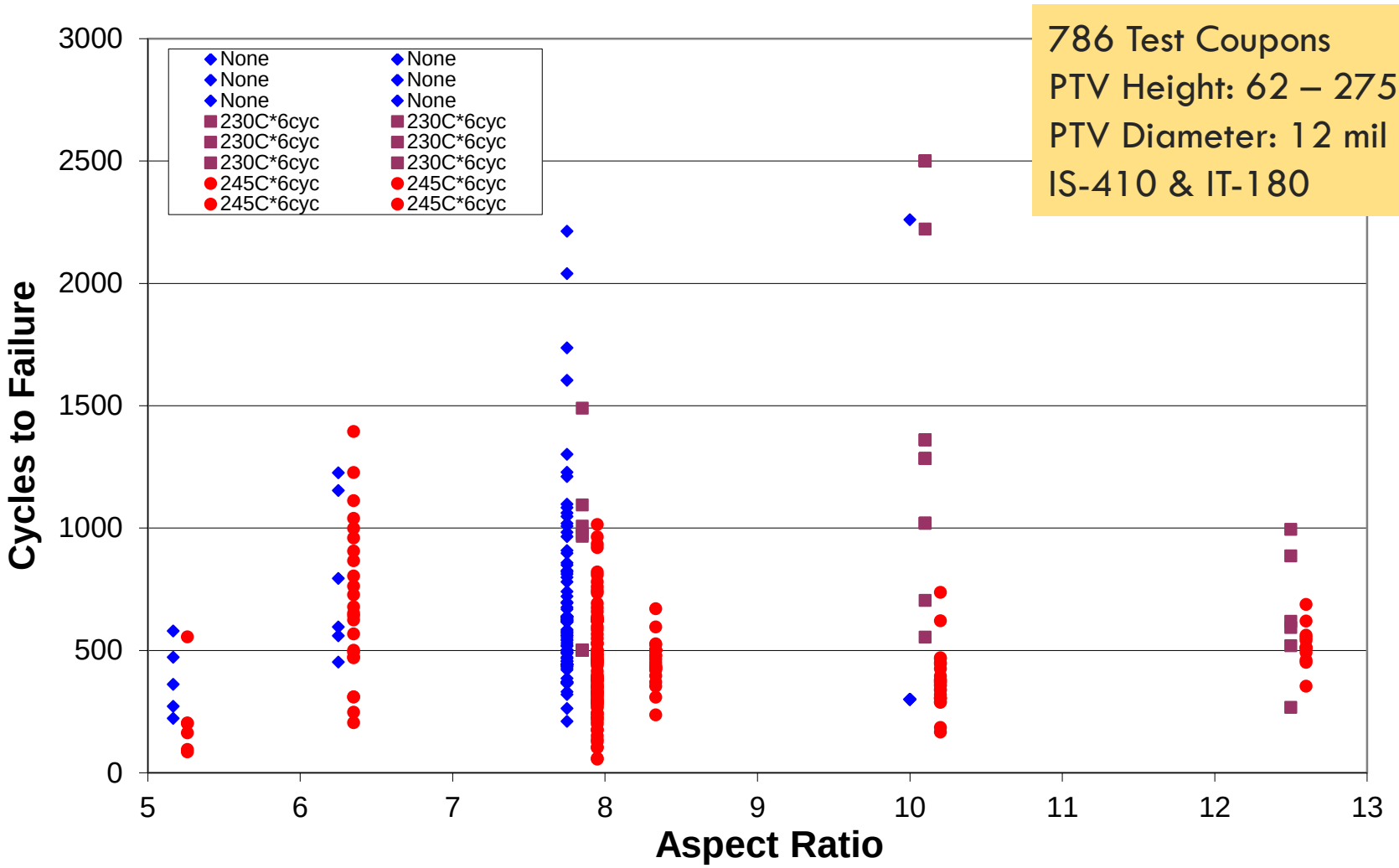




The Reality of PTV Performance (cont.)

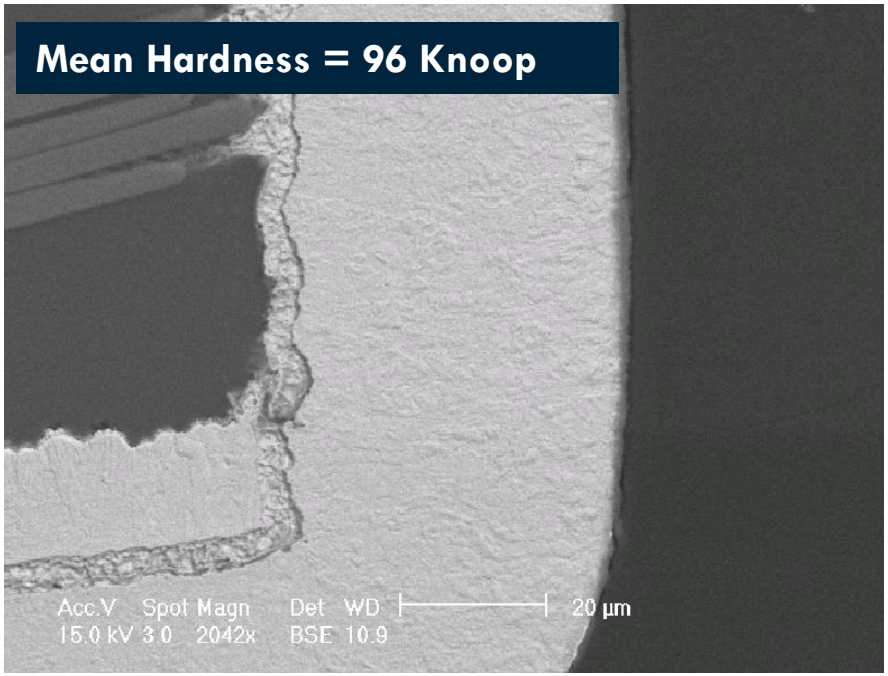
- PCB Manufacturers tend to be very aware of test requirements specified by larger/higher rel customers
  - Plating conditions are adjusted to meet the test requirements of those industries / customers

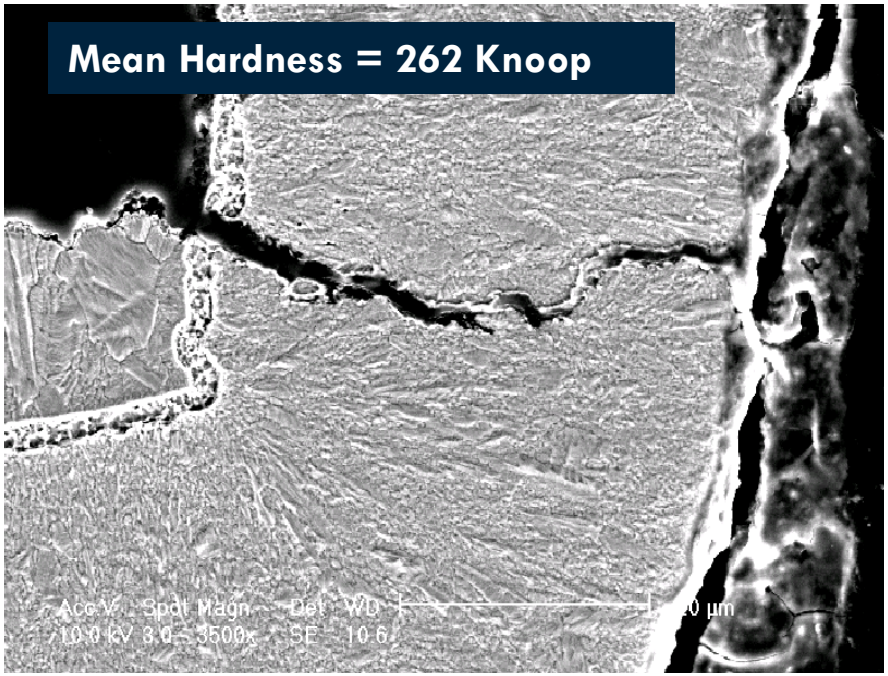
The Reality of PTV Performance



DfR Solutions

Post-Plating Measurements of Plating Properties

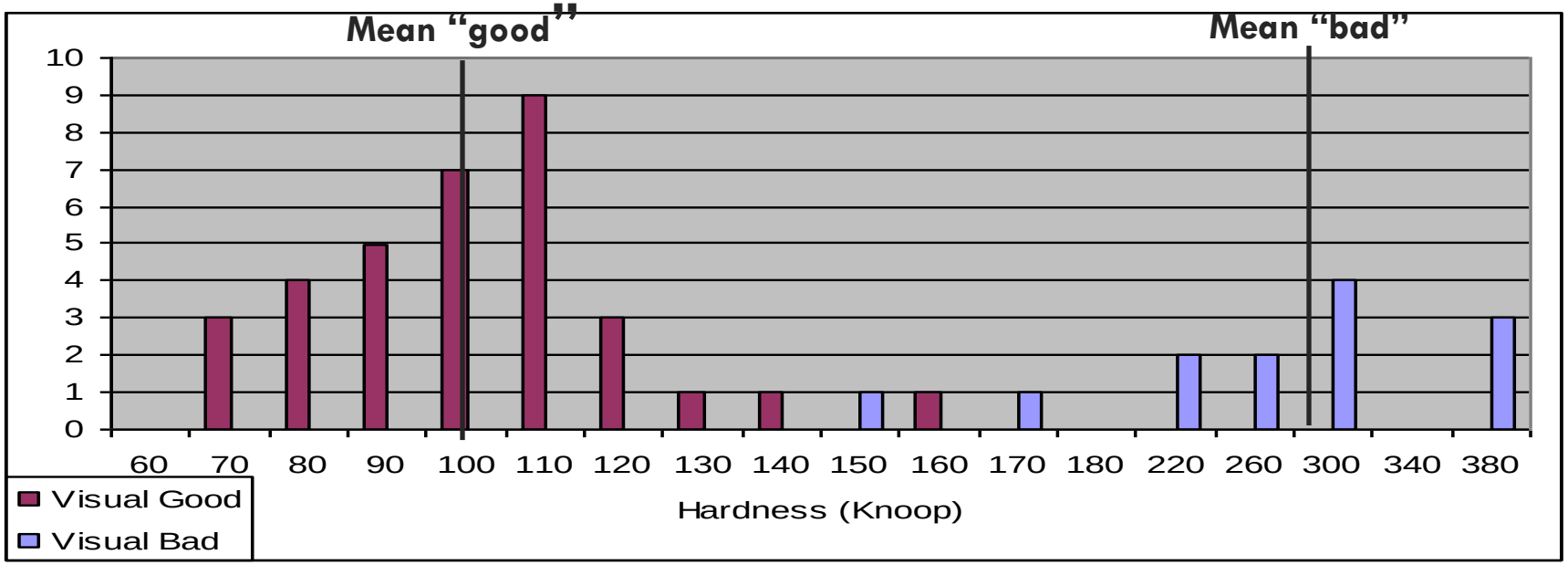




- One of the challenges of root-cause analysis of PTV cracking is the inability to directly measure strength/ductility of the plating
- Hardness and grain size measurements are potential substitutes

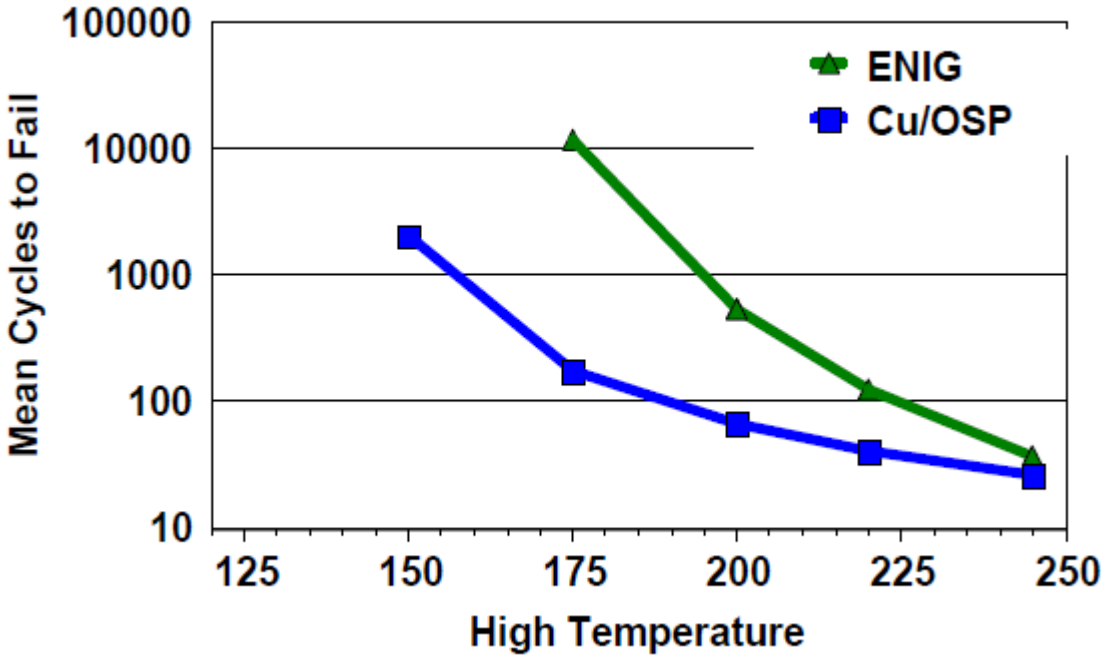
Post-Plating Measurements

- Hardness data indicated good separation between two populations
  - 100% correlation with cross section results
  - Boards with cracks had high hardness
  - Boards without cracks had low hardness



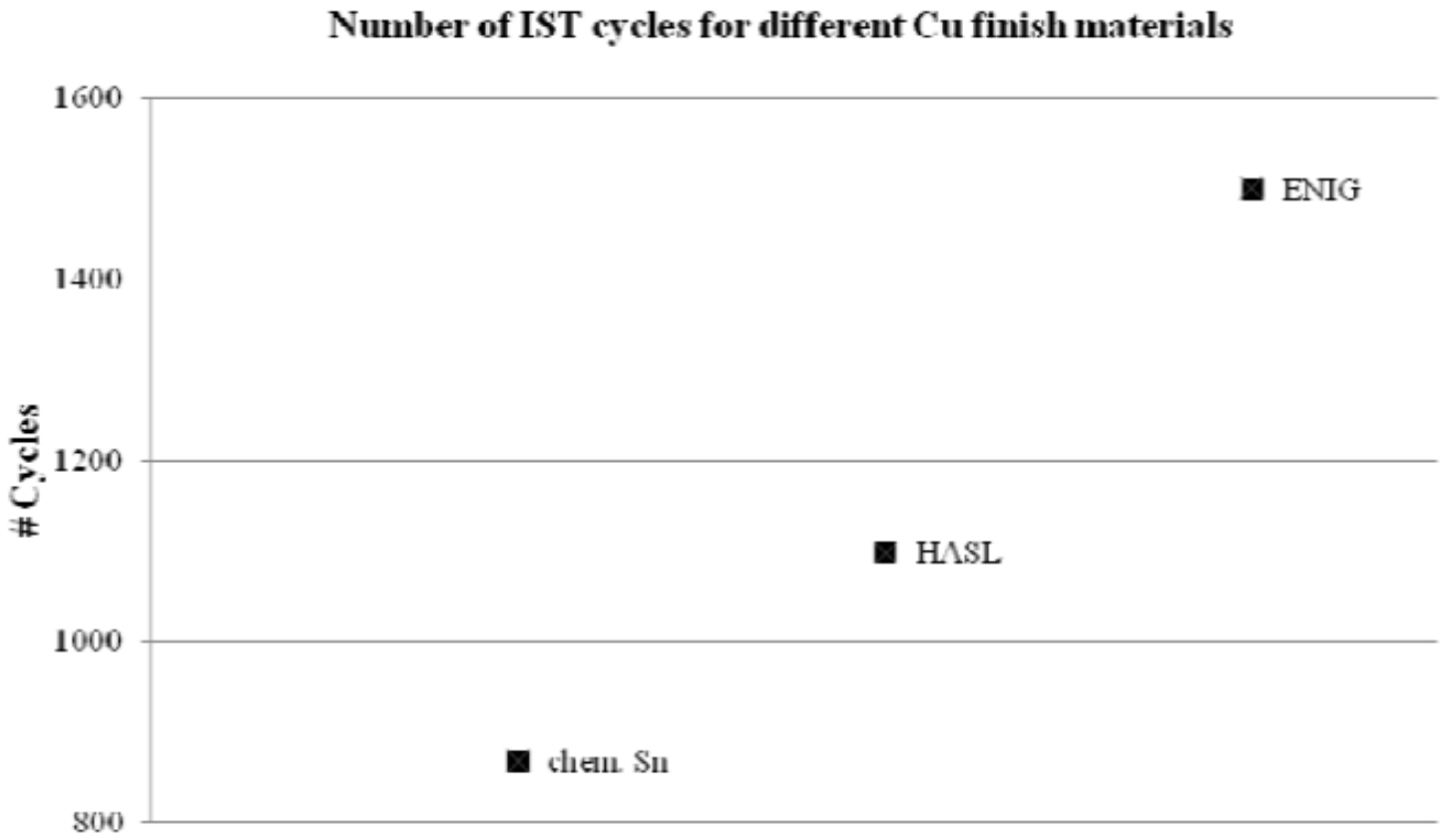
Other Platings

- Thick nickel plating down the barrel can also extend lifetime
  - Caveat: Poor nickel plating can result in much shorter times to failure



Proof is in the PTH -- Assuring Via Reliability from Chip Carriers to Thick Printed Wiring Boards, K. Knadle

Other Platings (cont.)



- S. Neumann, Theoretical and Practical Aspects of Thermo Mechanical Reliability in Printed Circuit Boards with Copper Plated Through Holes

How to Test/Qualify a Reliable PTV?

- There are currently six procedures for testing/qualifying a PTV
  - Modeling and simulation
  - Cross-sectioning + solder float/shock
  - Thermal shock testing (also thermal cycling)
  - Interconnect stress testing (IST)
  - Printed Board Process Capability, Quality, and Relative Reliability (PCQR2)
  - Highly Accelerated Thermal Shock (HATS)
- What does DfR recommend?

Test / Qualify PTV

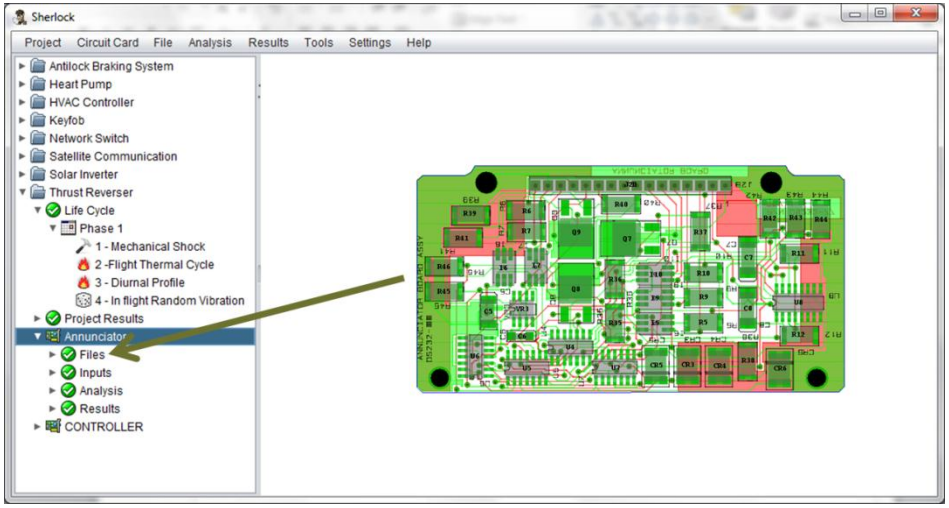
- Qualifying PTV is a two-step process
- The first step is to qualify the design and the PCB manufacturer
  - Initial qualification
- The second step is to initiate ongoing testing to monitor outgoing quality
  - Lot qualification

Initial Qualification

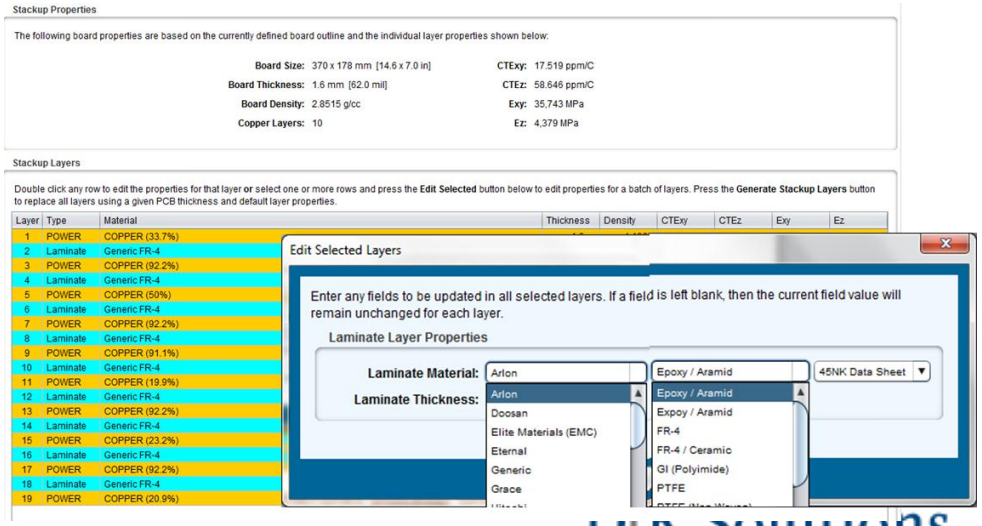
- Qualify the design through simulation / modeling
- DfR has implemented IPC TR-579 into our Automated Design Analysis software, Sherlock, to allow for rapid assessment of PTV robustness
- First step: Define the environment (test or field or both)

Simulation and Modeling

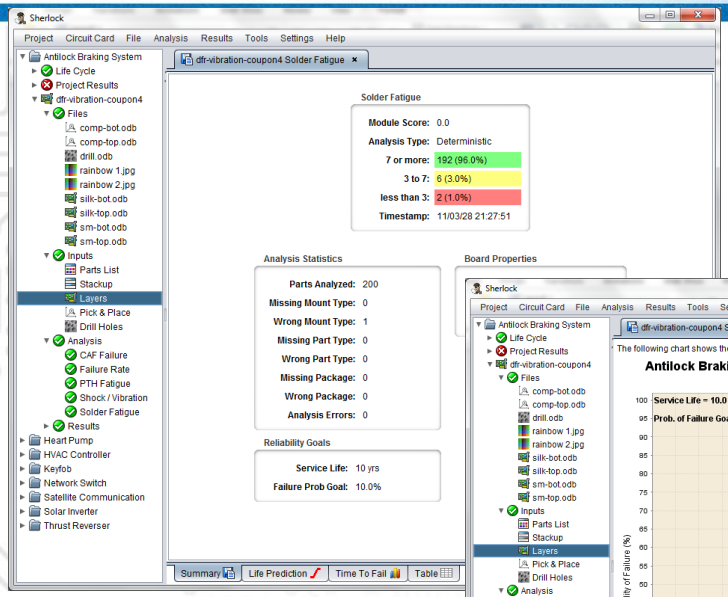
- Second step: Upload design information
  - Include thermal maps, if appropriate

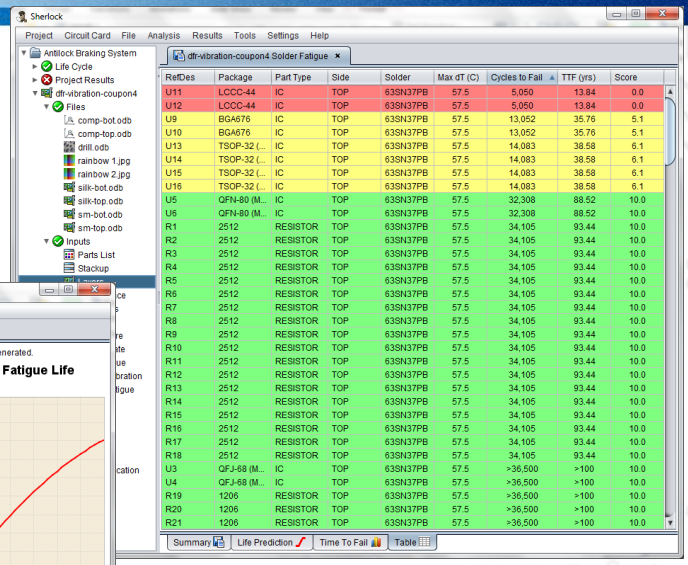


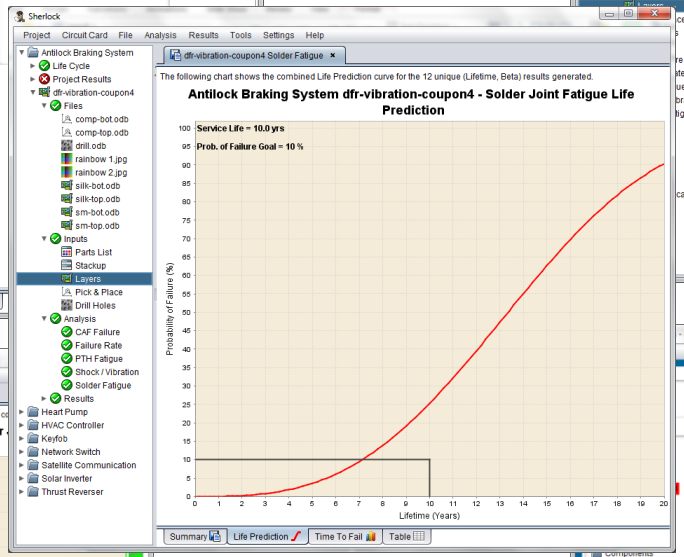
- Third step: Select the laminate and prepreg material
  - Stackup and copper percentage automatically identified

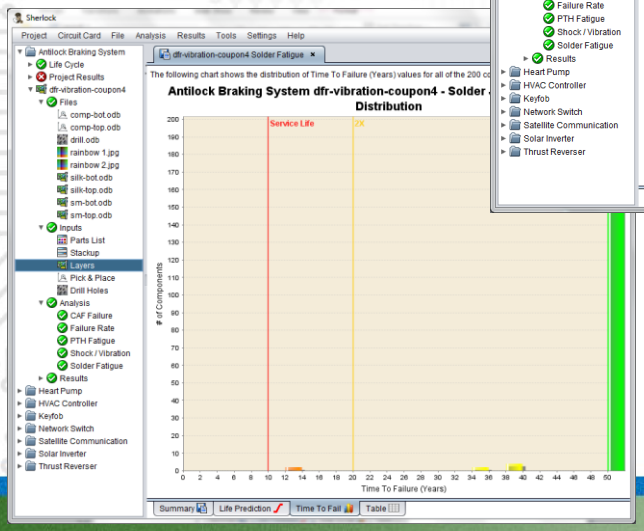


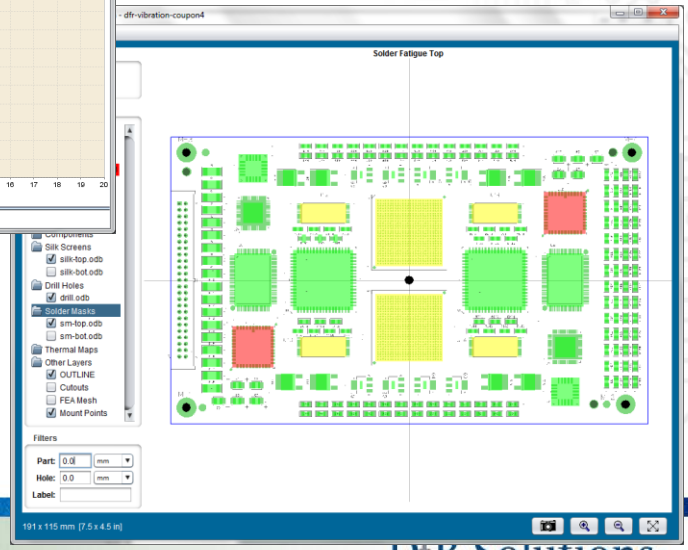
sherlock AUTOMATED DESIGN ANALYSIS Results: Five Different Outputs







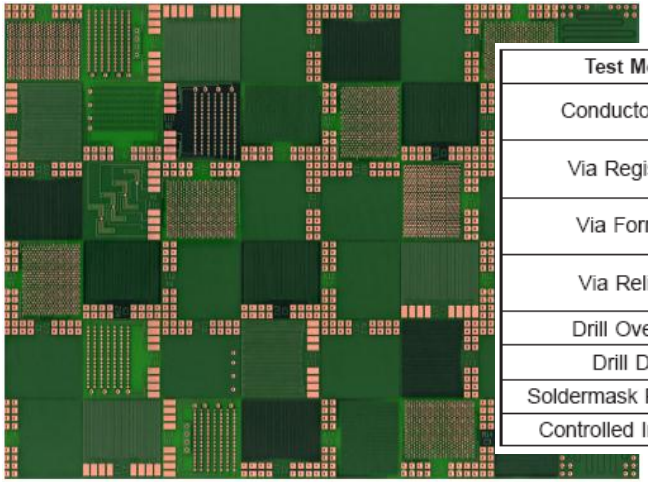




DfR Solutions
reliability designed, reliability delivered

Initial Qualification (PCQR2)

- Qualify the design and manufacturer through PCQR2
  - Consists of a coupon design, a test standard, and a database
  - 18″ x 24″ layout with 1″ x 1″ test modules (352)
  - 2 – 24 layers (rigid, rigid-flex)
  - Three panels / three non-consecutive lots
  - Simulated assembly (6X) and thermal cycling (HATS)



Test Module	Design Type	Capability Information	Quality Information
Conductor/Space	Outerlayer, 0.5-oz. innerlayer, 1-oz. innerlayer, and buried-core	Conductor and space defect density	Conductor width and height uniformity
Via Registration	Through, 1-deep blind, 2-deep blind, controlled-depth drill, and back-drill	Via probability of breakout	
Via Formation	Through, 1-deep blind, 2-deep blind, buried-core, controlled-depth drill, and back-drill	Via defect densit	Via net resistance coefficient of variation
Via Reliability	Through, 1-deep blind, 2-deep blind, buried-core, controlled-depth drill, and back-drill	Yield loss	Percent change in resistance
Drill Overshoot	Controlled-depth drill	Probability of overshoot	
Drill Depth	Back-drill	Secondary drill depth	
Soldermask Registration	Outerlayer	Clearance yield	
Controlled Impedance	Single-ended and differential	Impedance uniformity	

PCQR² (cont.)

- Advantages
  - Industry standard (IPC-9151)
  - Plug and play
  - Provides real data for understanding of PCB supplier capabilities and comparison to the rest of the industry through the use of an anonymous database

- Disadvantages
  - Industry-certified monopoly
  - $2K - $5K, not including panel costs

Lot Qualification

- Interconnect stress testing (IST) is the overwhelming favorite of high reliability organizations
  - Small (1 x 4) coupon can fit along the edge of the panel
  - Testing is automated
  - Widely used
  - Ability to drive barrel fatigue and post separation

- Large number of holes (up to 300) and continuous resistance monitoring makes it far superior to cross-sectioning
  - And it should be cheaper!

IST – Issues / Awareness

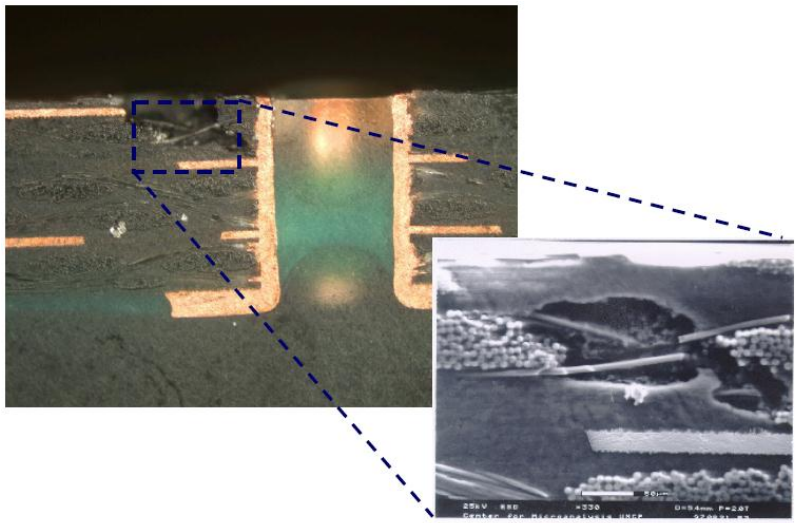
- Coupon design is critical (IST can be prone to problems)
- Need to specify preconditioning (IST or real reflow oven?)
- Need to specify frequency (every lot, every month, every quarter)
- Need to specify maximum temperature (some debate on the validity of results when above the Tg)
  - 130, 150, and 175C are the most common
- Need to specify requirements
  - Different markets/organizations specify different times to failure (300, 500, and 1000 cycles are most common)

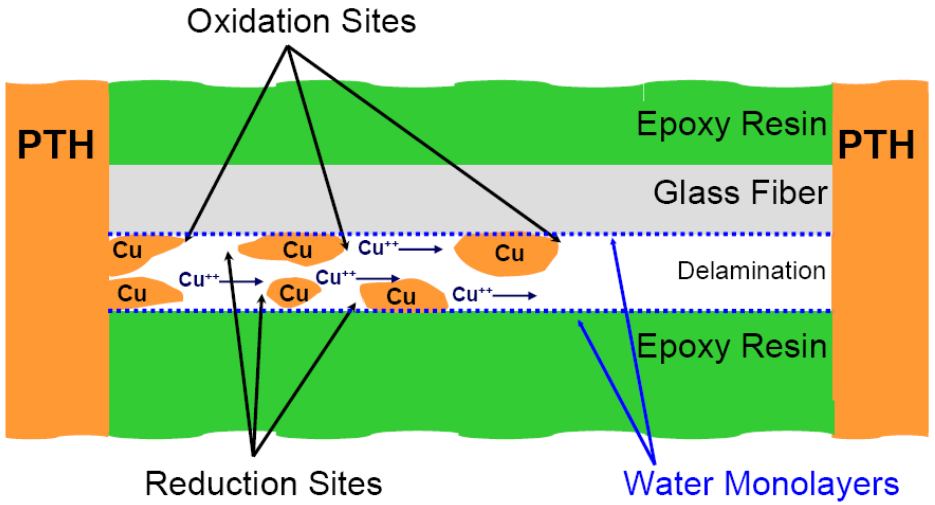
Conclusion

- The base knowledge and understanding of PTV Fatigue is robust
  - Decades of testing and simulation
  - Use of reliability physics is best practice
- Detailed understanding is still missing
  - Key expertise (process parameters, material properties, simulation, testing) is rarely in the same organization
  - Not a pure science activity (significant amount of human influence)
- Improvements in out-of-plane CTE and plating properties have greatly improved PTV performance
  - Avoiding defects continues to be the biggest risk

PCB Conductive Anodic Filaments (CAF)

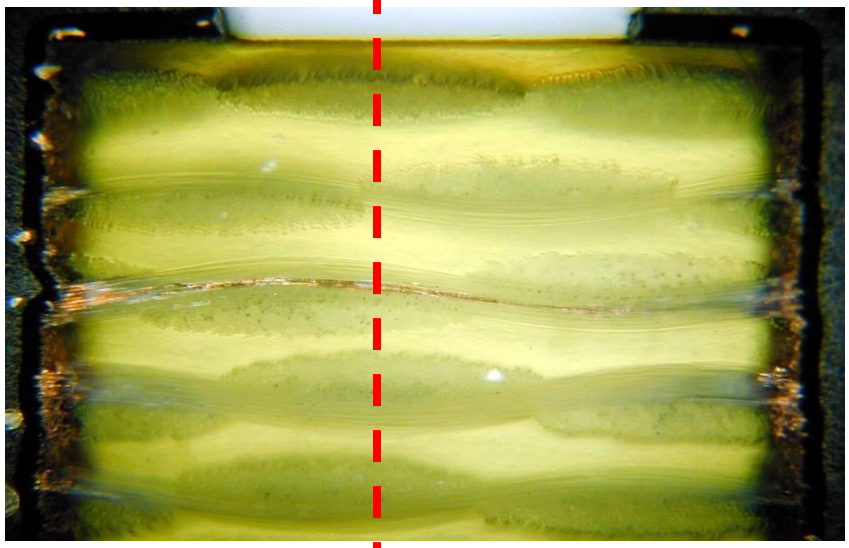
- CAF also referred to as metallic electro-migration
- Electro-chemical process which involves the transport (usually ionic) of a metal across a nonmetallic medium under the influence of an applied electric field
- CAF can cause current leakage, intermittent electrical shorts, and dielectric breakdown between conductors in printed wiring boards

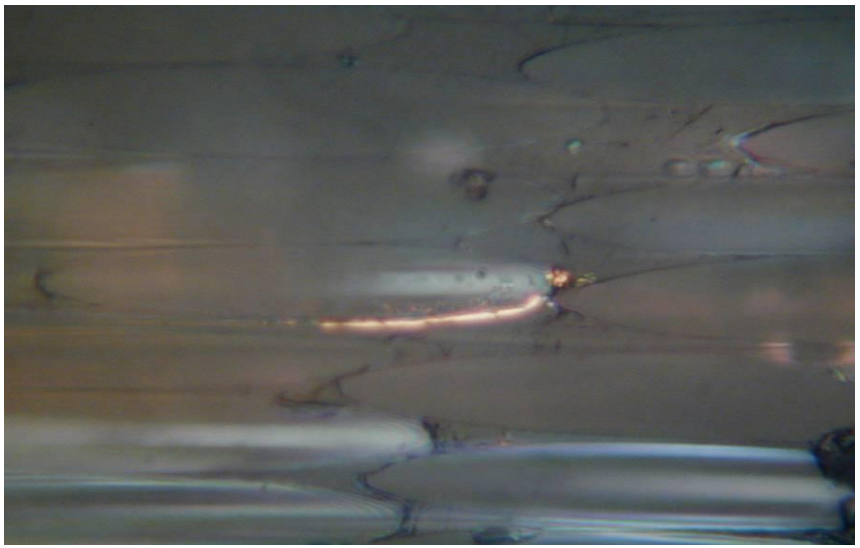




CAF: Examples

Influenced by electric field strength, temperature, humidity, laminate material, soldering temperatures, and the presence of PCB manufacturing defects.

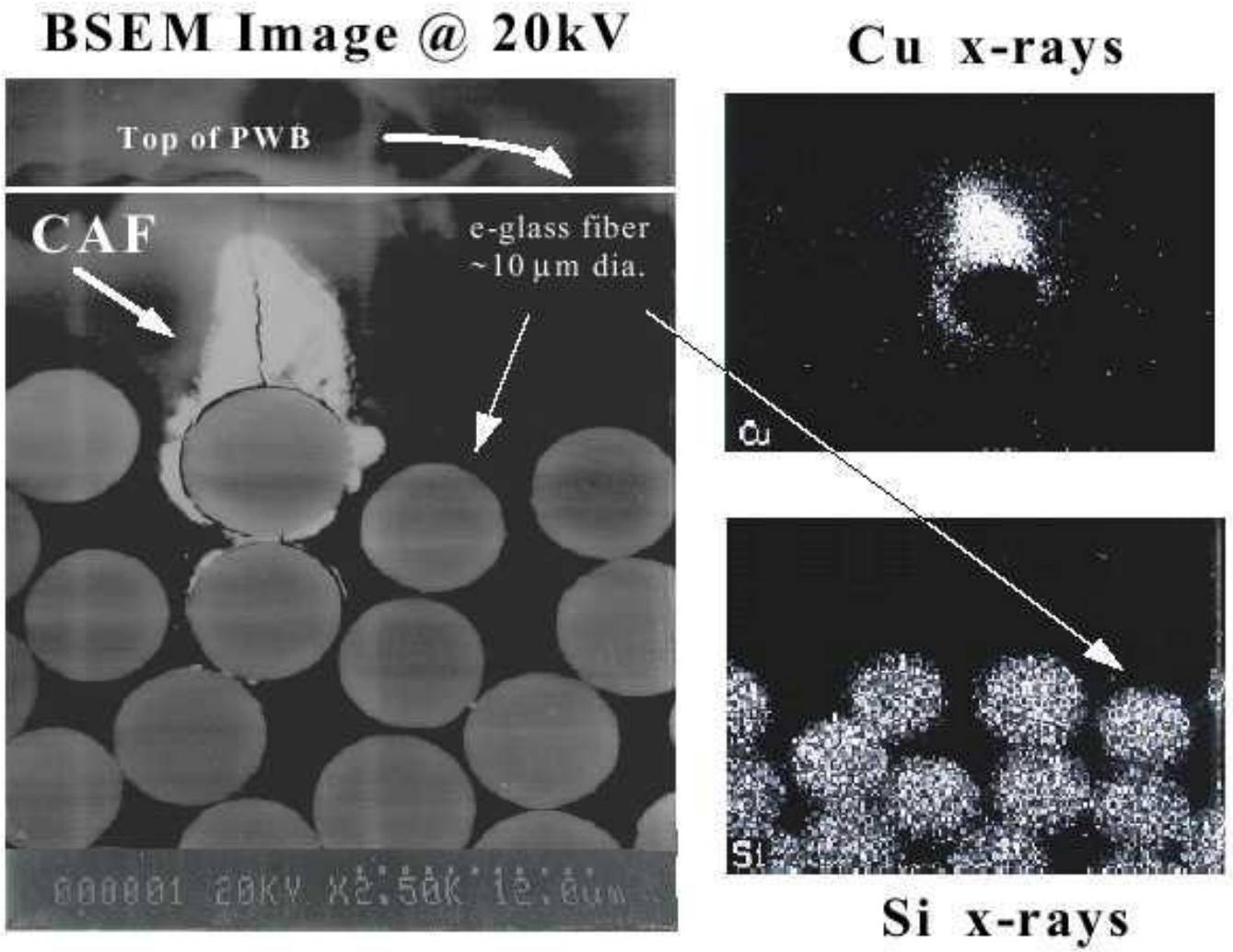




A:A Cross-Section

Request a CAF-resistant laminate and monitor PCB supplier plating & drilling processes!

CAF: Examples



DfR Solutions

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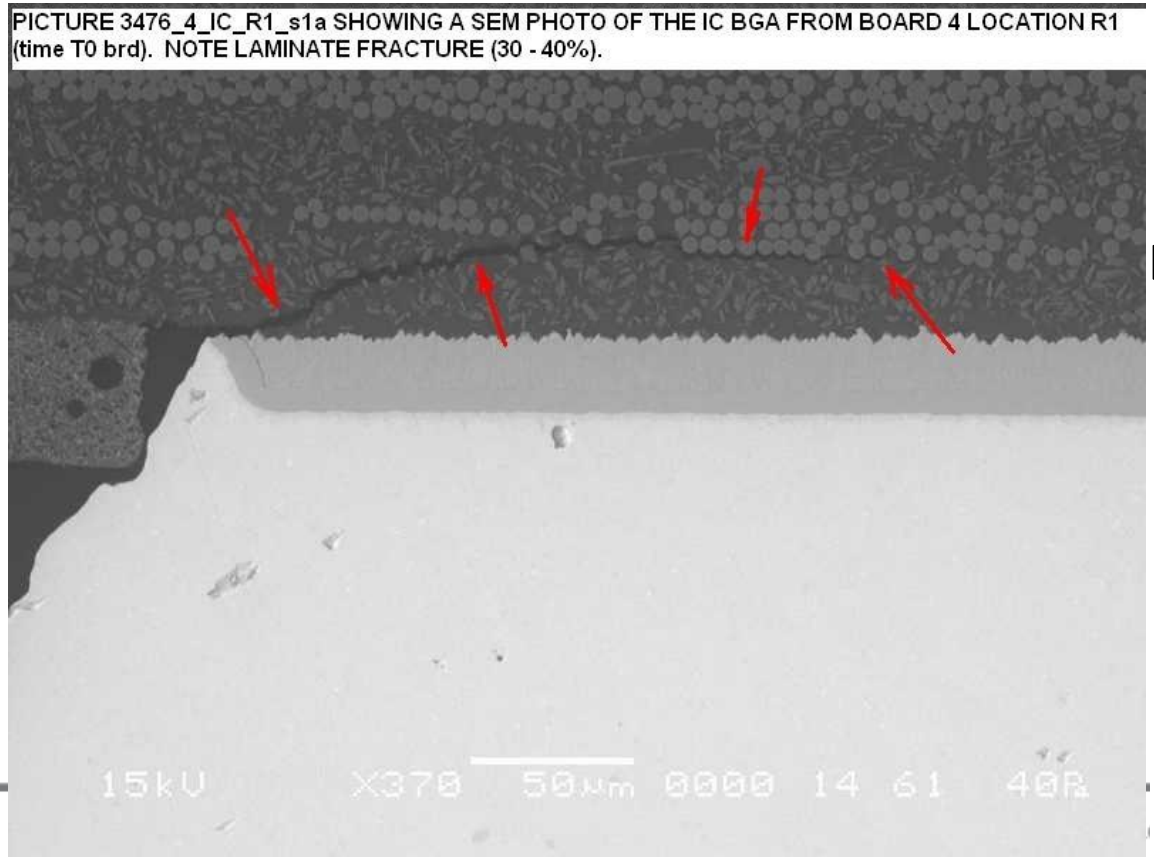
Strain Flexure Issues & Pad Cratering

Cleanliness

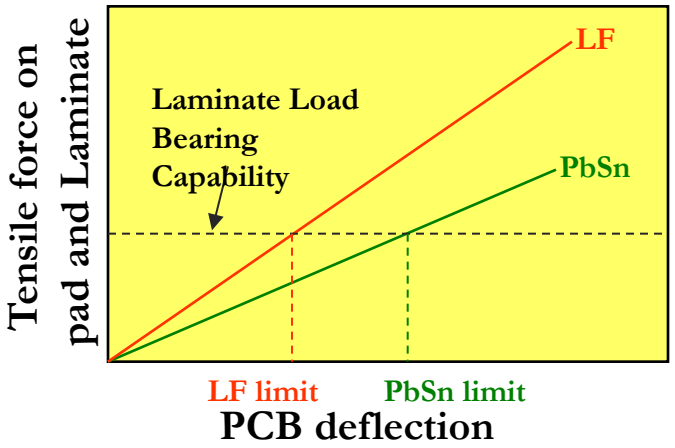
Electro-Chemical Migration (ECM)

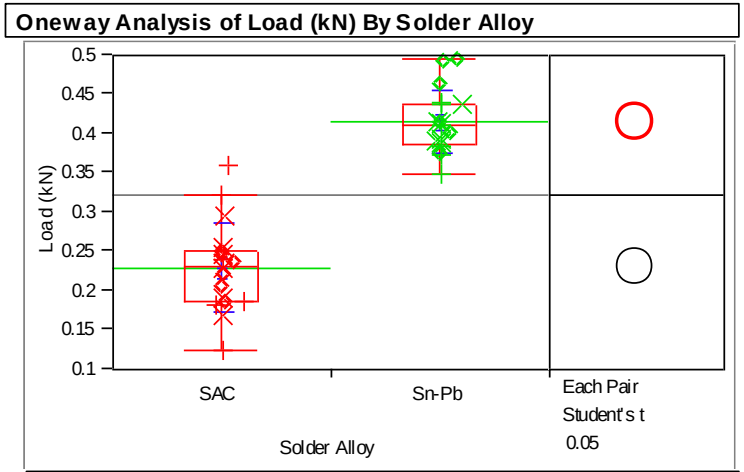
SAC Solder is More Vulnerable to Strain

Sources of strain can be ICT, stuffing through-hole components, shipping/handling, mounting to a chassis, or shock events.



NEMI study showed SAC is more Sensitive to bend stress.



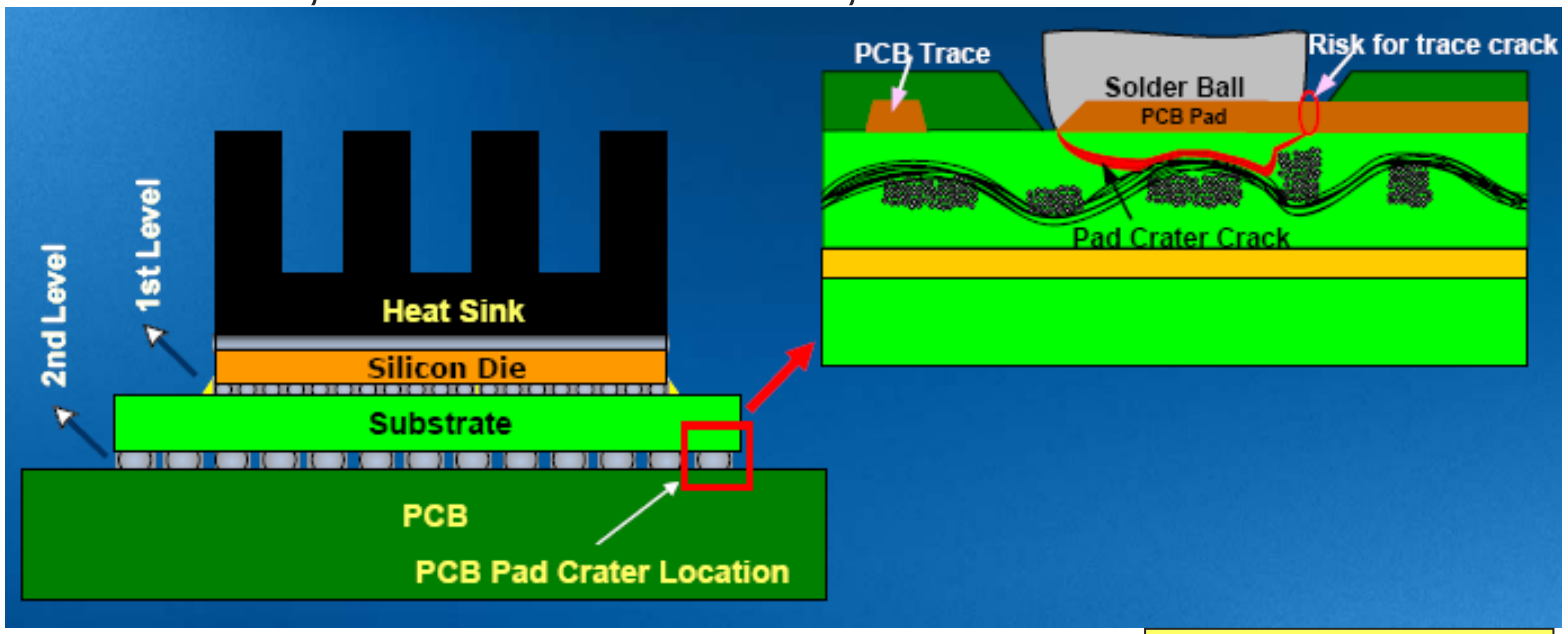


Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
SAC	18	0.230859	0.056591	0.01334	0.20272	0.25900
Sn-Pb	18	0.416101	0.040408	0.00952	0.39601	0.43620

Strain & Flexure: Pad Cratering

- Cracking initiating within the laminate during a dynamic mechanical event
  - In circuit testing (ICT), board depanelization, connector insertion, shock and vibration, etc.

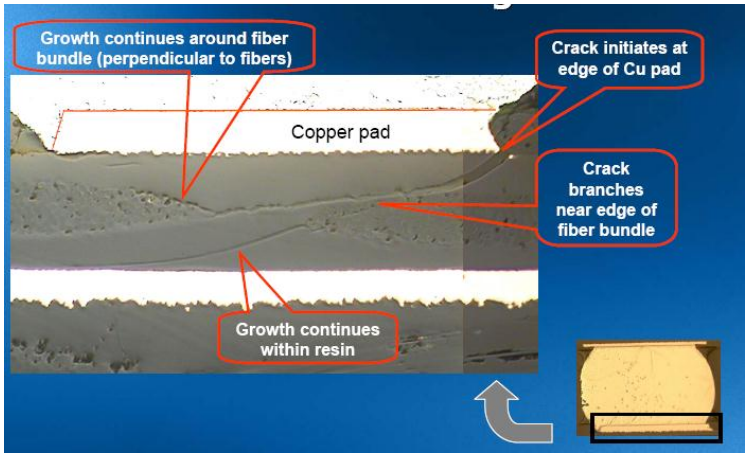


G. Shade, Intel (2006)

Pad Cratering

Intel (2006)

- Drivers
  - Finer pitch components
  - More brittle laminates
  - Stiffer solders (SAC vs. SnPb)
  - Presence of a large heat sink



- Difficult to detect using standard procedures
  - X-ray, dye-n-pry, ball shear, and ball pull

Potential Mitigations to Pad Cratering

- Design
  - Non-critical pads
  - Solder mask defined vs. non-solder mask defined
  - Pad Geometry
  - Layout & PCB thickness
- Limitations on board flexure
  - 750 to 500 microstrain, component and layout dependent
  - Process Control & Validation
- Corner Glue
- More compliant solder
  - SAC305 is relatively rigid, SAC105 and SNC are possible alternatives
- New laminate acceptance criteria and materials

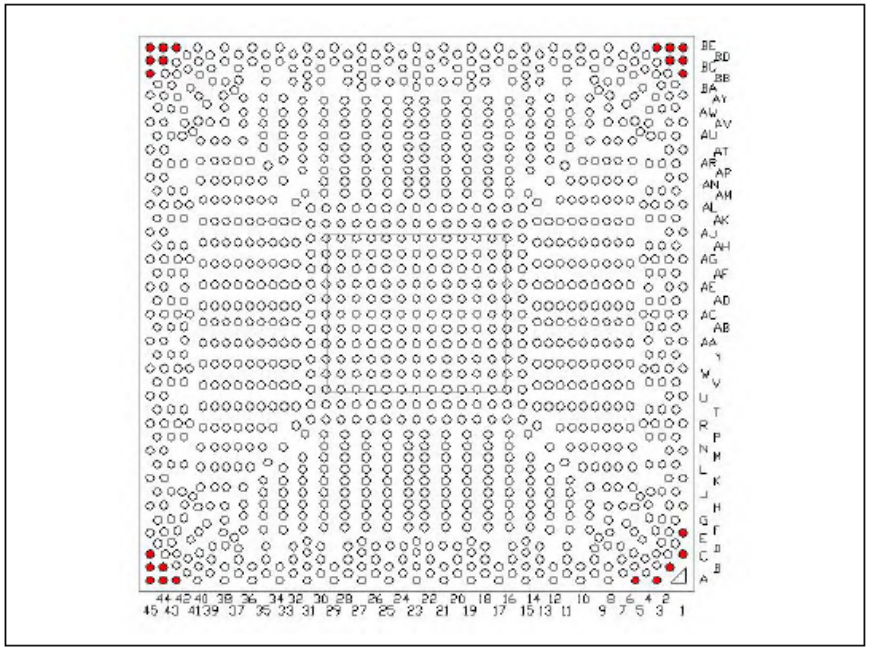
Component Supplier Practices Intel Example

Product Specifications

2.4 Non-Critical to Function Solder Balls

Intel has defined selected solder joints of the (G)MCH as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The (G)MCH signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. Figure 3 identifies the NCTF solder joints of the (G)MCH package.

Figure 3. Non-Critical to Function Solder Balls



Pad Geometry

- Pad design influences failure
  - Smaller pads result in higher stress under a given load
- Solder mask defined pads can provide additional strength
  - Increases tolerable strain
  - But, moves failure location from pad crater to intermetallic fracture

Contamination and Cleanliness

- Believed to be one of the primary drivers of field issues in electronics today
  - Induces corrosion and metal migration (electrochemical migration – ECM)
- Intermittent behavior lends itself to no-fault-found (NFF) returns
  - Driven by self-healing behavior
  - Difficult to diagnosis
- Pervasive
  - Failure modes observed on batteries, LCDs, PCBAs, wiring, switches, etc.
- Will continue to get worse

Future of Contamination / Cleanliness

- Continued reductions in pitch between conductors will make future packaging more susceptible
- Increased use of leadless packages (QFN, land grid array, etc.) results in reduction in standoff
  - Will reduce efficiency of cleaning, which may lead to increased concentration of contaminants
- Increased product sales into countries with polluted and tropical environments (East Asia, South Asia, etc.)
  - ECM occurrence very sensitive to ambient humidity conditions
- Pb-Free and smaller bond pads
  - Require more aggressive flux formulations

The Future: Reduced Spacings

- Critical distance effect?
  - Two studies by DfR staff
    - NaCl seeding
    - Conformal coating over no-clean flux residues
  - Over 300 coupons tested (IPC-B-25)
    - 6.25, 12.5, and 25 mil spacings; 40C/93%RH, 65C/88%RH, 85C/85%RH
  - No ECM at 25 mil spacings

- Experience based on older designs may not be valid
- Test coupons must have the same spacing and same electric field as actual product

Parameter	Spacing
Peripheral Flip Chip Solder Bumps	5 mil (120 μm)
Thin Shrink Small Outline Package (TSSOP) Leads	7 mil (170 μm)
PCB External Traces (low voltage line)	4 mil (100 μm)
BGA Substrate Traces	2 mil (48 μm)

Failure Mode

- Why do you care about excessive contamination or insufficient cleanliness?

Electrochemical Migration

(note: not Electromigration; completely different mechanism)

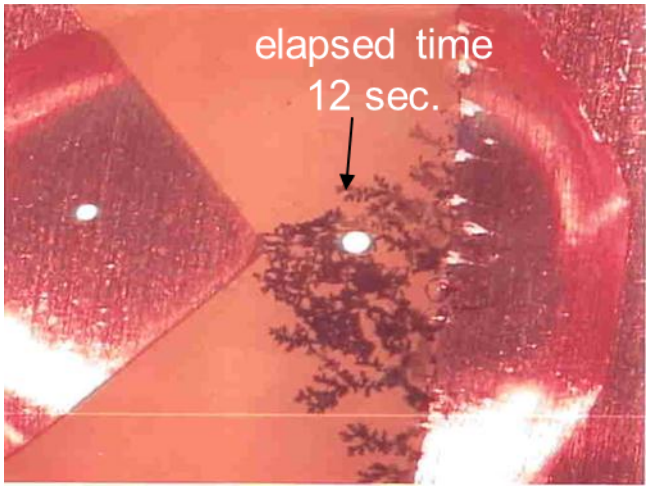
- Understanding the mechanism provides insight into the drivers and appropriate mitigations

What is ECM?

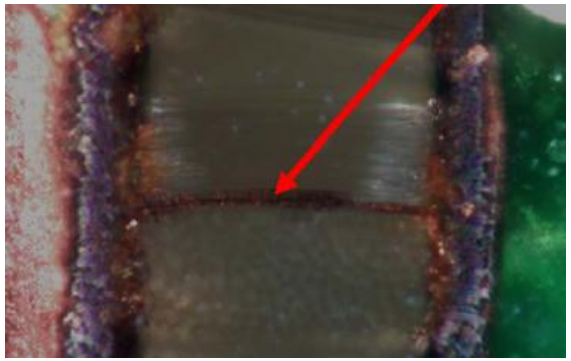
- Movement of metal through an electrolytic solution under an applied electric field between insulated conductors
- Electrochemical migration can occur on or in almost all electronic packaging
  - Die surface
  - Epoxy encapsulant
  - Printed board
  - Passive components
  - Etc.

ECM Mechanisms

- Some ECM Mechanisms have more definitive descriptions
- Dendritic growth
  - Descriptor for ECM along a surface that produces a dendrite morphology
  - "Tree-like", "Feather-like"



- Conductive anodic filaments (CAF)
  - Descriptor for migration within a printed circuit board (PCB)



PCB Cleanliness: Moving Forward

- Extensive effort to update PCB Cleanliness Standards
- IPC-5701: Users Guide for Cleanliness of Unpopulated Printed Boards (2003)
- IPC-5702: Guidelines for OEMs in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (2007)
- IPC-5703: Guidelines for Printed Board Fabricators in Determining Acceptable Levels of Cleanliness of Unpopulated Printed Boards (Draft)
- **IPC-5704: Cleanliness Requirements for Unpopulated Printed Boards (2010)**

Nominal Ionic Levels

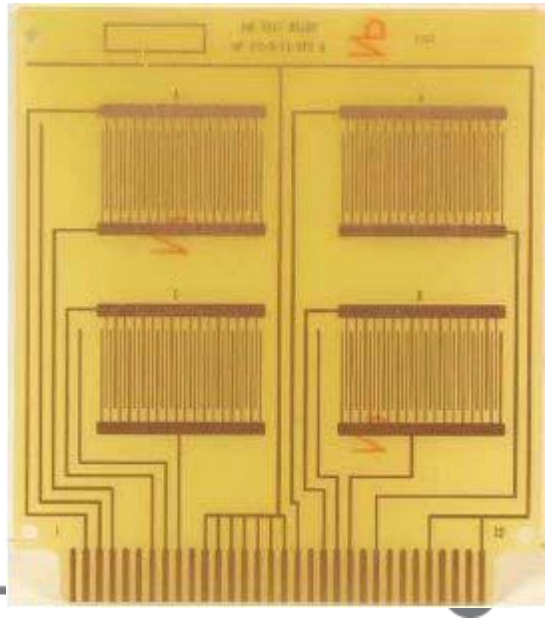
- Bare printed circuit boards (PCBs)
  - Chloride: 0.2 to 1 µg/inch^2 (average of 0.5 to 1)
  - Bromide: 1.0 to 5 µg/inch^2 (average of 3 to 4)
- Assembled board (PCBA)
  - Chloride: 0.2 to 1 µg/inch^2 (average of 0.5 to 1)
  - Bromide: 2.5 to 7 µg/inch^2 (average of 5 to 7)
  - Weak organic acids: 50 to 150 µg/inch^2 (average of 120)
- Higher levels
  - Corrosion/ECM issues at levels above 2 (typically 5 to 10)
  - Corrosion/ECM issues at levels above 10 (typically 15 to 25)
  - Corrosion/ECM issues at levels above 200 (typically 400)
- General rule
  - Dependent upon board materials and complexity

Cleanliness Control

- Incoming PCB Cleanliness
  - Cleanliness testing performed using ROSE (resistivity of solvent extracted) or Omega-Meter method (ionic cleanliness, NaCl equivalent)
- Consider cleanliness requirements in terms of IC (ion chromatography) test for PCBs using WS flux
  - Don't use ROSE or Omegameter test as single option (at all? Risk from dirty IPA)
  - Inspection method with accept/reject limit
  - Sampling criteria
- Control cleanliness throughout the process from start to finish.

Process Material Qualification – SIR Recommendation

- Validate compatibility and performance of all new process materials using SIR testing.
  - IPC-B-52 SIR TEST VEHICLE (shown below)
  - IPC-A-52:Cleanliness and Residue Evaluation Test Board – Single User CD-ROM
    - The IPC-B-52 test board is intended to be a process qualification vehicle, with the materials of construction and source of test boards to be representative
    - https://portal.ipc.org/Purchase/ProductDetail.aspx?Product_code=5e7a8626-b486-db11-a4eb-005056875b22



Surface Finishes

Importance of Surface Finish

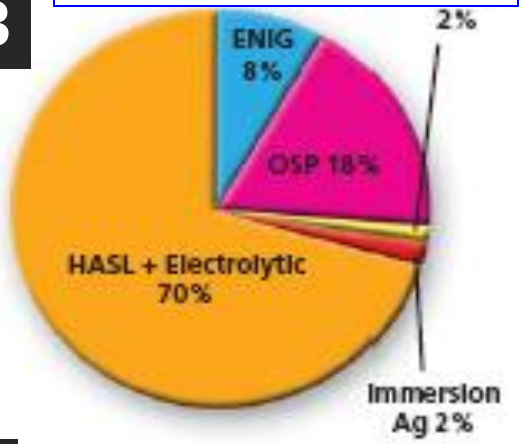
- The selection of the surface finish to be used on your PCBs could be the most important material decision made for the electronic assembly.
- The surface finish influences the process yield, the amount of rework necessary, field failure rate, the ability to test, the scrap rate, and of course the cost.
- One can be lead astray by selecting the lowest cost surface finish only to find that the total cost is much higher.
- The selection of a surface finish should be done with a holistic approach that considers all important aspects of the assembly.

Surface Finishes - Post Pb-Free

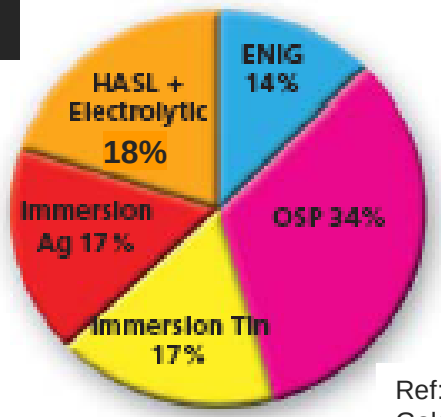
- Multiple Pb-Free Surface Finish Options Now Exists.
  - No clear winner, no ideal solution.
- Each PCB surface has different advantages and disadvantages that affects fabrication, solderability, testability, reliability, or shelf life.
- The 5 most popular Pb-Free Surface Finishes are:
  - Electroless nickel/immersion gold (ENIG)
    - And ENEPIG (electroless Pd added)
  - Immersion silver (ImAg)
  - Immersion tin (ImSn)
  - Organic solderability preservative (OSP)
  - Pb-free HASL.
- These finishes (except for Pb-free HASL) have been in use for several years.
- Newer finishes are currently being developed (direct Pd, PTFE-like coatings, etc.

Surface Finishes, Worldwide

2003



2007



Ref: J. Beers Gold Circuits

DfR Solutions

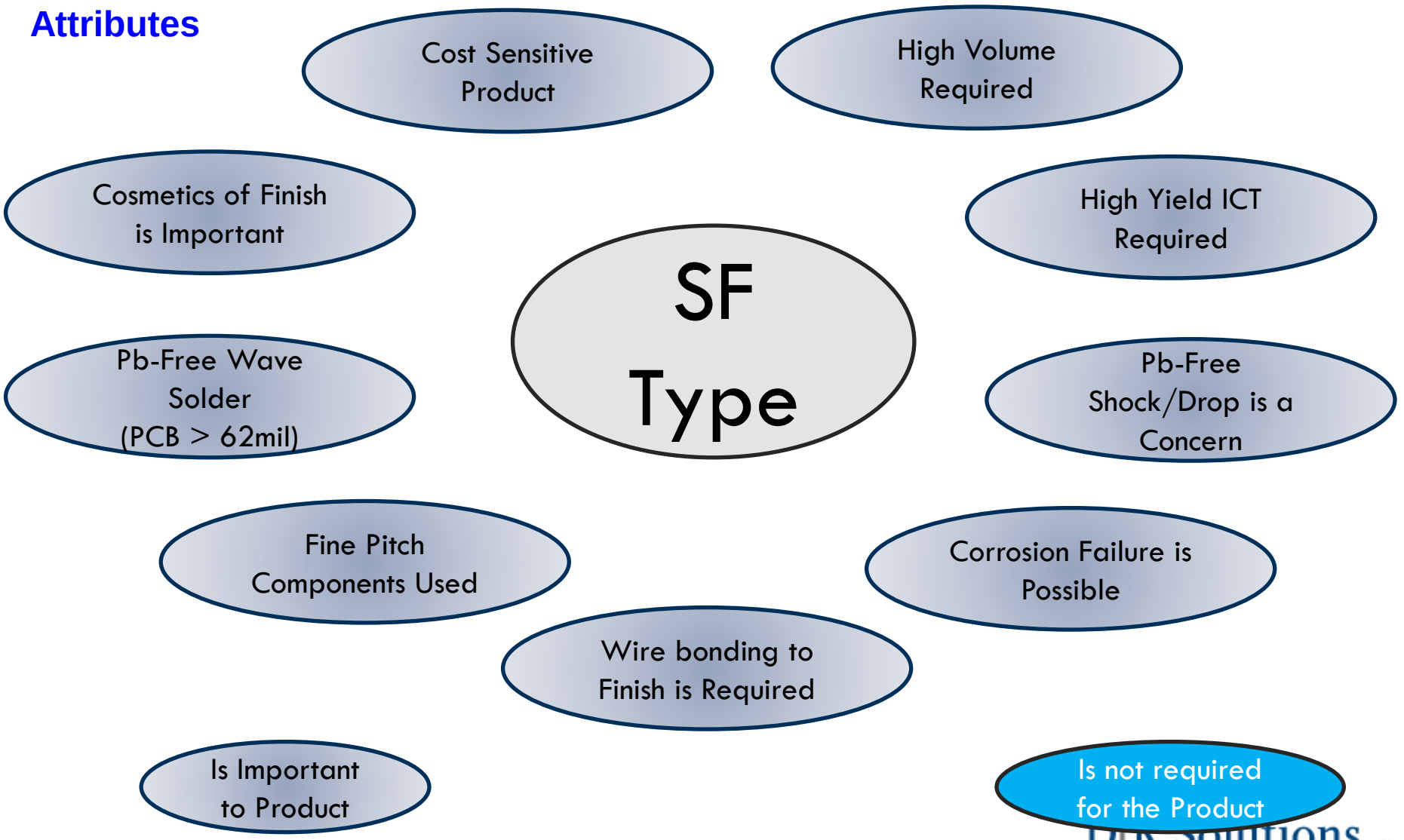
Surface Finish Selection Approach

- *Component Procurement:* Select the cheapest one and let the engineers figure out how to use it.
- *PCB Engineer:* Select the finish that is easiest for the suppliers to provide (their sweet spot); let the assembler figure out how to use it.
- *Assembly Engineer:* Select the finish that provides the largest process window for assembly and test.
- *Sustaining Engineer:* Select the finish that minimizes field failures.
- *CEO:* Select the finish that minimizes the overall cost (including reliability risk).

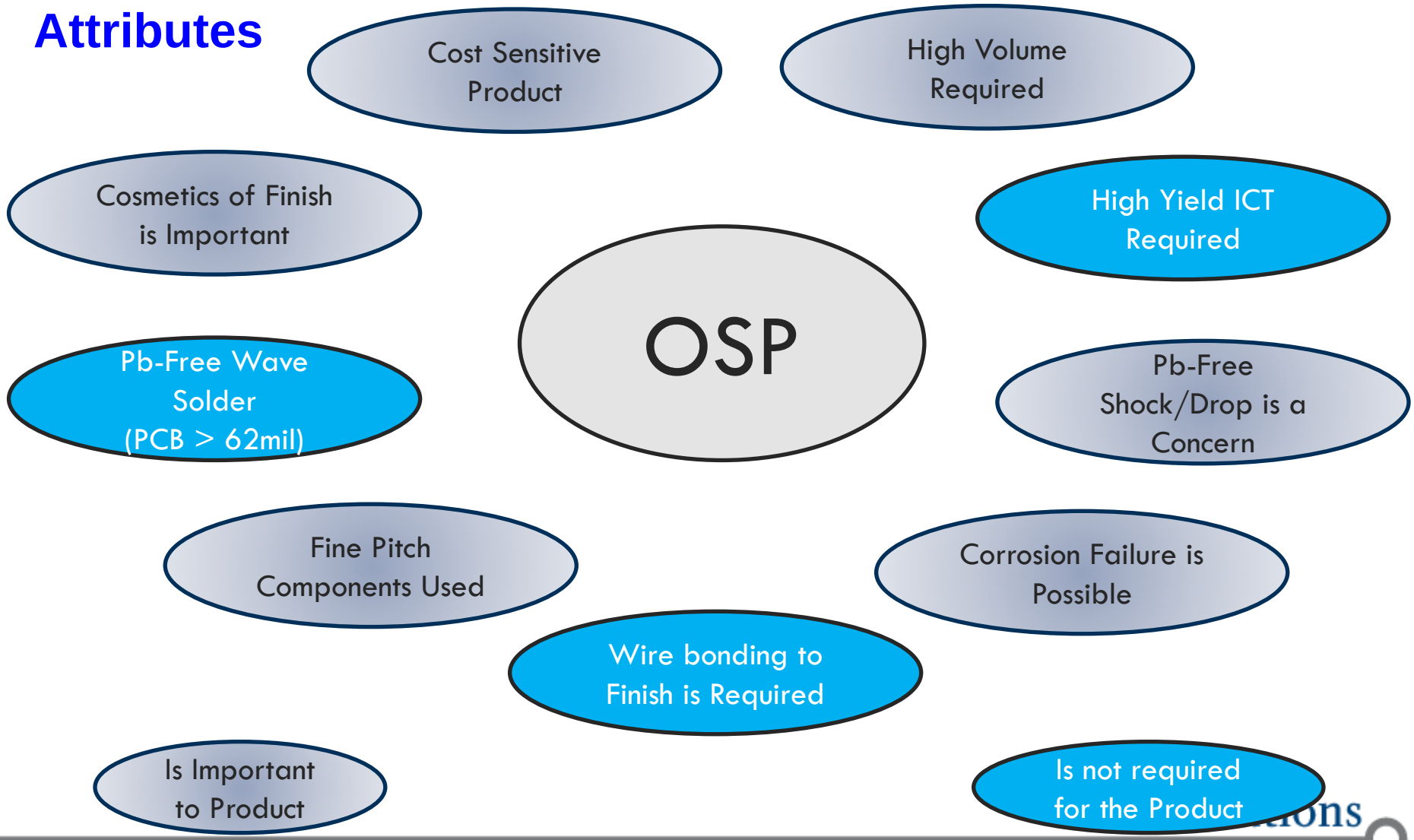
Surface Finish Selection Considerations

- Cost sensitivity
- Volume of product (finish availability)
- SnPb or LF process
- Shock/Drop a concern?
- Cosmetics a concern?
- User environment (corrosion a concern)?
- Fine pitch assembly (<0.5 mm)
- Wave solder required (PCB > 0.062")
- High yield ICT is important?

Surface Finish Selection Guideline

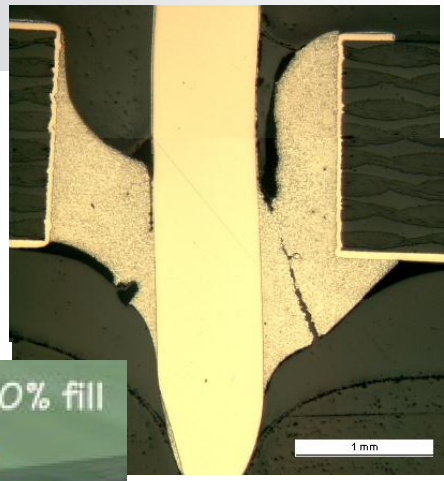


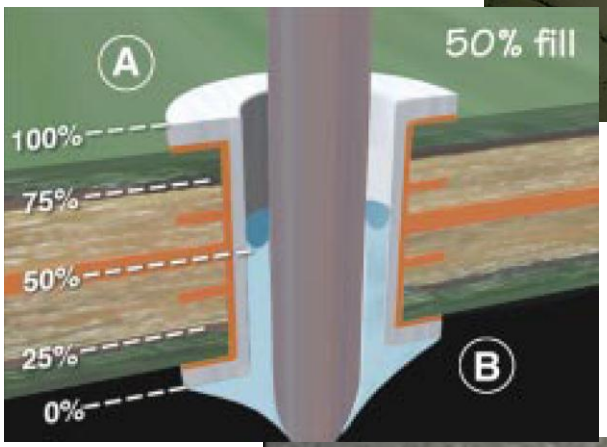
Surface Finish Selection Guideline



OSP Issues: Plated Through-Hole Fill

- Solder fill is driven by capillary action
- Important parameters
  - Hole diameter, hole aspect ratio, wetting force
  - Solder will only fill as long as its molten (key point)
- OSP has lower wetting force
  - Risk of insufficient hole fill
  - Can lead to single-sided architecture
- Solutions:
  - Changing board solderability plating
  - Increasing top-side preheat
  - Increasing solder pot temperature (some go as high as 280ºC)
    - Not recommended!
  - Changing your wave solder alloy

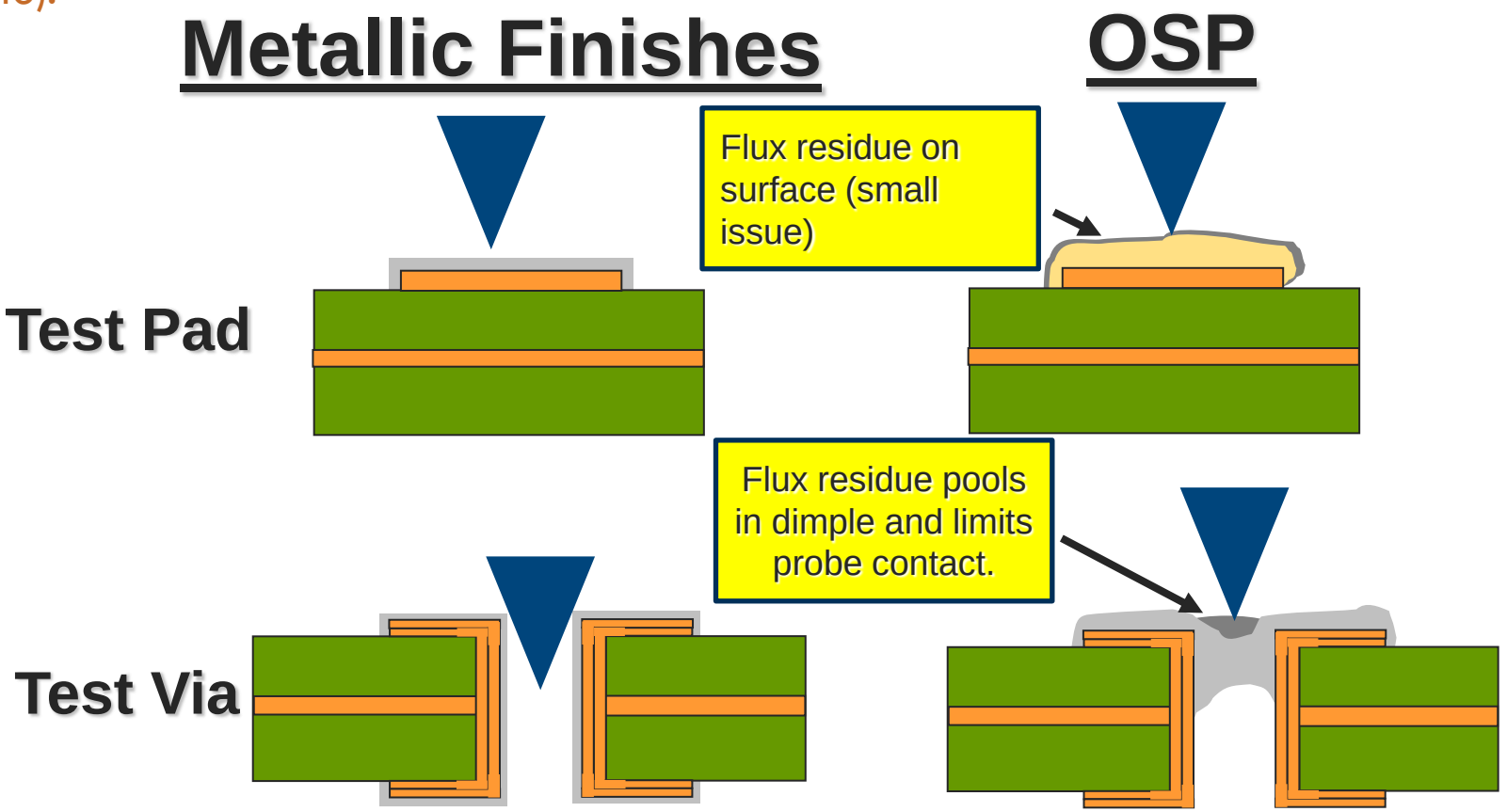




P. Biocca, Kester

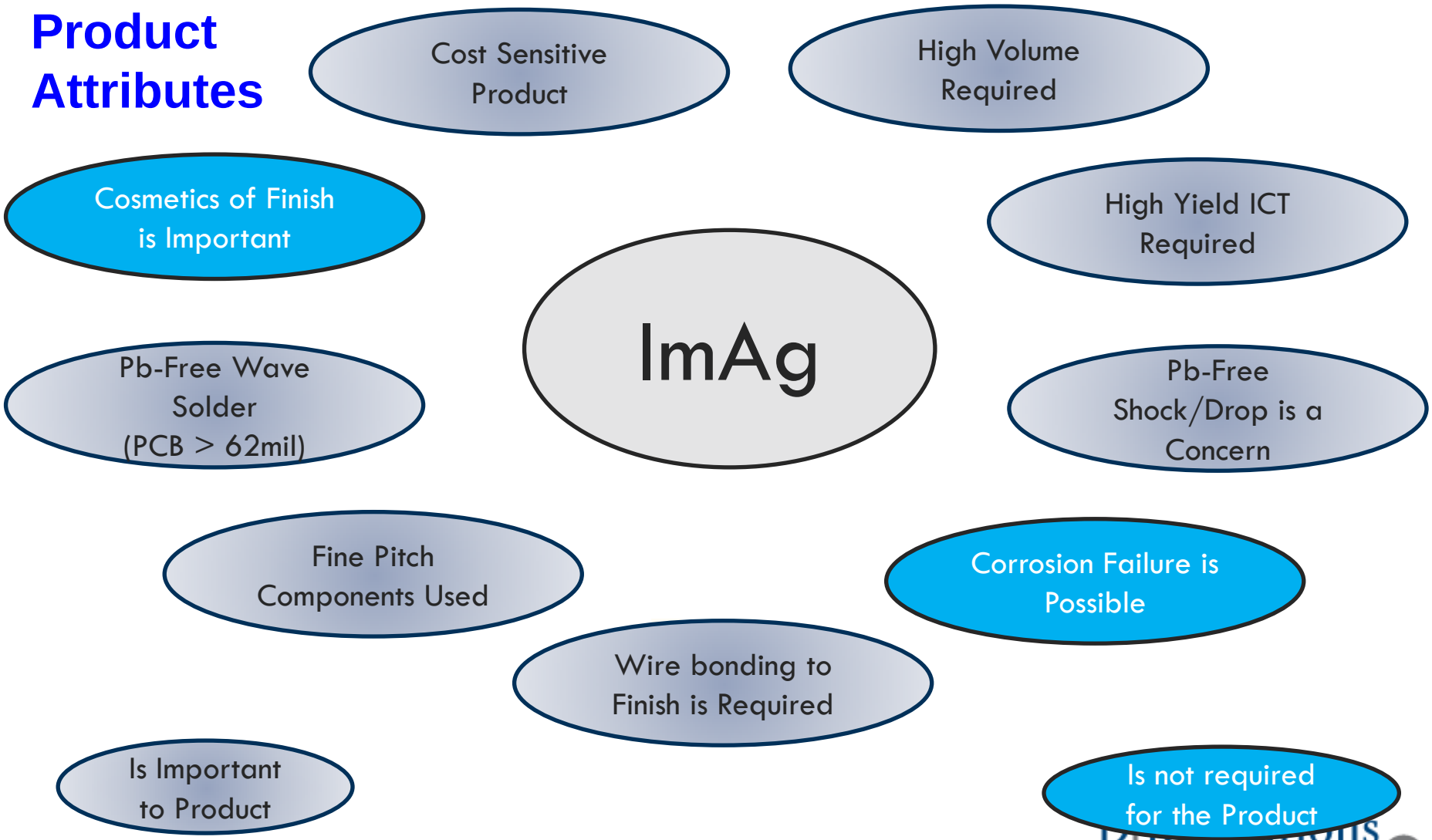
In Circuit Test w/ OSP – test via challenges

- Probing through HT OSP is not recommended.
- Solder paste is printed over OSP test pads/vias (leaving flux residue with no-clean paste).



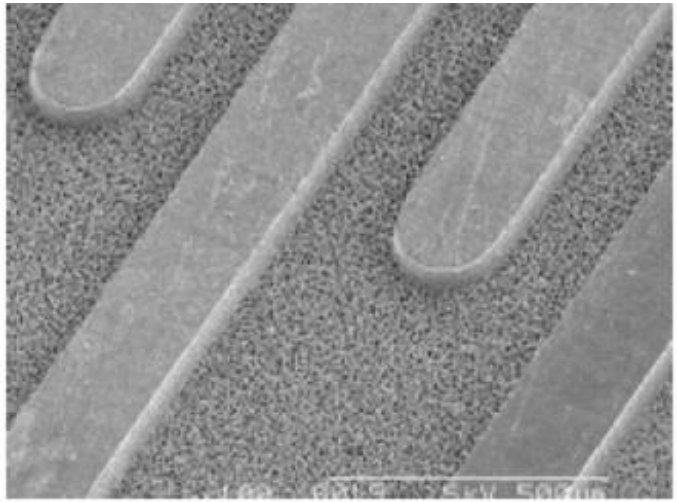
Space constraints on PCB make it difficult to eliminate test vias.

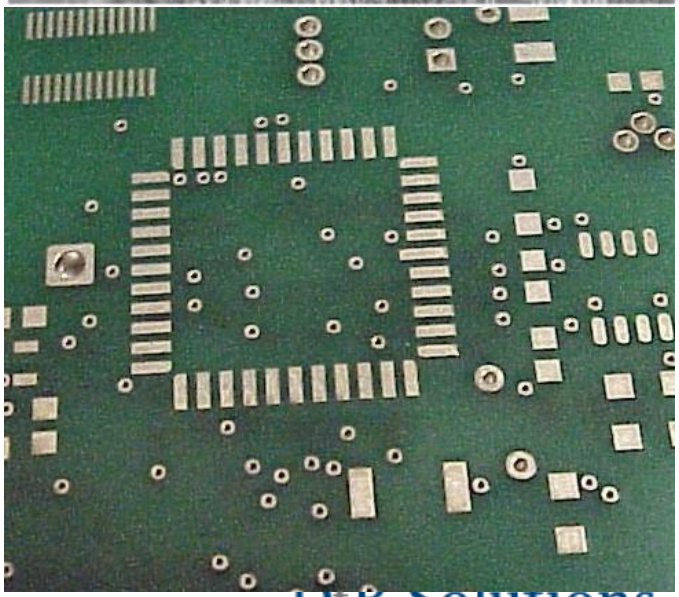
Surface Finish Selection Guideline



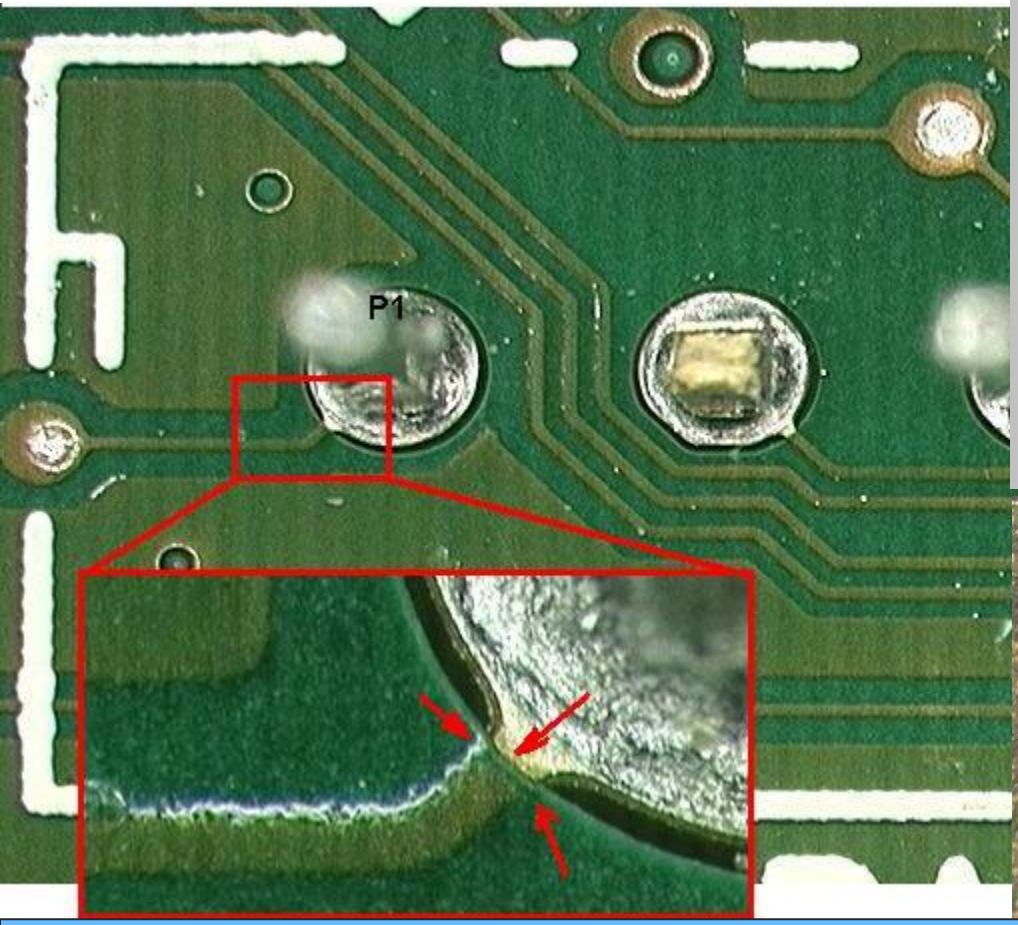
Immersion Silver Ag (ImAg)

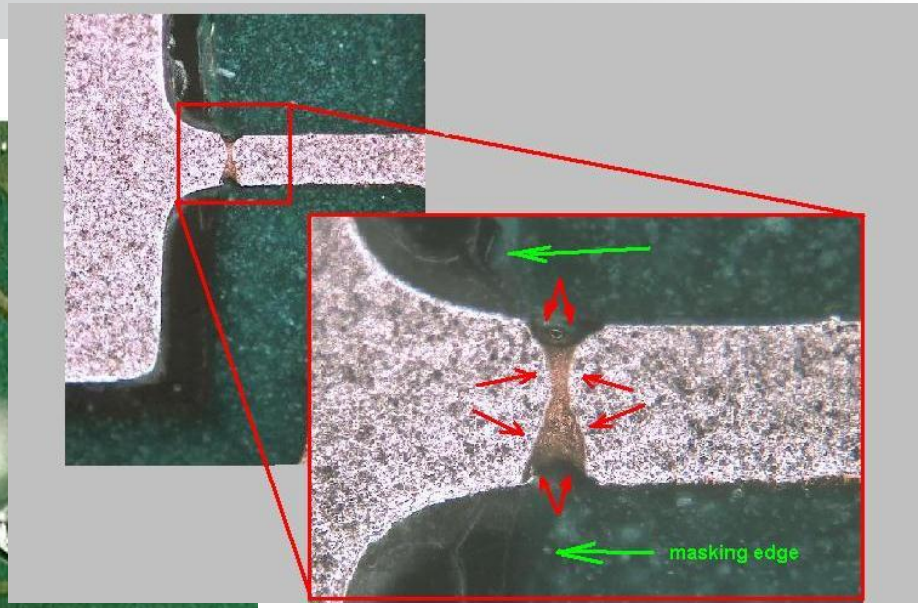
- Single material system
  - Specified by IPC-4553
- Thickness is typically 6-20 u”
- Benefits
  - Good flatness & coplanarity
  - Good shelf life if packaged properly.
  - Good oxidation resistance & shelf life.
  - Good wettability and reflow performance.
  - Good testability
  - Low cost

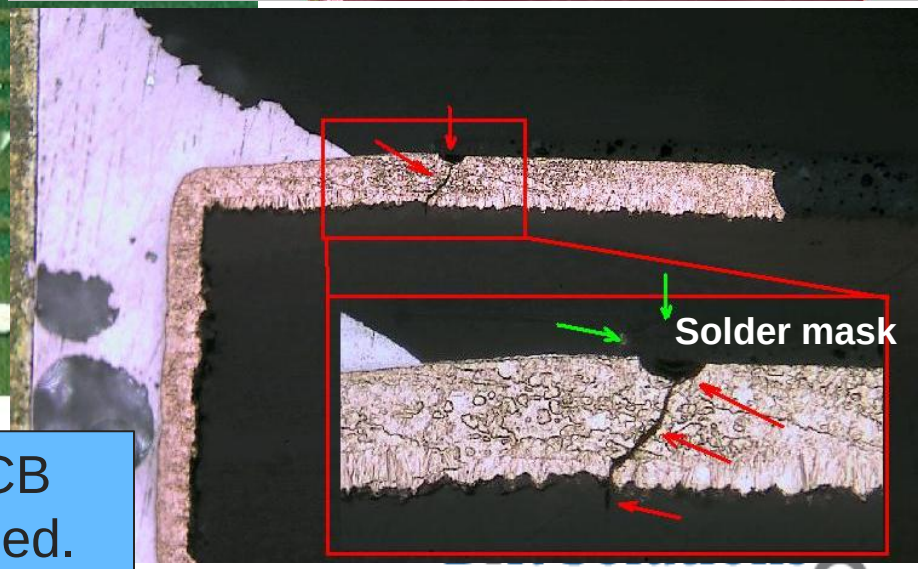




ImAg Trace Etching

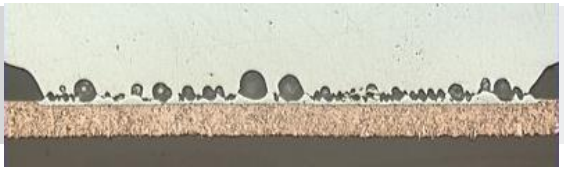






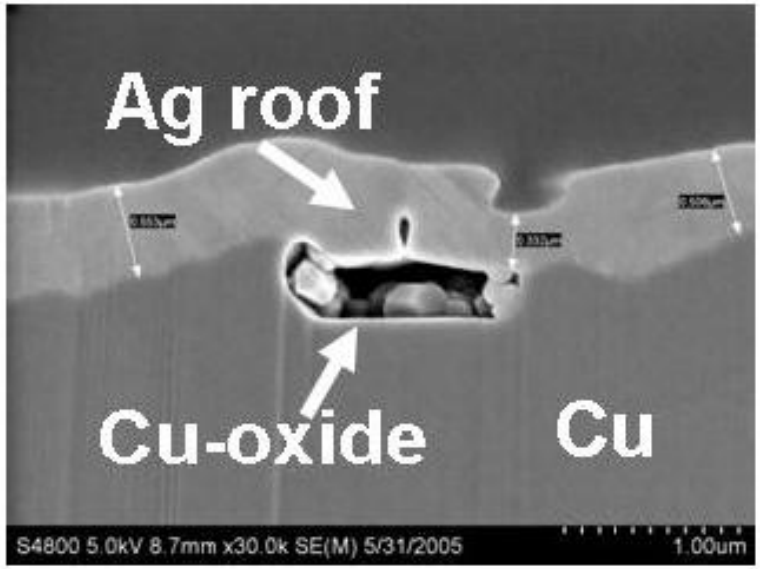
Galvanic etching can occur SM edge if PCB rinsing and drying not adequately performed.

ImAg - Microvoids



- Void under silver causes void at interface.

Microvoids survived shock testing but cause early failure in thermal cycling.



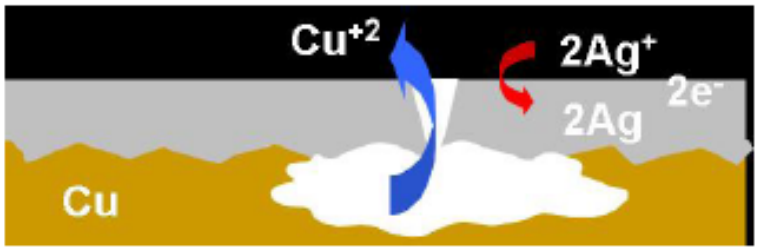
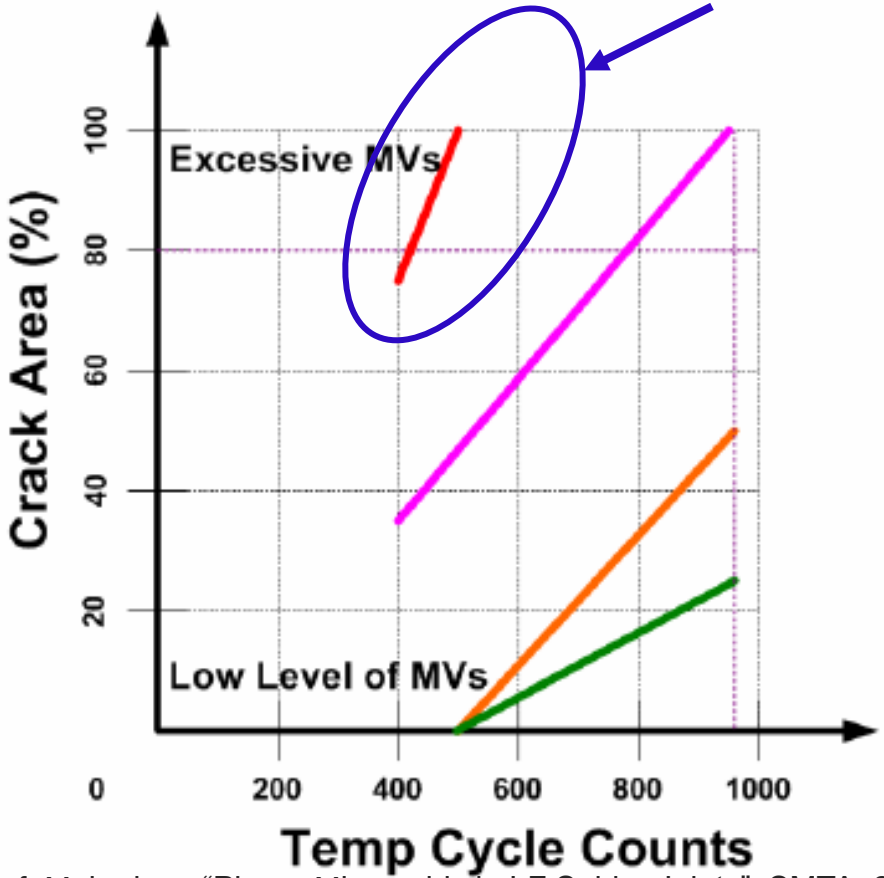
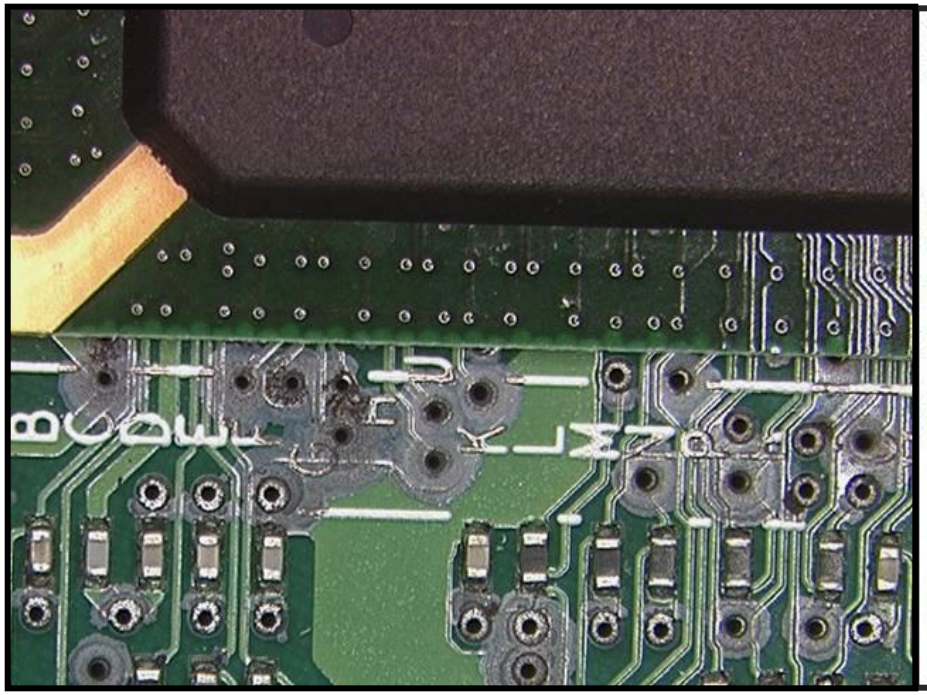


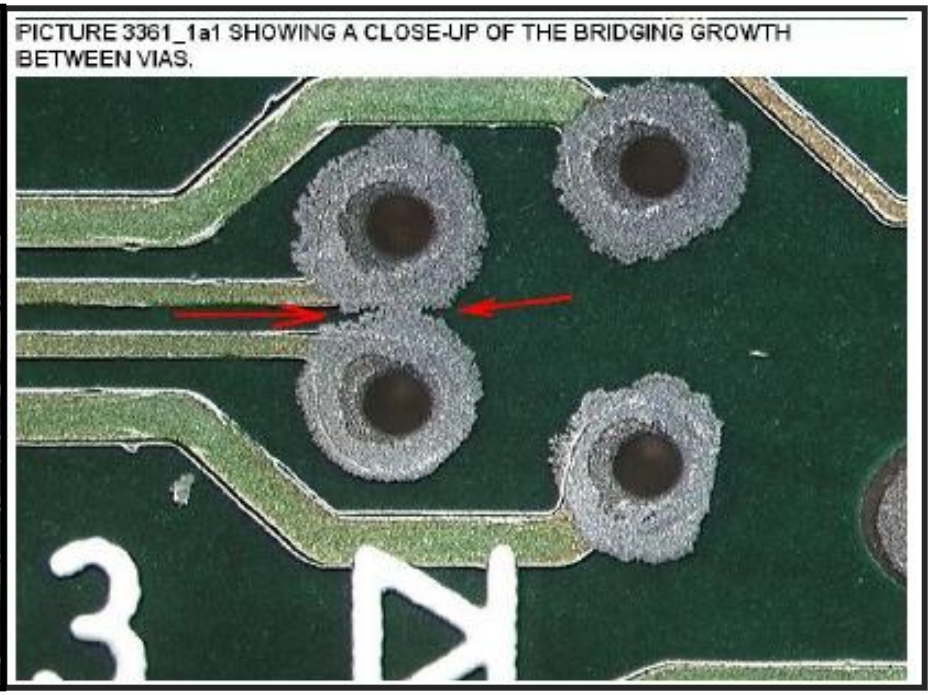
Figure 31. The small Cu area with respect to the surrounding Ag surface bias the current density causing Cu+ ions to stream-out into the ImAg bath, at the same time, the Cu- electrons re-routed to satisfy Ag+ ion reduction away from this region.



Ref: Mukadam, "Planar Microvoids in LF Solder Joints", SMTA, 2006.

Typical Creep Corrosion





- Corrosion product is poorly conductive (resistance of about 1Mohm).
- Conductivity is higher when the humidity is high.
- Field returns often function fine – since corrosion product has dried out.
- Features most sensitive to leakage current will trigger the system failure (failing symptoms can vary system-to-system).
- Visual inspection is often required to diagnose.

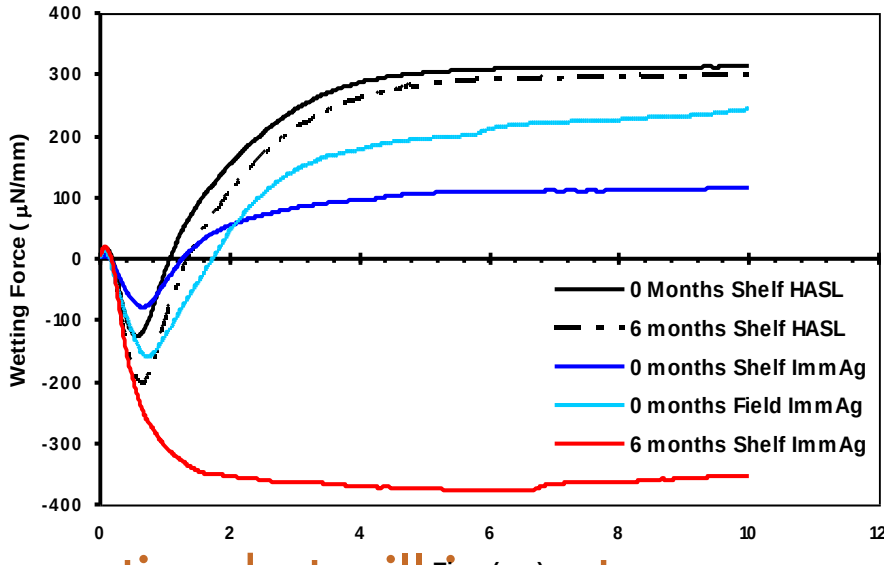
ImAg Creep Corrosion - Affected Locations

- Paper mills
- Rubber manufacturing (tires for example).
- Fertilizer
- Waste water treatment
- Mining/smelting
- Cement or asphalt production
- Petrochemical
- Clay modeling studios
- Regions of the world with poor air quality
- Etc. - includes companies nearby such industries

• Product is less impacted if airflow to PCBA is restricted.

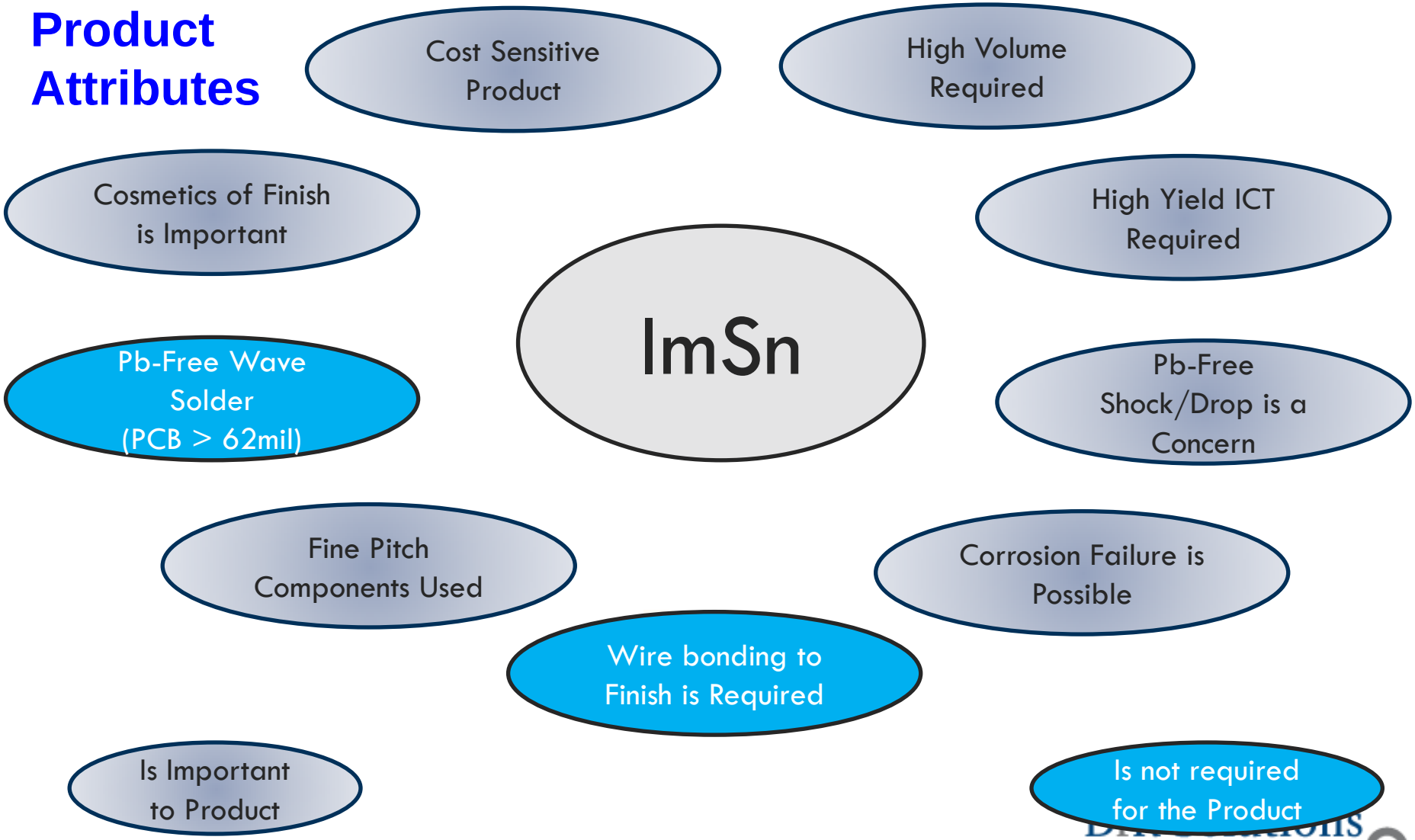
Impact of Tarnish

- Shelf life can be an issue
  - If not stored in protective bags
  - Significant degradation when exposed to corrosive gases



- Tarnish after assembly is mostly cosmetic – but will impact perception of quality.
- If PCBA is visible to user tarnish may be an issue.
- Scrap costs may increase considerably if PCBAs are repaired and sent back into service.
  - Boards that appear black but are still functional are often thrown out.

Surface Finish Selection Guideline

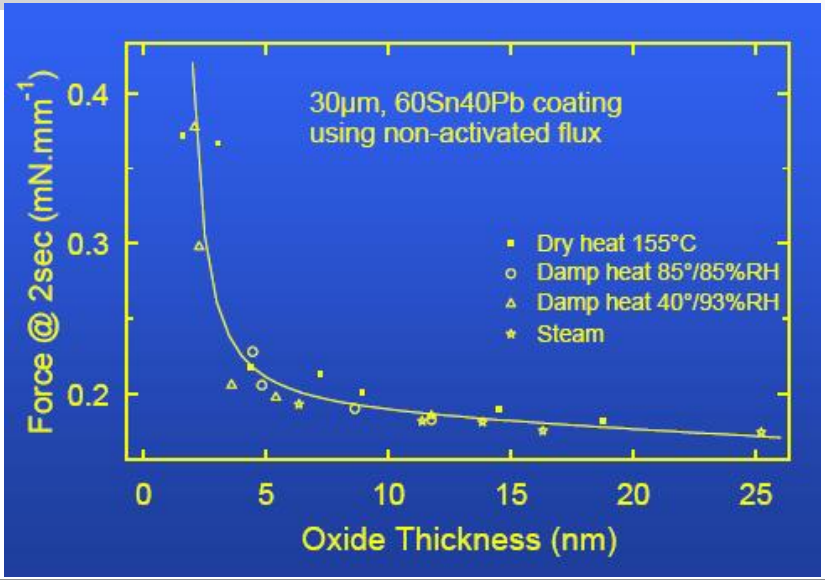


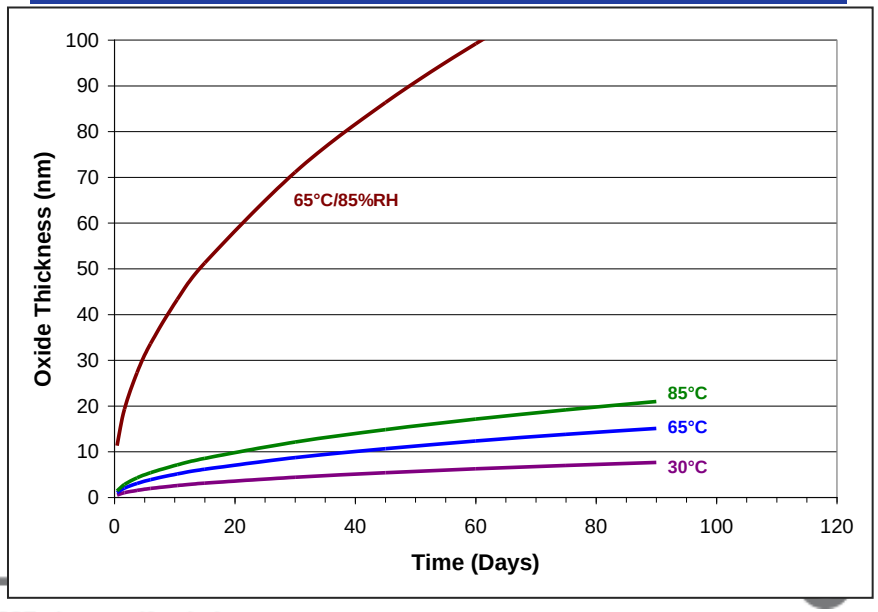
Immersion Sn (ImSn)

- A single material system
  - Specified by IPC-4554
    - Standard thickness: 1 micron (40 microinches)
    - Some companies spec up to 1.5 microns (65 microinches)
- Benefits
  - Excellent flatness, low cost
- Not as popular a choice with PCB fabricators.
  - Environmental and health concerns regarding thiourea (a known carcinogen)
  - Some concern regarding tin whiskering (minimal)

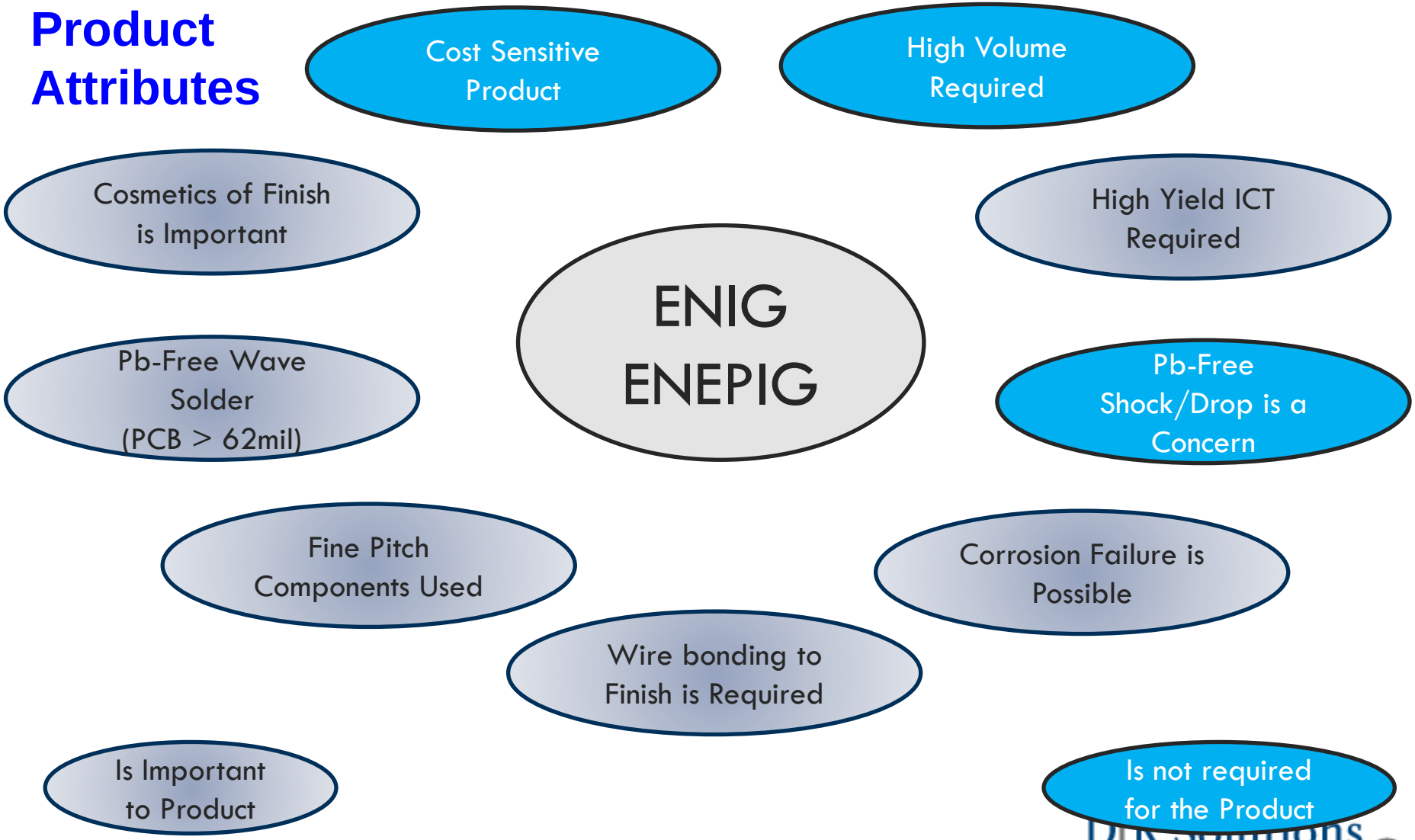
ImSn: Quality Issues & Failure Mechanisms

- Insufficient thickness.
  - **Decreases solderability during storage or after 2nd reflow – due to IMC growth through the thickness.**
- Solderability problems with Oxide thickness greater than 5 nm.
  - Excessive oxide thicknesses (50-100nm) periodically observed.
- Drivers of oxidation.
  - Exposure to humid conditions (>75%RH)
    - Greatly accelerates oxide growth through the creation of tin hydroxides.
      - Use sealed moisture/air tight wrapping for shipping and cool, low humidity storage.
  - Cleanliness of the raw board.
    - Contaminates breaks down self-limiting nature of tin oxides.
    - Accelerates oxide growth.



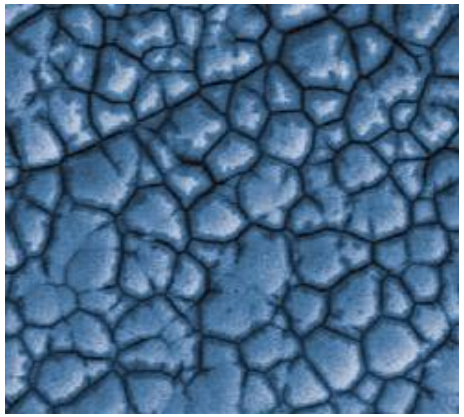


Surface Finish Selection Guideline

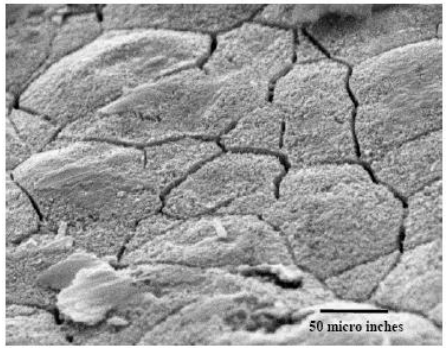


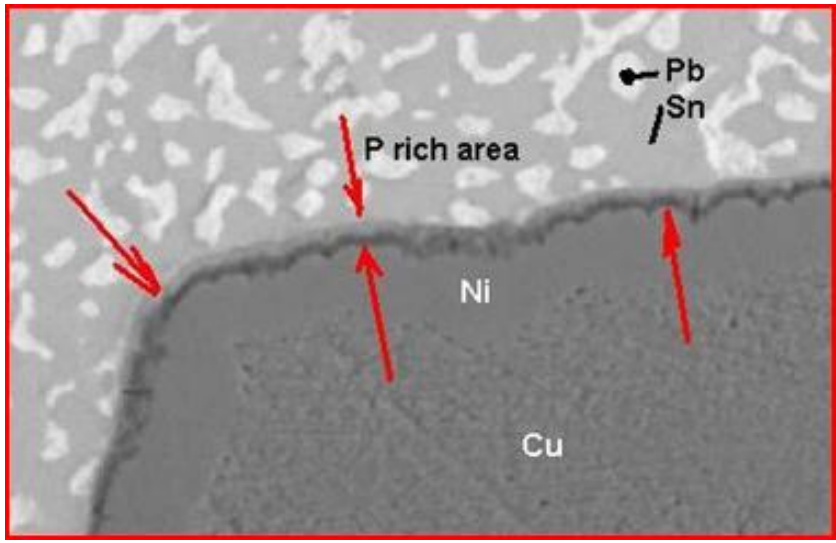
ENIG: Primary Reliability Risks

- Black pad drivers
  - Phosphorus content
    - High levels = weak, phosphorus-rich region after soldering
    - Low levels = hyper-corrosion (black pad) Insufficient Phosphorous will not prevent corrosion during the highly acidic immersion gold (IG) process.
  - Cleaning parameters
  - Gold plating parameters
  - Bond pad designs
- Causes a drop in mechanical strength
  - Difficult to screen
  - Can be random (e.g., 1 pad out of 300)
- Ni-Sn intermetallic produces a brittle interface when used with SAC solder.



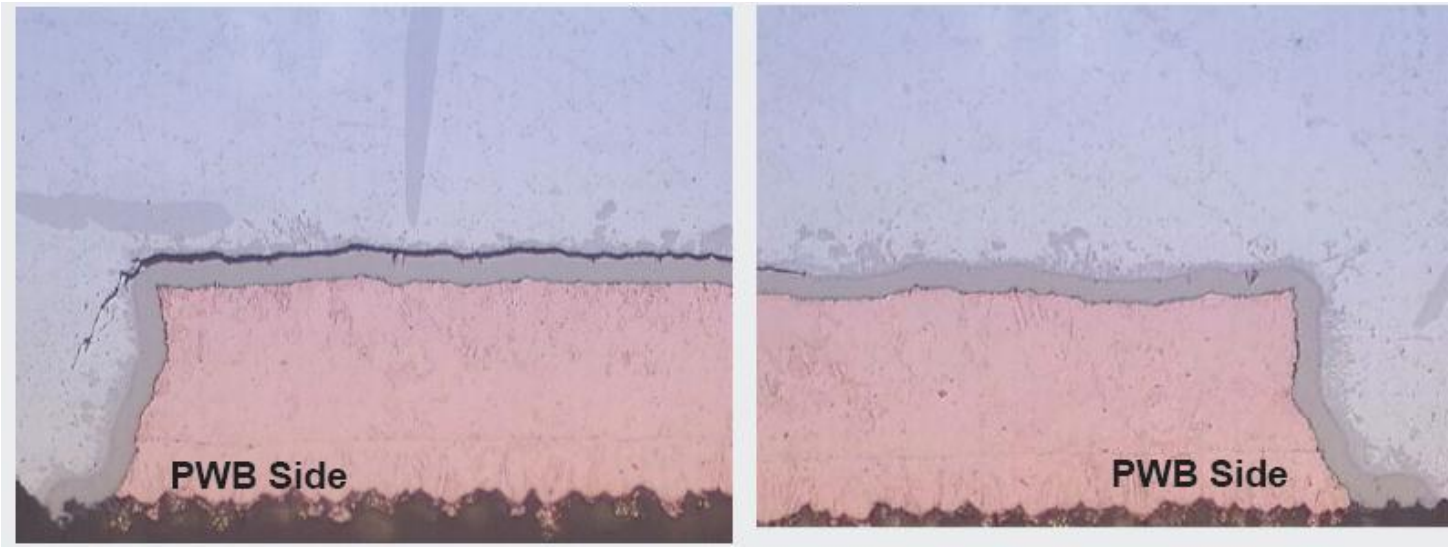
Images of Black Pad





Phosphorus-Rich Dark Streak

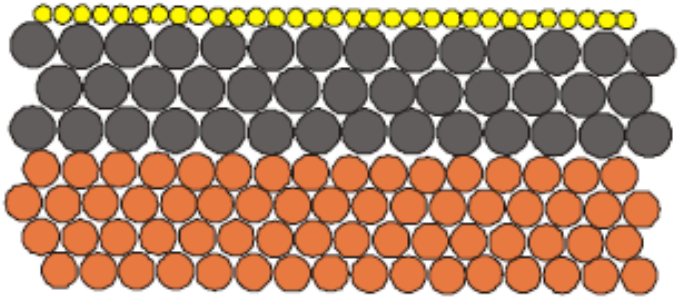
ENIG - Ni Interface Issues w/ SAC



Brittle SnNi intermetallics fail more easily with a high modulus LF solder ball. These cracks resulted from product handling.

Electroless Nickel/Immersion Gold (ENIG)

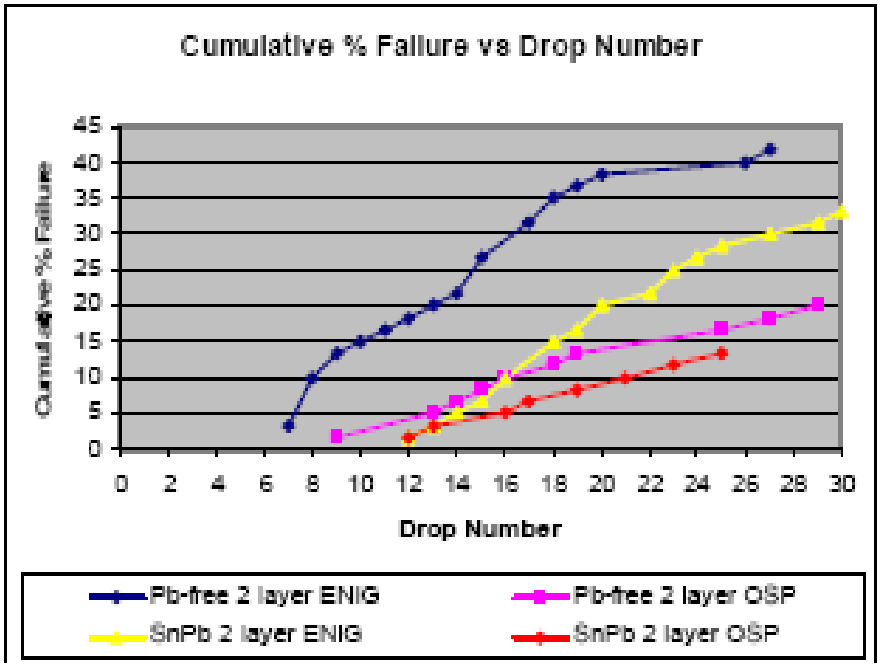
- Two material system.
  - Defined by IPC-4552 Specification for Electroless Nickel/Immersion Gold.
  - Electroless nickel.
    - 3 – 6 microns
  - Thin Immersion gold top coat
    - 0.08-0.23 microns

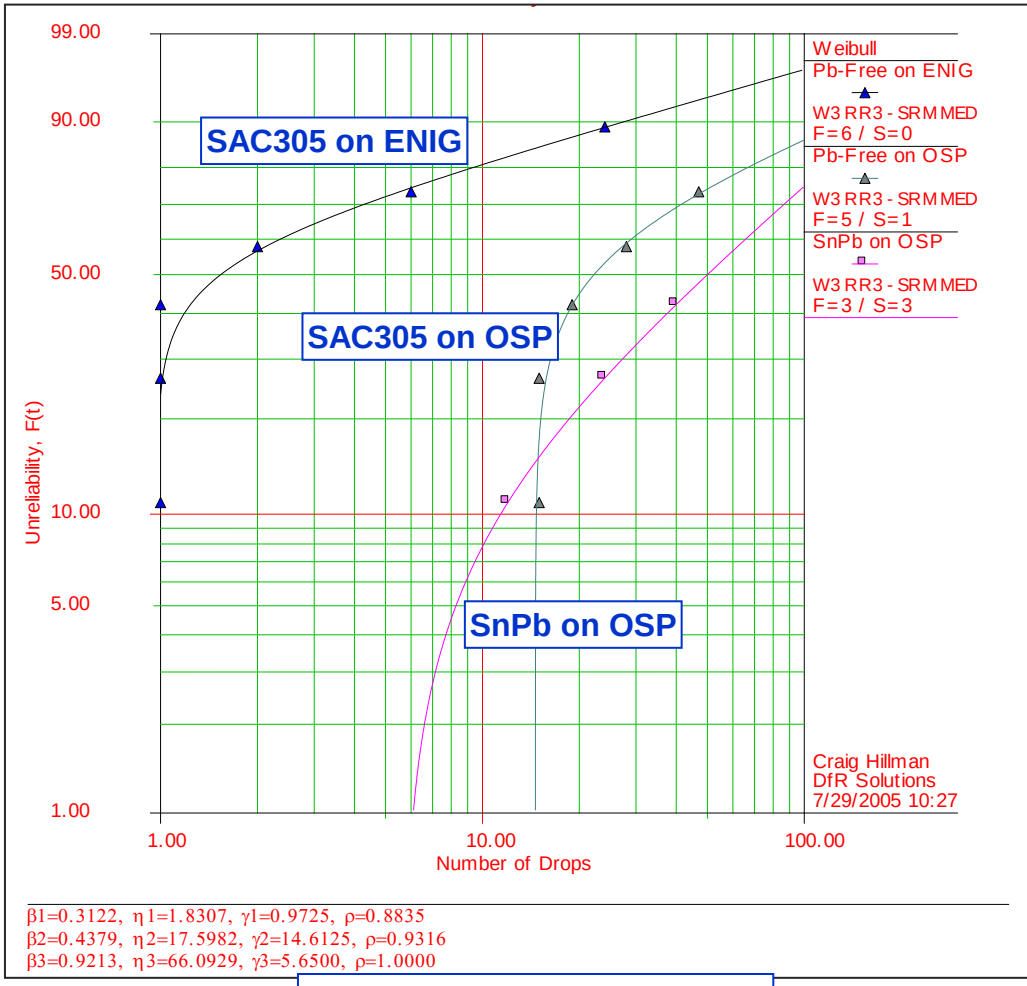


- Benefits
  - Excellent flatness and long-term storage (shelf life).
  - Excellent oxidation resistance and wetting properties.
  - Robust for multiple reflow cycles,
  - Supports alternate connections (wirebond, separable connector) & electrical testability.
  - Moderate costs.
  - Gold readily dissolves into solder and does not tarnish or oxidize making it an excellent choice for a surface finish.
    - But gold cannot be directly plated onto copper, since copper diffuses into gold, which allows the Cu to reach the surface and oxidize which reduces solderability.
    - Nickel is serves as a barrier layer to copper, the thin gold coating protects the nickel from oxidizing.

ENIG: Mechanical Shock with SAC305 solder

- ENIG Less Robust than OSP.
- SAC less robust than SnPb
- Plating is an important driver
  - SnNi vs. SnCu intermetallics





35x35mm, 312 I/O BGA

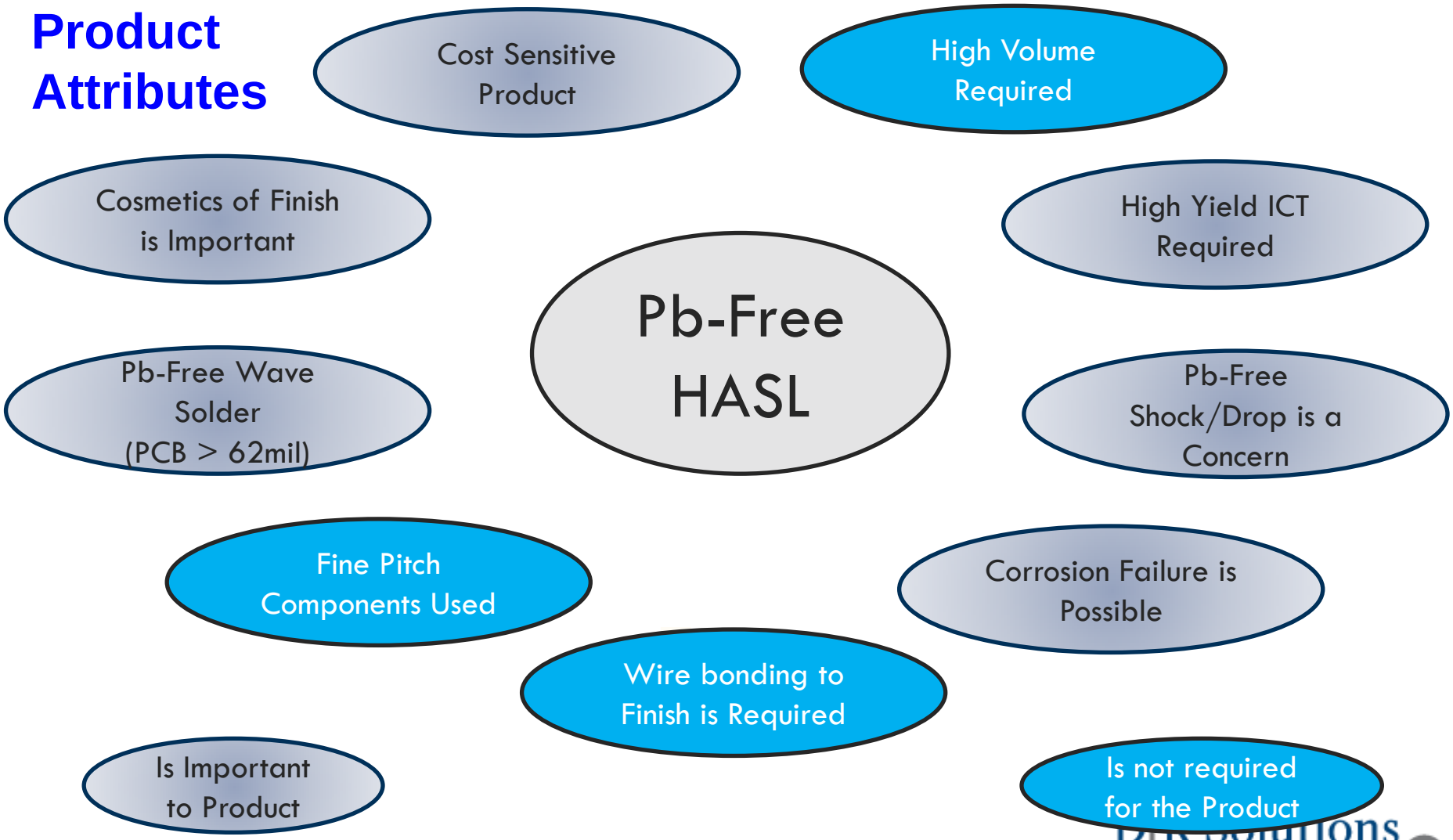
DfR Solutions

ENEPIG

Electroless Ni – Electroless Pd – Immersion Au

- Addition of the electroless palladium layer provides two primary advantages.
  1. It prevents black pad (since gold bath doesn't come in contact with Ni).
  2. It enhances the wire bondability of the finish.
- Pd thickness is typically in the range 2-30 microinches.

Surface Finish Selection Guideline

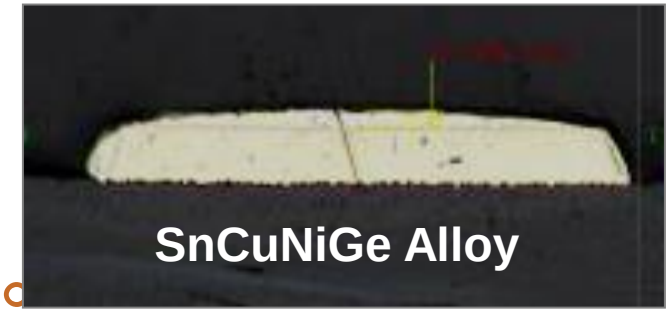


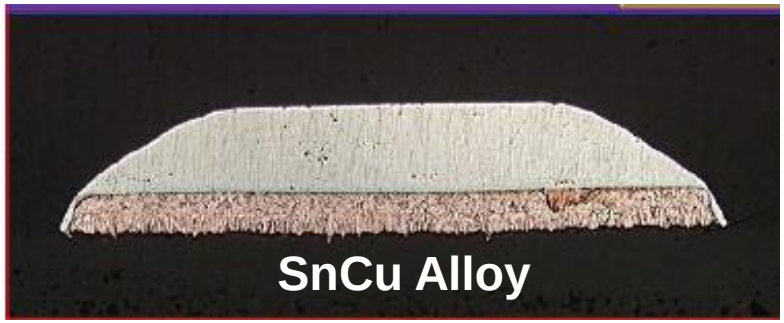
Pb-Free HASL (Hot Air Solder Leveling)

- Good choice when excellent solderability is required
  - Thick boards that require LF wave soldering.
  - Robust in multiple reflow cycles.
  - Long shelf life required
- Flatness not as good as other finishes (but an improvement over SnPb HASL).
  - Could potentially be a problem with very fine pitch components
- High volume equipment is not yet in production.
  - Horizontal LF lines are available but few are in production since high volume demand is needed to make them cost effective.

Pb-Free HASL: Ni-modified SnCu

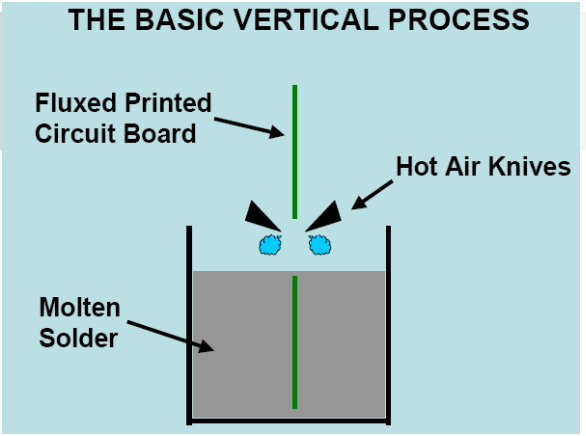
- Alloy selection is critical.
  - Sn-Cu will result in high Cu dissolution and poor planarity.
  - SnCuNiGe provides high fluidity and reduced Cu dissolution.





- Ro
  - **Cu** creates a eutectic alloy with lower melt temp (227C vs. 232C), forms intermetallics for strength, and reduces copper dissolution
  - **Ni** suppresses formation of β-Sn dendrites, controls intermetallic growth, grain refiner
  - **Ge** prevents oxide formation (dross inhibitor), grain refiner

LF HASL – Critical Parameters



Pre-Clean:

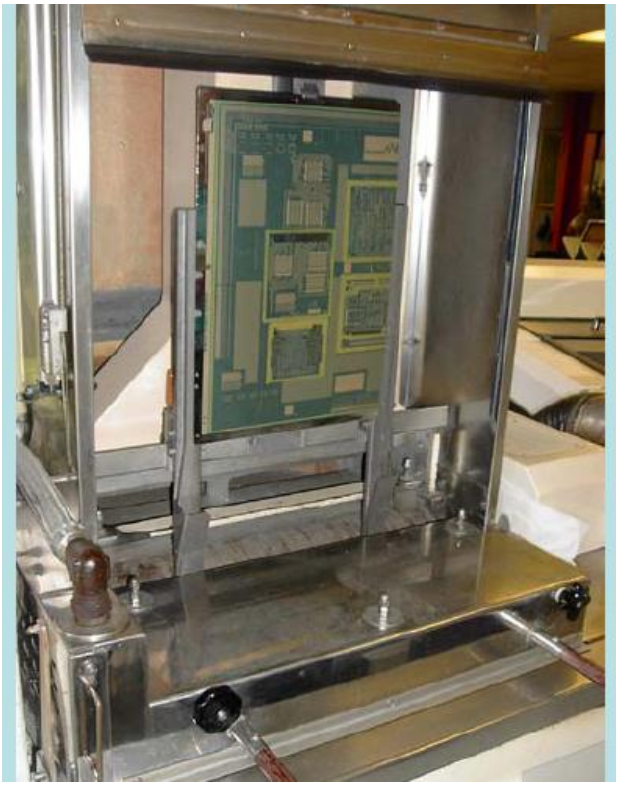
- Micro-etching rate
- Flux

HASL:

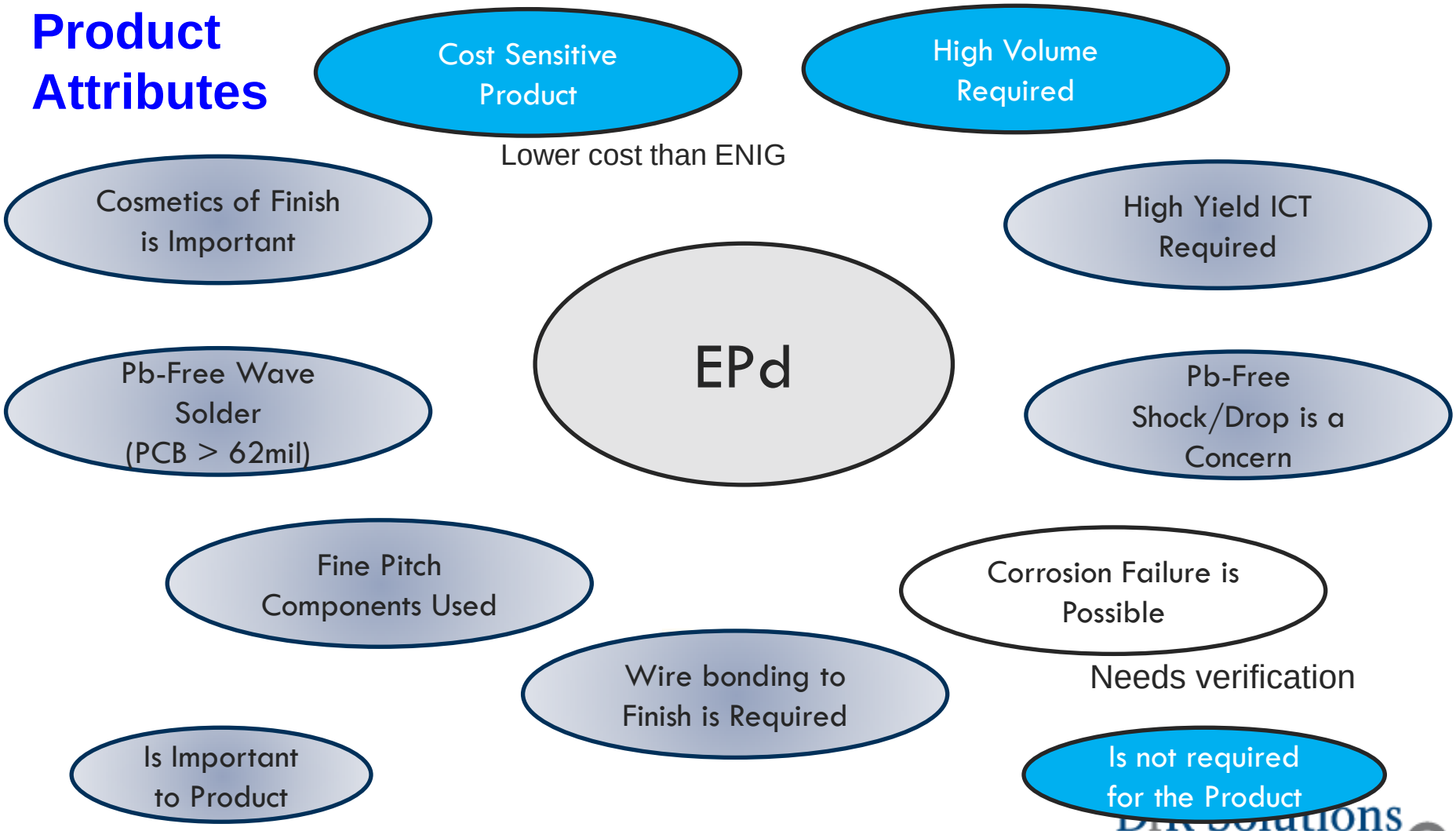
- LF Alloy
- Pot temperature (~265C)
- Front & Back air knife pressure
- Front & Back air knife angle
- Distance between air knife & PCB
- Lifting speed
- Dwell time (~ 2-4 sec)

Post-Clean:

- Final flux clean and rinsing

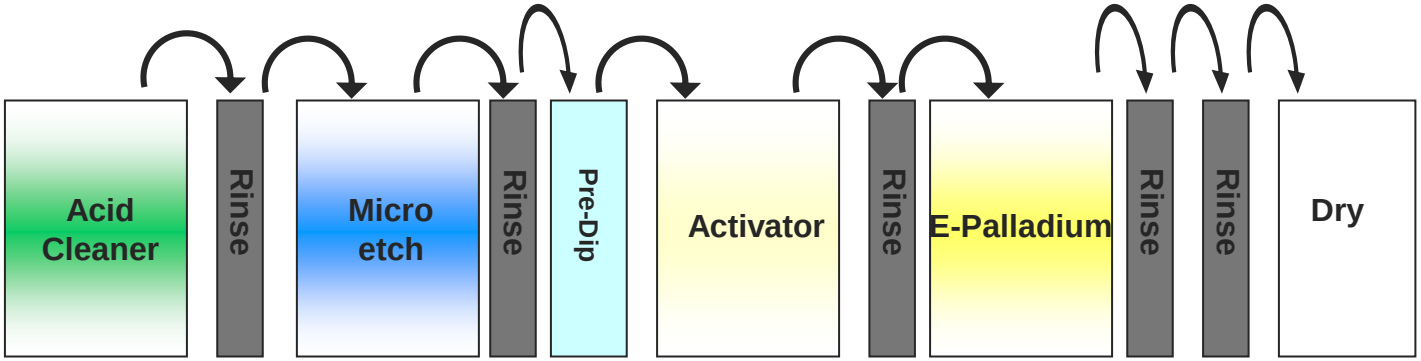


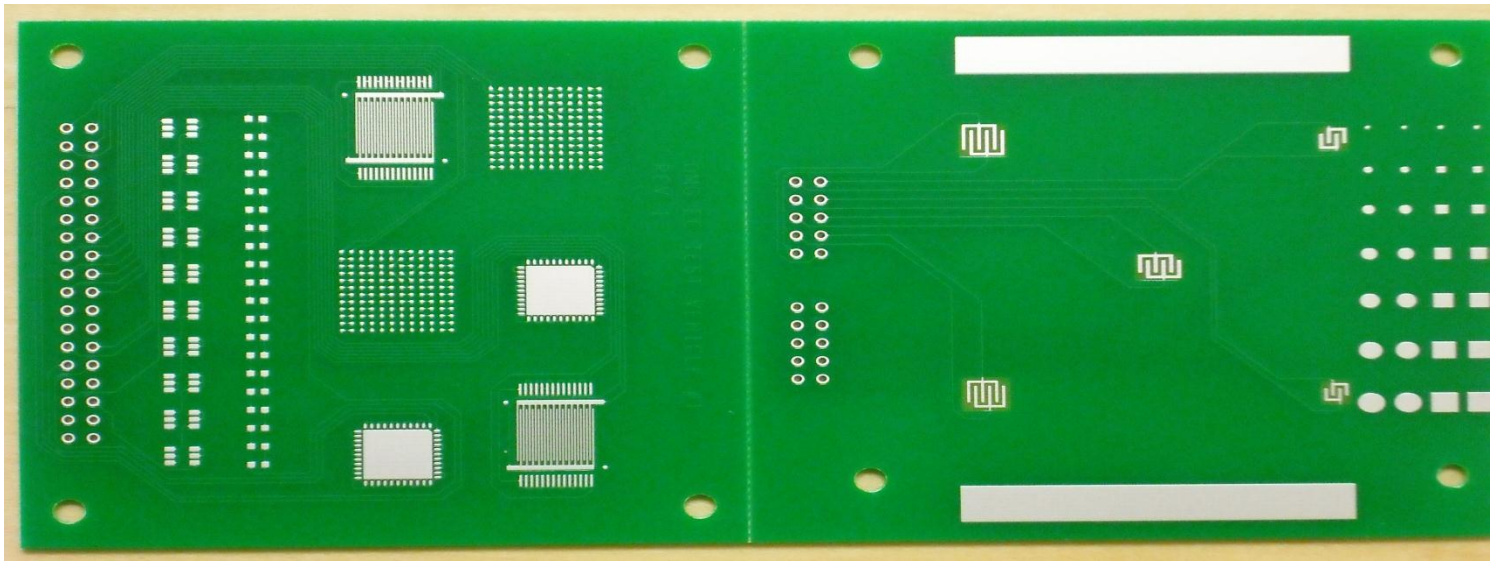
Newer Finishes to the Market



Electroless Pd

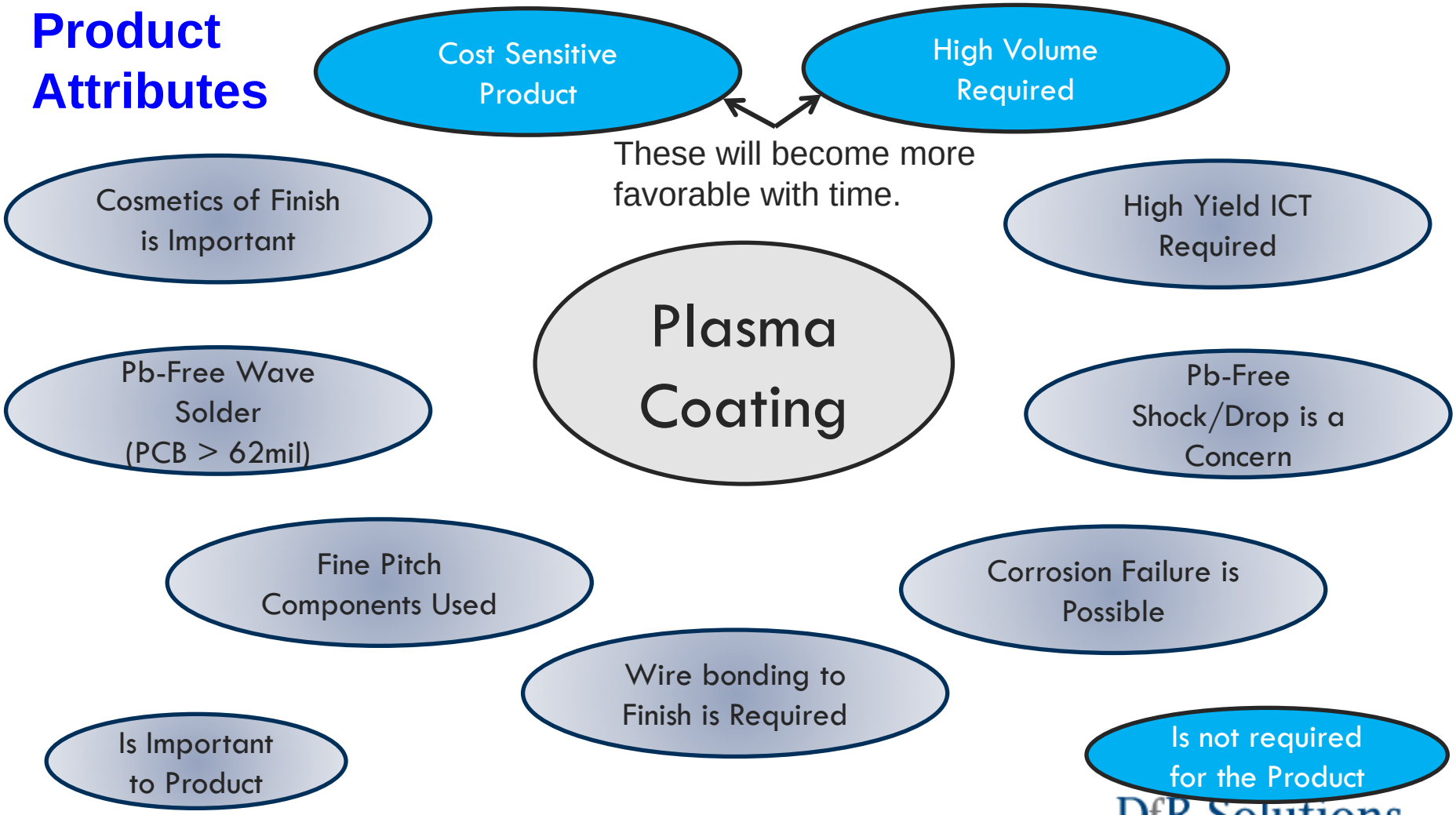
Process Sequence





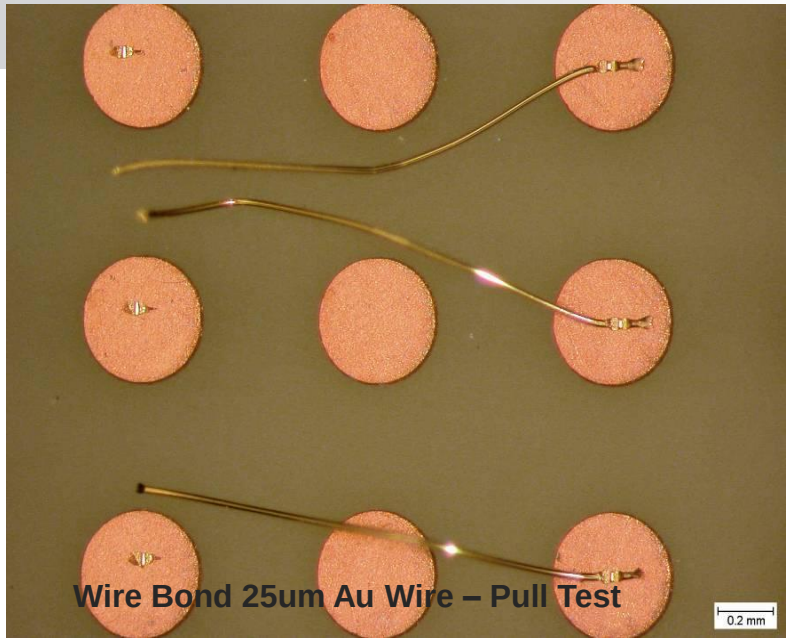
Courtesy of OMGI

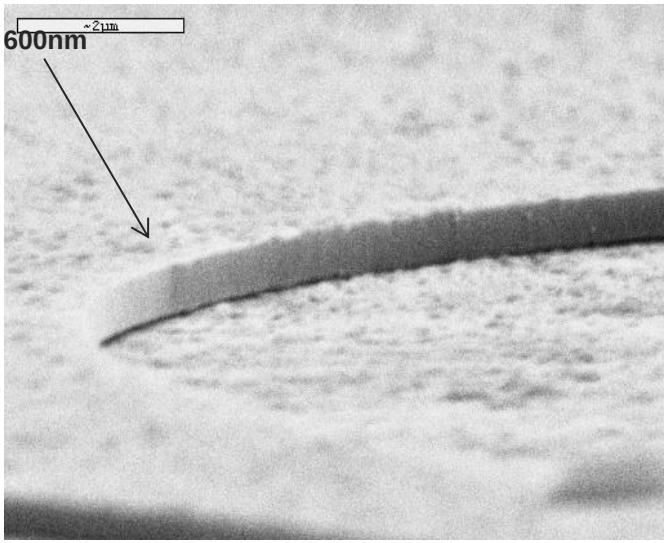
Newer Finishes to the Market

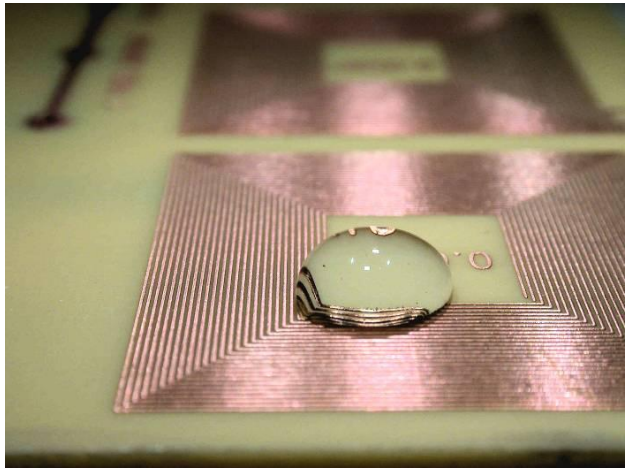


Plasma Coated Finish

- Coated in plasma chamber.
- Many panels coated simultaneously.
- Film is 60 nm thick.
- Flux breaks through film at elevated temperature.
- Hydrophobic and acid resistant







Courtesy of Semblant

Examples of Best Application Fits

- OSP (but must address ICT issues)
  - Hand held electronics
  - Notebook computers
  - Basic desktop computers
  - Basic consumer electronics & power supplies
  - Simple Pb-free Medical or aerospace (thin PCBs)
- ENIG or ENEPIG
  - SnPb medical and aerospace
  - Pb-free that is not susceptible to shock

Examples of Best Fits

- ImAg
  - Fully enclosed hand held electronics
  - Basic consumer electronics – low power and airflow
- ImSn
  - Simple consumer electronics (not fully enclosed)
  - Simple medical or aerospace applications (1 side)
  - Low to moderate volume peripheral components
- LF HASL
  - Thick LF PCBs going into business environments (servers, telecom equipment)
  - Complex Pb-Free medical or aerospace?

What to do if there is no SF fit?

- If no SF fits your specific requirements, design modifications may be required and tradeoffs made.
- For example, I need low cost, high volume, corrosion resistant, with good ICT capability.
  - One solution might be to use ImAg but plug the vias with soldermask to protect from corrosion (but some cost is sacrificed).
  - Another is to use OSP but implement cleaning to remove flux residue for probing (cost is again sacrificed).

Example

- Another example might be the desire to use ENIG for a Pb-free product where shock is a concern.
  - One solution might be to underfill critical components sensitive to shock (cost adder).
  - Another might be to dampen the shock by better design of the enclosure (possible cost adder).

Summary

- The surface finish you select will have a large influence on quality, reliability and cost.
- It is a complex decision that impacts many areas of the business.
- Select a finish that optimal for the business (and not just one function).
- Know that there are engineering tricks to improve on weak areas of each finish.
- Stay current in this field because new developments continue to be made.

Summary

- To avoid design mistakes, be aware that functionality is just the beginning. Design reliability in!
- Be aware of industry best practices
- Maximize knowledge of your design as early in the product development process as possible
- Practice design for excellence (DfX)
  - Design for manufacturability
  - Design for sourcing
  - Design for reliability
  - Design for environment

Conclusions

- Design for Reliability is a valuable process for lowering cost, reducing time-to-market, and improving customer satisfaction
- PoF is a powerful tool that can leverage the value of DfR activities
- Successful DfR / PoF implementation requires the right combination of personnel and tools and time limitations

Instructor Biography

- Cheryl Tulkoff has over 22 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She has held leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years is an ASQ Certified Reliability Engineer and a member of SMTA and iMAPS.

- She has a strong passion for pre-college STEM (Science, Technology, Engineering, and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.

Contact Information

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