Reliable Plated Through-Via Design and Fabrication

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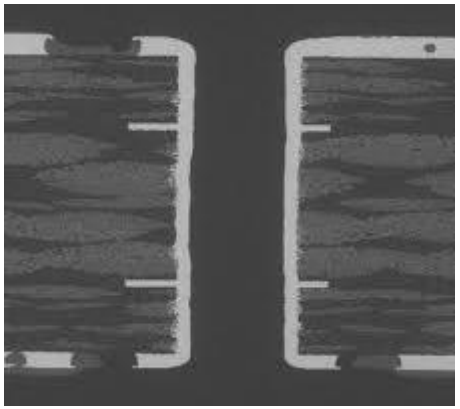
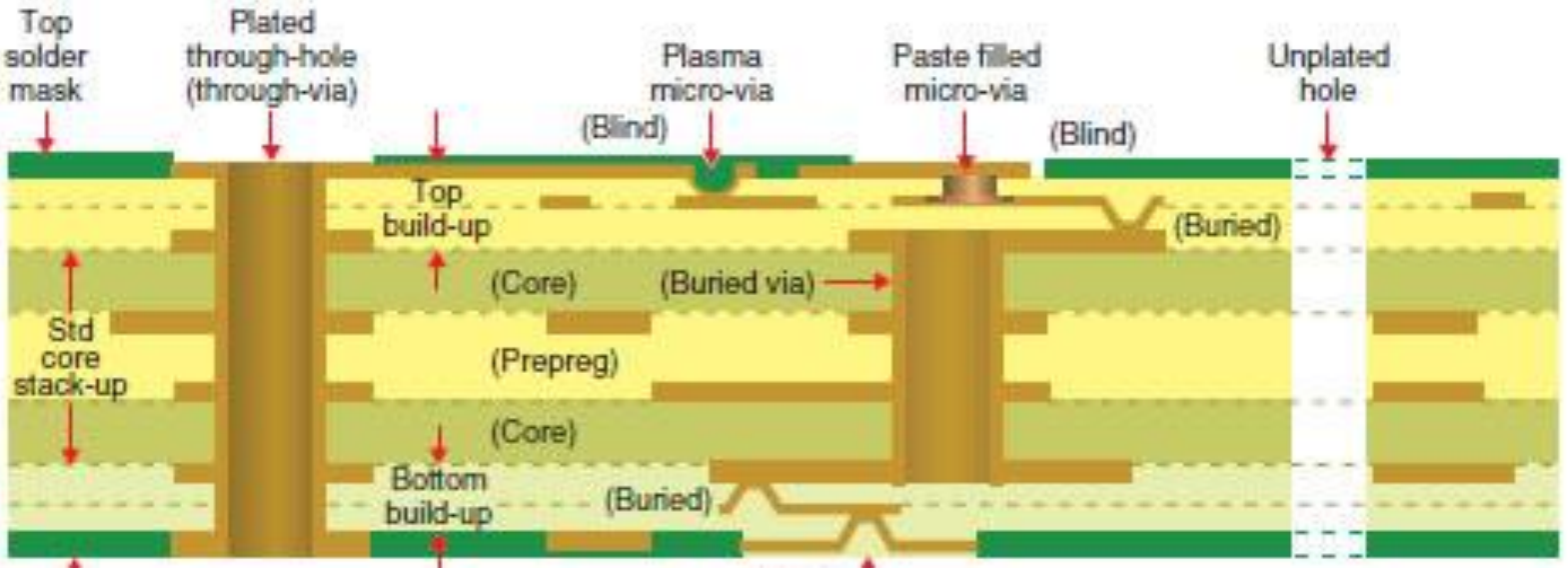
DfR Solutions
reliability designed, reliability delivered

What is a Plated Through Via?

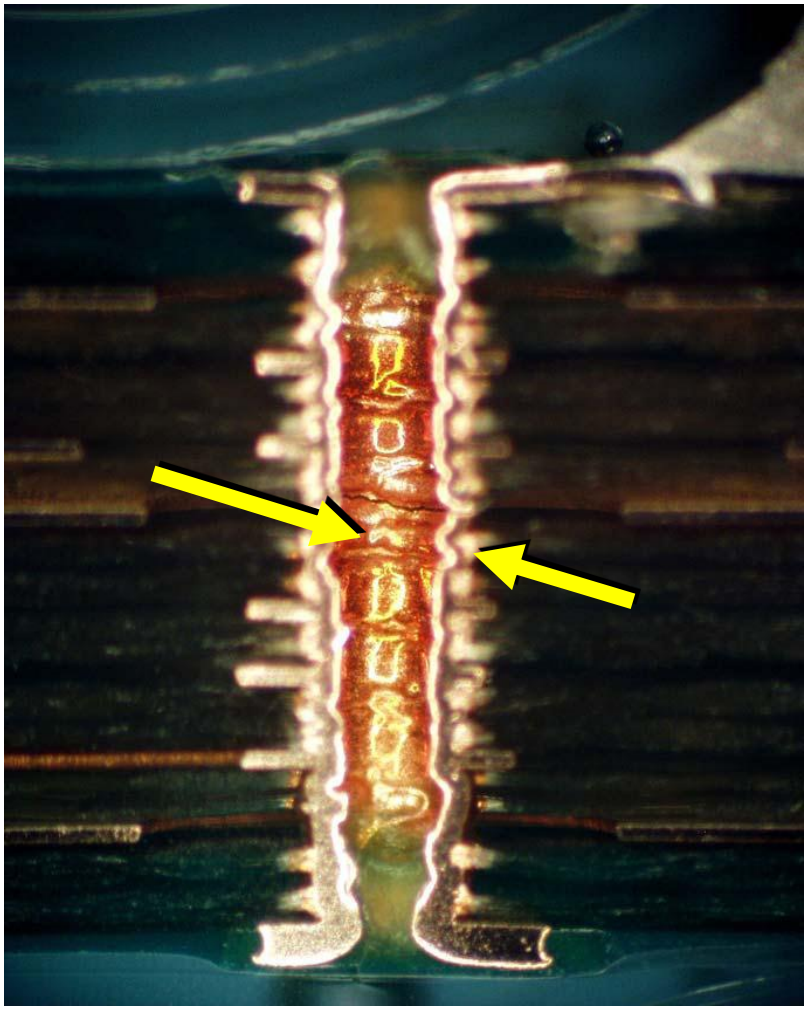
- A plated through via (PTV) is an interconnect within a printed circuit board (PCB) that electrically and/or thermally connects two or more layers
- PTV is part of a larger family of interconnects within PCBs





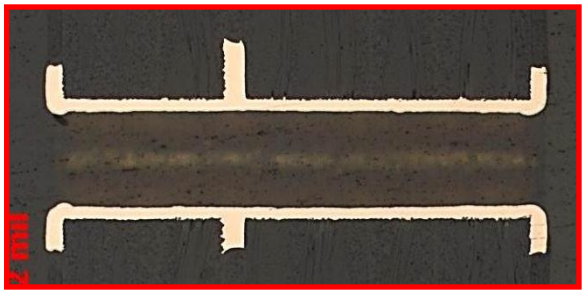
How do PTV's Fail?

- The dominant failure mode in PTV tends to be barrel fatigue
- Barrel fatigue is the circumferential cracking of the copper plating that forms the PTV wall
- Driven by differential expansion between the copper plating (~17 ppm) and the out-of-plane CTE of the printed board (~70 ppm)



How to Design a Reliable PTV?

PTH Architecture
(height / diameter)



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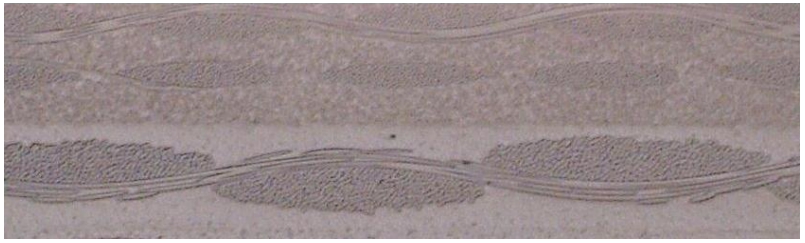
PCB Material
(modulus / CTE)



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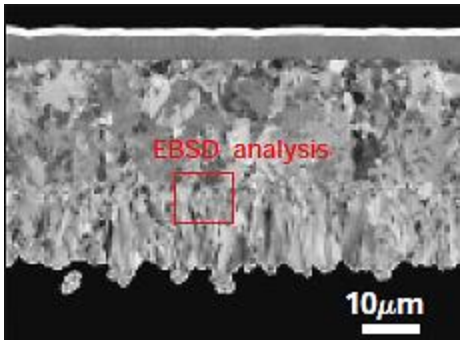
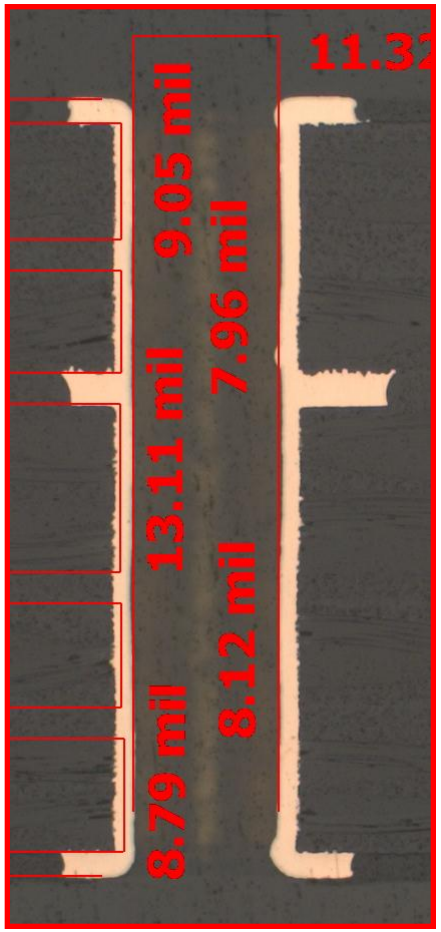
Plating
(thickness / material)

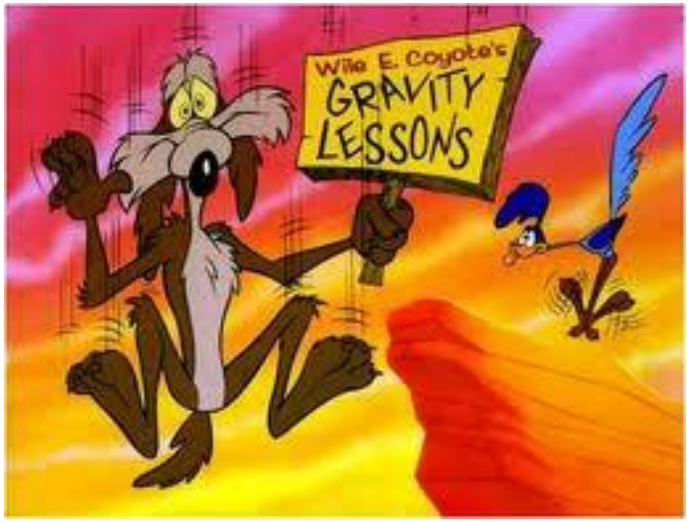


PTV Architecture

- PTV Height
  - Driven by the PCB thickness
  - 30 mil (0.75 mm) to 250 mil (6.25 mm)
- PTV Diameter
  - Driven by component pitch/spacing
  - 6 mil (150 micron) to 20 mil (500 micron)
- Key Issues
  - Be aware that PCB manufacturing has cliffs
  - Quantify effect of design parameters using IPC TR-579



The PTV Cliff



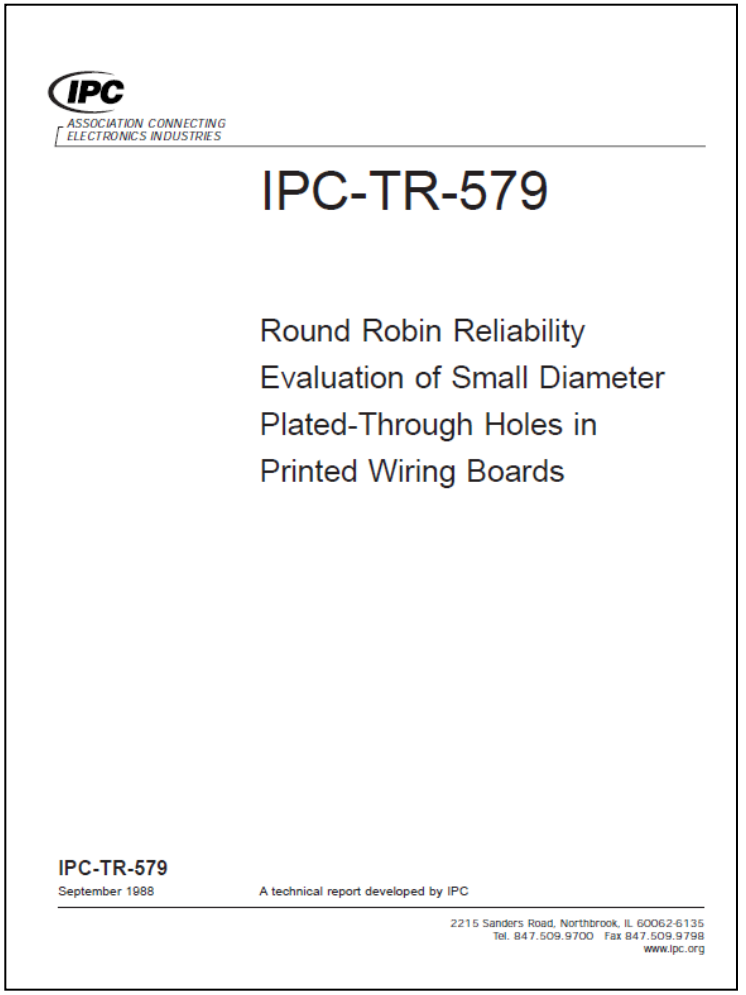
- Data from 26 PCB manufacturers
- Wide range of PCB designs
  - 6 to 24 layer
  - 62 to 125 mil thickness
- Results after six lead-free reflows
  - Initial defects segregated

Process Attribute	Hole/land (mils)	Count	Min	Q1	Median	Q3	Max
Yield Loss from Assembly Simulation (%) Threshold: Open	8 / 18	6	0.00	0.00	0.31	3.24	17.16
	10 / 20	15	0.00	0.00	0.00	1.13	4.60
	12 / 22	26	0.00	0.00	0.00	0.00	5.23
	13.5 / 23.5	26	0.00	0.00	0.00	0.00	4.09
	14.5 / 24.5	19	0.00	0.00	0.00	0.00	0.00
	16 / 26	11	0.00	0.00	0.00	0.00	0.00

Courtesy of CAT

IPC TR-579

- Round Robin Reliability Evaluation of Small Diameter (<20 mil) Plated Through Holes in PWBs
- Activity initiated by IPC and published in 1988
- Objectives
  - Confirm sufficient reliability
  - Benchmark different test procedures
  - Evaluate influence of PTH design and plating (develop a model)



Assessment of IPC-TR-579

- Advantages
  - Analytical (calculation straightforward)
  - Validated through testing
  - Provides guidance on relative influence of design/material parameters

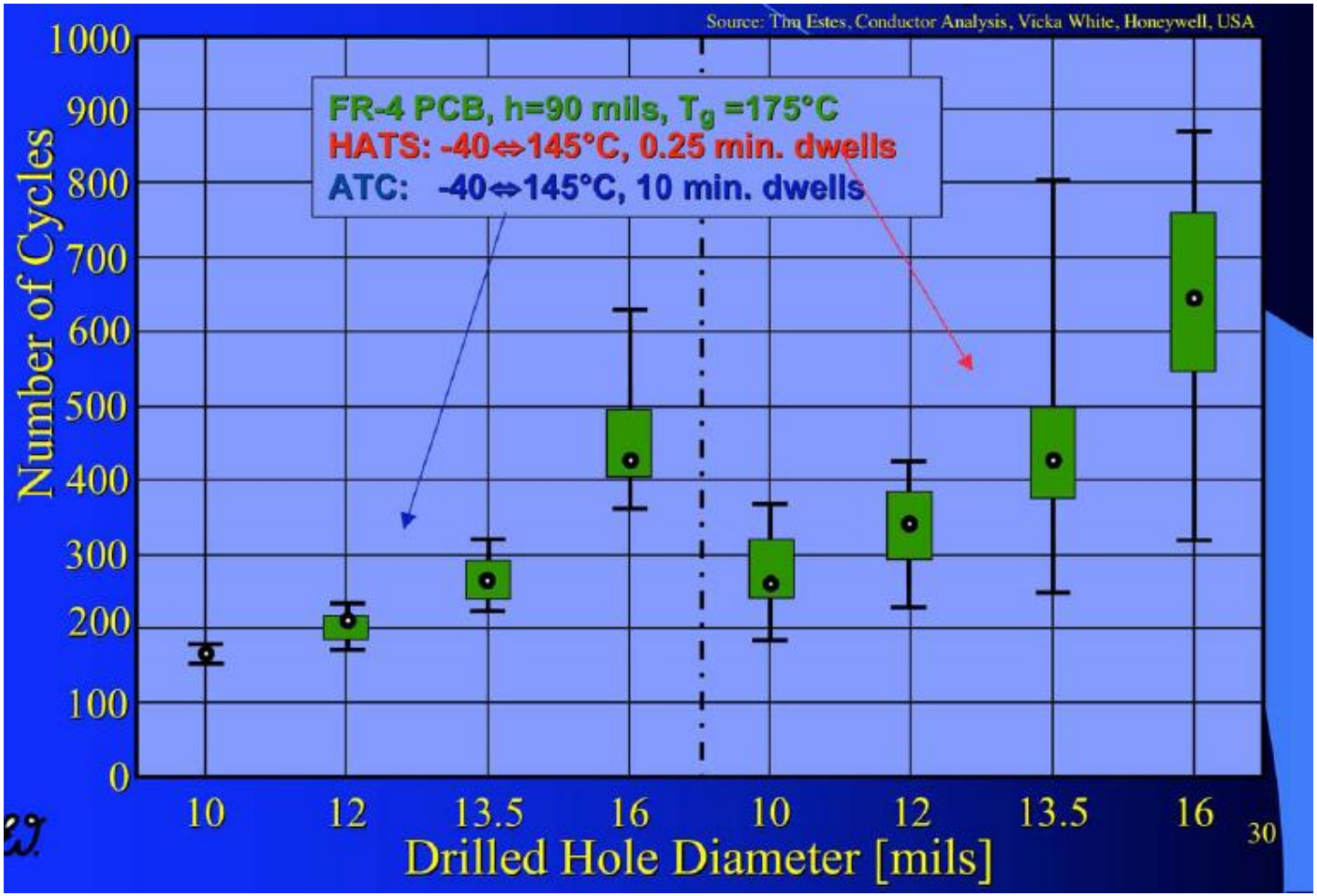
- Disadvantages
  - No ownership
  - Validation data is ~18 years old
  - Unable to assess complex geometries (PTH spacing, PTH pads)
    - Complex geometries tend to extend lifetime
  - Difficult to assess effect of multiple temperature cycles
    - Can be performed using Miner's Rule
  - Simplified assumptions (linear stress-strain above yield point)
  - How does one determine the quality index in the design phase?
  - Does not account for the effect of fill
  - Does not consider other failure modes (knee cracking, wall-pad separation, etc.)

The Effect of Design Parameters (Height / Diameter)

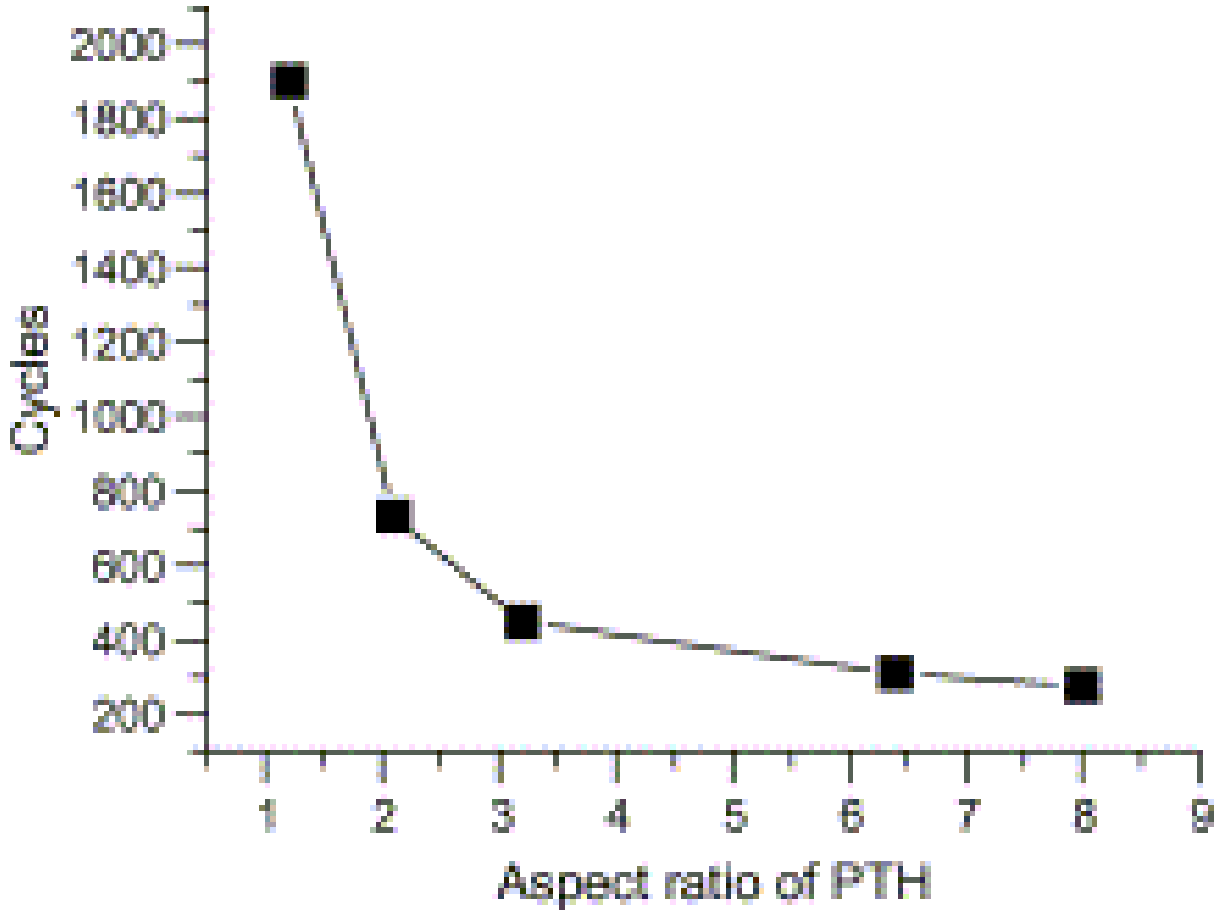
- Reduce the PTV Height (PCB Thickness)
  - Reduce laminate/prepreg thickness (2.7 to 4 mil is current limitation)
  - Results in minimal cost changes and minimal effect on design
  - Has the least effect on PTH reliability

- Increase PTV Diameter
  - Typically not an option due to spacing issues
  - An important, but significant effect (dependent on a number of other variables)
  - Example: Moving from 10 mil to 12 mil diameter on a 120 mil board, 50C temp cycle, will result in approximately 20% improvement

Effect of Design Parameters (cont.)



Effect of Design Parameters (cont.)



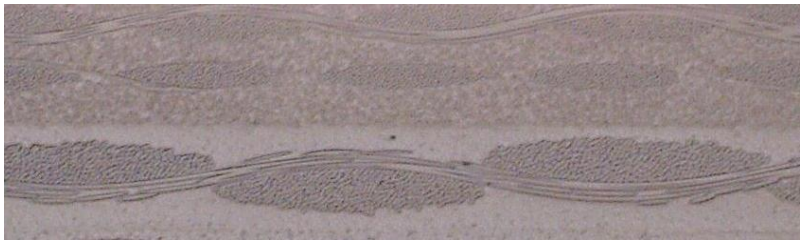
F. Su, et. al., Microelectronics Reliability, June 2012

PCB Materials and PTV Reliability

- Historically, two material properties of concern
  - Out-of-plane coefficient of thermal expansion (CTE_z)
  - Out-of-plane elastic modulus ('stiffness')(E_z)

- Key Assumption: No exposure to temperatures above the glass transition temperature (Tg)

- The two material properties (CTE and E) are driven by choices in resin, glass style, and filler



Laminate Datasheets

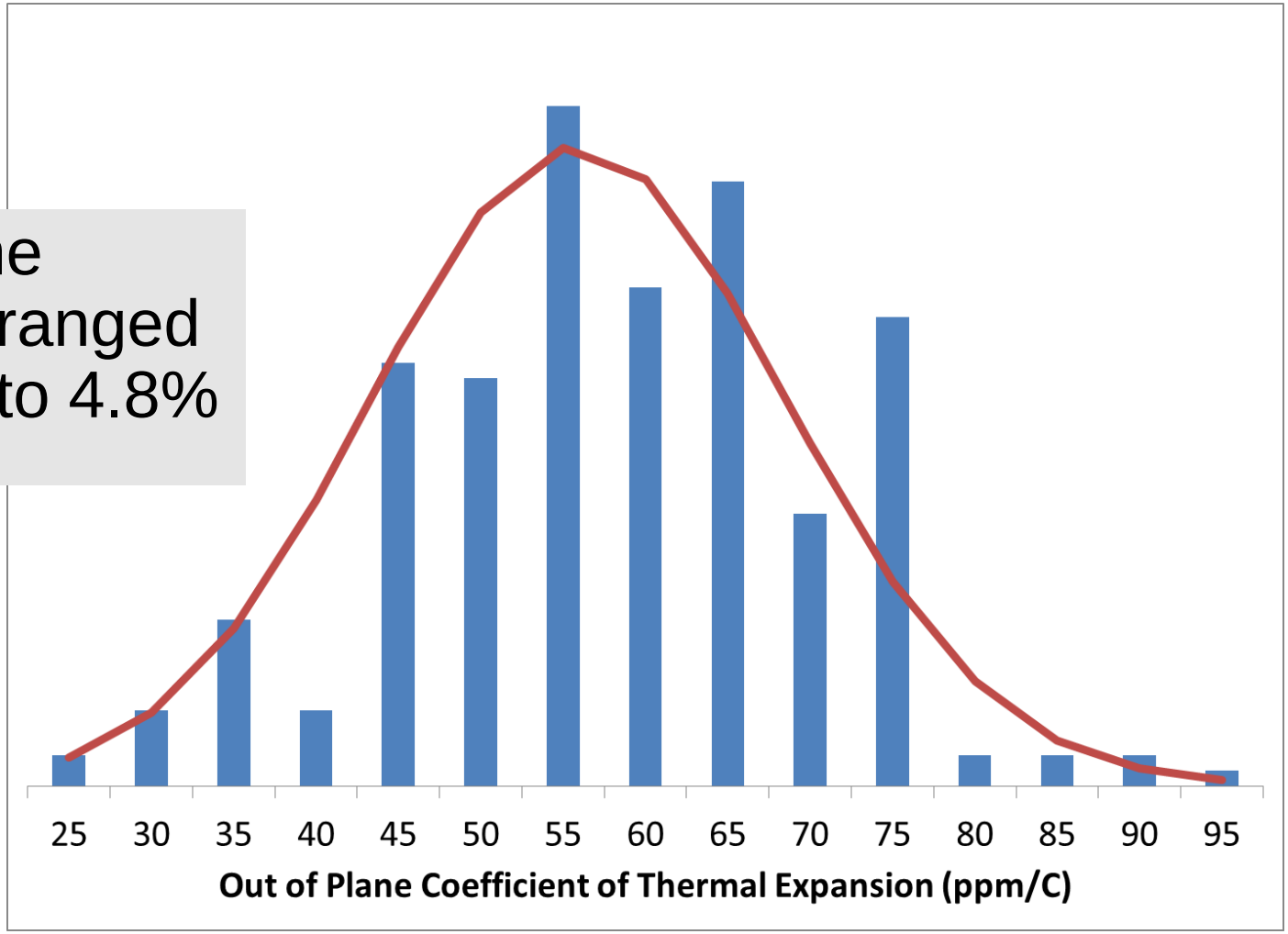
- Out-of-plane CTE (CTEz) is almost always provided on the laminate datasheet
  - Sometimes in ppm/C above and below the Tg
  - Sometimes in % between 50-260C

- Out-of-plane modulus (Ez) is almost never provided on the laminate datasheet
  - Requires calculation based on in-plane laminate properties,
    glass fiber properties, glass fiber volume fraction, and Rule-of-Mixtures / Halpin-Tsai models

$$1/E_{laminate} = V_{epoxy}/E_{epoxy} + V_{fiber}/E_{fiber}$$

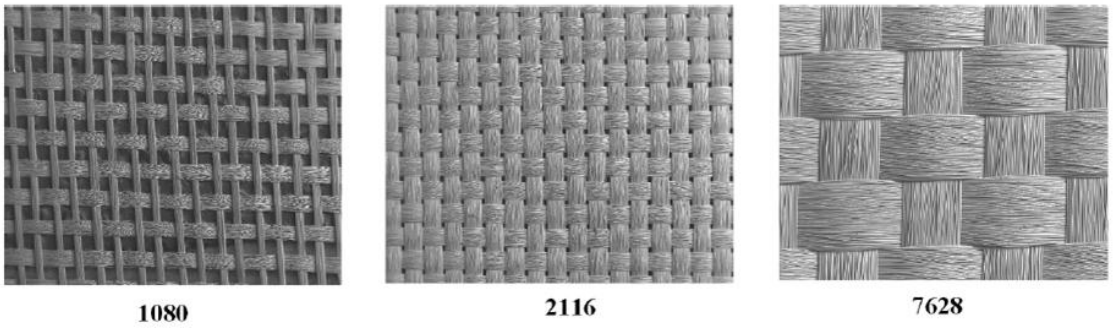
Survey of 300 Different FR-4 Datasheets

- Out-of-plane expansion ranged from 1.4% to 4.8%



Glass Style

- PCB laminates (and prepregs) are fabricated with a variety of glass styles



- Problem: All datasheet properties are for laminate with 7628 glass style
  - Most laminate (and all prepreg) in complex PCBs have a low volume fraction of glass (i.e., 1080 or 106)

Glass Style	Resin Volume Content	Fiber Volume Content
1027	0.86	0.14
1037	0.86	0.14
106	0.84	0.16
1067	0.84	0.16
1035	0.83	0.17
1078	0.82	0.18
1080	0.79	0.21
1086	0.78	0.22
2313	0.74	0.26
2113	0.72	0.28
2116	0.71	0.29
3313	0.71	0.29
3070	0.68	0.32
1647	0.66	0.34
1651	0.66	0.34
2165	0.66	0.34
2157	0.66	0.34
7628	0.64	0.36

Glass Style and CTE

Glass Style	Modulus of Elasticity Ez (MPa)	CTEz (ppm)
1027	4380.4	73.9
1037	4380.4	73.9
106	4478.2	72.3
1067	4478.2	72.3
1035	4528.7	71.5
1078	4580.3	70.7
1080	4742.7	68.4
1086	4799.3	67.6
2313	5040.4	64.4
2113	5170.2	62.8
2116	5237.6	62.0
3313	5237.6	62.0
3070	5450.9	59.7
1647	5603.1	58.1
1651	5603.1	58.1
2165	5603.1	58.1
2157	5603.1	58.1
7628	5764.0	56.5

Laminate Properties (cont.)

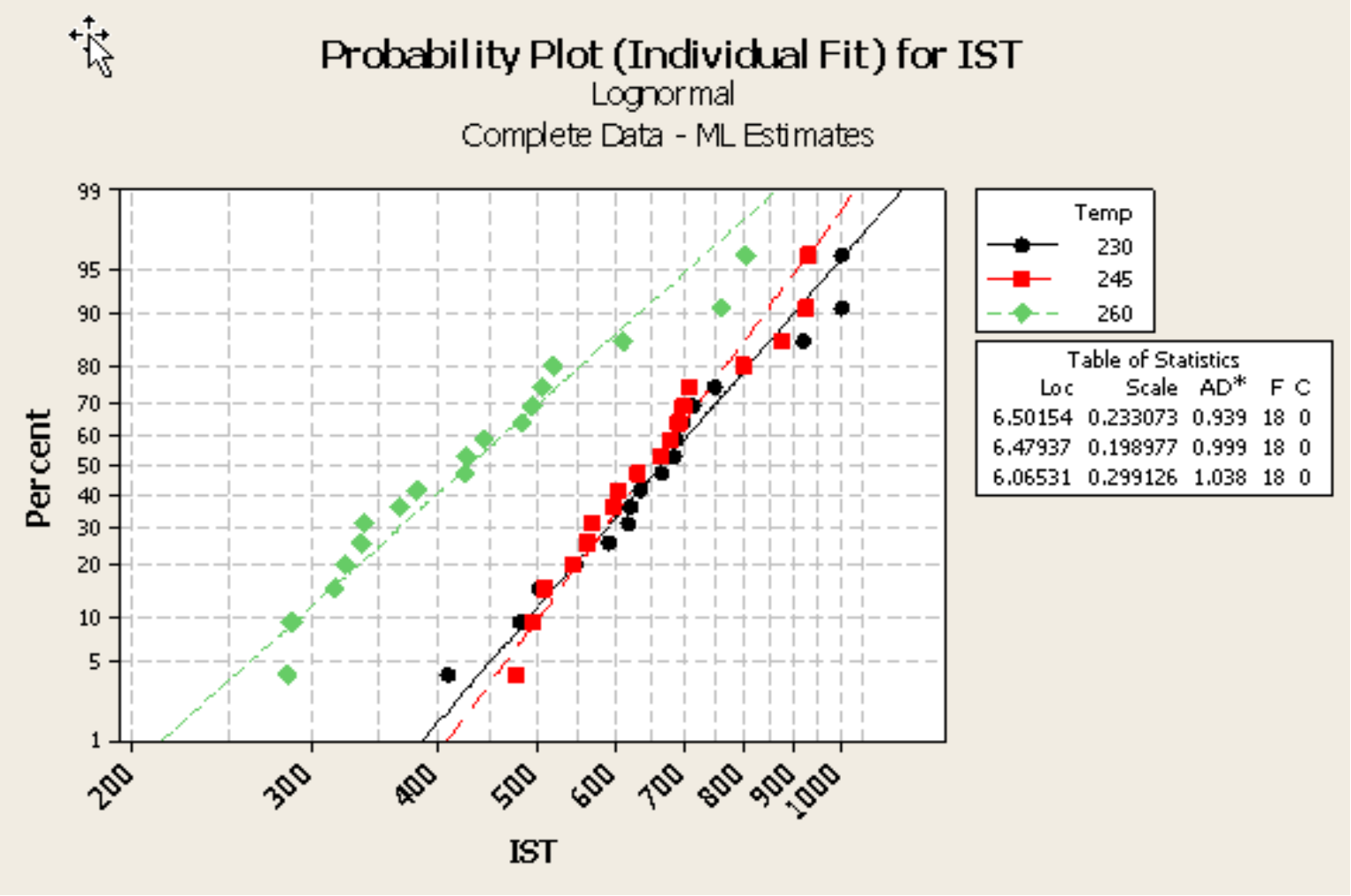
- More recently, additional laminate properties of concern due to Pb-free assembly
  - Glass transition temperature (Tg)
  - Time to delamination (T260, T280, T288, T300)
  - Temperature of decomposition (Td)

- Each parameter ‘supposedly’ captures a different material behavior
  - Higher number slash sheets (> 100) within IPC-4101 define these parameters to specific material categories

Thermal Parameters of Laminate

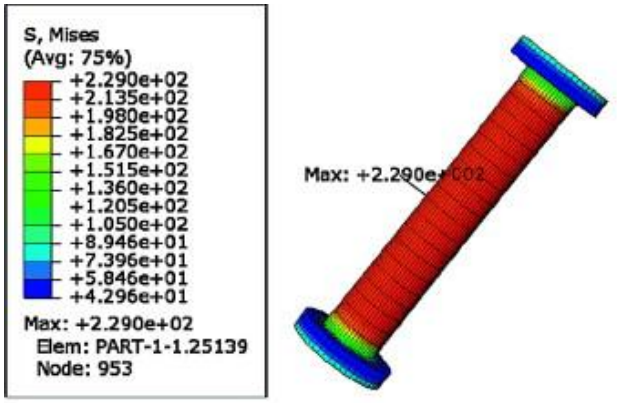
- Glass transition temperature (Tg) (IPC-TM-650, 2.4.24/2.4.25c)
  - Characterizes complex material transformation (increase in CTE, decrease in modulus)
- Time to delamination (T-260/280/288/300) (IPC-TM-650, 2.4.24.1)
  - Characterizes interfacial adhesion
- Temperature of decomposition (Td) (IPC-TM-650, 2.3.40)
  - Characterizes breakdown of epoxy material

PTV Degradation due to Assembly

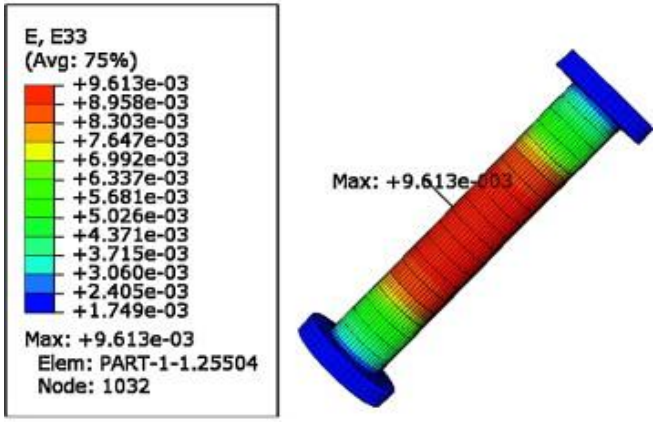


PCB Materials: Stackup

- Maximum stress in the PTV during thermal cycling tends to be in the middle of the barrel
- There is some concern that areas of high resin content in the middle of the barrel can be detrimental
- Non-functional pads (NFP)
  - Some debate as to their influence on barrel fatigue on higher aspect ratio PTV



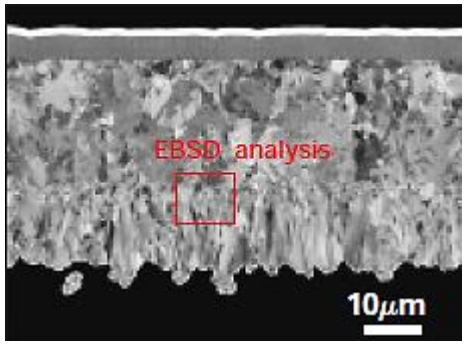
(a) The Mises stress field of PTH at 150°C



(b) The residual strain field of PTH after 3 cycles

F. Su, et. al., Microelectronics Reliability, June 2012

Plating (Thickness and Material Properties)

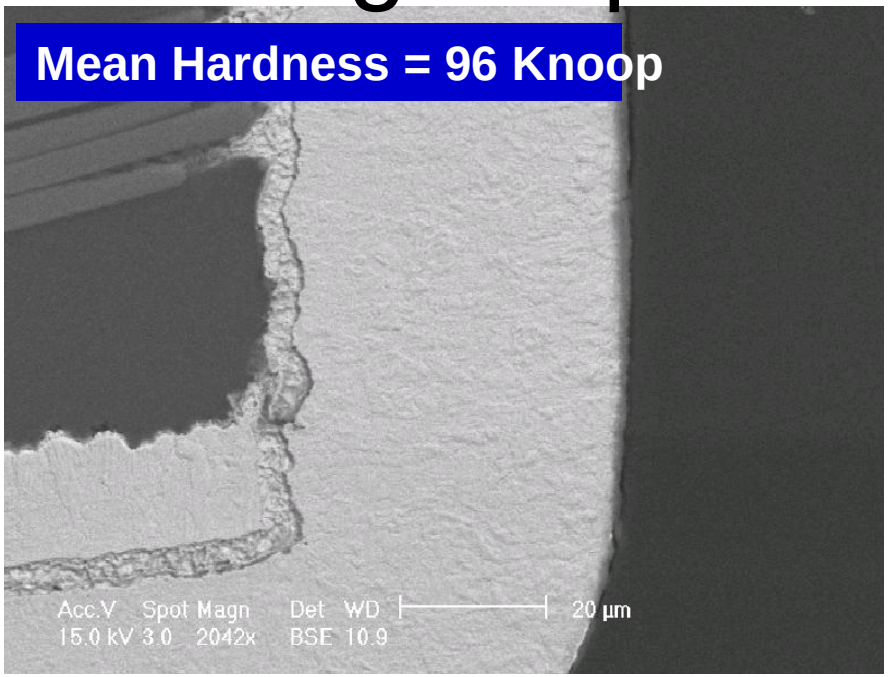


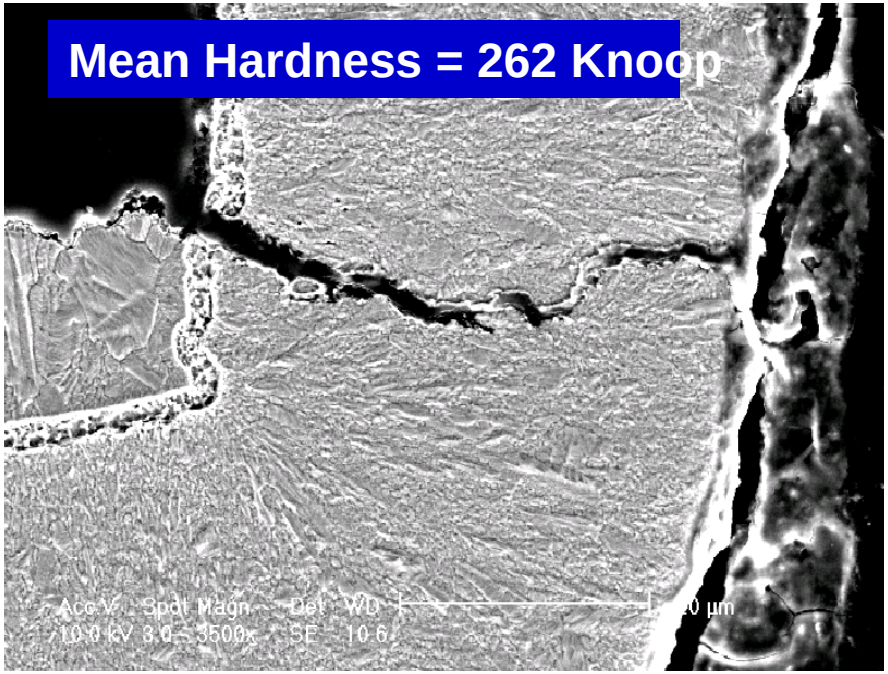
- Considered to be the number one driver for PTV barrel fatigue
- Classic engineering conflict
  - Better properties (greater thickness, higher plating strength, greater elongation) typically require longer time in the plating bath
  - Longer time in the plating bath reduces throughput, makes PCBs more expensive to fabricate
- PCB fabricators, low margin business, try to balance these conflicting requirements
  - Key parameters are thickness, strength, and elongation (ductility)

Plating Thickness

- Specifications tend to range from 0.8 mil (20 microns) to 1.0 mil (25 microns) to 1.2 mil (30 microns)
- Plating thickness can be less of an issue than previously
- New formulations to fill microvias can drive an accelerated plating process
  - Some PCB manufacturers, depending on the design and production volume, will plate the PTV almost closed

Post-Plating Measurements of Plating Properties

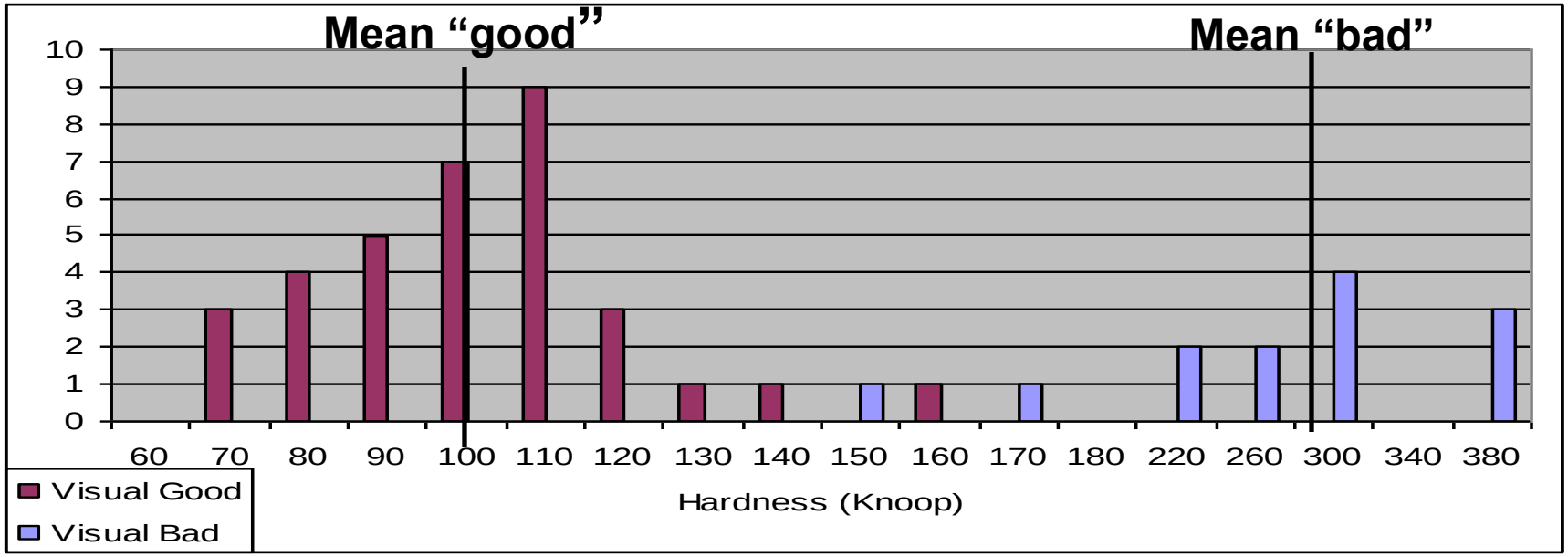




- One of the challenges of root-cause analysis of PTV cracking is the inability to directly measure strength/ductility of the plating
- Hardness and grain size measurements are potential substitutes

Post-Plating Measurements

- Hardness data indicated good separation between two populations
  - 100% correlation with cross section results
  - Boards with cracks had high hardness
  - Boards without cracks had low hardness



Hardness data generated by Mike Sosnowski of EMC

How to Manufacture a Reliable PTV?

Drilling

+

Plating

Hole preparation (desmear / electroless / direct metal) is important, but not as critical as drilling and electrolytic plating

Drilling

- Drill bit manufacturers tend to provide PCB manufacturers recommendations on key process parameters
  - Speeds and feeds
  - Stackup guidelines (number of PCBs of a given thickness that can be stacked during drilling)
  - Entry and exit material
  - Number of drilling operations before repointing
  - Number of repoints / sharpening

- There is no ‘right’ answer for process parameters
  - PCB manufacturer may buy a more expensive drill bit, but repoint more often

Plating (Electrolytic)

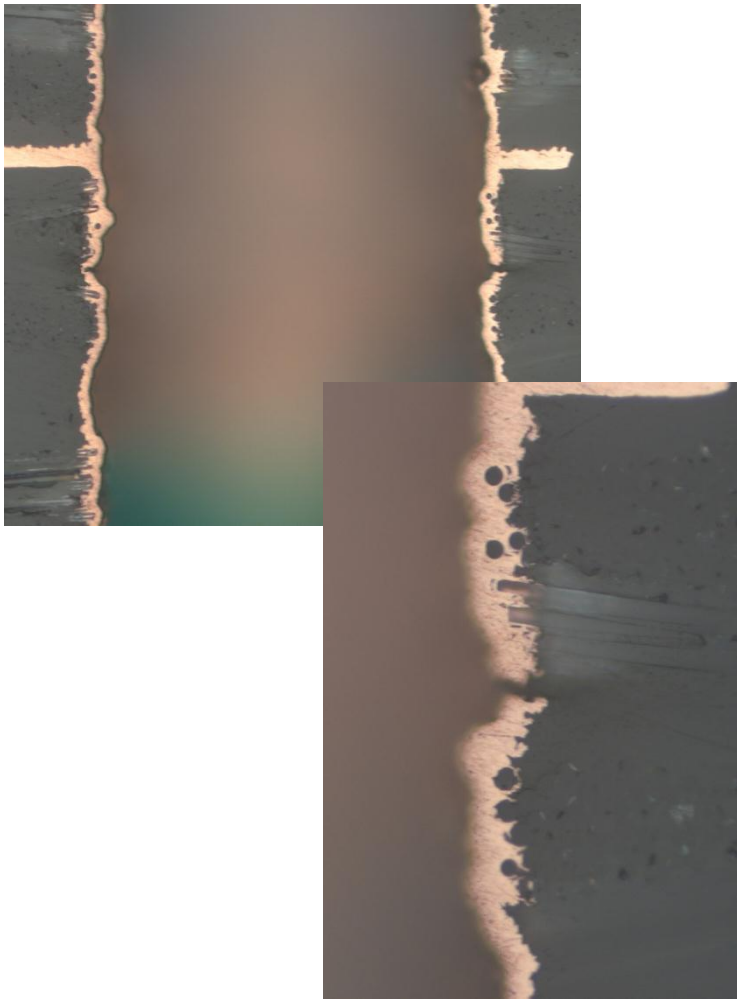
- Just like drilling, plating chemistry manufacturers tend to provide PCB manufacturers with guidance on process parameters and equipment
  - Many will provide a ‘turn-key’ installation
  - Can result in a lack of knowledge if PCB manufacturers do not perform their own DoE
- Large variation in plating chemistries, process and equipment

Copper Plating (cont.)

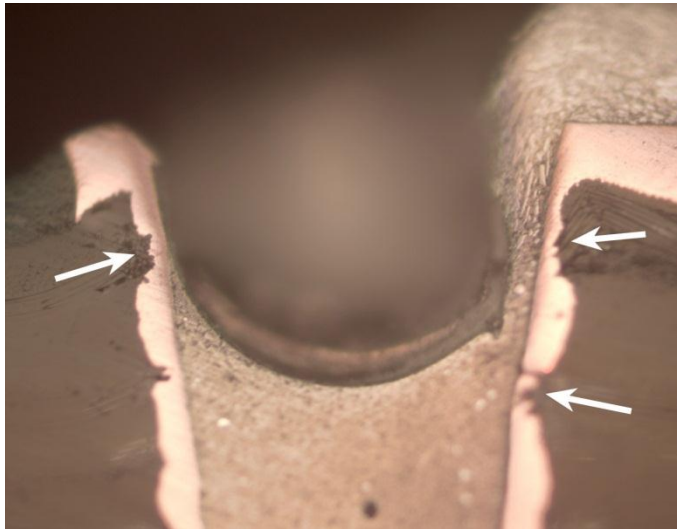
- Chemistry: Primarily sulfuric acid copper, but a number of proprietary additives (brighteners, levelers, etc.)
- Process: Primarily Flash / Strike / Panel followed by Pattern
  - Thick boards (e.g., 180 mil) with high aspect ratio (12:1) PTV can require additional plating steps (up to 3 to 4 total)
- Equipment: Primarily vertical, but increasing interest in horizontal conveyorized
  - DC or pulse reversed
  - Soluble vs. insoluble anodes

Insufficient Plating Thickness

- ANSI/IPC-A-600 requires an average plating thickness of 20 um, with isolated areas allowed to reach 15 um.
- Insufficient plating thickness is caused by either insufficient current/time in the copper plating bath or poor throwing power.
- When insufficient plating thickness is observed throughout the PTH, instead of just at the center, the root-cause is more likely insufficient current/time in the plating bath.

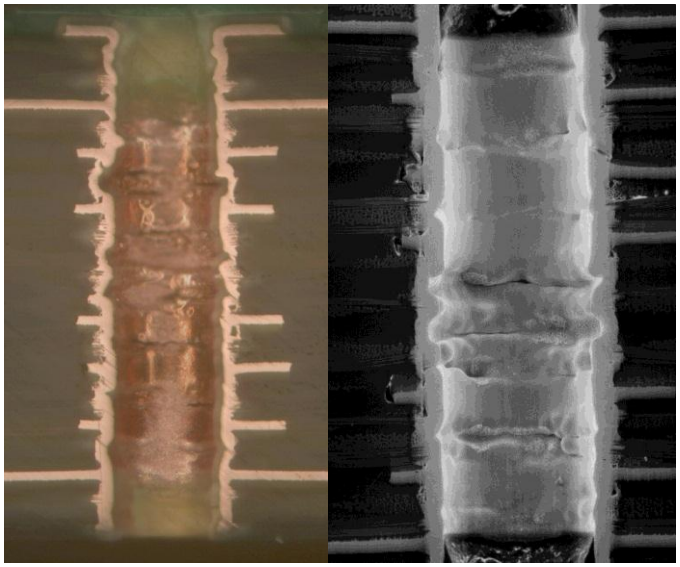


Glass Fiber Protrusion



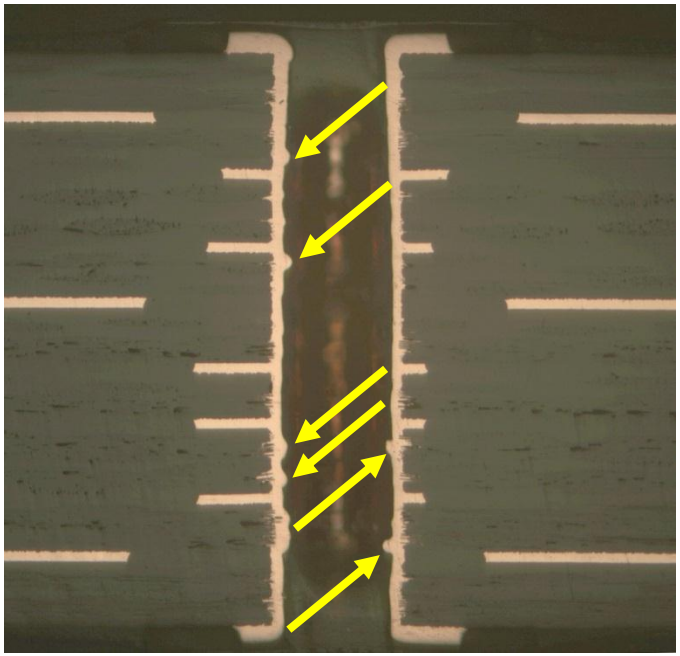
- Glass fiber protrusion into PTH walls affects PTH plating thickness and hence can contribute to PTH cracking.
- Glass fiber protrusion may be due to process control variabilities during hole drilling, hole preparation or application of flash copper.
- Glass fiber protrusion is allowed by IPC guidelines only if the min. plating thickness is met.

Plating Folds



- Plating folds create detrimental stress concentrations.
- Rough drilling or improper hole preparation can cause plating folds.
- Rough drilling can be caused by poor laminate material, worn drill bits, or an out-of-control drilling process.
- Improper hole preparation is due to excessive removal of epoxy resin caused by incomplete cure of resin system or a preparation process (desmear/etchback) that is not optimized.

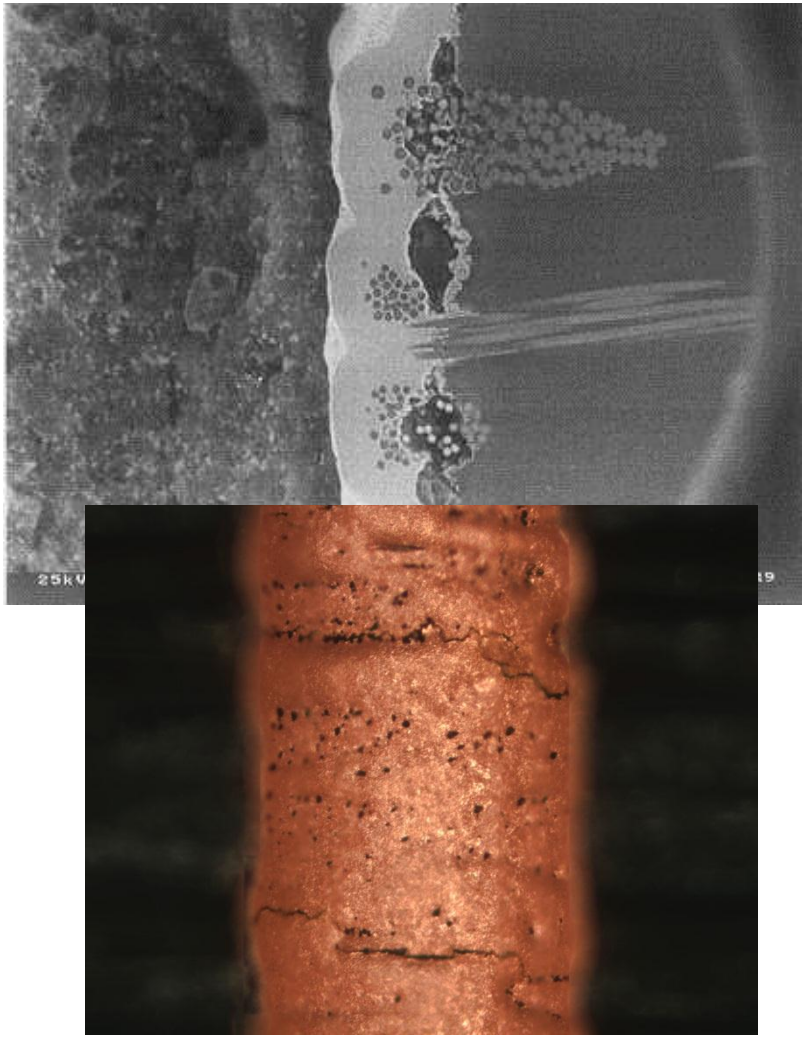
Plating Nodules



- Root causes of nodulation include poor drilling, particles in solution, solution temperature out of range, or brightener level in excess.
- The relatively straight hole walls and the lack of particles in the nodules seemed to suggest the later two as root cause.
- The presence of plating nodules can be detrimental to high reliability.
- Plating nodules create highly stressed areas in the plating wall and can possibly reduce lifetime under temperature cycling.
- ANSI/IPC-A-600 states that nodules are acceptable if the hole diameter is above the minimum specified.

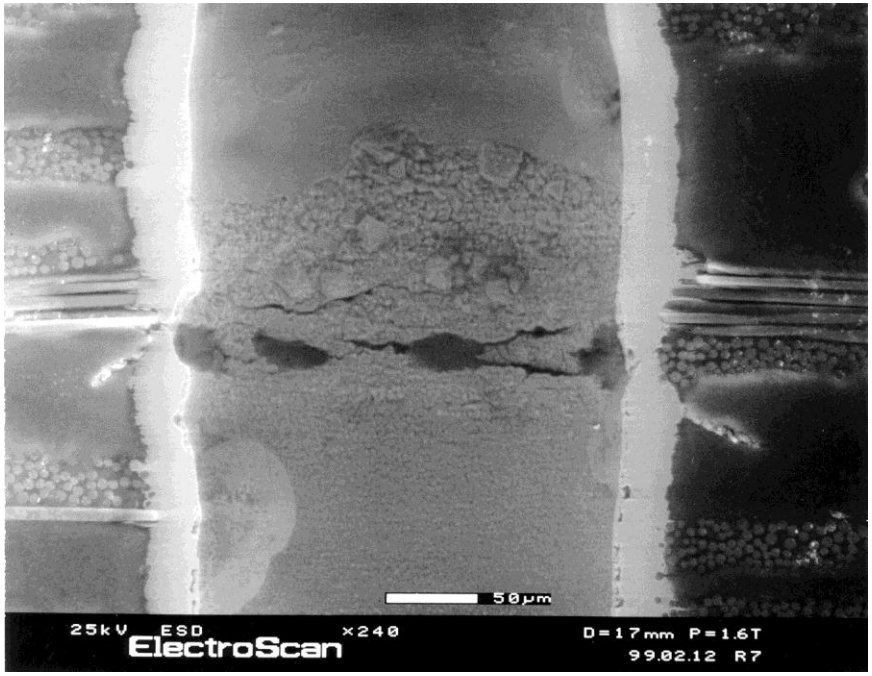
Plating Voids

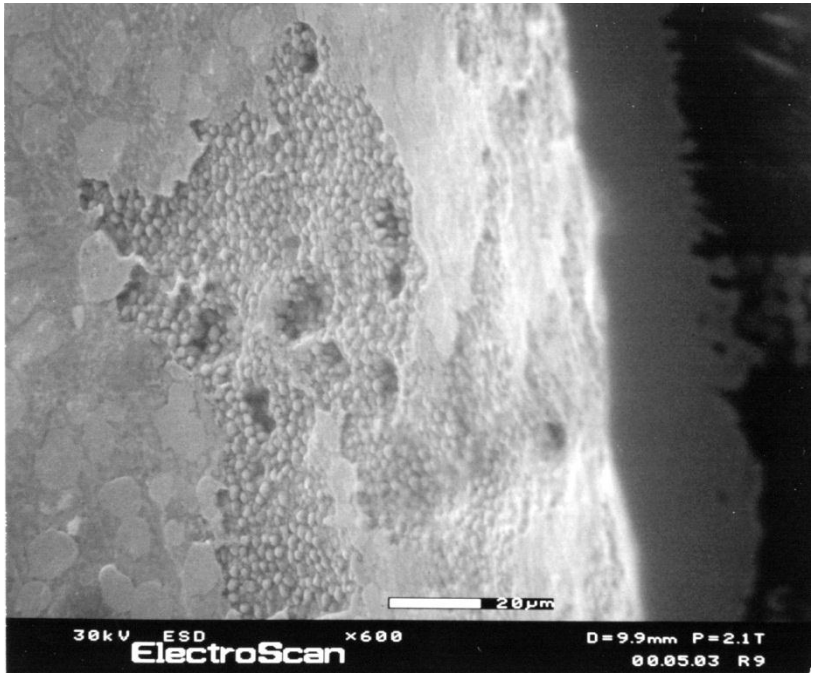
- Plating void is a generic term to describe voids present in and around the PTH wall.
- Can cause large stress concentrations, resulting in crack initiation.
- The location of the voids can provide crucial information in identifying the defective process.
  - Around the glass bundles
  - In the area of the resin
  - At the inner layer interconnects (aka, wedge voids)
  - Center or edges of the PTH



Etch Pits

- Occur due to either insufficient tin resist deposition or improper outerlayer etching process and rework.
- Cause large stress concentrations locally, increasing likelihood of crack initiation. Large etch pits can result in a electrical open.





How to Test/Qualify a Reliable PTV?

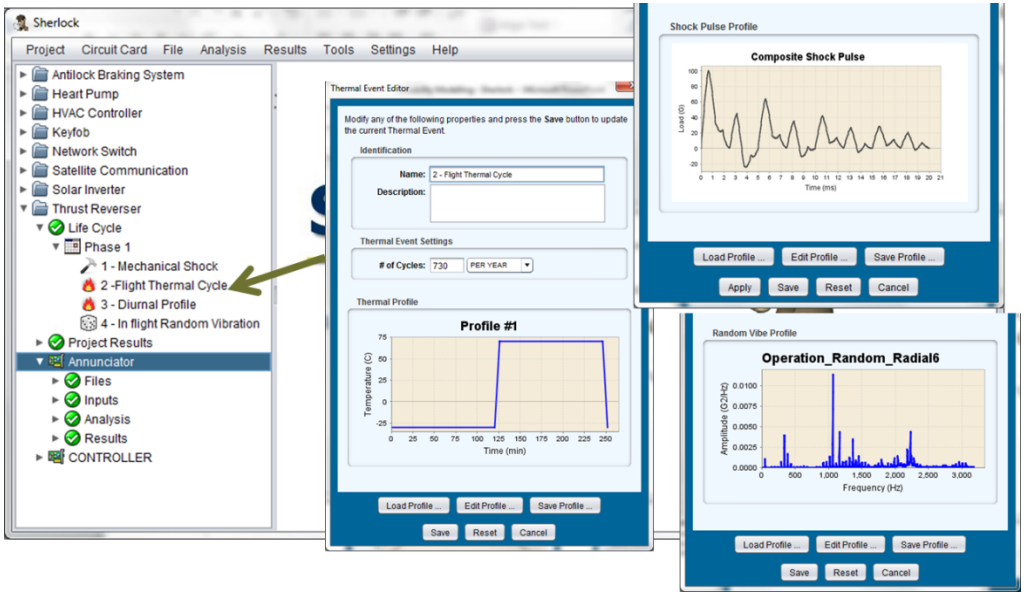
- There are currently six procedures for testing/qualifying a PTV
  - Modeling and simulation
  - Cross-sectioning + solder float/shock
  - Thermal shock testing (also thermal cycling)
  - Interconnect stress testing (IST)
  - Printed Board Process Capability, Quality, and Relative Reliability (PCQR2)
  - Highly Accelerated Thermal Shock (HATS)

Test / Qualify PTV

- Qualifying PTV is a two-step process
- The first step is to qualify the design and the PCB manufacturer
  - Initial qualification
- The second step is to initiate ongoing testing to monitor outgoing quality
  - Lot qualification

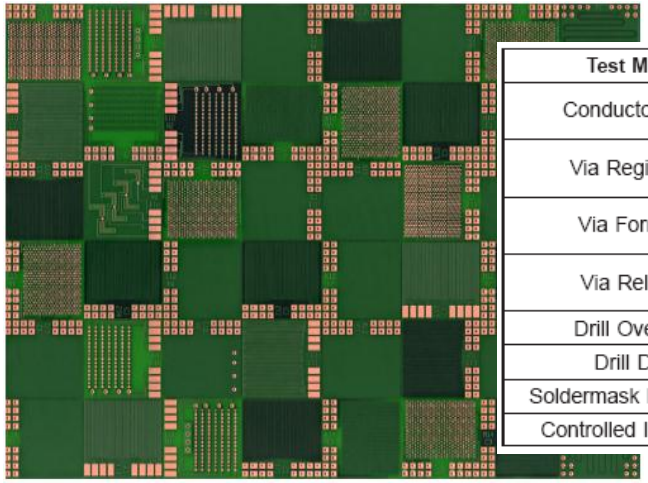
Initial Qualification

- Qualify the design through simulation / modeling
- IPC TR-579 implemented into Automated Design Analysis software, Sherlock, to allow for rapid assessment of PTV robustness
- First step: Define the environment (test or field or both)



Initial Qualification (PCQR2)

- Qualify the design and manufacturer through PCQR2
  - Consists of a coupon design, a test standard, and a database
  - 18″ x 24″ layout with 1″ x 1″ test modules (352)
  - 2 – 24 layers (rigid, rigid-flex)
  - Three panels / three non-consecutive lots
  - Simulated assembly (6X) and thermal cycling (HATS)



Test Module	Design Type	Capability Information	Quality Information
Conductor/Space	Outerlayer, 0.5-oz. innerlayer, 1-oz. innerlayer, and buried-core	Conductor and space defect density	Conductor width and height uniformity
Via Registration	Through, 1-deep blind, 2-deep blind, controlled-depth drill, and back-drill	Via probability of breakout	
Via Formation	Through, 1-deep blind, 2-deep blind, buried-core, controlled-depth drill, and back-drill	Via defect densit	Via net resistance coefficient of variation
Via Reliability	Through, 1-deep blind, 2-deep blind, buried-core, controlled-depth drill, and back-drill	Yield loss	Percent change in resistance
Drill Overshoot	Controlled-depth drill	Probability of overshoot	
Drill Depth	Back-drill	Secondary drill depth	
Soldermask Registration	Outerlayer	Clearance yield	
Controlled Impedance	Single-ended and differential	Impedance uniformity	

PCQR^2 (cont.)

- Advantages
  - Industry standard (IPC-9151)
  - Plug and play
  - Provides real data for understanding of PCB supplier capabilities and comparison to the rest of the industry through the use of an anonymous database
- Disadvantages
  - Industry-certified single source
  - $2K - $5K, not including panel costs

Lot Qualification

- Interconnect stress testing (IST) is the overwhelming favorite of high reliability organizations
  - Small (1 x 4) coupon can fit along the edge of the panel
  - Testing is automated
  - Widely used
  - Ability to drive barrel fatigue and post separation
- Large number of holes (up to 300) and continuous resistance monitoring makes it far superior to cross-sectioning
  - And it should be cheaper!

IST – Issues / Awareness

- Coupon design is critical (IST can be prone to problems)
- Need to specify preconditioning (IST or real reflow oven?)
- Need to specify frequency (every lot, every month, every quarter)
- Need to specify maximum temperature (some debate on the validity of results when above the Tg)
  - 130, 150, and 175C are the most common
- Need to specify requirements
  - Different markets/organizations specify different times to failure (300, 500, and 1000 cycles are most common)

Conclusion

- The base knowledge and understanding of PTV Fatigue is robust
  - Decades of testing and simulation
  - Use of reliability physics is best practice
- Detailed understanding is still missing
  - Key expertise (process parameters, material properties, simulation, testing) is rarely in the same organization
  - Not a pure science activity (significant amount of human influence)
- Improvements in out-of-plane CTE and plating properties have greatly improved PTV performance
  - Avoiding defects continues to be the biggest risk

Speaker Biography

- Cheryl Tulkoff has over 22 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She has held leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years, is an ASQ Certified Reliability Engineer and a mer of SMTA and iMAPS.

- She has a strong passion for pre-college STEM (Science, Technology, Engineerir and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.

Thank You!

- Questions?
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