Non-Functional Pads (NFPs)

Should They Stay or Should They Go?

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Abstract

- There is an ongoing debate as to the influence of non functional pads (NFPs) on reliability especially as related to barrel fatigue on higher aspect ratio plated through vias.

- In an attempt to gather common practices and supporting data, industry experts were surveyed. The overwhelming response indicated that most suppliers do remove unused / non functional pads.

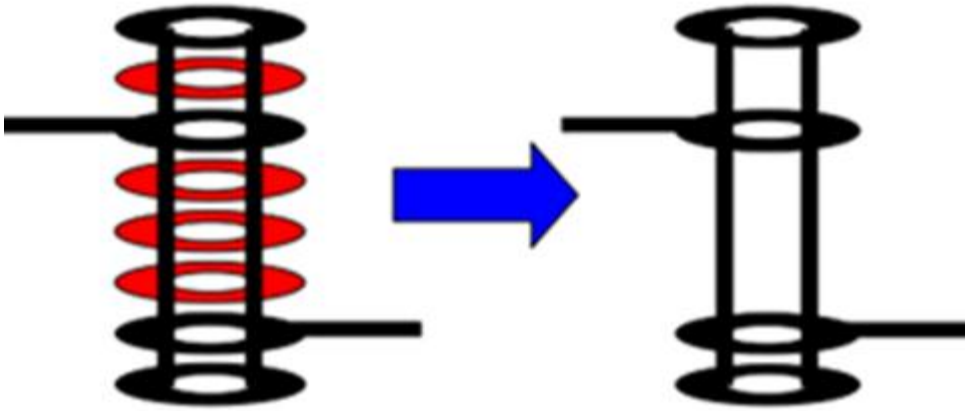
- No adverse reliability information was noted with respect to the removal of unused pads; conversely, leaving them can lead to an issue called telegraphing. In all responses, remove or keep NFPs, the primary reason given was to improve the respective fabricators' processes and yields.

Abstract (continued)

- Companies that remove the unused pads do so primarily to extend drill bit life and produce better vias in the boards, which they considered the primary reliability issue.
- For those that keep the unused pads, the primary reason given is that they believe it helps with Z-axis expansion of the board due to Coefficient of Thermal Expansion (CTE) issues. However, with the newer materials being utilized for Pb-free assembly, this concern seems to have abated.
- In general, the companies responding did not feel that removing the unused pads would create a reliability issue. All suppliers said that their response was the same regardless of whether polyimide glass or epoxy glass materials were involved.

Introduction

- Non-functional pads (NFPs)
  - Pads on internal or external layers that are not connected to active conductive patterns on the layer
  - Ongoing debate regarding their influence on printed board (PB) reliability



NFPs Present NFPs Removed

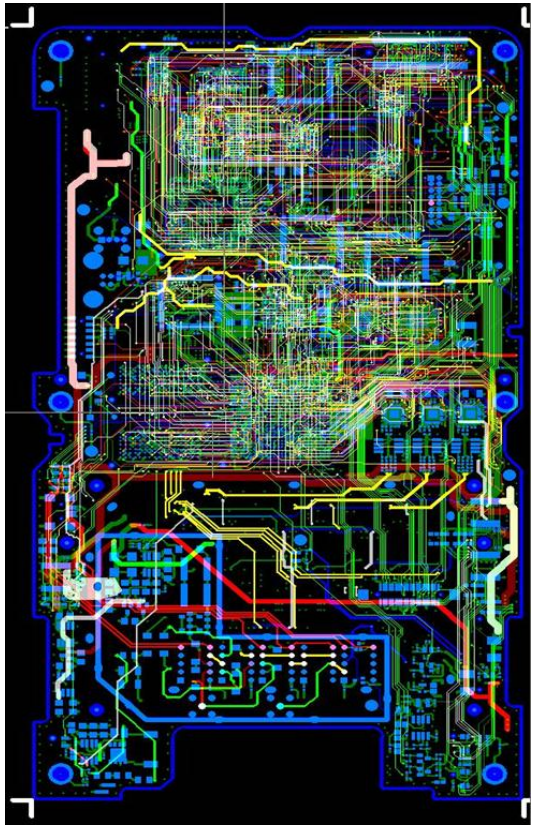
Industry Survey

- To gather common practices and reliability data, industry experts were surveyed

- 14 US printed board fabricators participated
  - Additional 8 fabricators received the survey but did not respond

Industry Survey

- Printed Board (PB) Description
  - IPC Class 3 Requirements
  - FR4 (170°C) and Polyimide (220°C)
  - HASL Finish, Sn63Pb37 only (not Pb-free)
  - Thickness range: 0.020” to 0.125”
  - Layer Count: 16 max
  - Inner Copper (oz): 0.5 to 2.0,
  - Outer Copper (oz): 1.0 to 3.0



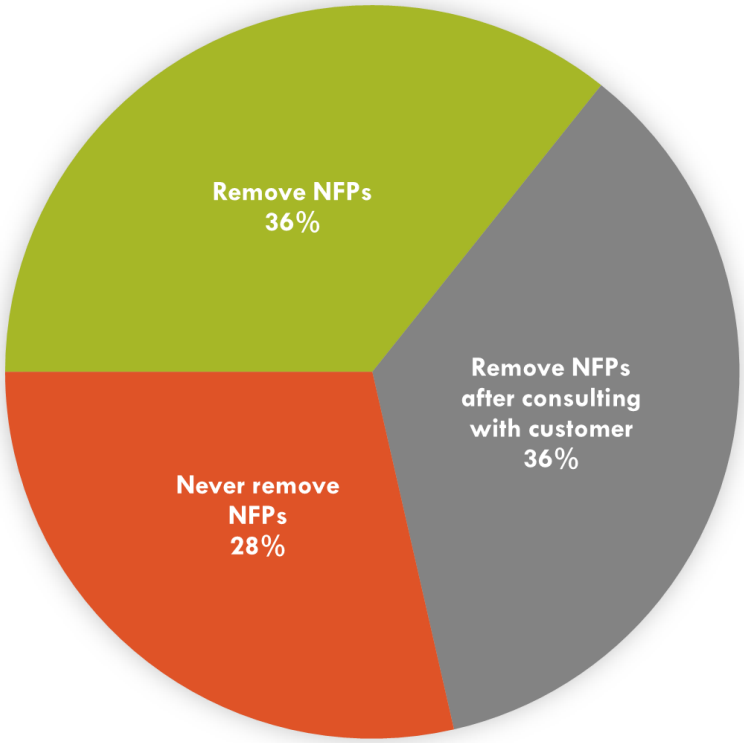
Industry Survey Questions

1. *What is your procedure with respect to non-functional inner layer pads?*
2. *Do you keep them or remove them as a function of board material type, overall thickness, layer count, copper thickness?*
3. *Is this a standard practice?*
4. *If you remove or don't remove non-functional pads, what is the reason for doing so?*
5. *If you remove them, do you have reliability data that you could share indicating whether there is or is not a reliability issue?*
6. *Is the answer the same for epoxy glass and polyimide board materials?*
7. *Is the answer the same if the circuit is high speed?*

Survey Summary

1. *What is your procedure with respect to non-functional inner layer pads?*

   - 5 companies remove them
   - 5 companies stated that they would remove the pads, but usually after receiving permission from their customer
   - 4 companies never remove them



Survey Summary

2. *Do you keep them or remove them as a function of board material type, overall thickness, layer count, copper thickness?*
   - These characteristics did not alter any company's decision to either keep or remove the unused pads

Survey Summary

3. *Is this a standard practice?*
   - Every company responded that their response was their standard practice

Survey Summary

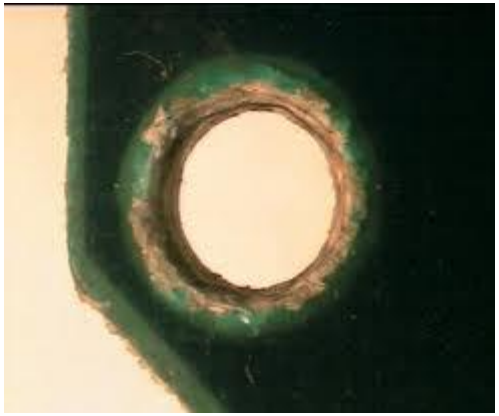
4. *If you remove or don't remove non-functional pads, what is the reason for doing so?*

Why Remove NFPs?

- Reduce drill wear
- Faster automated optical inspection (AOI)
  - Less features to review
- Reduce shorts / Improve clearance / Reduce misregistration
  - Tight registration, spacing
  - Improves yields
    - Reduces cost

Why Remove NFPs?

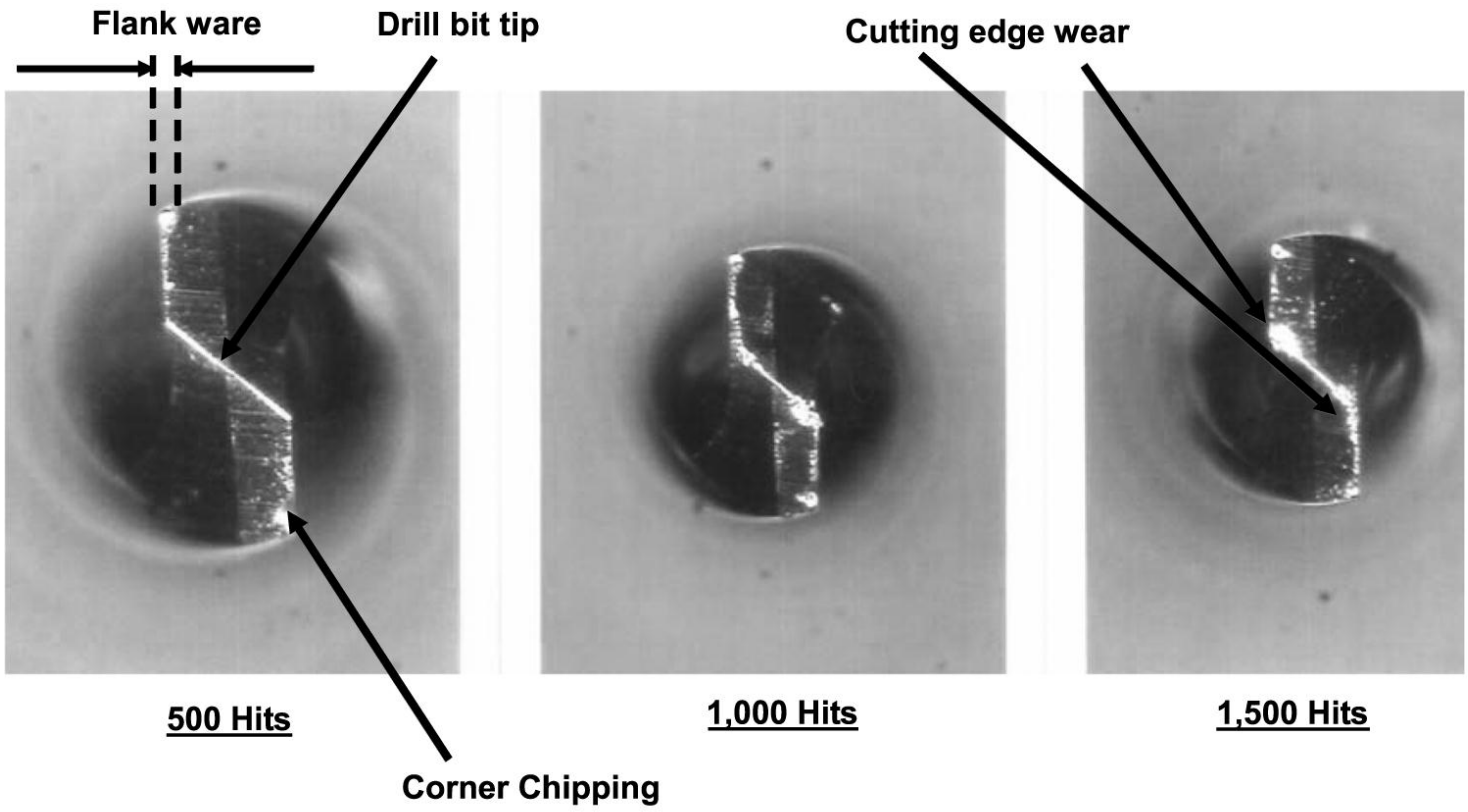
- Reduce drill wear & drill damage



http://www.epectec.com/pcb/gallery

Why Remove NFPs?

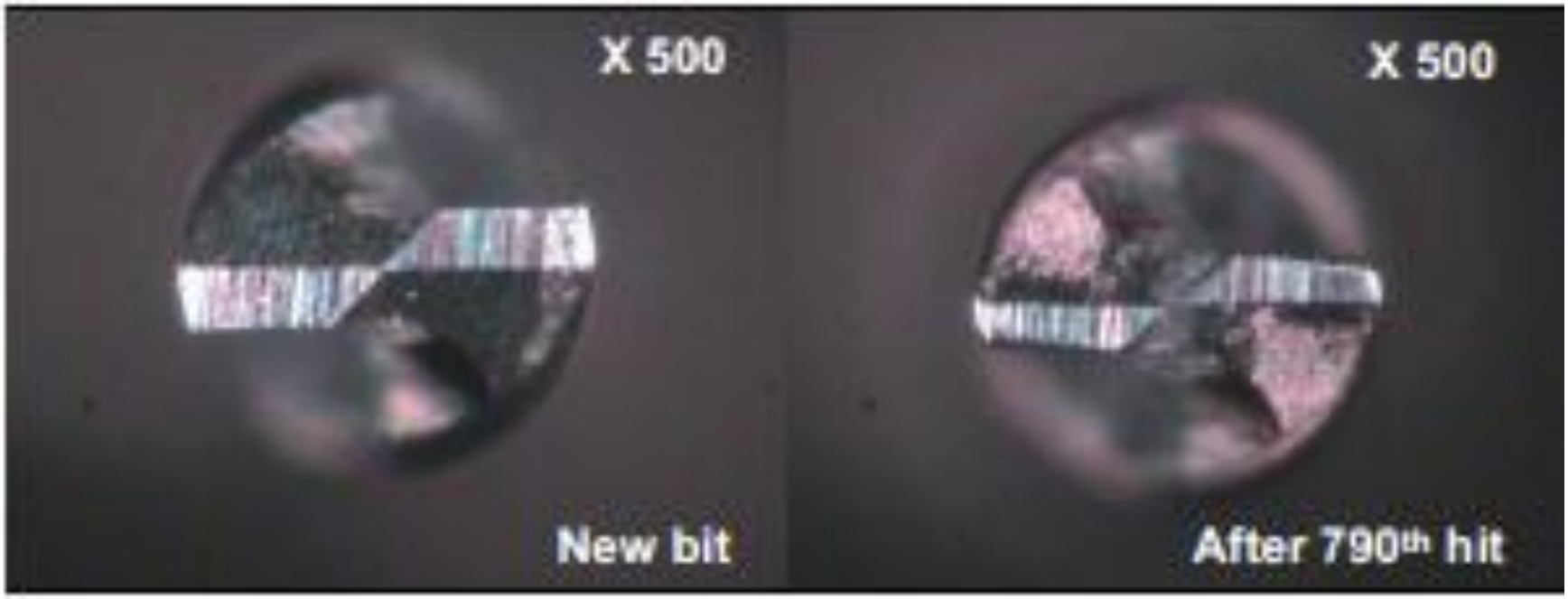
- Reduce drill wear & drill damage



Note: Evidence of corner chipping is also seen which is counted in the measurement of the flank wear

Why Remove NFPs?

- Reduce drill wear & drill damage



Drilling Burr Minimization and Energy Saving for PCB Production, LMAS 2011

Why Remove NFPs?

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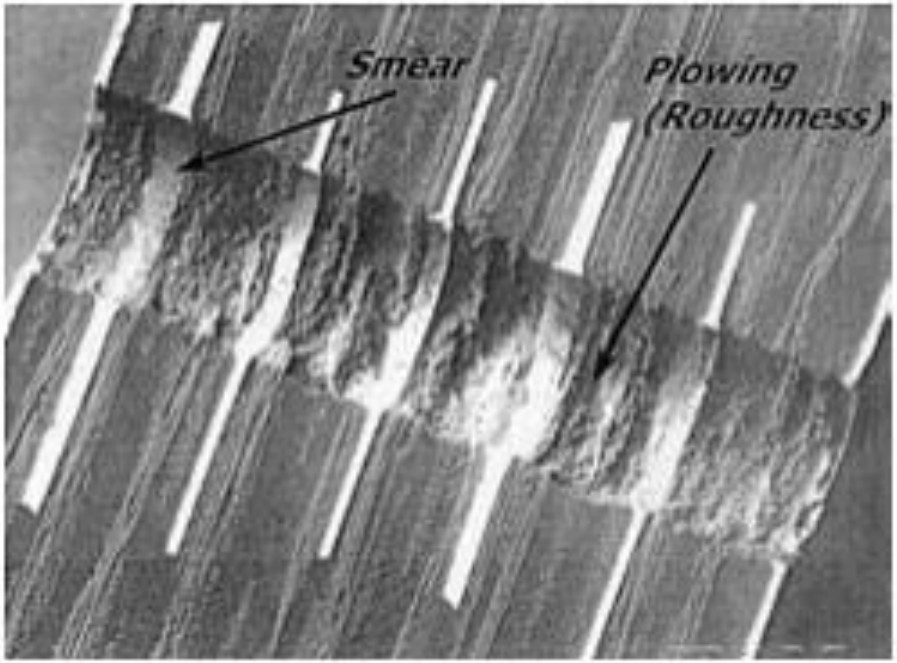
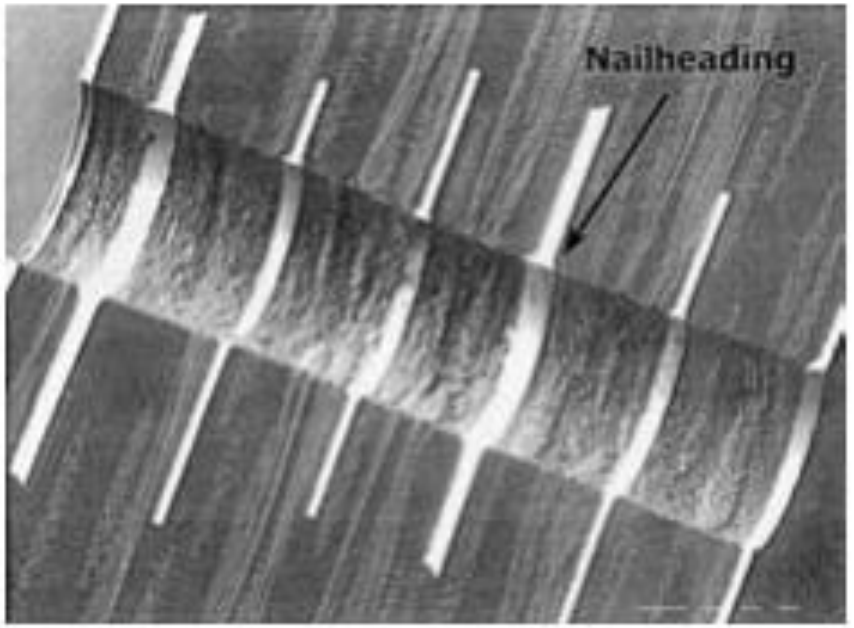
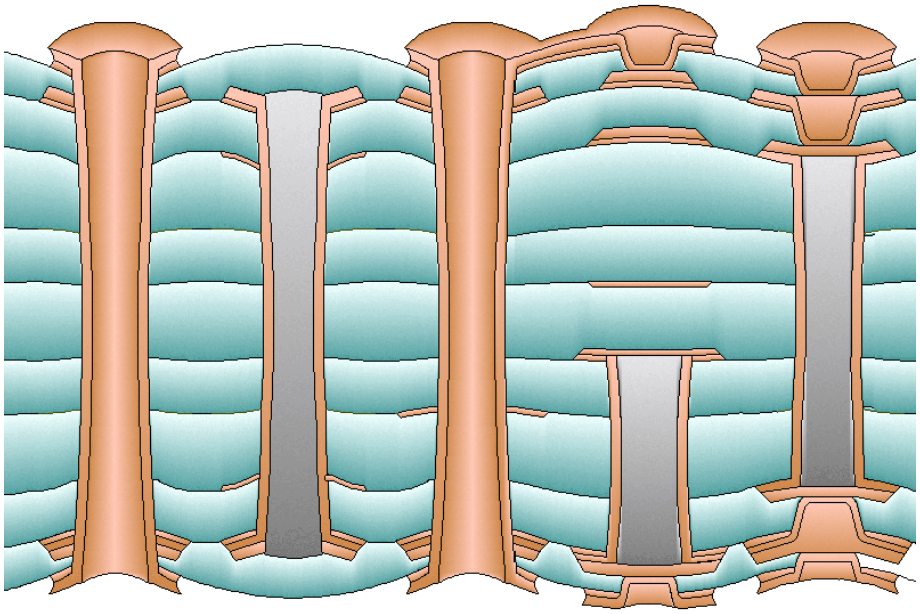




Drilling Processes
http://www.matrixelectronics.com/pdfs/solutions/Understanding%20the%20Drilling%20Processes.pdf

Why Keep NFPs?

- Concern for accidental removal of a functional pad
- Belief that they anchor the hole and improve reliability
- More copper that can be retained on any layer, the better the dimensional stability

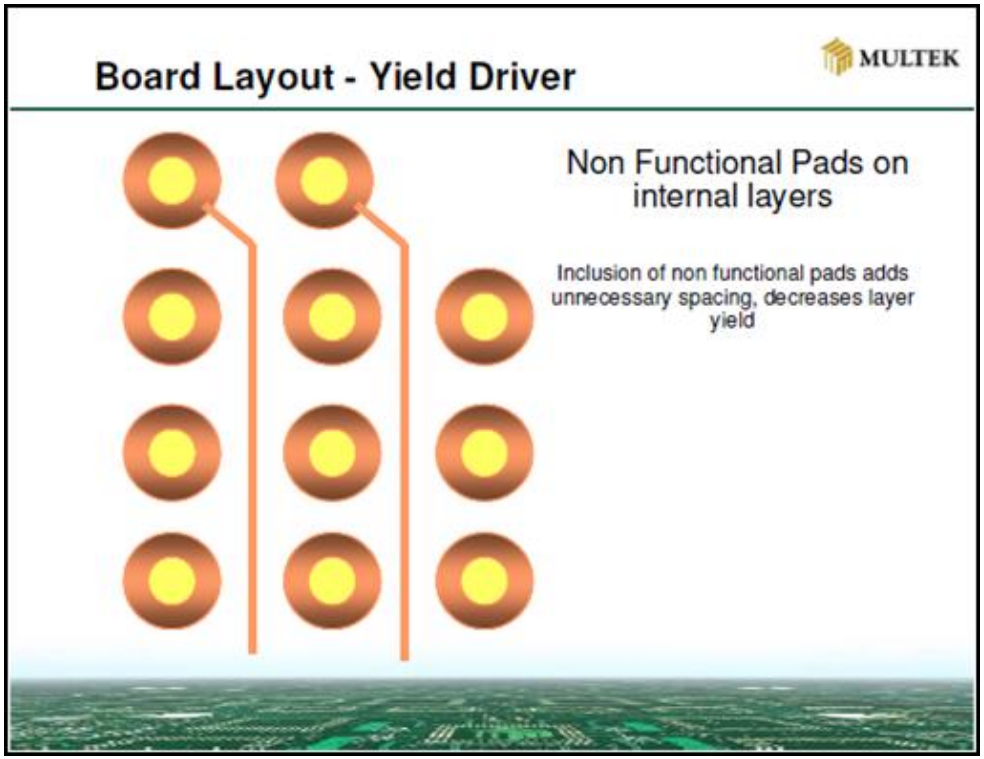


Cross Section of Typical Interconnections at 260C,

Design and Construction Affects on PWB Reliability, PWB Interconnect Solutions

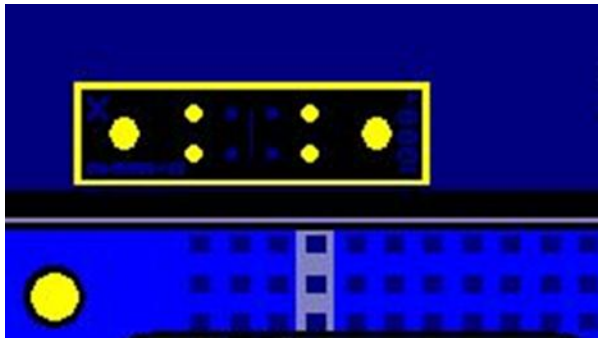
PB Fabricator Guidance

- Routinely recommend removal of non-functional pads
  - Spacing
  - Yield



Survey Summary

5. *If you remove them, do you have reliability data that you could share indicating whether there is or is not a reliability issue?*
   - *Limited actual or internal testing available*
   - *Some reliance on industry standards*
     - *IPC 6012, Class 3*
   - *Anecdotal evidence*



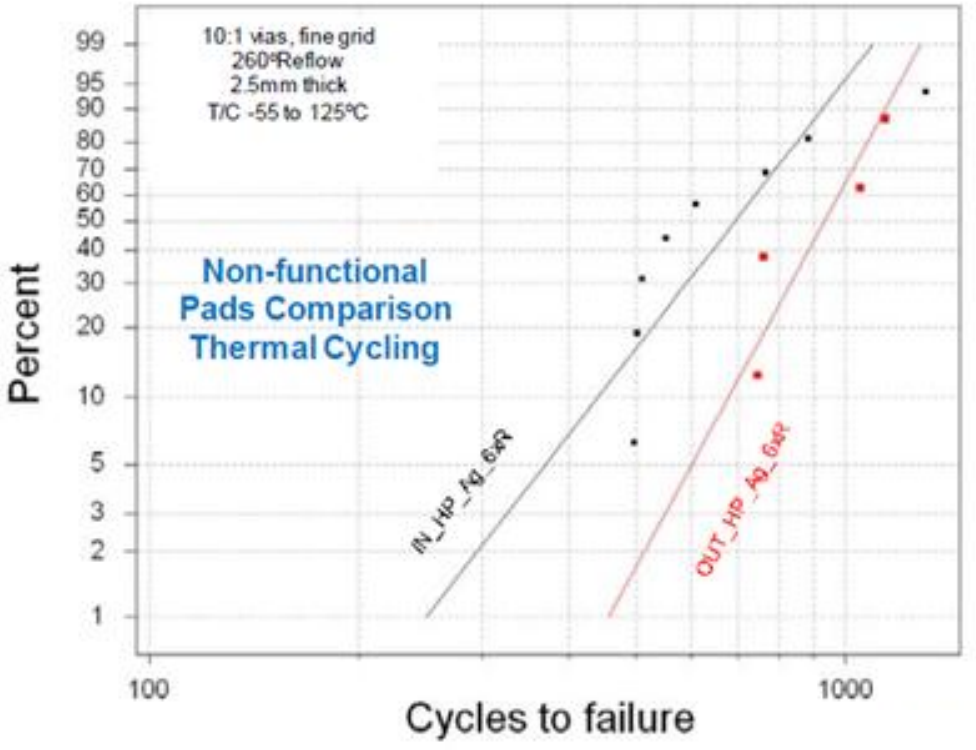
Example of an internal test coupon used for NFP evaluation

Reliability Data & NFPs

- Data sparse
  - Literature review
  - Industry Experts

PTH Reliability for High Aspect Via Holes

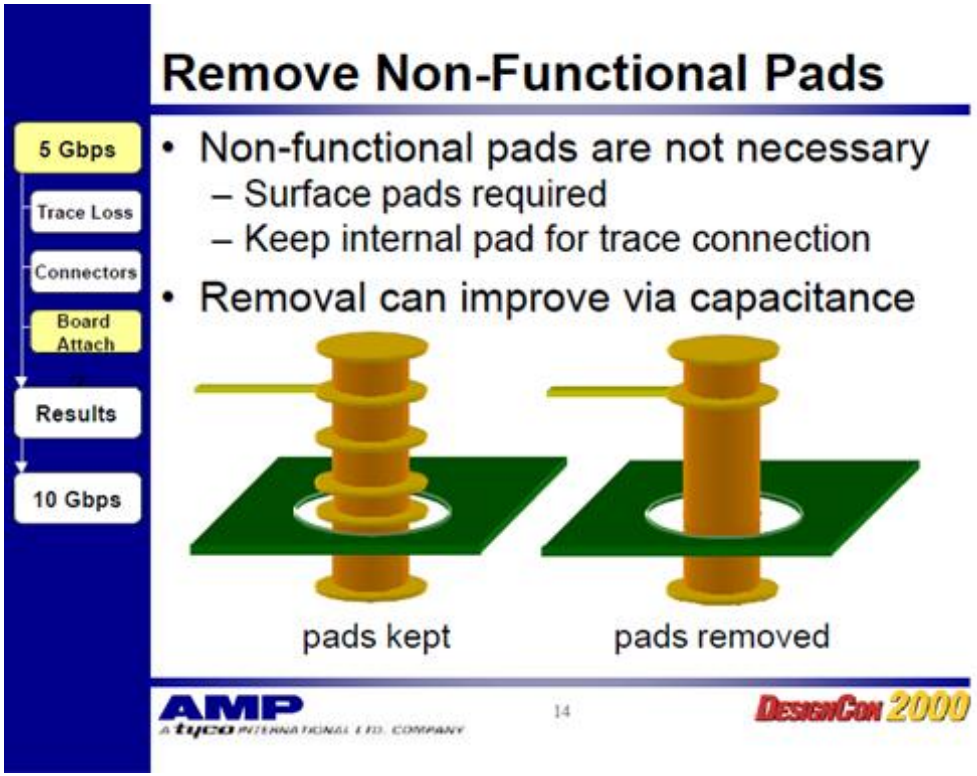
- NPL reported higher percentage and earlier fails of vias with NFPs
  - Black Line is NFPs IN
  - Red Line is NFPs OUT



[2] Wickham Martin, "Through Hole Reliability for High Aspect Via Holes," NPL Webinar June 11, 2013

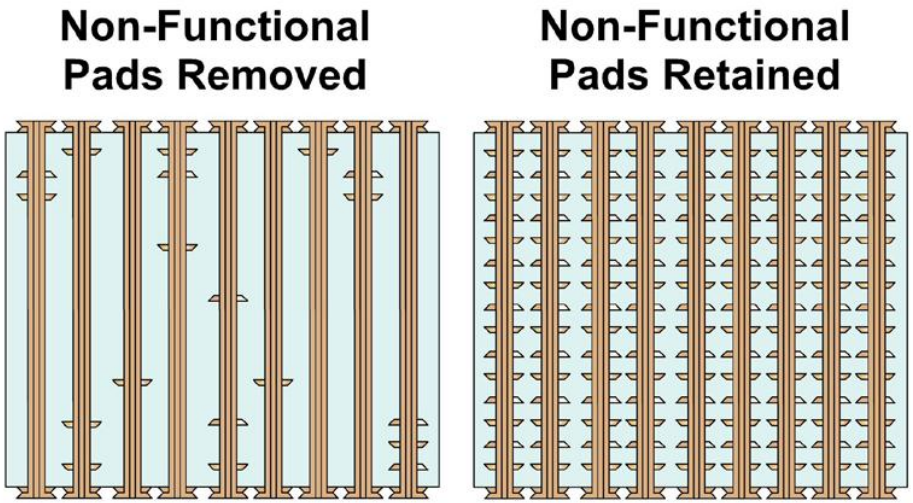
NFPs & High Speed Designs

- Design guidance from component manufacturers recommends removal
  - Especially for high aspect ratio vias



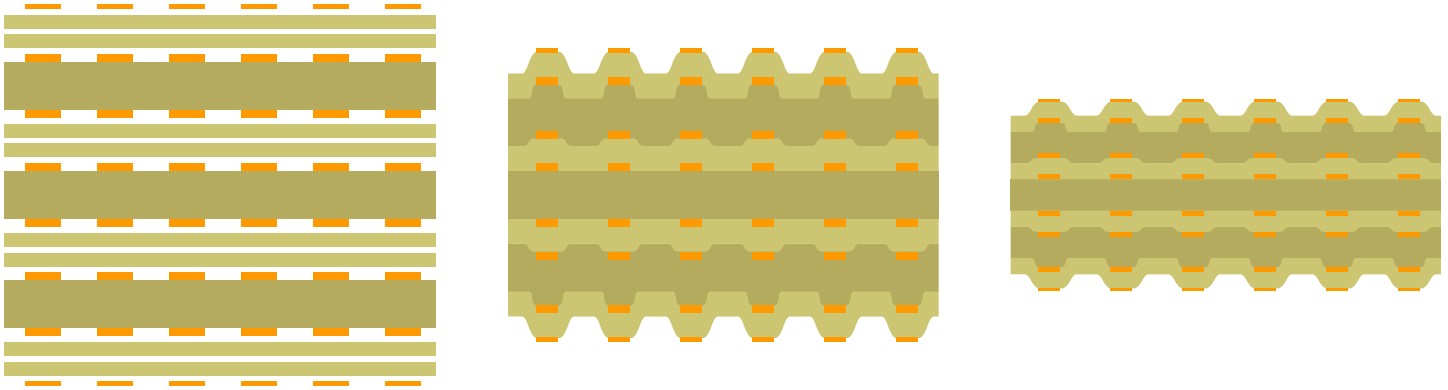
Reliability Data (continued)

- PWB Interconnect reports that “presence of non-functional pads is a determent [*sic*] to the reliability of PWBs”
  - Speculated about telegraphing phenomenon: excess copper at PTHs results in resin starvation between pads

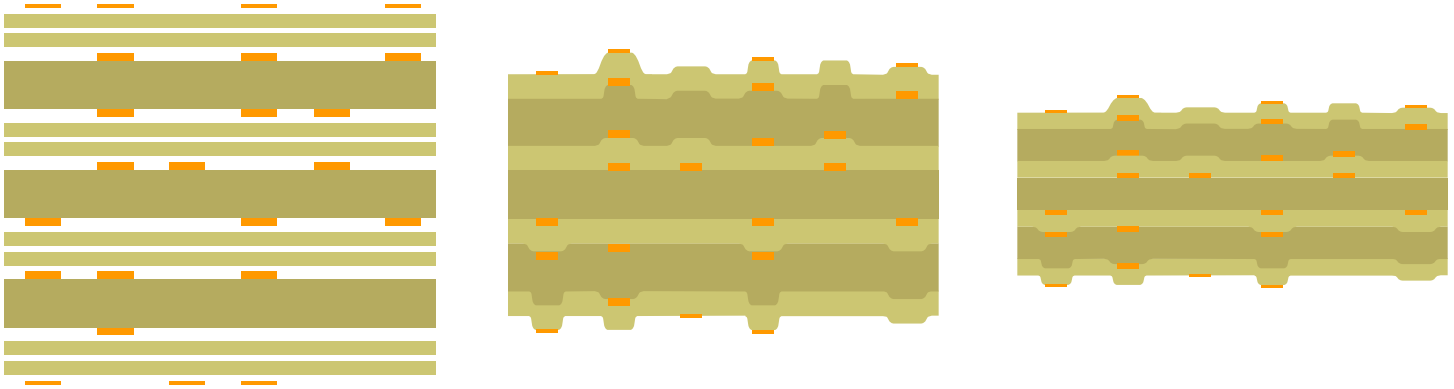


Telegraphing Schematic

NFPs Left In



NFPs Removed



Survey Summary

6. *Is the answer the same for epoxy glass and polyimide board materials?*
   - All suppliers said that their response was the same for these materials

NFPs & Rigid Flex Boards

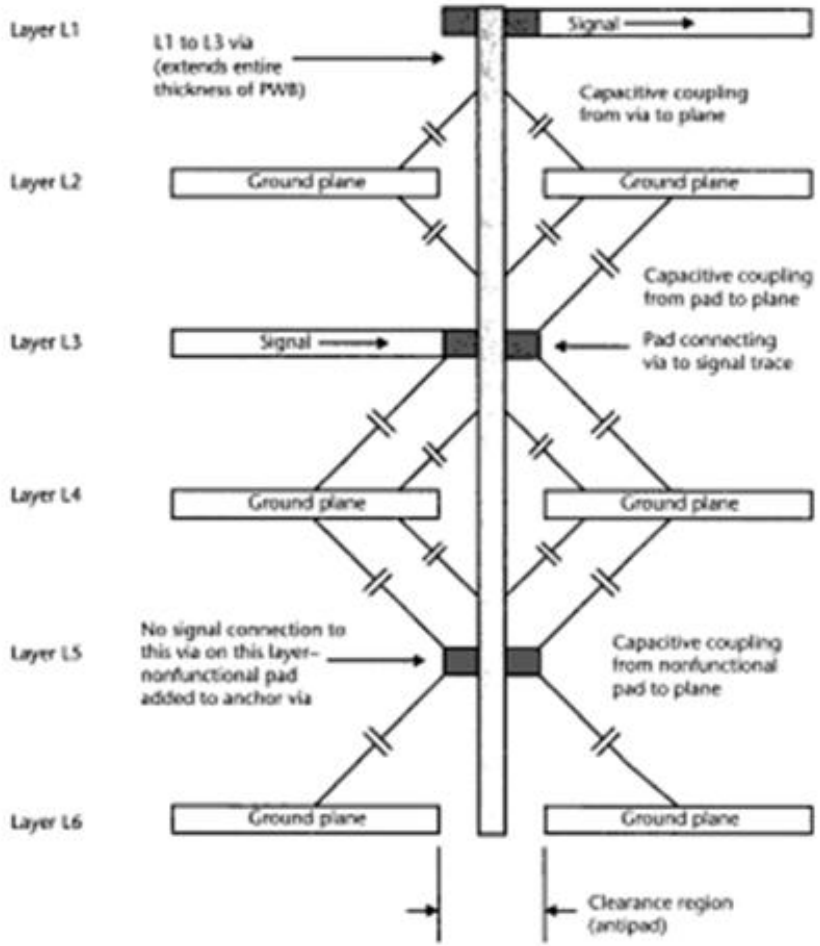
- Fabricators leave the unused pads in place to provide additional reinforcement for the Kapton Mylar flex material

Survey Summary

7. *Is the answer the same if the circuit is high speed?*
   - “Yes. More so for high speed because non-functional pads (NFP’s) have a signal integrity (S.I.) impact on the holes (from a supplier typically removes the unused pads).”
   - “No, for high speeds, these unused lands increase loss (>10Gbps) (from a supplier that typically keeps the pads).”

NFPs & High Speed Designs

- NFPs shown to negatively impact signal integrity of high speed/high frequency designs
  - NFP removal reduces parasitic capacitance
  - Published papers & presentations



NFP Capacitively Coupling to Plane

A. Ciccomancini Scogna, “Signal Integrity Analysis of a 26 Layers Board with Emphasis on the Effect of Non-Functional Pads,” IEEE EMC 2008 Symposium.

Expert Opinions

- It depends!
  - Design dependent
    - Use caution on flex and rigid flex
    - Evaluate options
    - High density and high speed considerations
  - Opt for selective removal
    - Remove NFPs where possible

Summary

- No specific reliability issue associated with the removal of unused pads for standard rigid multilayer boards
- 2/3 of the surveyed fabricators removed the pads routinely or after approval from their customer
- No “one size fits all” approach to NFP removal
- Companies need to devise a strategy based on the design and materials used and document those needs clearly to their printed board fabricators
- Experts do all recommend removal of NFPs where possible

References

INDUSTRY REFERENCES

- [1] A. Ciccomancini Scogna, “Signal Integrity Analysis of a 26 Layers Board with Emphasis on the Effect of Non-Functional Pads,” IEEE EMC 2008 Symposium.
- [2] Wickham Martin, “Through Hole Reliability for High Aspect Via Holes,” NPL Webinar June 11, 2013.
- [3] Birch, Bill, “Discussion on Non-functional Pad Removal/Backdrilling and PCB Reliability,” PWB Interconnect Solutions Inc. 103-235 Stafford Road West, Nepean, Ontario, Canada K2H 9C1.
- [4] Reid, Paul, “Design and Construction Affects on PWB Reliability,” PWB Interconnect Solutions, IPC APEX EXPO.
- [5] Thierauf, Stephen, High-speed Circuit Board Integrity, Artech House, January 2004.
- [6] Barker, Donald & Dasgupta, Abhijit, Chapter 20 “Thermal Stress Issues in Plated-Through-Hole Reliability” in Thermal Stress and Strain in Microelectronic Packaging, Van Nostrand Reinhold, 1993.

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- [7] Frank, Bill, “Design for Manufacture,” Multek.
- [8] Sanmina, “PCB Fabrication: Opti-Via Technology for Improved Signal Integrity at Higher Frequencies.”

DESIGN AND APPLICATION NOTE REFERENCES

- [9] Altera AN-672, “Transceiver Link Design Guidelines for High-Gbps Data Rate Transmission,” 02/15/2013.
- [10] Altera AN-529, “Via Optimization Techniques for High Speed Channel Design,” May 2008.
- [11] Rothermal, Brent et al, “Practical Guidelines for Implementing 5 Gbps in Copper Today, and the Roadmap to 10 Gbps,” DESIGNCON 2000.

IMAGE REFERENCE

- [12] Non Functional Pad Removal. http://wiki.fed.de/images/7/70/Empfehlung_zu_Non_Functional_Pad_Removal.pdf.

Author Biography

- Cheryl Tulkoff has over 22 years of experience in electronics manufacturing with an emphasis on failure analysis and reliability. She has worked throughout the electronics manufacturing life cycle beginning with semiconductor fabrication processes, into printed circuit board fabrication and assembly, through functional and reliability testing, and culminating in the analysis and evaluation of field returns. She has also managed no clean and RoHS-compliant conversion programs and has developed and managed comprehensive reliability programs.

- Cheryl earned her Bachelor of Mechanical Engineering degree from Georgia Tech. She is a published author, experienced public speaker and trainer and a Senior member of both ASQ and IEEE. She has held leadership positions in the IEEE Central Texas Chapter, IEEE WIE (Women In Engineering), and IEEE ASTR (Accelerated Stress Testing and Reliability) sections. She chaired the annual IEEE ASTR workshop for four years, is an ASQ Certified Reliability Engineer and a member of SMTA and iMAPS.

- She has a strong passion for pre-college STEM (Science, Technology, Engineering, and Math) outreach and volunteers with several organizations that specialize in encouraging pre-college students to pursue careers in these fields.

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