

Cloud and Data Center Reliability

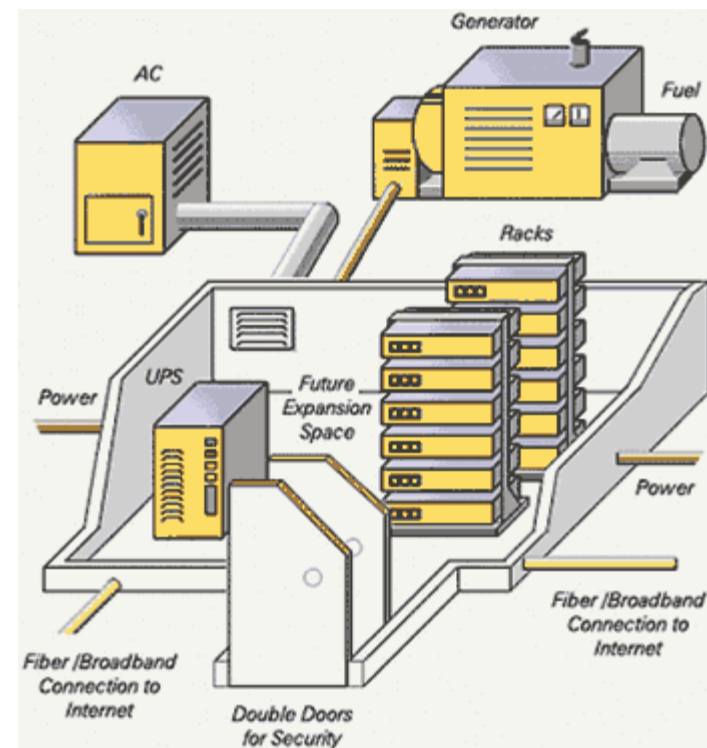
Open House 2015
Edward Wyrwas

What is the cloud?

- The cloud is a collection of data centers which comprises the internet, world-wide-web, dark-nets, etc.
- The cloud and data centers should be considered synonymous.
- “Cloud computing is using the internet to access someone else’s software running on someone else’s hardware in someone else’s data center”

software on hardware located somewhere

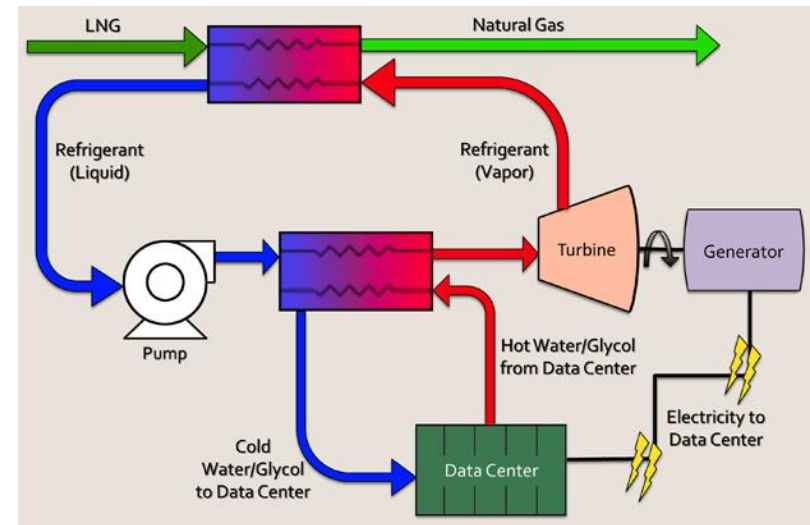
Data Center Constituents



DfR's lab service capabilities cover electronics at every tier

Infrastructure

- **Power Management**
 - Power lines (230kV)
 - Backup power generators
 - Battery Backup
 - Power distribution unit (208/230V)
 - Rack power strips (120V)
 - Rack-based battery backup
- **HVAC**
 - Cooling system (cold aisles)
 - Air distribution, blowers, etc.
 - Thermostats and Control
- **Real time management and prognostics tools**



Networks

Hardware:

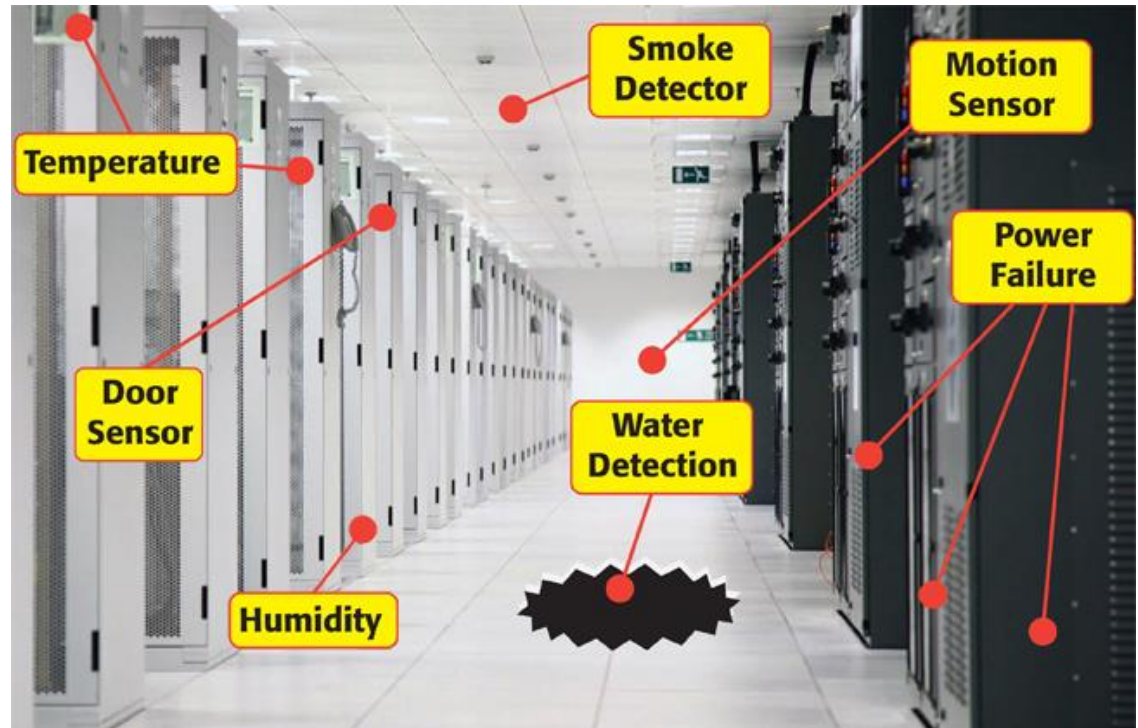
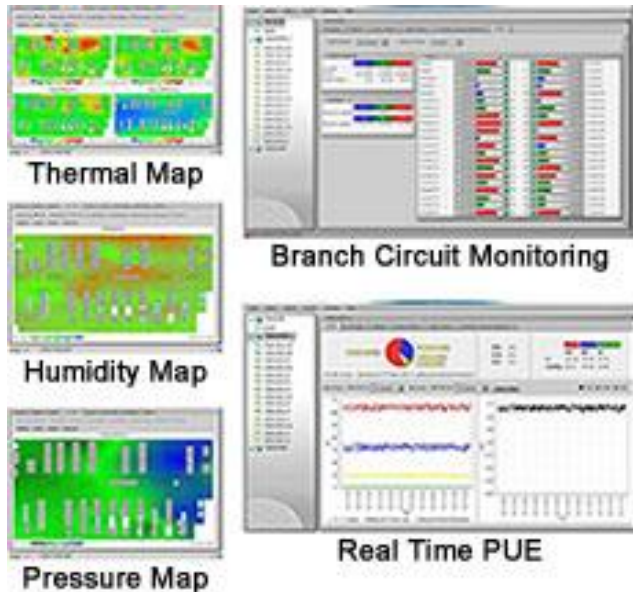
- Routers and switches
- Fiber channel transceivers
- Redundant wiring (think interconnects)

Software:

- Applications
- Load balancing and fail over
- Redundant data transfers
- Send/Receive/Acknowledge



Prognostic Sensors



- Will sensor performance degrade?
 - Short answer – yes!

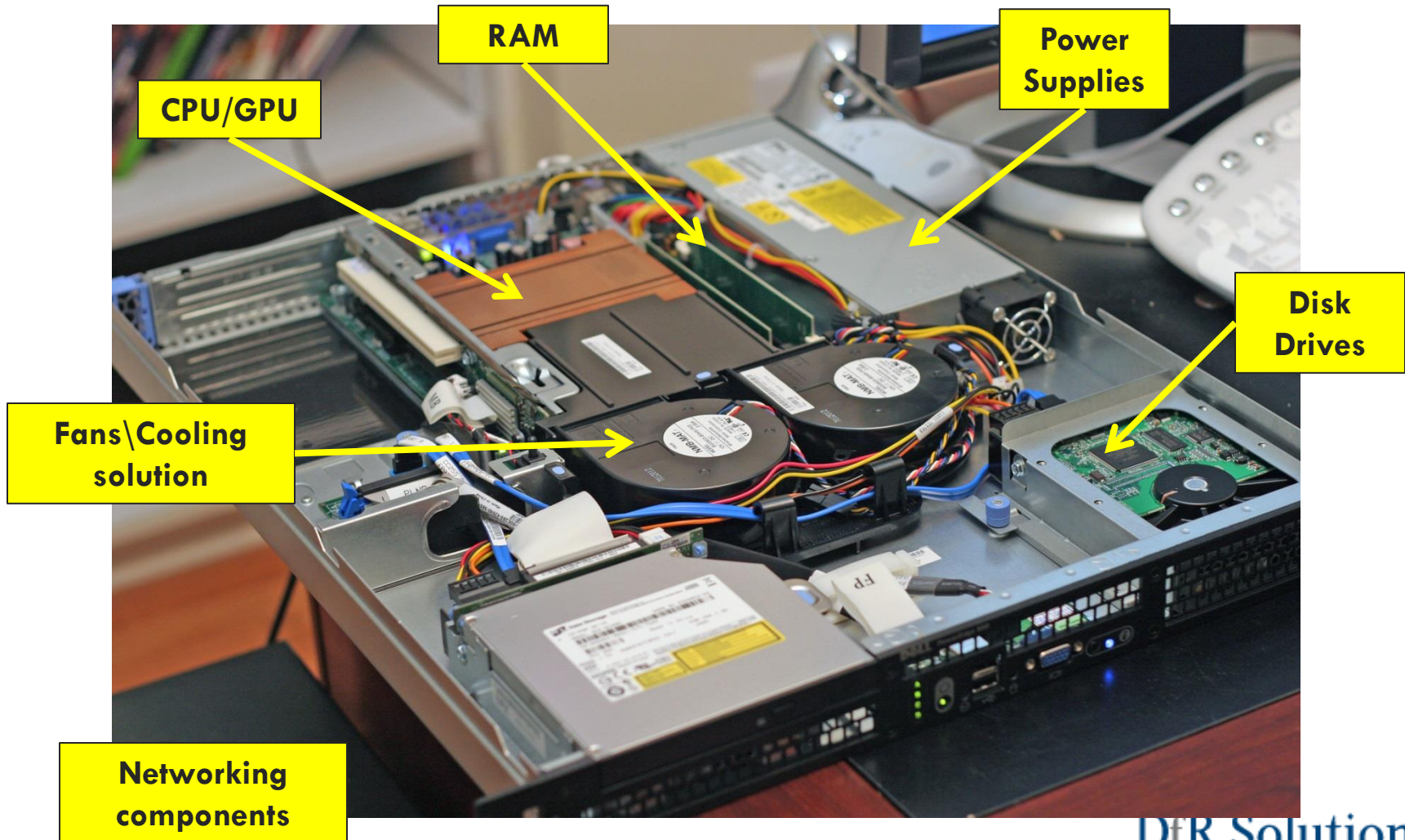
Rack Space = Servers

- Servers are:
 - specialized computers that manage a centralized resource or service on a network
 - i.e. print server, web server
 - capable of 24x7x365 run time
- Servers contain:
 - Redundant power supplies
 - Large memory banks (RAM)
 - Large storage banks (ROM)
- Most racks capable of holding 42x 1U servers or many more blade servers



DfR Solutions

Components in a Traditional Desktop PC are also in servers, network equipment, sensor control, etc.



How to compute reliability of a cloud?

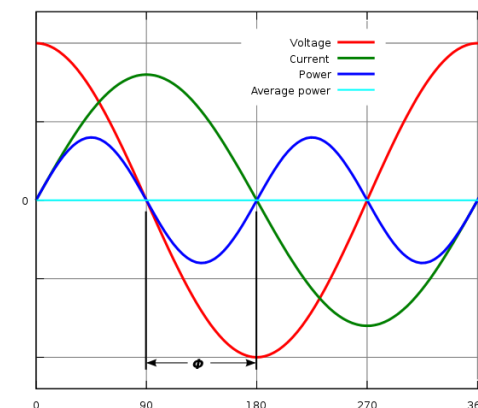
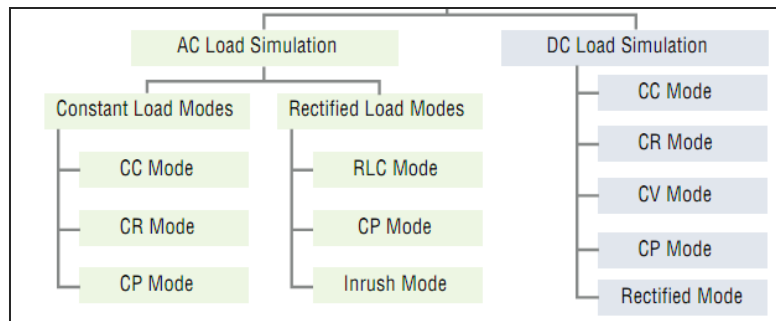
- Reliability of the system
 - as comprised by a multitude of parallel and series components,
 - with some redundancy at multiple locations,
 - can be achieved by performing some physics-of-failure-based tests, achieve defensible results and perform some extrapolation mathematics.
 - Common topic: redundancy
-
1. Perform a defensible accelerated life test for all life limited components in the system
 2. Calculate failure rate from test *failures and confidence level*
 3. Convert to a desired metric
 - $MTBF \approx 1 / \text{failure rate}$
 - $AFR = 1 - e^{(-8760/MTBF)}$
 - $\text{Reliability} = e^{(-t/MTBF)}$

Testing @ DfR Solutions

- DfR Solutions has developed software, firmware and hardware to test the various components of computers
 - Passive components
 - Sub-assemblies (e.g. fans, stepper motors, hard drives, solid state drives, power supplies)
 - Microprocessors (CPU) , graphics processors (GPU), Memories (DRAM, SRAM, Flash)
 - Discrete ICs such as FETs and diodes

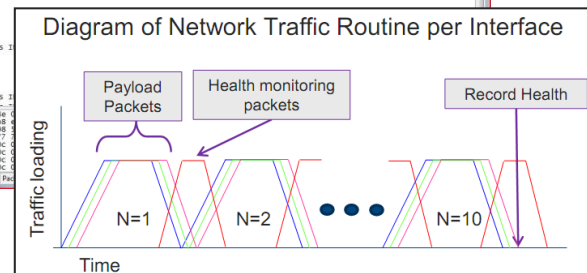
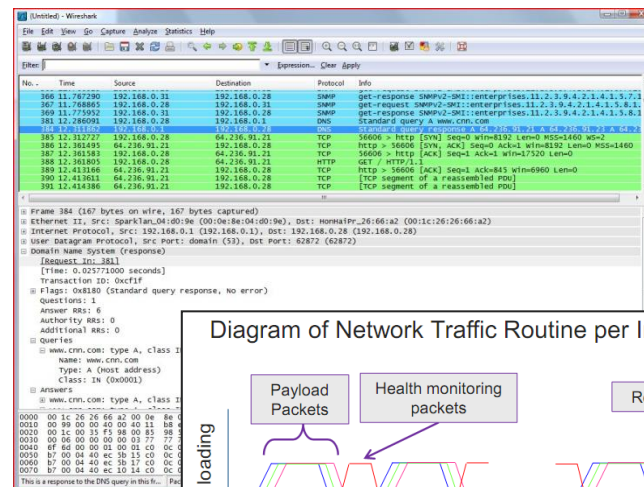
PDU Testing @ DfR Solutions

- DfR Solutions performed benchmarking studies on various power distribution units (PDUs)
- Variable current load levels (4-20Amp) and temperatures (40° - 60°C)
- Simulated failure mode test
 - E.g. Loss of controller power supply, loss of network communication
- Accelerated life test to simulate 10 years constant operation



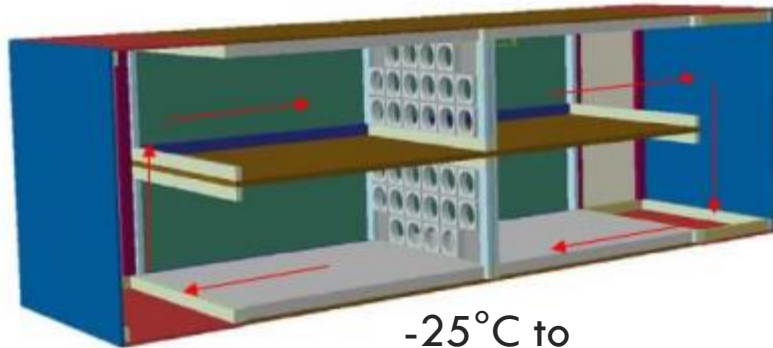
Network Testing @ DfR Solutions

- DfR Solutions performed benchmarking studies on various network node technologies
- Environmental Testing: Constant temperature, temperature cycling, humidity exposure
- Functional exercising
 - Denial of service, quality of service, routing, network simulation, latency, power cycling



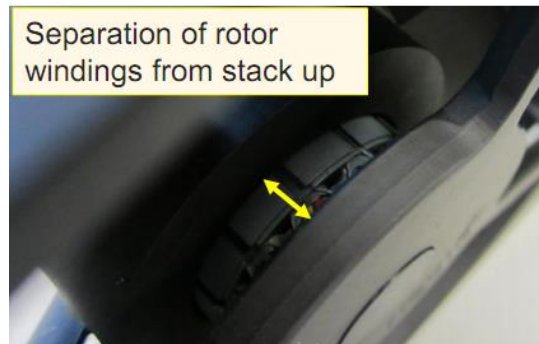
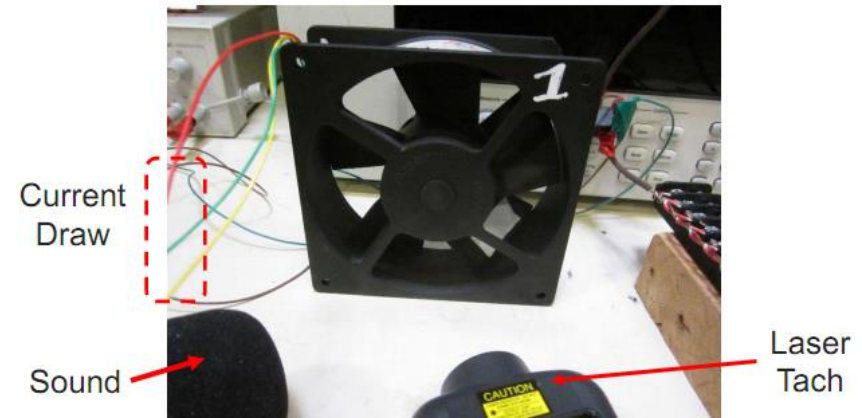
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Fan Testing



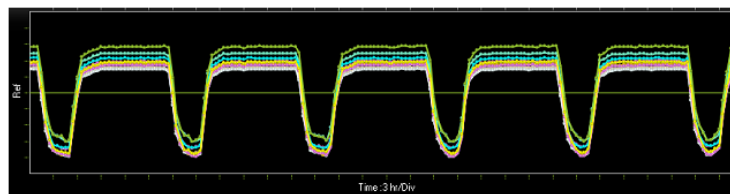
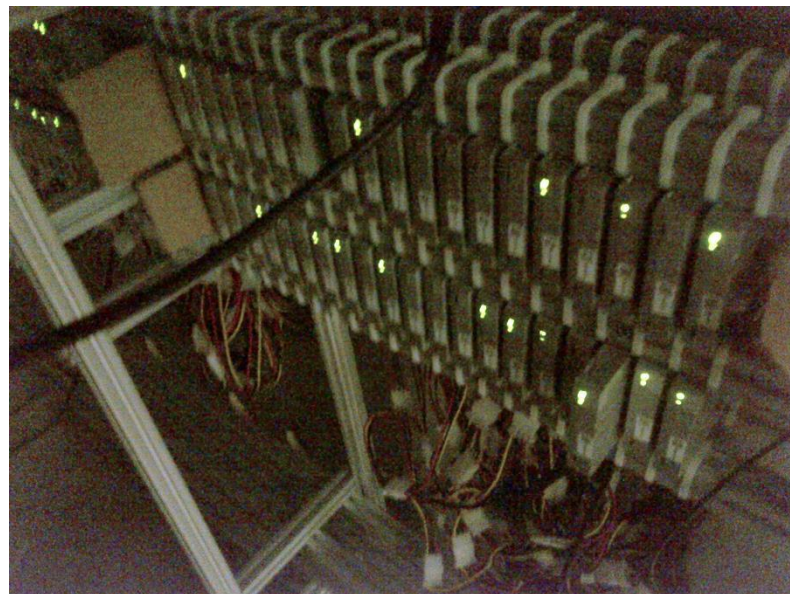
-25°C to
+90°C

- Temperature extremes, cycling
- Power cycling
- Current, sound and tachometer monitoring (failure criteria)
- Vibration/mechanical shock



Storage Media

- Statistically confident data payload – randomization of file size, file type, logical address, etc.
- Hard drives
- Solid state drives
- Multiple interface types



Screenshot of Temperature Monitoring

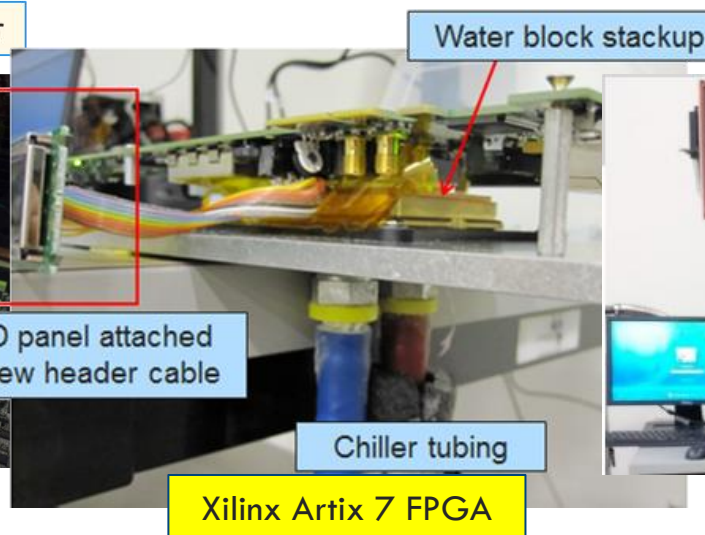
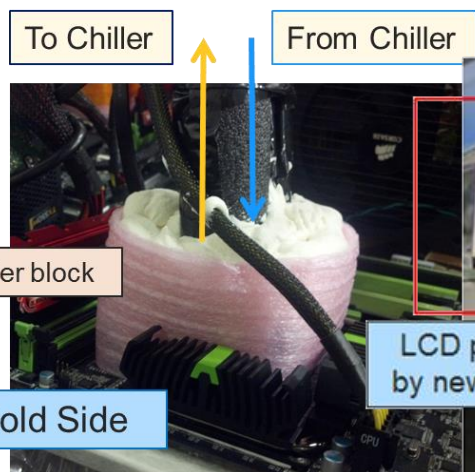
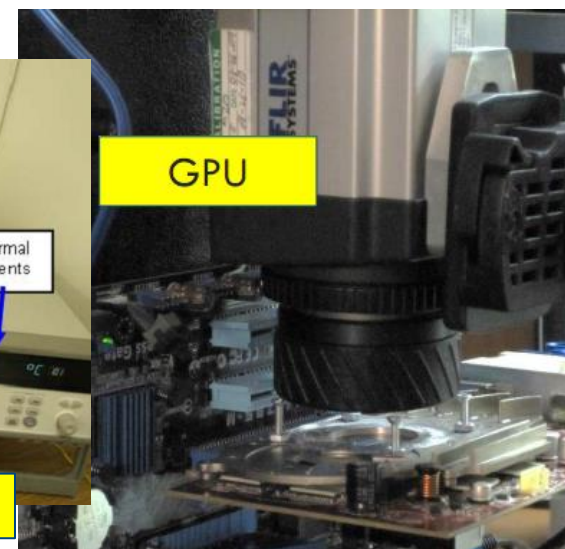
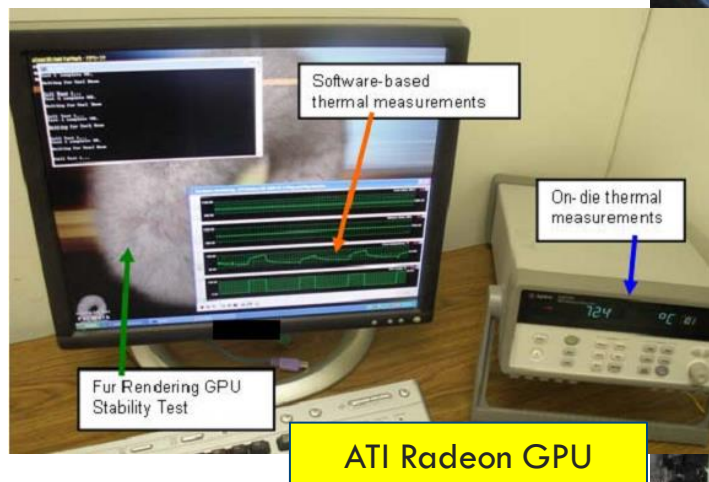
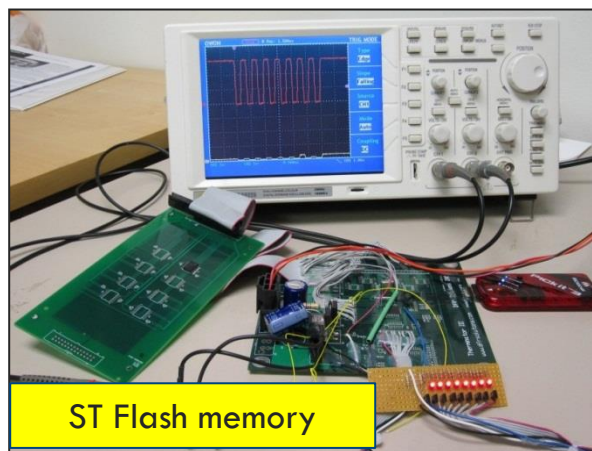
Temperature measurements during the 45°C Hot Dwell

Channels		Modify Y-Axis View				Current Data
ID Color	Graph	Scale Y	Move Y Ref			
101		8	C	40	C	57.25700 C
102		8	C	40	C	49.67800 C
103		8	C	32	C	56.92000 C
104		8	C	40	C	54.48000 C
105		8	C	40	C	56.82500 C
106		8	C	24	C	43.63700 C
107		8	C	32	C	45.90000 C
108		8	C	32	C	42.84700 C
109		8	C	32	C	43.46300 C
110		8	C	32	C	44.50900 C

Case temperatures

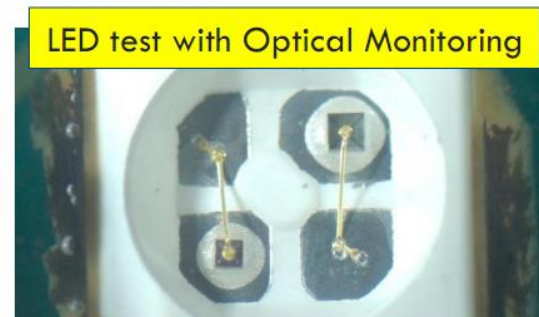
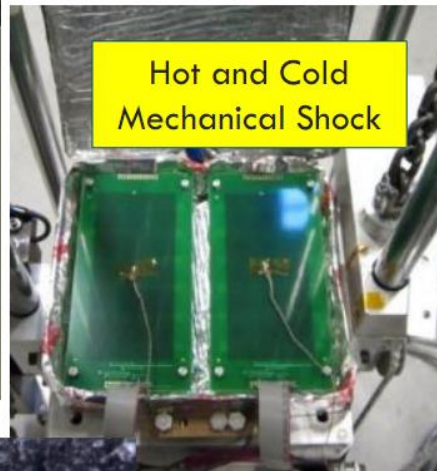
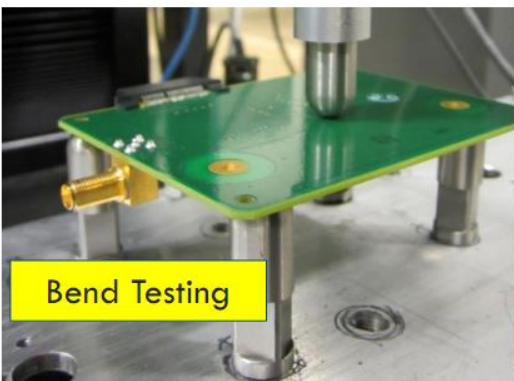
Ambient temperatures

Complex Integrated Circuits

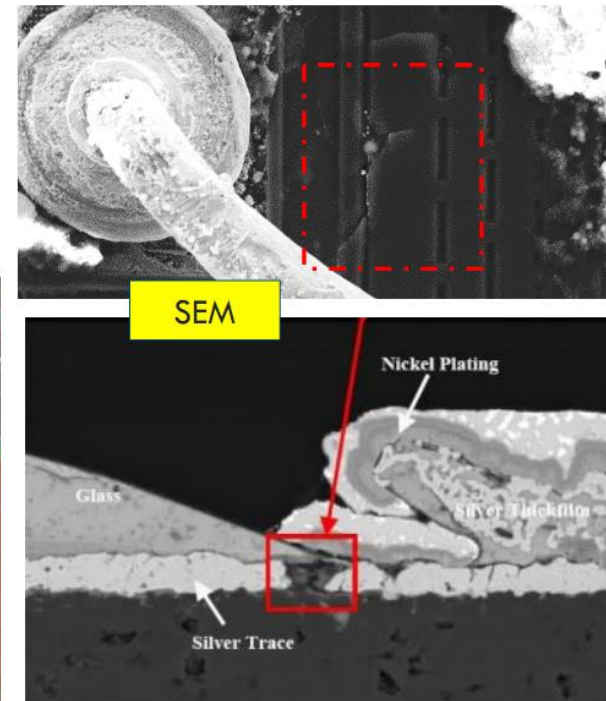
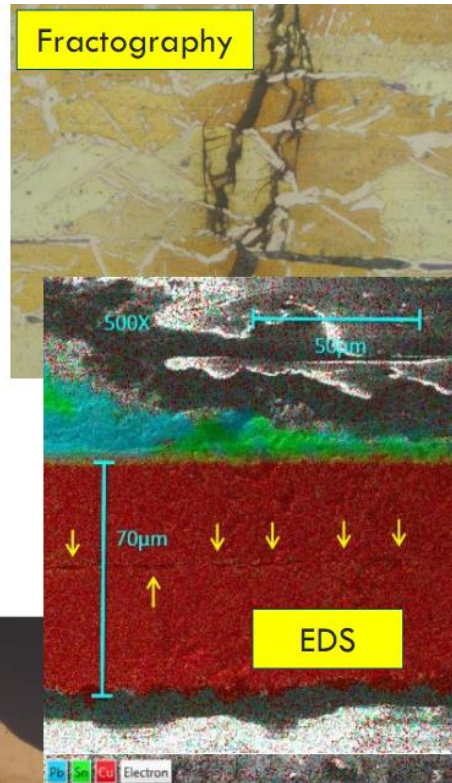
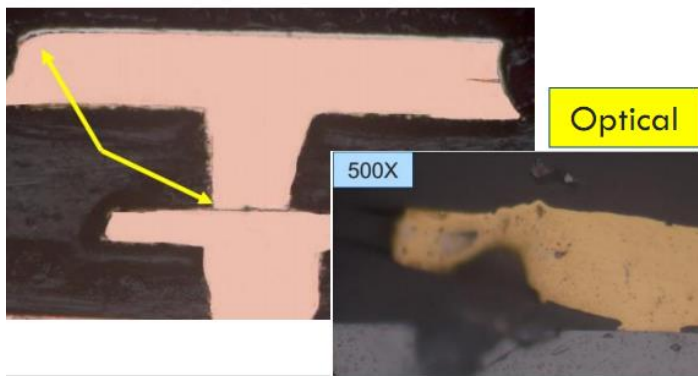
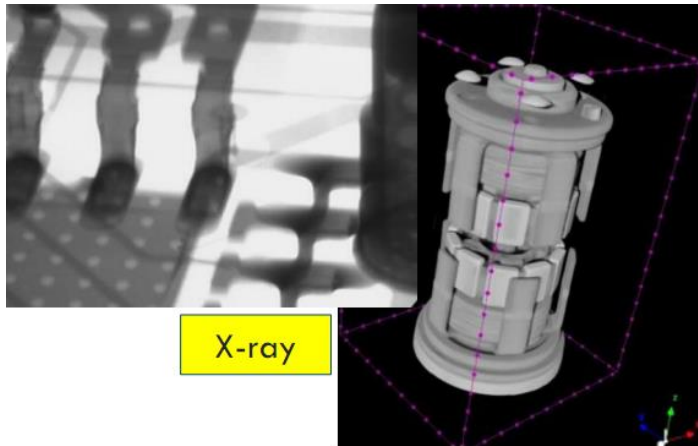


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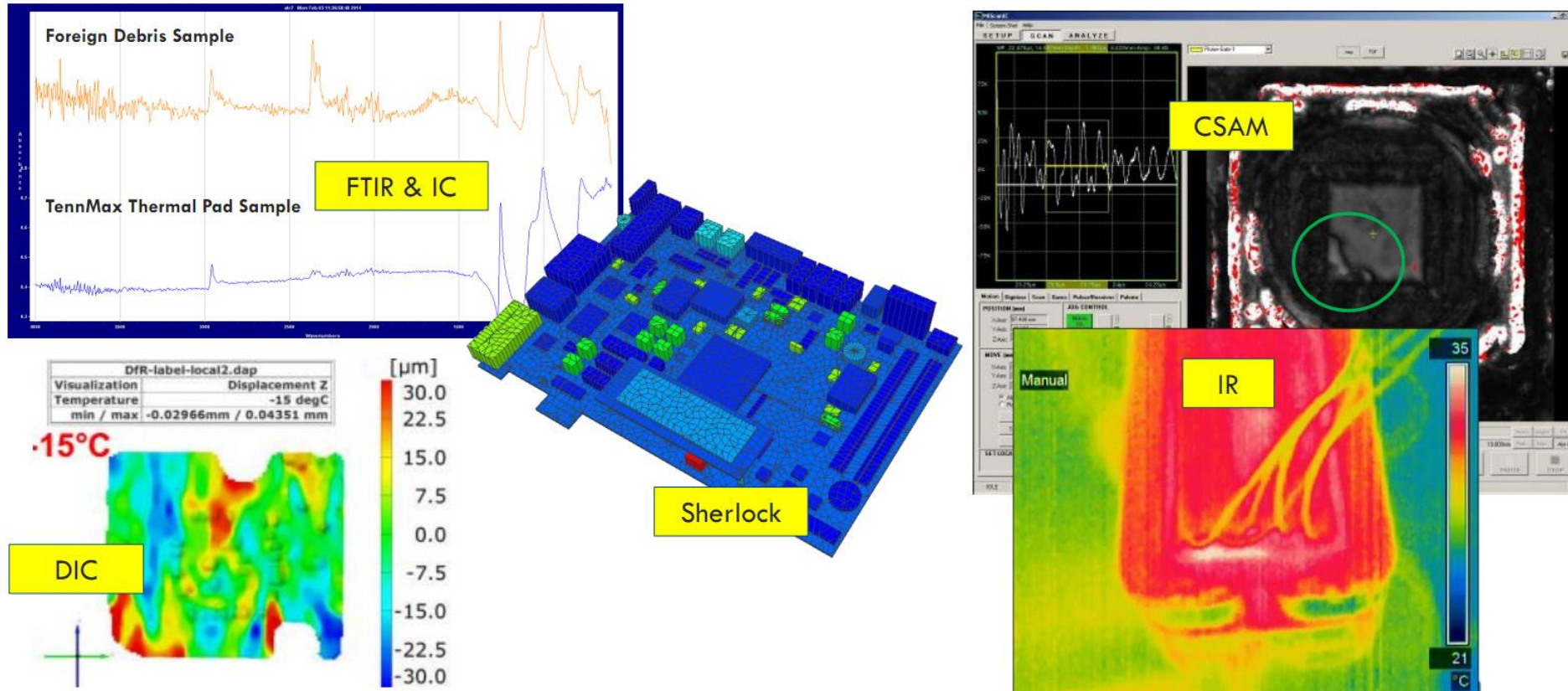
Package Level Testing



Failure Mode Identification

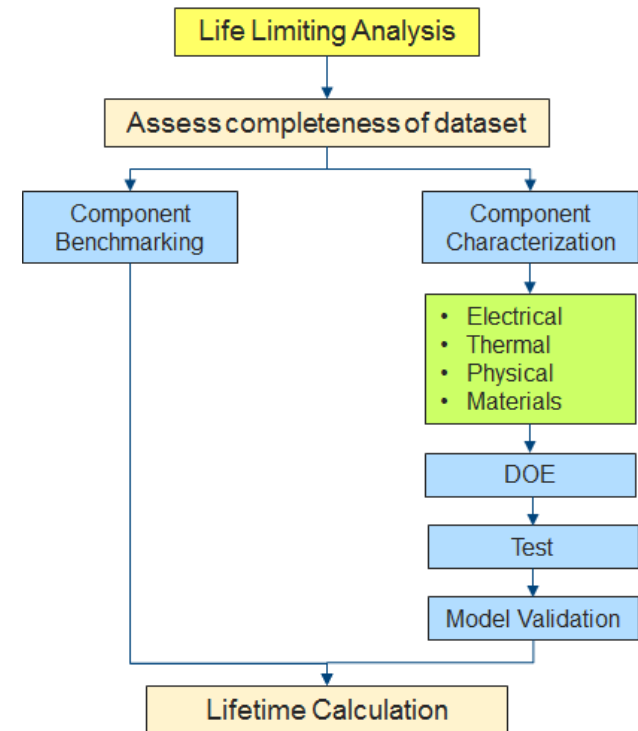


Failure Mode Identification (Cont'd)



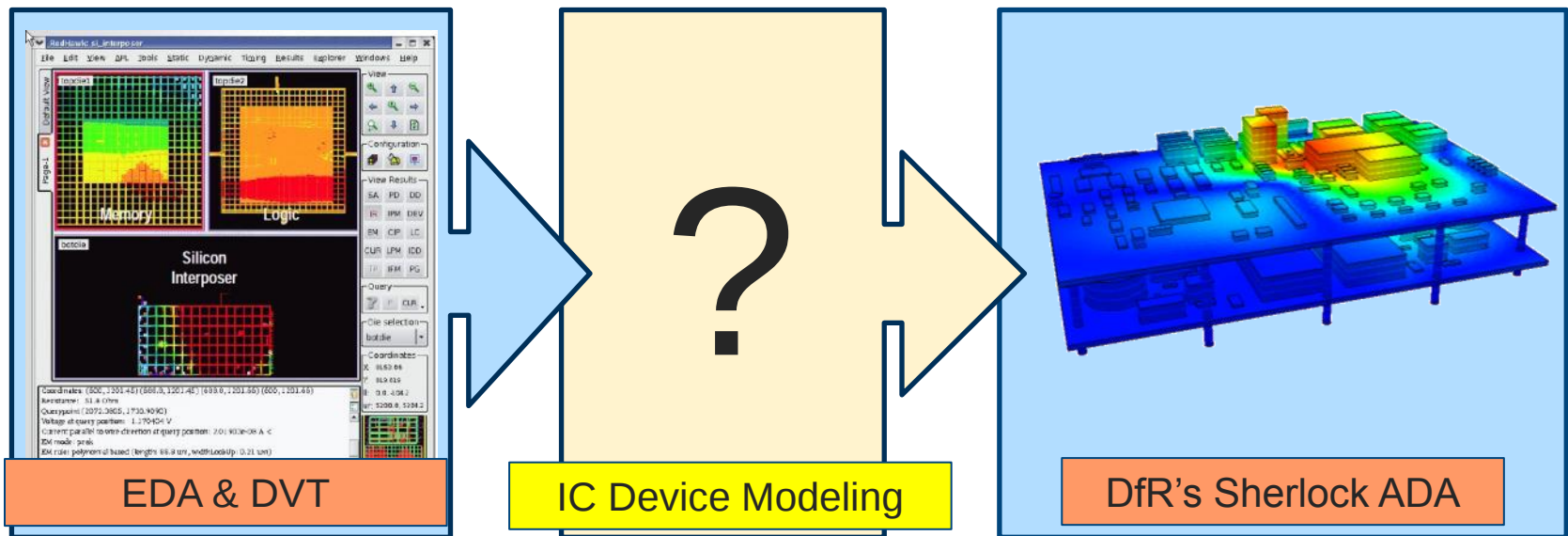
Modeling Capabilities

- DfR Solutions has turnkey solutions for component modeling to include its Sherlock ADA software, IC Wearout tool and FEA modeling integration with Sherlock using Abaqus and Ansys
- Allow us to rapidly model mechanical and thermal behavior of electronic components
- DfR validates and develops these models through in-house testing and analytical techniques
 - Thermal cycling and constant temperature, humidity, vibration, mechanical shock
 - SEM/EDX, FTIR, XRF, Digital Image Correlation, Dynamic mechanical analysis



Predictive Modeling – Integrated Circuits

- Predictive modeling tools using test structure experimental data, physics, materials and layout geometries have shown to be a critical tool in assessing the reliability of electronics. Reliability tools exist for device designers and board level analyses.



- A reliability prediction process that uses accelerated test data of commercial off the shelf (COTS) devices, thermal and electrical stress conditions similar to field applications, and device complexity metrics are necessary to create a device level reliability modeling tool.

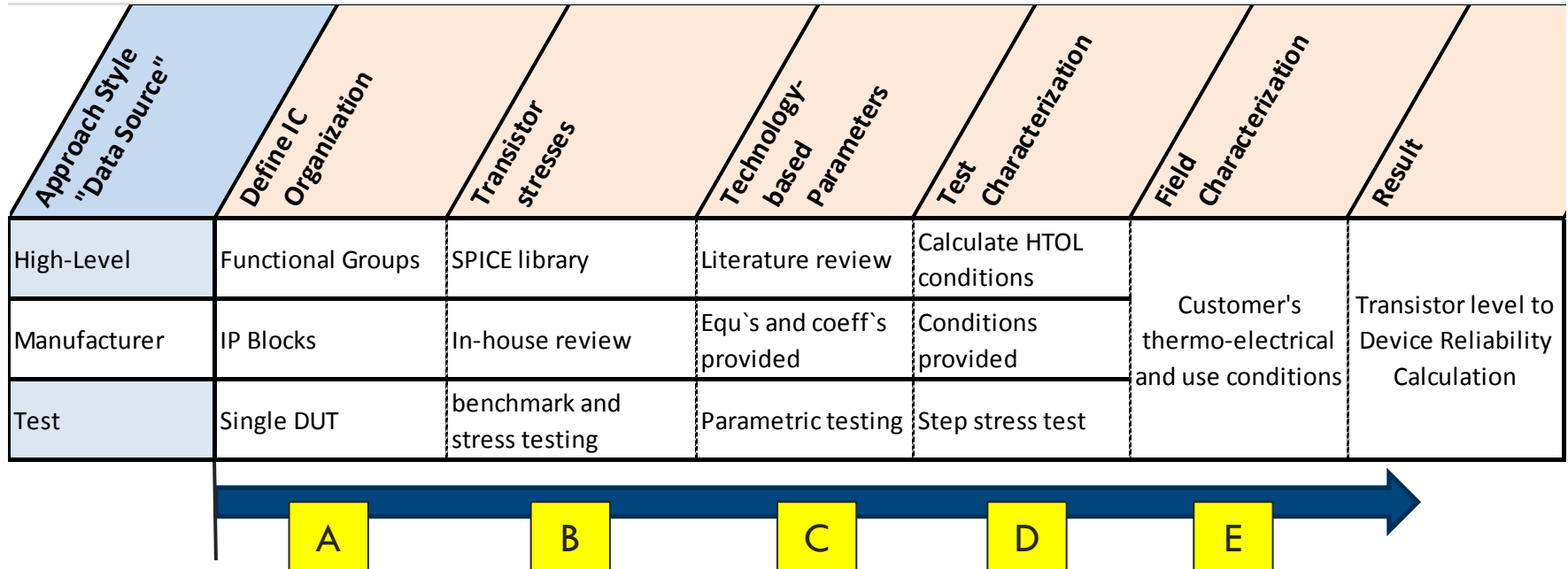
Should We Be Concerned About Life Limited Components?

- *It is a fallacy to say that integrated circuits will not fail because they have no moving parts. The sole reason they work is by the movement of charge carriers (electrons and holes) within them.*
- **Having a proactive understanding of mechanisms inherent to semiconductor devices...**
 - Failure signatures are often misinterpreted as electrical overstress, electrostatic discharge or caused by poor quality substrates that should have been screened out of production
 - Blame is placed on application, usage profile and environment rather than design or component selection

"The notion that a transistor ages is a new concept for circuit designers," ... aging has traditionally been the bailiwick of engineers who guarantee the transistor will operate for 10 years or so...But as transistors are scaled down further and operated with thinner voltage margins, it's becoming harder to make those guarantees... transistor aging is emerging as a circuit designer's problem.

IEEE Spectrum, June 2009

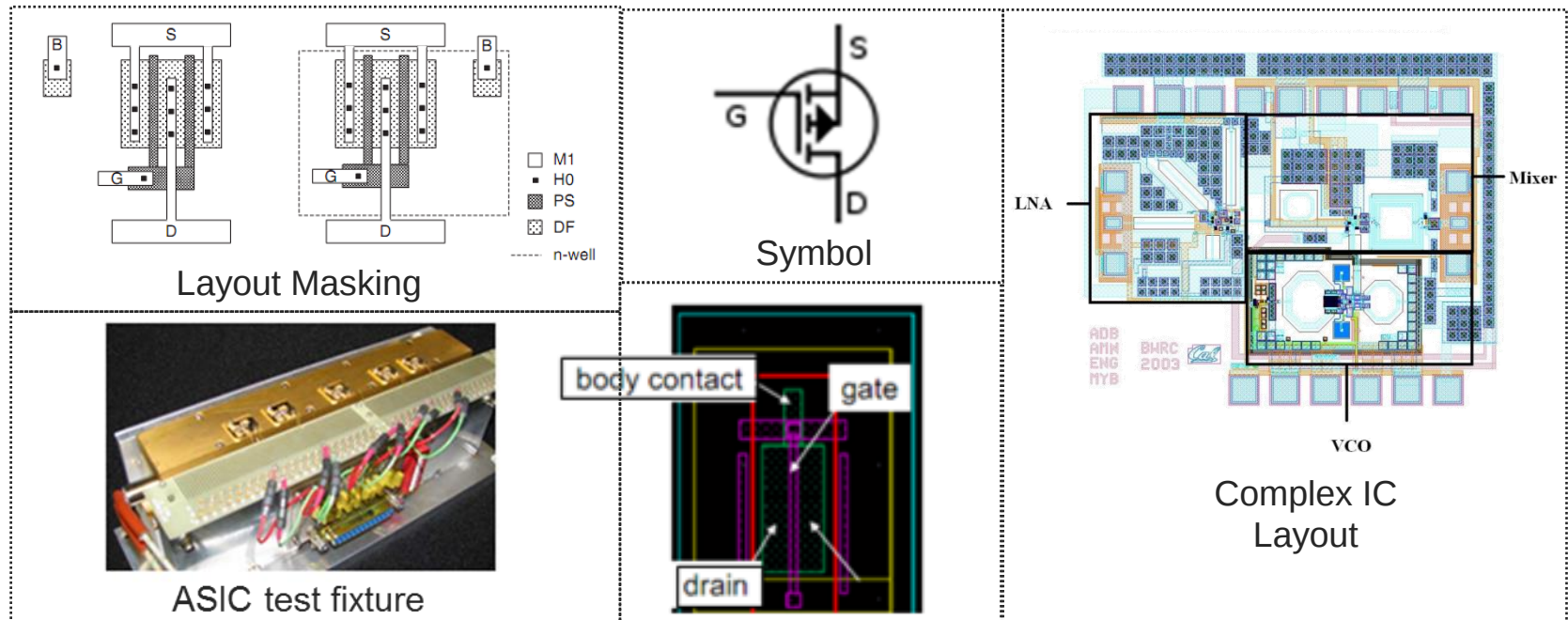
Integrated Circuit Wearout Assessments



"Horizontal (multiple source) flow"

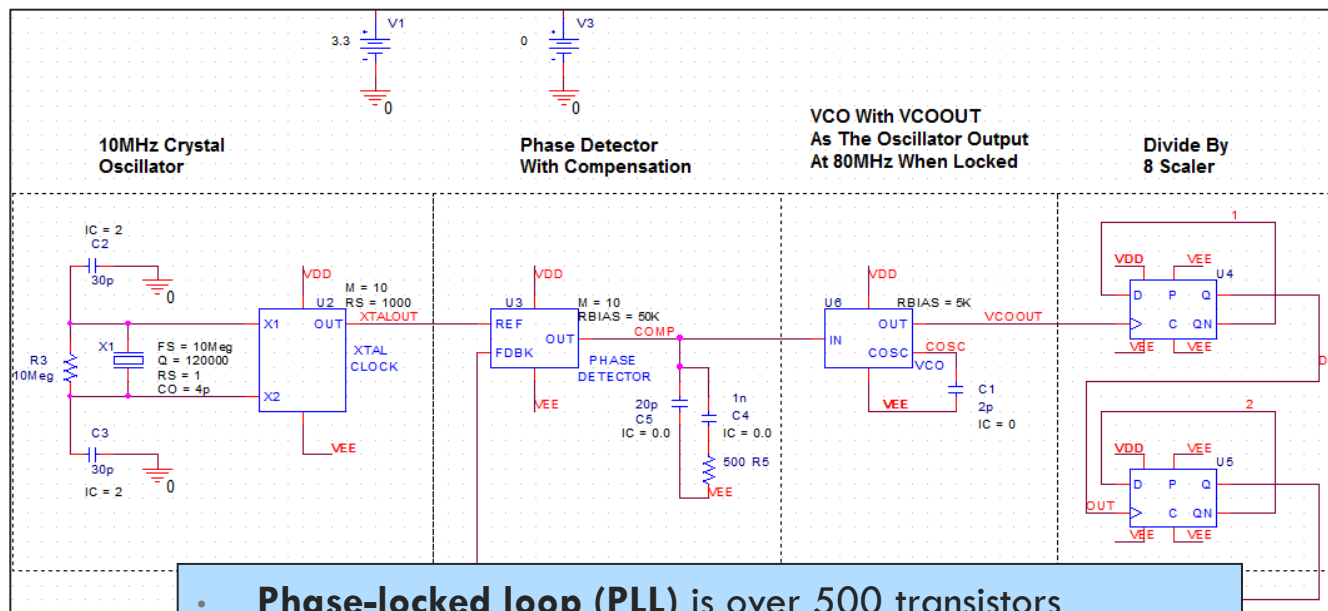
[A] Device Characterization

- Complex ICs can be resolved as being built from IP blocks or considered a single DUT
- Ideally, all IP blocks can be classified as an organization of transistors
- Testing or simulations performed on IP blocks with measureable parameters can determine mechanism weighting factors from electrical conditions and material properties



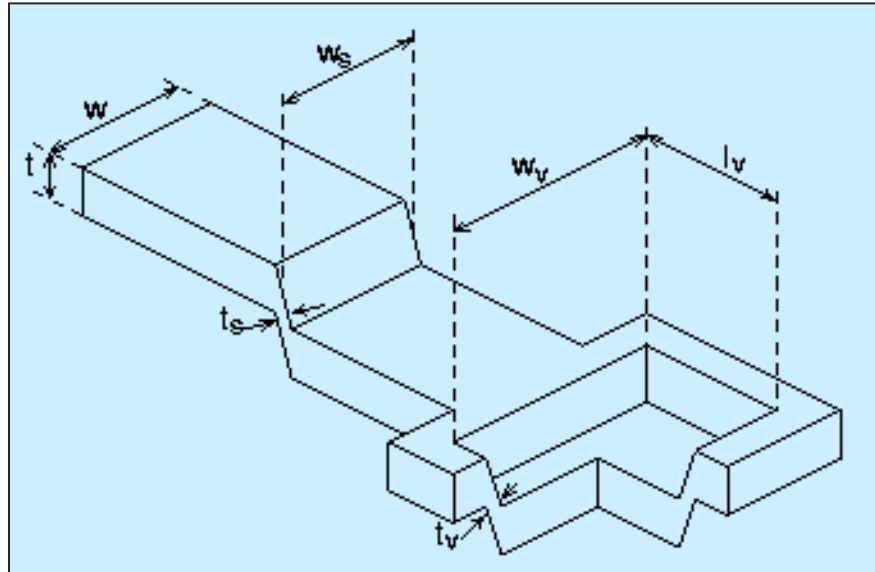
[B] Transistor Stresses

- Establish relevancy of failure mechanisms, weighting factors and inputs into Physics-of-Failure algorithms based on
 - Quantity and location of transistors within circuit (SPICE benchmarking)
 - In situ characterization using circuit-level stress loading (Device testing)



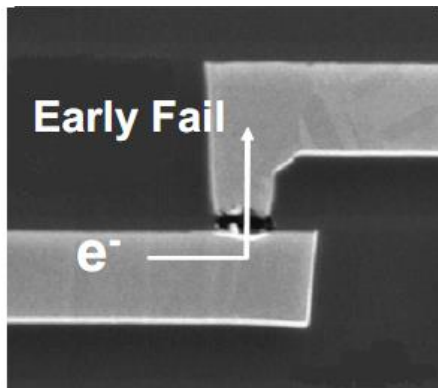
- Phase-locked loop (PLL)** is over 500 transistors
- Circuit designed using **CMOS library** and components built from transistor models
- All transistors are analyzed against electrical criteria

[C] Technology Parameters



- Electromigration
- Dielectric Breakdown
- Bias Temperature Instability
- Hot Carrier Effects
- Solder Fatigue

$$t t f_x = A_x * w * t * J^{-n} * e^{(E_a/kT)}$$



Shift in orientation of lattice (boundary)



Homogeneous lattice of metal atoms (grain)

Triple point

*electromigration modeling shown

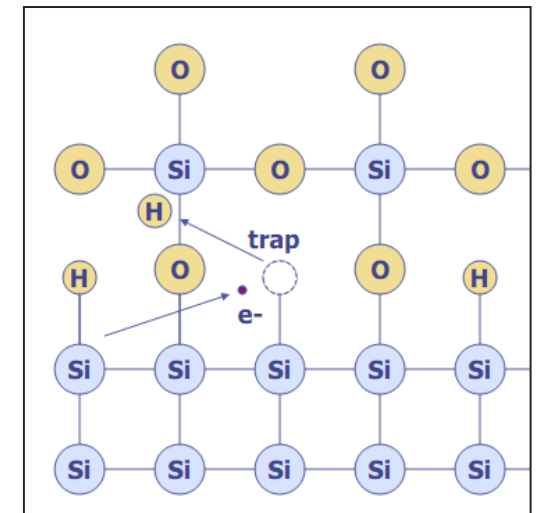
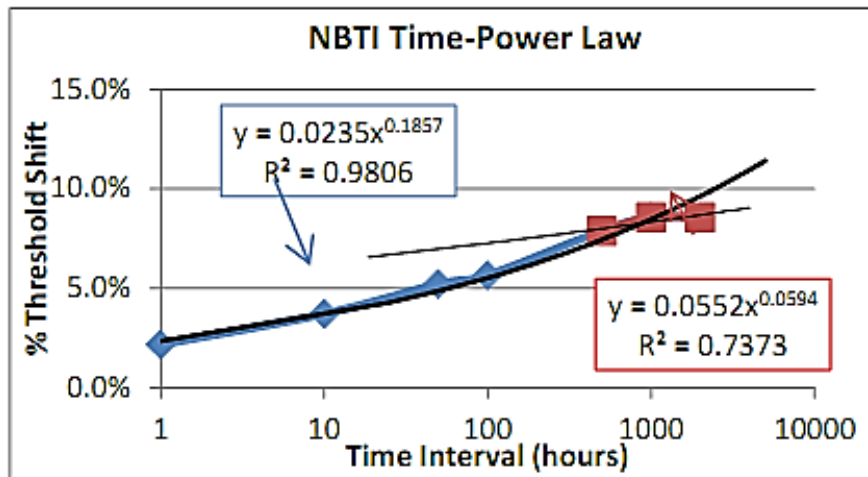
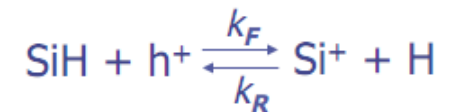
[D] Test Characterization

- **Test Conditions**
 - Apply drain bias and step stress gate voltage
 - Monitor drain current and gate voltage (V_{th})
- **NBTI Model**
 - Plot electrical parameters
 - Resolve NBTI voltage coefficient from plot of V_{th} shift

$$\Delta V_T(t) := t^n$$

Time-Power Law

Reaction-Diffusion Model (RD)



Manufacturer/Testing Approach

Presented at IRIC '13 and MAPLD '13

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[E] Field Correlation

Example from NBTI ASIC Case Study

Table 1: NBTI and PFET Model Parameters

Variable	Stress Value	Nominal Field Value
Drain Voltage (V _D)	0.0V	-0.9V
Gate Voltage (V _G)	-1.0V	-0.9V
Temperature	125°C (398.15 K)	35°C (308.15 K)
Voltage Constant (γ)	5.39	
Boltzmann's Constant (k _B)	8.61734E-5 eV/K	
Activation Energy for NBTI	0.2eV	
Ideal Drain Current (I _d)	26.25 micro-amps	
Width of Transistor (W)	21 micron	
Length of Transistor (L)	56 nanometer	
Thickness of Oxide (t _{ox})	1.16 nanometer	
Threshold Voltage (V _T)	0.3 Volts	

$$\lambda_T := N * \sum \left(\frac{N_F}{N} \right) * P_F * \sum (K_{i,F} * \lambda_i)$$

Failure Rate of Complex IC

- Number of unique functional groups
- Total number of functional groups
- Contribution to functional group failure of each mechanism

$$AF_{NBTI} := \left(\frac{V_{gs1}}{V_{gs2}} \right)^{\gamma} e^{\left(\frac{E_a}{k} \frac{T_1 - T_2}{T_1 T_2} \right)}$$

Acceleration Transform for NBTI

$$\lambda_{use} := AF_{NBTI}^{-1} * \lambda_{stress}$$

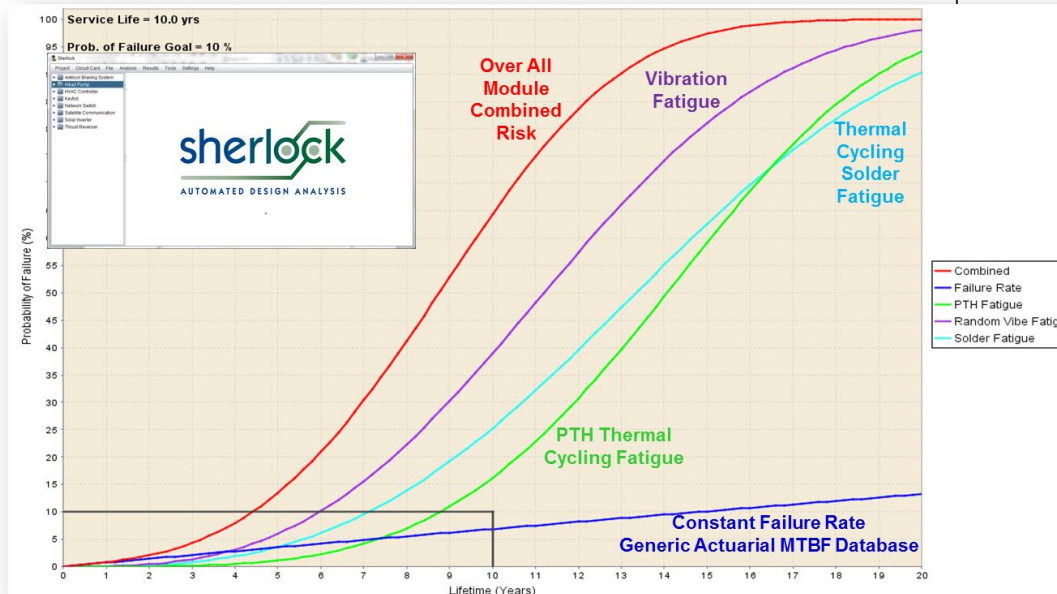
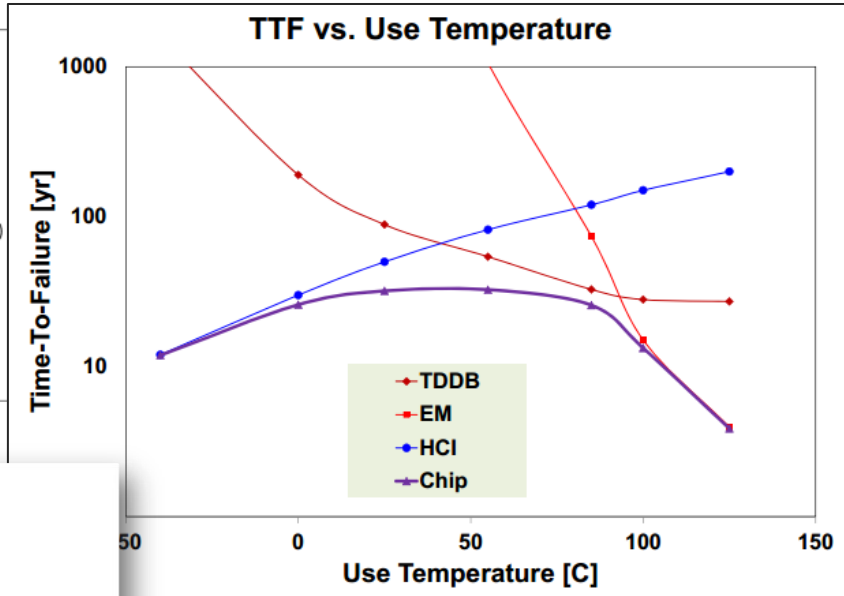
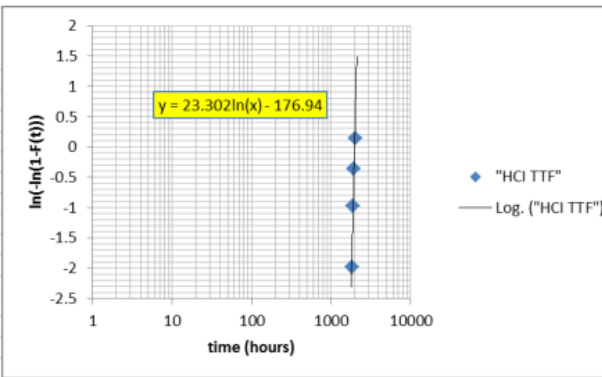
Correlation to field stress

- Calculation was performed on one PFET using the individual PFET model
- Acceleration factors of **1.75X voltage** and **5.5X temperature**

Reliability Prediction – Determining MTBF

TTF (hours)	RANK	Median Rank Estimation (CDF)	$\ln(-\ln(1-F(t)))$
1848	1	0.1296	-1.974458694
1896	2	0.3148	-0.972686141
1920	3	0.5000	-0.366512921
2016	4	0.6852	0.144767396

Bernard's Equation: Median Rank = (Rank - 0.3) / (# Samples + 0.4)	
Samples	5
best fit parameters	
m	23.302
y-int	-176.94
MR(Eta)	-0.00032771 [LN(-LN(1-0.632))]
Eta (hours)	1985 ~ falls within sample set



Integrated Circuit Wearout Study @ DfR Solutions

- **Phase I – Component Feature Identification/Classification Process Development:**
 - Perform a study to investigate a processes in which to identify material and layout geometries of commercial devices in a low cost, highly repeatable method. The ability to categorize device complexity and utilization of its features in terms of electrical and thermal stressors will be demonstrated at two technology nodes for each device type under analysis.
 - Realistic model constituents: die size & materials, die attach, wire bonds, package style and materials, solder joints (2nd level), PCB stackup and thermal solution
- **Phase II – Predictive Model Development:**
 - Develop and demonstrate a reliability prediction process for commercial devices at sub-micron technologies. Field-based application testing of commonly used integrated circuits will be performed to provide a baseline for the reliability of specific device features under high stress conditions. Reliability of device features should be expressed as normalized values directly related to measureable physical parameters of integrated circuits.
 - DfR has developed a stress test process for CPU, GPU, FPGA, Flash memory
 - DfR has package, solder joint and PCB stackup features within its Sherlock ADA tool
- **Phase III – Process Automation and Tool Development:**
 - Optimize the data gathering and testing methodology above to streamline the process using automated visual recognition of device features and inputs of thermal stress using digital image correlation and IR imaging. Develop a smart user interface with database for rapid identification of device complexity to feed the predictive model.
 - Create a 3D model of physical stackup of device on 2"x2" PCB for trade-off analysis of thermal and electrical profiles

- Questions, comments, and feedback can be directed to:

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ewyrwas@dfrsolutions.com

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- For information on Sherlock Automated Design Analysis™ or to access free white papers on various reliability topics:

www.DfRSolutions.com