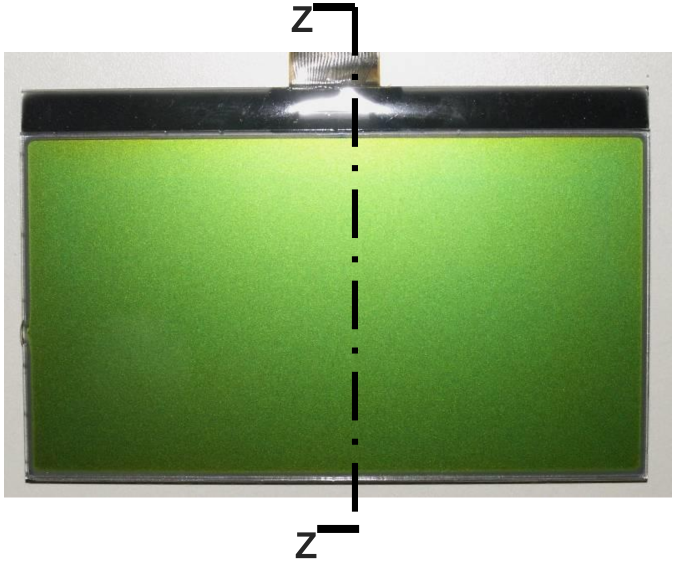
LCD Failure Modes – It's All About Quality

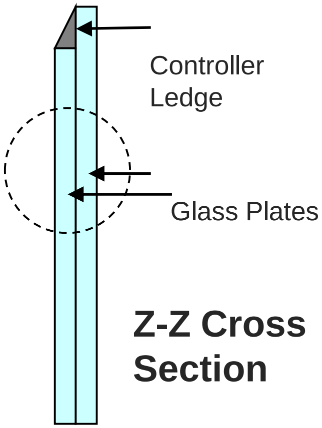
Edward Wyrwas

Experimental Procedure

- DfR Solutions performs a systematic process to investigate the cause of failure in LCD modules. The assessment focuses on the constituents of the assembly where process variability may occur.
- When evaluating LCD modules, the most common location of issues is at the ledge, where the LCD is bonded to the flex circuit using an anisotropic conductive film (ACF) and then sealed to prevent moisture ingress.

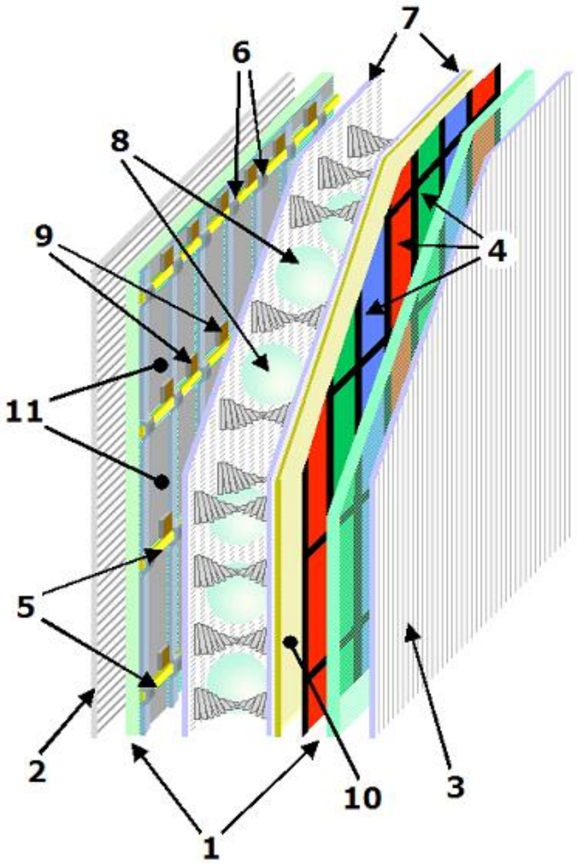


Generic LCD Module Diagram



Z-Z Cross Section

Background: LCD Construction

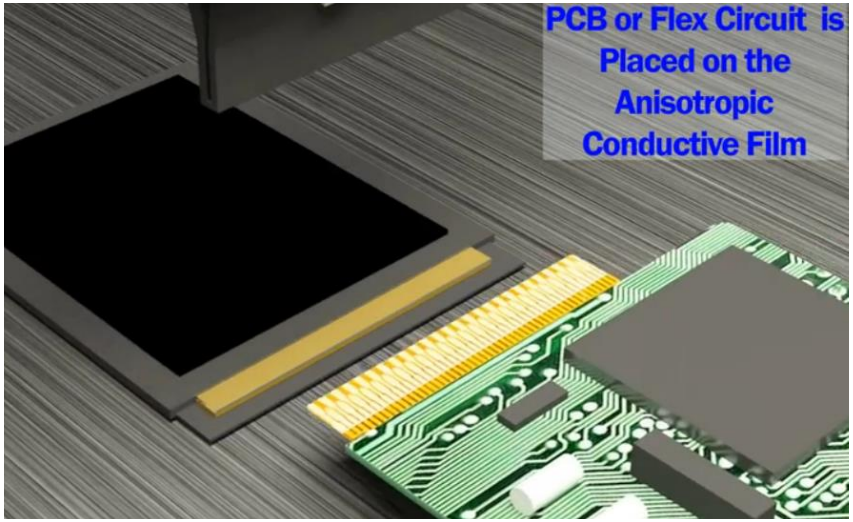


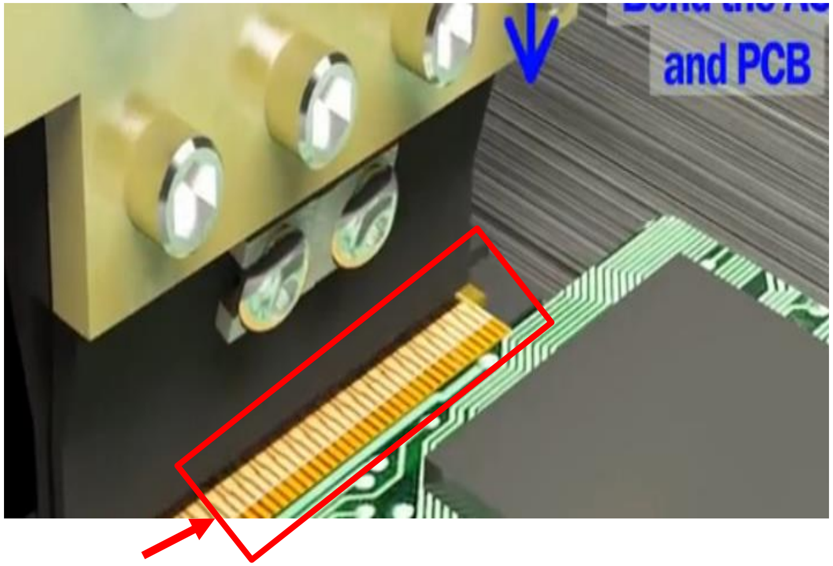
1. Glass substrates
2. Horizontal polarizer
3. Vertical polarizer
4. RGB color filter
5. Horizontal control lines
6. Vertical control lines
7. Polymer layers
8. Spacers
9. Thin Film Transistors (TFT)
10. Front Electrode
11. Rear electrode

- Inspection of LCD devices requires a high magnification microscope (200-500X magnification) with the capability to focus “through” the surface to inspect constituents located between the sandwiched glass

LCD Technology: Anisotropic Conductive Adhesive (ACA)

- Anisotropic Conductive Adhesive or ACA is an epoxy system used to make electrical connections between drive electronics and substrates such as chip on glass (COG) and flex on glass (FOG)

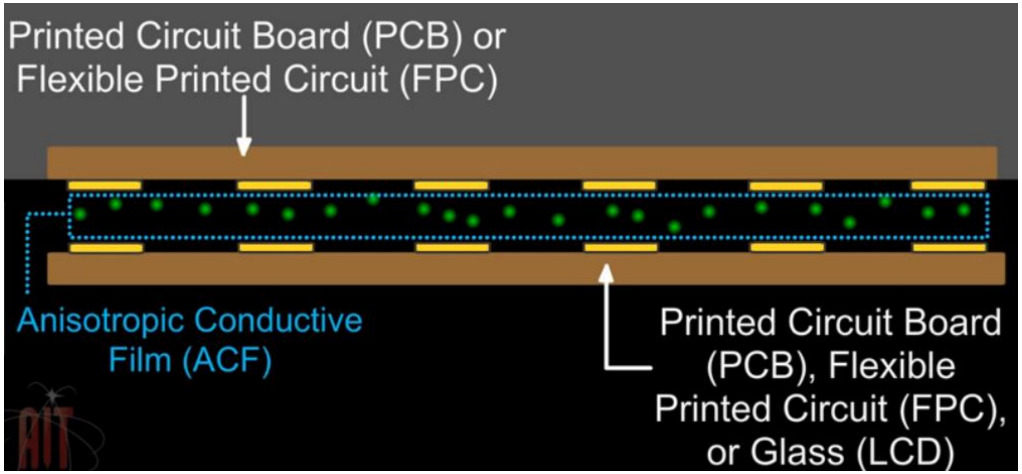


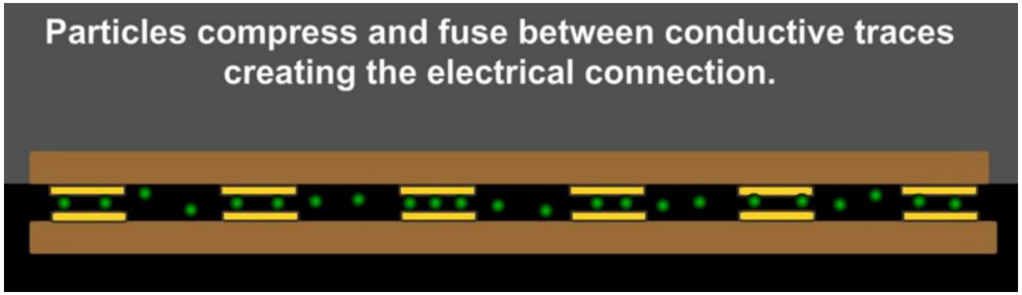


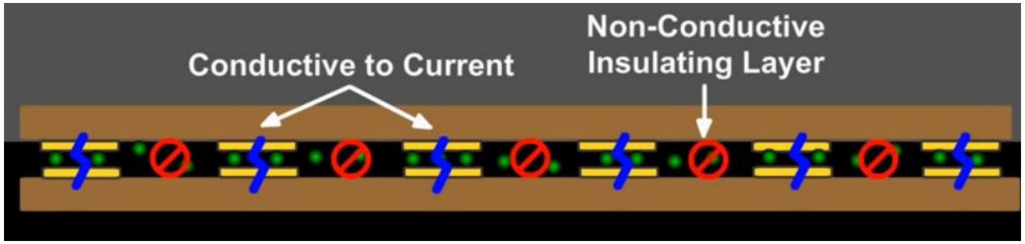
What takes place in this sandwiched interface is depicted on the next slide

LCD Technology: ACA (Cont'd)

- Process control is important to ensure the ACA, Glass, COG and hot bar all are flat
- Temperature (inductive heating), force, x-y-z alignment, and z-travel are parameters that should be calibrated before production




Particles compress and fuse between conductive traces creating the electrical connection.



Common Defects in LCD Modules

Defect	Occurrence (% of Total)
Point defect	32.6
Particles, scratches, dirt	24.7
Breakage	4.9
Line Defects	7.7
Faulty Cell Gap	6.1
Other	20.4

Reference: Liquid Crystal Flat Panel Displays: Manufacturing science and technology
By William C. O'Mara

- The failure mechanisms and defects discussed are:
  - Stuck pixels (TFT failure)
  - Spacers non-uniformity
  - TFT delamination
  - Display bulging
- This assessment will also focus on the following items (not in order):
  - Perimeter sealant
  - Liquid crystal fill plug
  - Ledge sealant
  - Anisotropic conductive adhesive
  - Chip on Glass
  - Flex Assembly
  - Any electrical or signal anomalies

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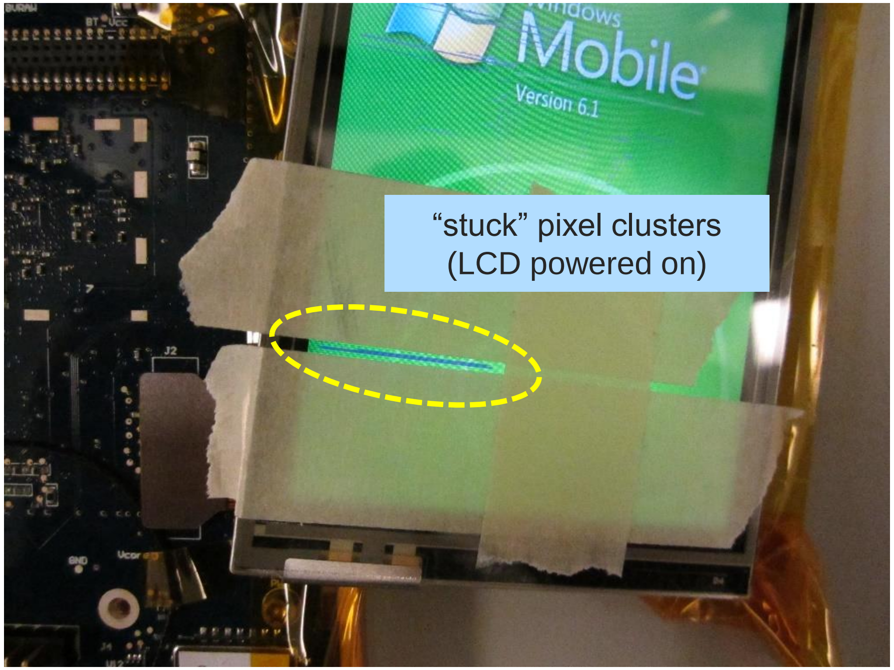
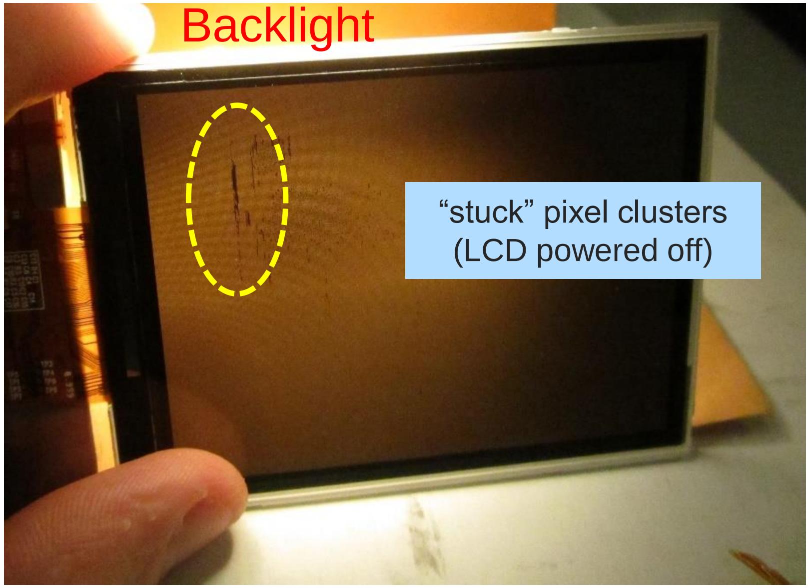
- Let’s Discuss Pixel Anomalies

Stuck On vs Stuck Off Failure Behavior





- The failed and intermittently failed LCD modules had characteristics of “stuck” pixel clusters in the powered on or powered off states

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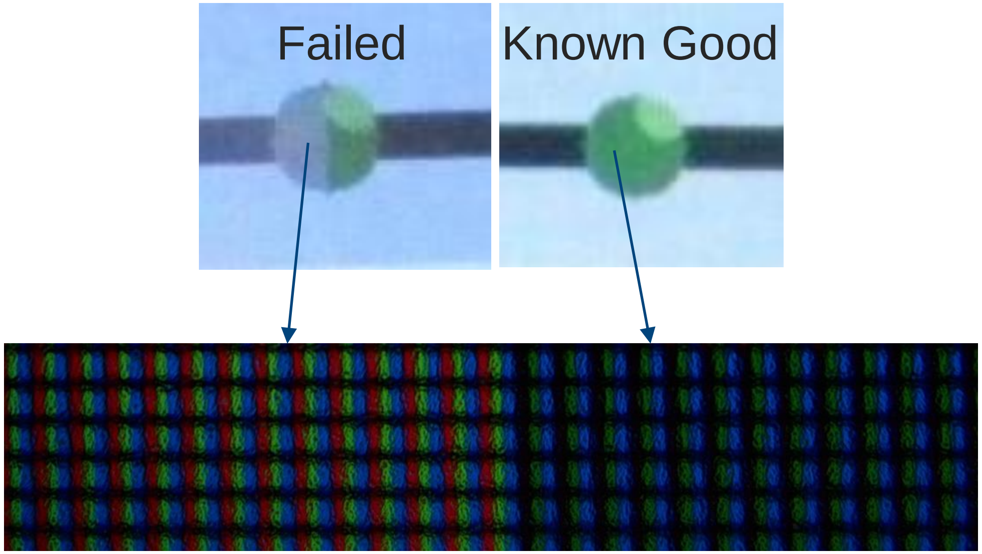
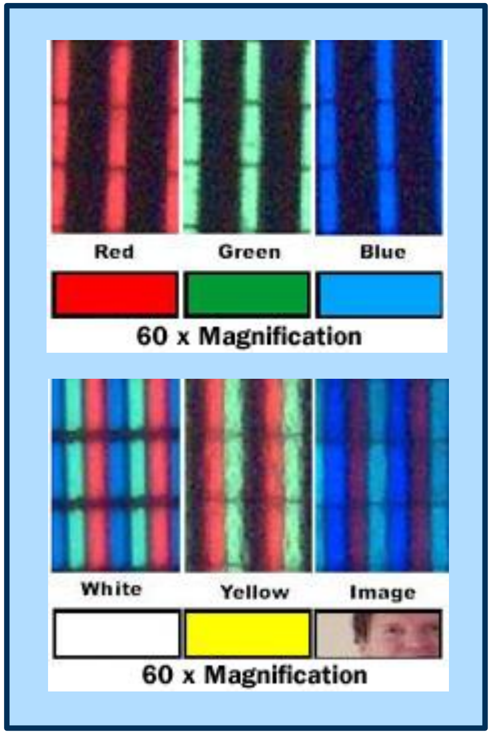
Grayscale Failure Behavior

- Example: The characteristic of failure is lack of green pixels on the left side of the display
  - Upon investigation we find the red channel was constantly toggling on and off which is making the image gray scale

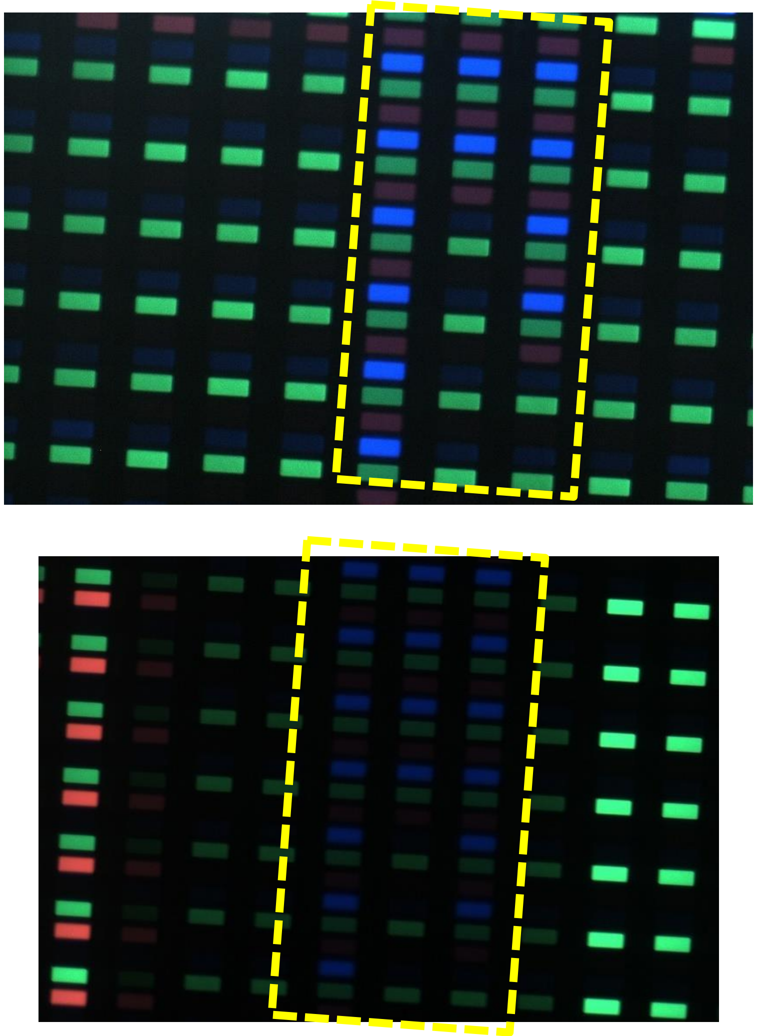


Red present

No Red present



Behavior: Pixels Stuck On



- Blue and red pixels are illuminated when they shouldn't be
- Screening process:
  - Power up LCD on inverted microscope
  - Using a *dark-field* filter, focus on glass in front of color filter
  - Examine pixel array colors using solid color palette of red, blue, green, white and black
- Failure mechanism:
  - Electrical short in TFT matrix and/or electrical continuity issues with the chip-on-glass

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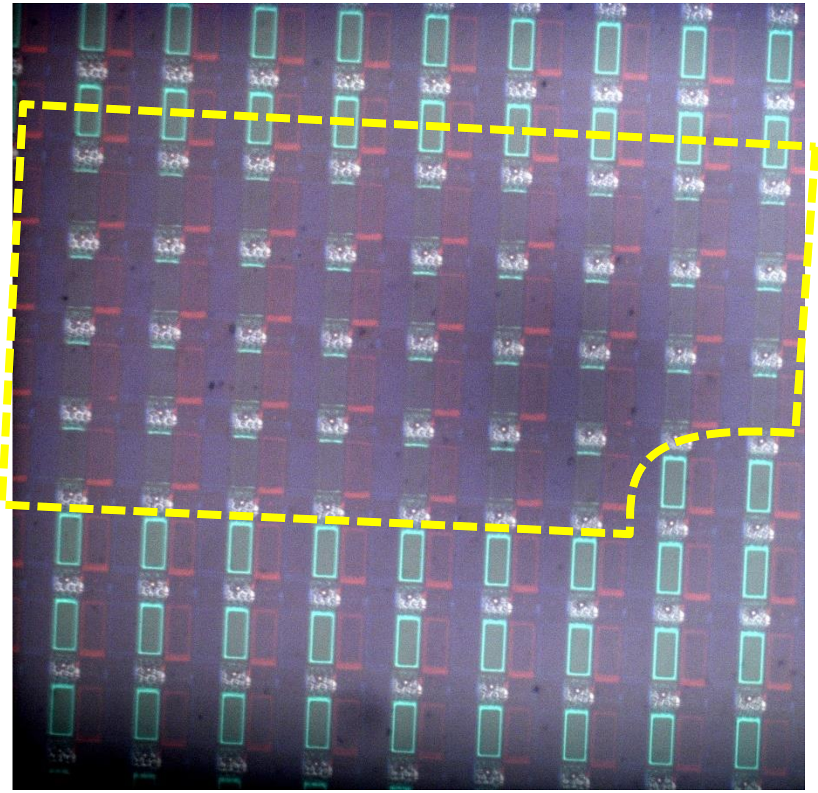
Behavior: Pixels Stuck Off



- Green and red pixels do not illuminate when they should be
- Screening process:
  - Power up LCD on inverted microscope
  - Using a *bright-field* filter, focus on pigment color filter within glass sandwich
  - Examine pixel array colors using solid color palette of red, blue, green, white and black
- Failure mechanism:
  - Electrical open in TFT matrix and/or electrical continuity issues with the chip-on-glass

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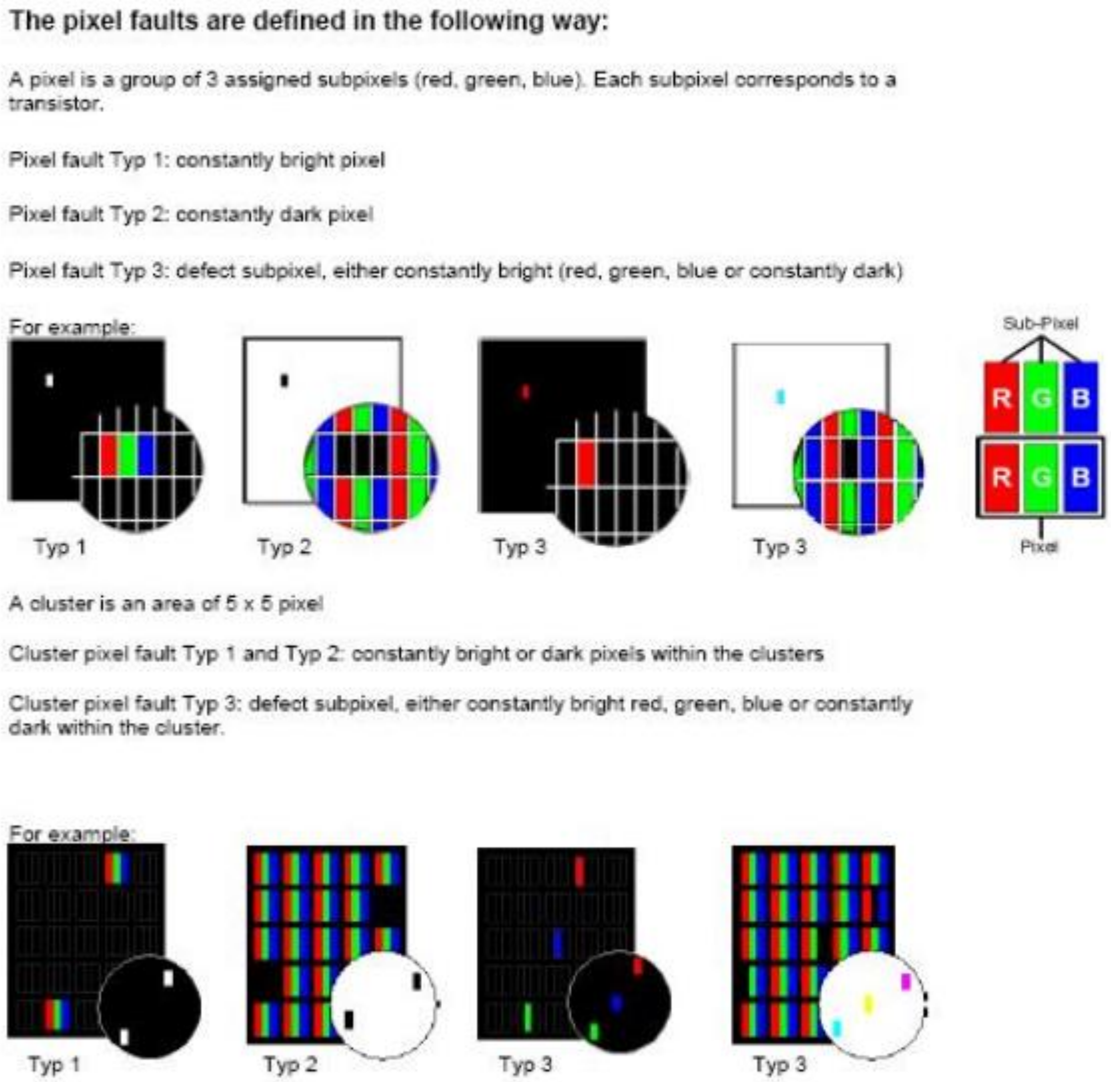
Discussion: Pixel Fault Definitions



The pixel faults are defined in the following way:

A pixel is a group of 3 assigned subpixels (red, green, blue). Each subpixel corresponds to a transistor.

Pixel fault Typ 1: constantly bright pixel

Pixel fault Typ 2: constantly dark pixel

Pixel fault Typ 3: defect subpixel, either constantly bright (red, green, blue or constantly dark)

For example:

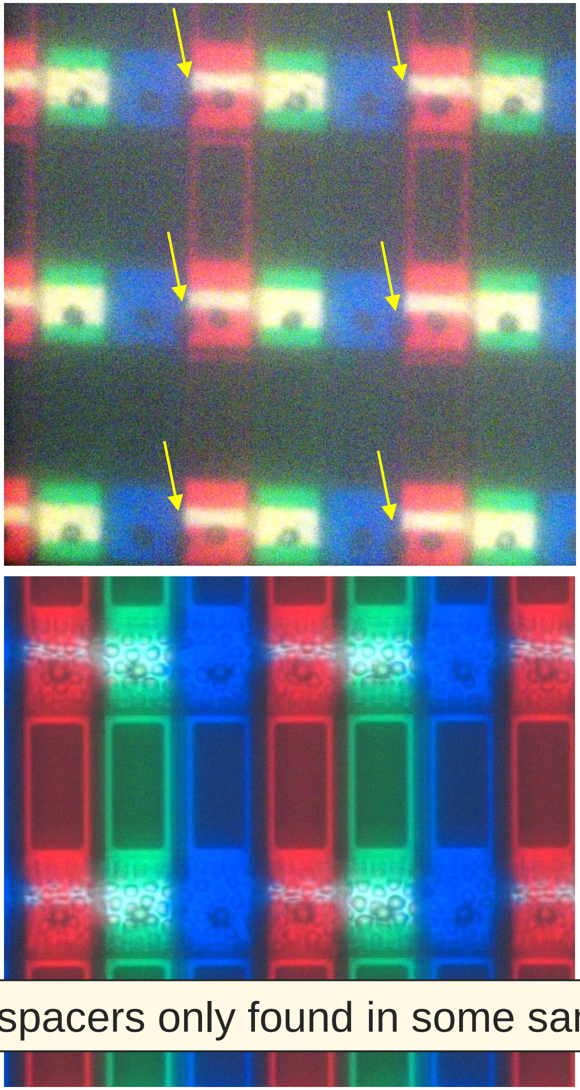
A cluster is an area of 5 x 5 pixel

Cluster pixel fault Typ 1 and Typ 2: constantly bright or dark pixels within the clusters

Cluster pixel fault Typ 3: defect subpixel, either constantly bright red, green, blue or constantly dark within the cluster.

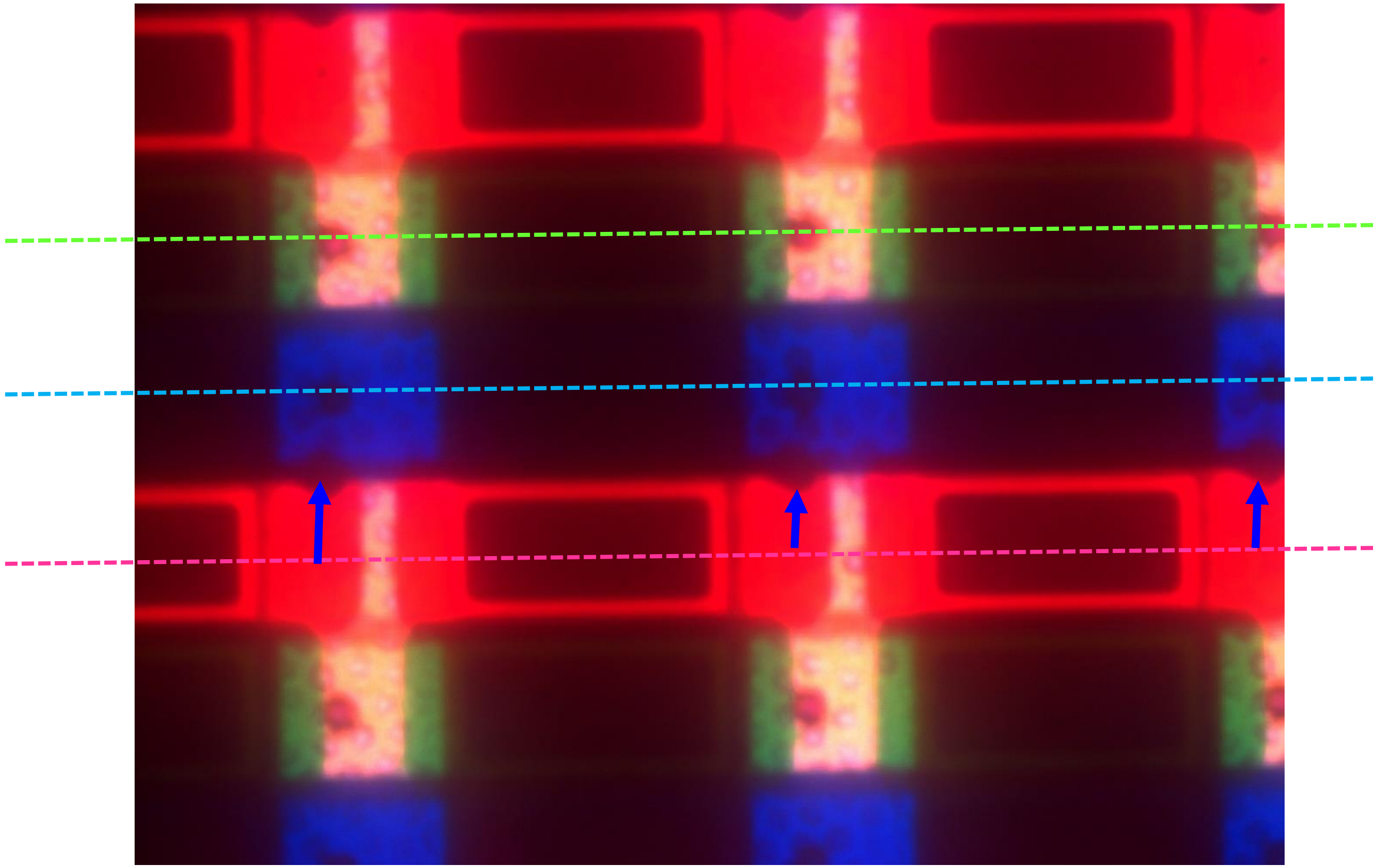
For example:

Non-Uniformity of Spacers/Extra Spacers


Extra spacers only found in some samples

- Pixels do not illuminate when they should be
- Screening process:
  - Power up LCD on inverted microscope
  - Using a *dark-field* filter, focus on pigment color filter within glass sandwich
  - Examine pixel array colors using solid color palette of red, blue, green, white and black
- Failure mechanism:
  - Non-uniformity in cell gap height causing active-unfilled area

Non-Uniformity of Spacers/Extra Spacers or Debris (Cont’d)



Green sub-pixel spacers

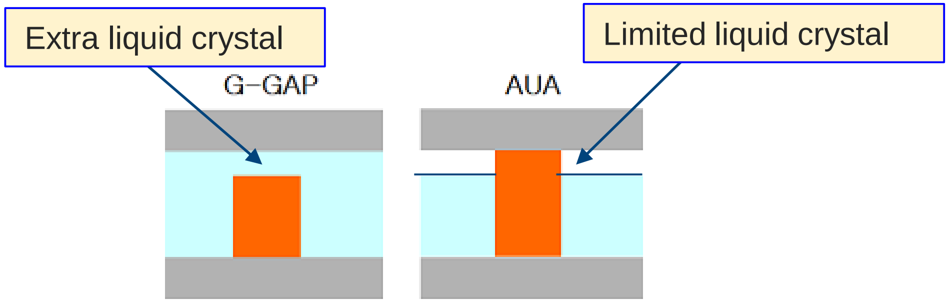
Blue sub-pixel spacers

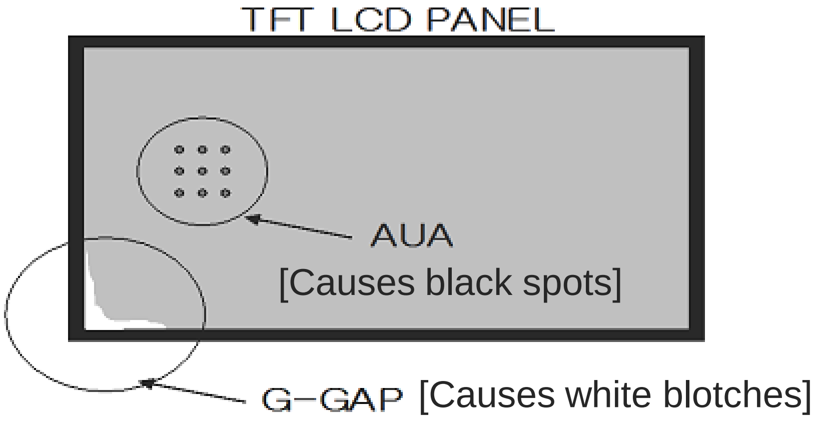
Red sub-pixel spacers aren’t where they should be

The spacers are supposed to be patterned on the color filter glass at each sub-pixel

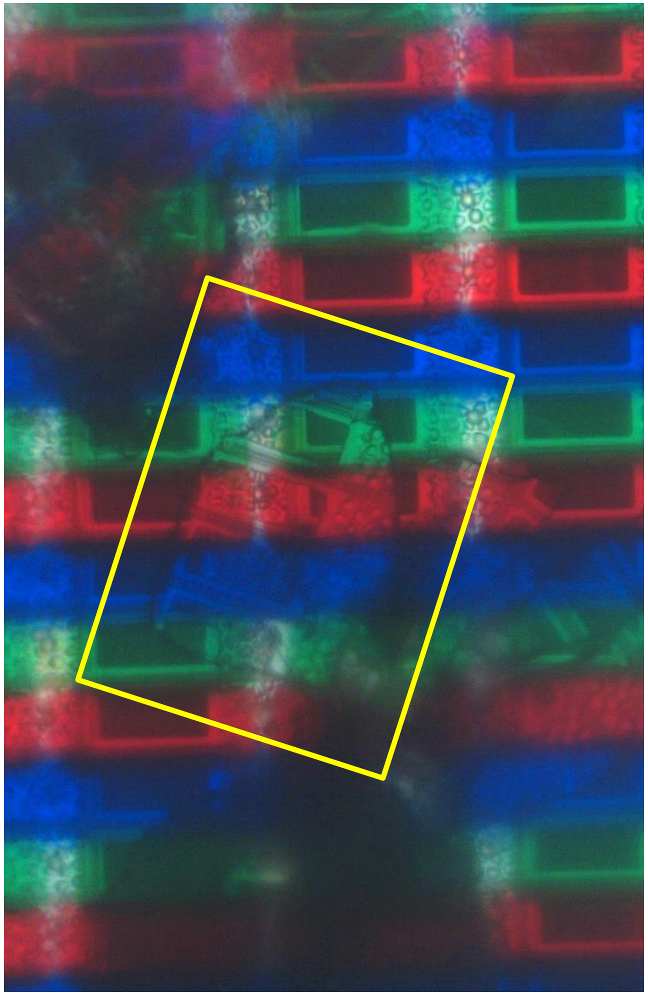
Discussion: Uniformity of Spacers

- Defects of LCD panel such as an active unfilled area (AUA) or gravity gap (G-GAP) come from the non-uniformity of the spacer thickness which depends on the liquid crystal's filling state (a function of temperature, compression of the glass and vacuum of the fill environment).
  - Gravity gap: the liquid crystal in the panel is pulled down by gravity and it enlarges the cell gap. This resembles overfilling of the liquid crystal cell.
- If the spacer thickness is different in some areas on the panel, the over-filled or under-filled volume will be inversely proportional to the spacer thickness.
- Both AUA and G-GAP defects can occur as soon as the LCD is filled with liquid crystal or occur a few months after the LCD is made.





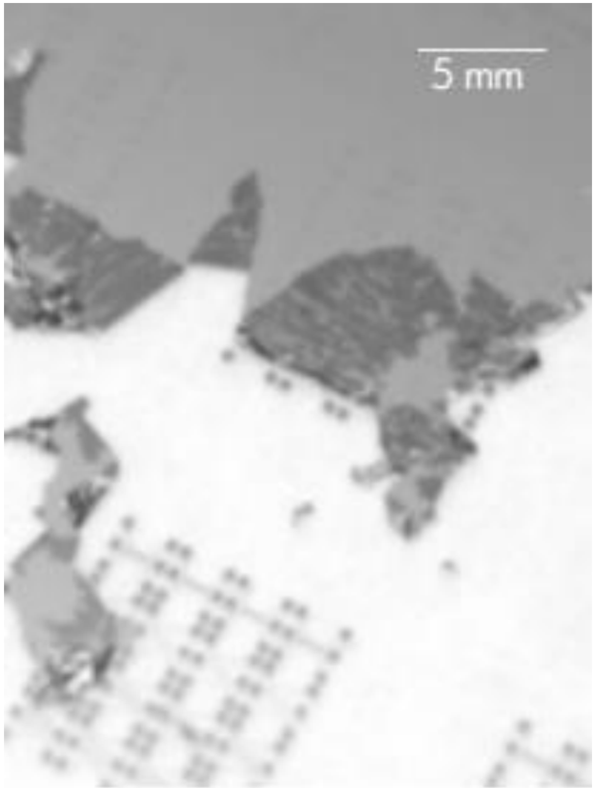
Delamination of TFT Metallization



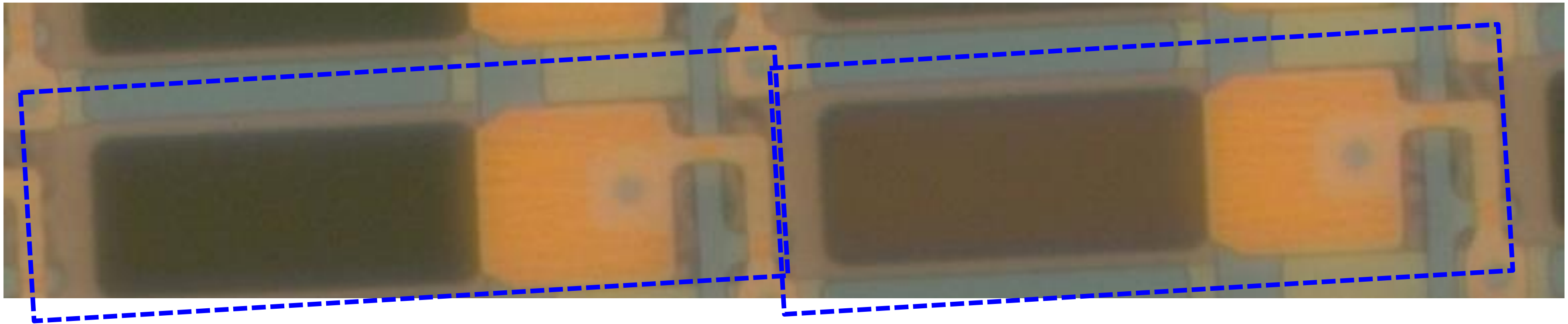
- Pixels look grayscale due to blocked light output
- Screening process:
  - Power up LCD on inverted microscope
  - Using a *polarized light* filter, focus on the TFT array from the color side of the glass sandwich
  - Examine pixel array colors using solid color palette of red, blue, green, white and black
- Failure mechanism:
  - Mobile TFT metallization is bridging the active matrix
  - Noteworthy observation – orientation of debris does not affect color filter (colored rows are intact)

Discussion: TFT Delamination

- A reference image of gate delamination due to poor adhesion of the deposited metals is shown
- This failure mode takes place when there is a CTE mismatch between the substrate and the deposited materials. It also takes place when the substrate is not uniformly heated (or rapidly cooled) during the deposition process.



Thin-Film-Transistor (TFT) Array



Illuminated “working” sub-pixel

Non-illuminated “dead” sub-pixel

- Sometimes it is possible to identify electrode patterning issues within the thin film transistor array
- The differences in opacity of the pixel itself is due to the surface tension of the liquid crystal on the opposing side of the glass
- Screening process:
  - Non-powered up LCD on inverted microscope
  - Using a *polarized light* filter, focus on the TFT array from the side opposite of the color side of the glass sandwich
  - Examine metallization, passivation and layering of the TFT constituents for anomalies

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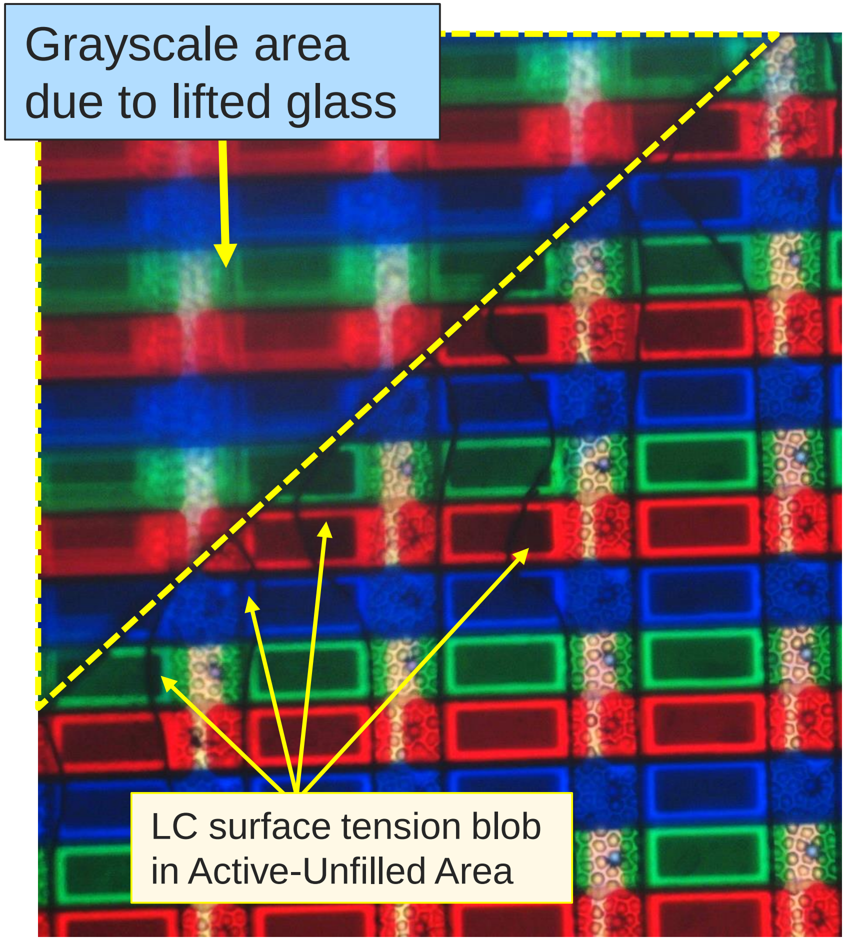
Working LCD Comparison



Grayscale area due to lifted glass

LC surface tension blob in Active-Unfilled Area

- The LCD referenced here was intentionally cracked.
- The screen was examined using a *dark-field* filter to determine the effects of the surface tension of the liquid crystal within the TFT cell array.
- It was observed that liquid crystal (LC) would become movable within the array and appear to be voided. Upon illumination of the screen, a gray scale appearance was *not* noted, except in the area that the glass sandwich was less than parallel.

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Touch Mura Appearance


Customer's Failed LCD

(a) (b)

. *Mura* images at different inspecting angle. (a) Both black and white *mura* can be inspected. (b) Only white *mura* can be inspected.

- During manufacturing, thermo-mechanical compression of the glass sandwich causes deformation of the spacers. Spacers towards the center of the display are plastically deformed, while those towards its periphery elastically deform. The uniformity throughout the display is less than optimal.
- Liquid crystal's function is based on the cell height at each pixel. If the spacers are non-uniform, then the light refraction through the liquid crystal is distorted. This effect can take place from external pressure on the screen or excessive internal cell pressure.
- The effect is a brownish/blackish blotch within the LCD viewable region.

Discussion: Liquid Crystal Display Bulge

- As previously discussed, liquid crystal cell gap is an important parameter to have nominal light refraction through the TFT array
- The glass sandwich is assembled using a hot bar process similar to that used in flex to glass and chip on glass bonding
- The bulge problem originates from the elastic deformation of spacers rather than from the shrinkage of the sealant during temperature changes or curing process.
    - During the hot bar process, the spacers are deformed into ellipsoid due to external pressure on the glass.
    - After hot bar process is completed, the external pressure exerted is released. The spacers in the cell center resume their former shape, but the spacers towards the cell periphery are prevented from resuming their original shape. The perimeter sealant keeps these areas more rigid which keeps the spacers in a compressed state.
    - This results in a cell gap in the perimeter smaller than the spacer diameter, and the cell gap in the cell center is larger than the cell diameter. The characteristics resemble both gravity-gap and active-unfilled area pixel behaviors.

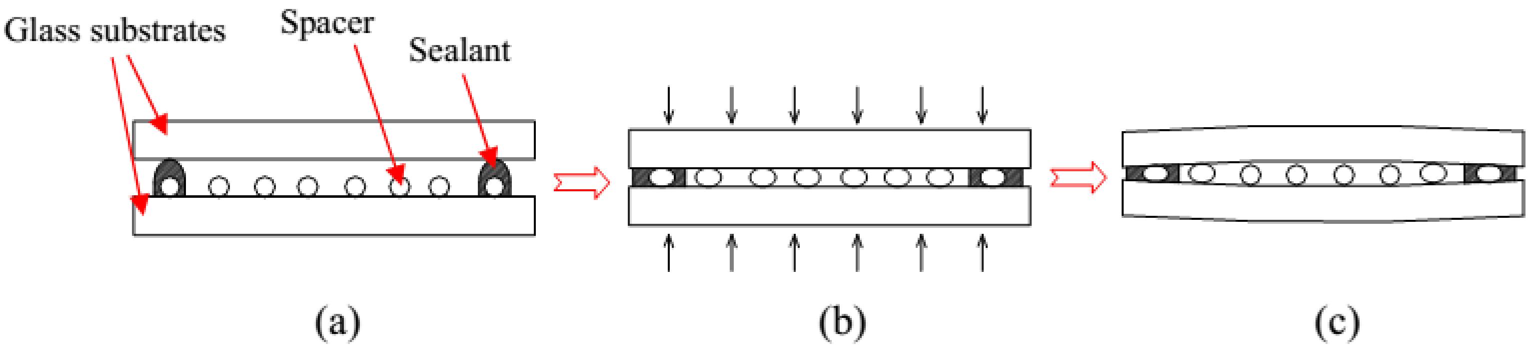
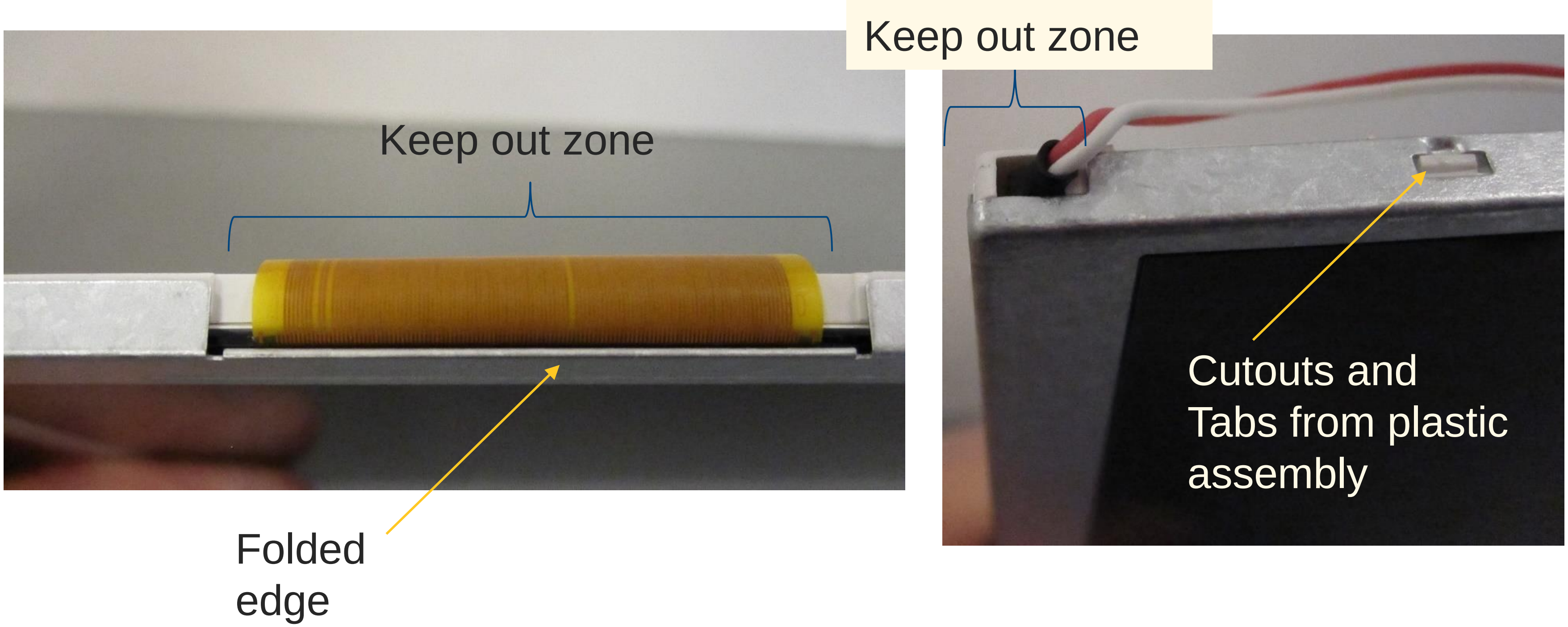


Fig. 2. (a) Before hot press; (b) During hot press; (c) After hot press.

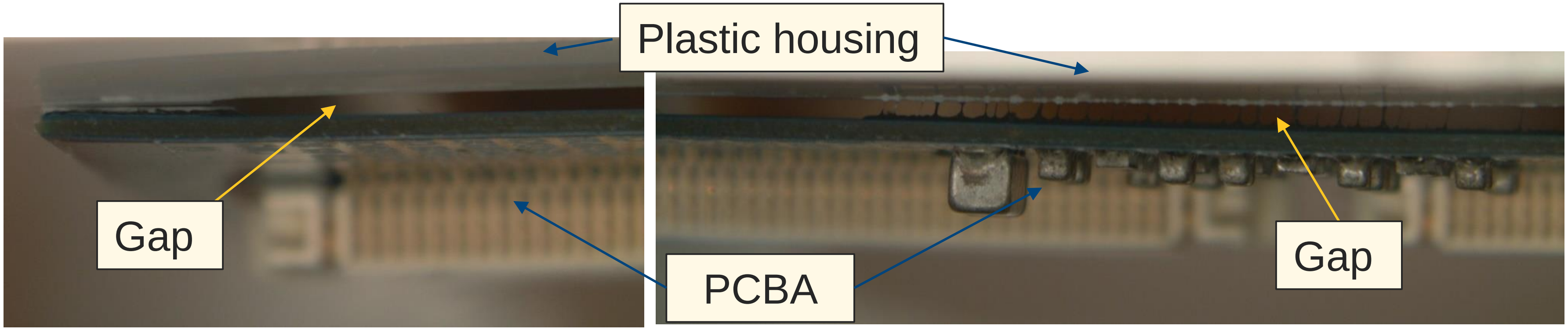
- Let’s Discuss Construction Anomalies

LCD Module – Mechanical Assembly



- Key item in a good assembly is a sufficient gap in the housing for the flex and LED power cables
  - There are no sharp edges or pinch points in the vicinity

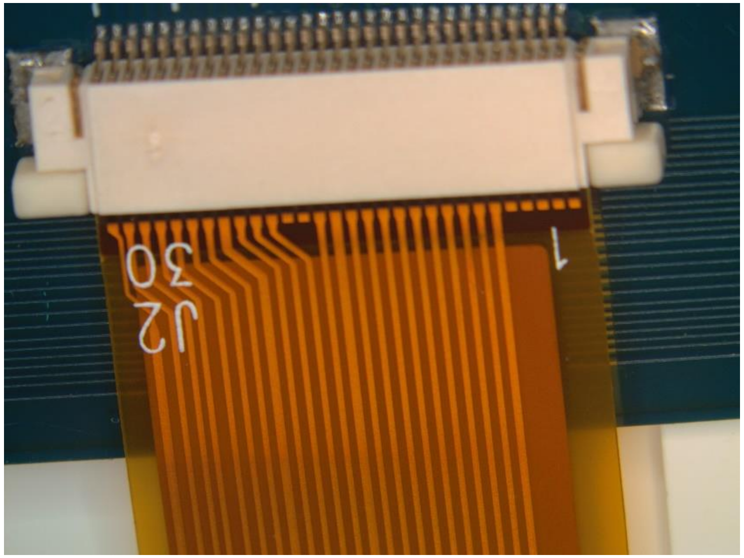
LCD Module – Mechanical Assembly

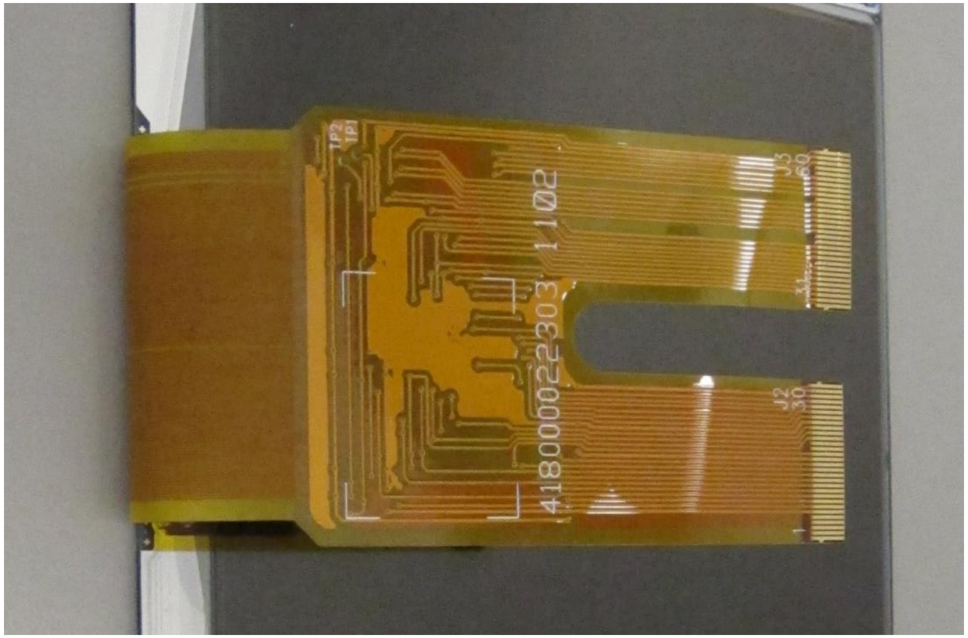


- Issues may occur in other stages of assembly. Here we see the PCBA adhesive was only attached on one side. The other side has non-bonded adhesive tape.
- The PCB was *not* flexed to take these images. It was merely held vertically.

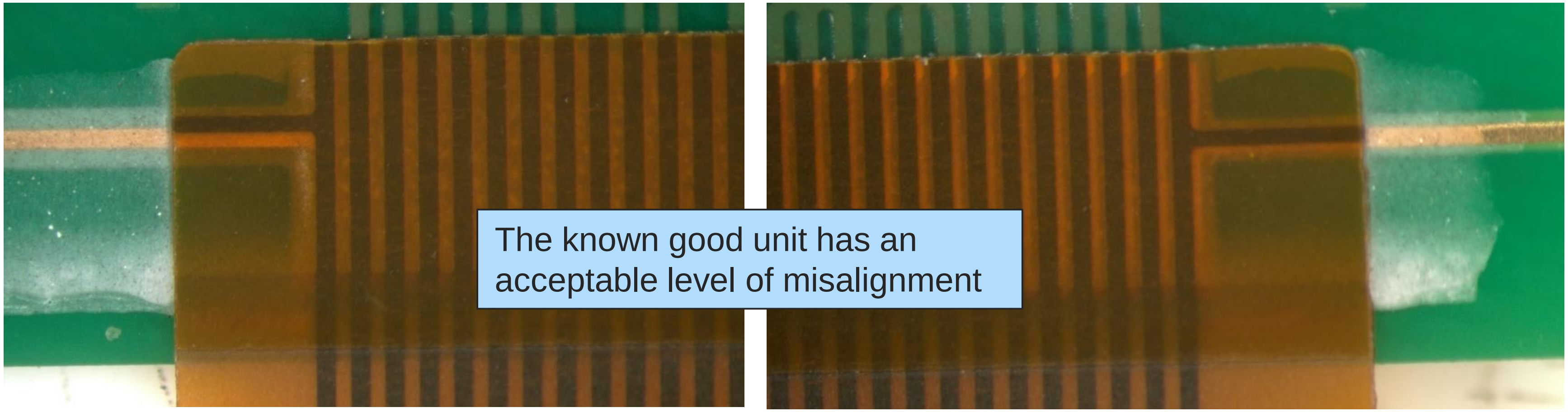
Visual Inspection – Flex Cables

- The flex cables are a good design
  - Corse and thin conductor lines are separated
  - Solid shielding plane does not impair flexibility
  - Single piece of flex with sufficient margin around periphery, tapered angles with no 90° cutouts

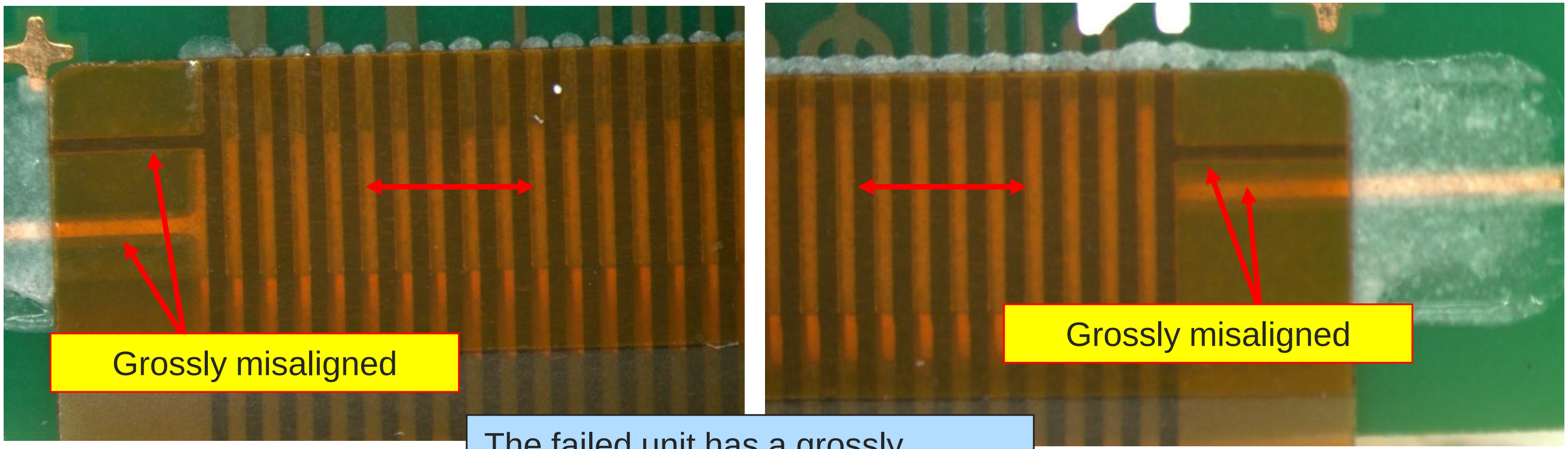




Visual Inspection – Flex Attached to PCB



The known good unit has an acceptable level of misalignment



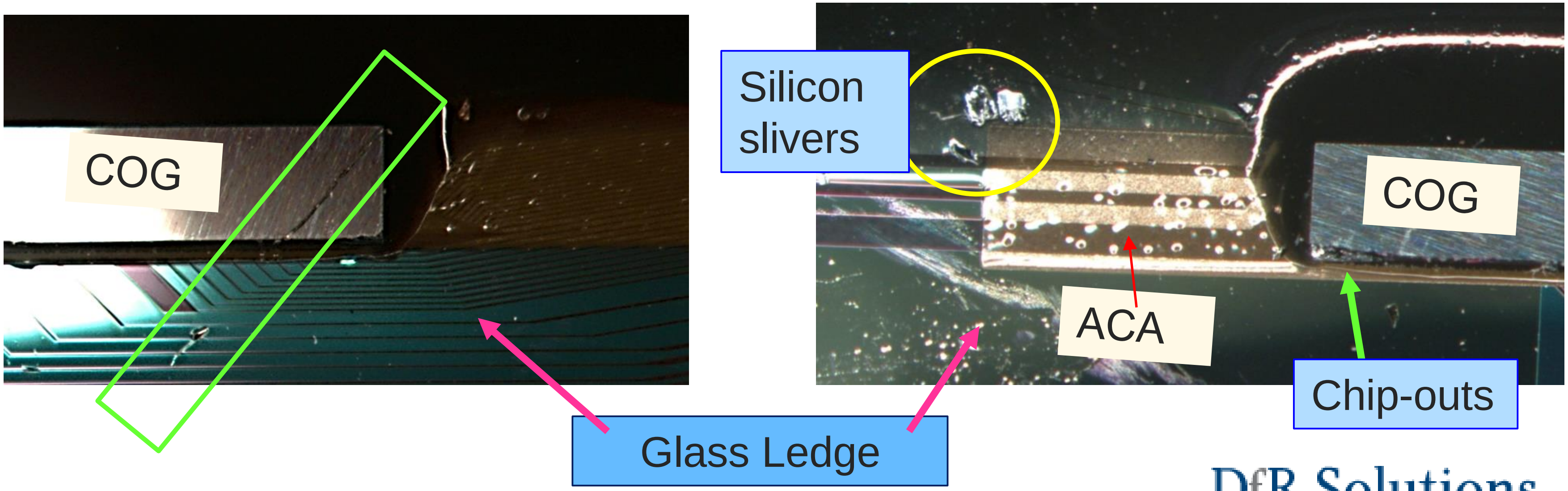
Grossly misaligned

Grossly misaligned

The failed unit has a grossly misaligned flex-on-PCB connection

Other Findings: Cleanliness, Damaged Components

- Tooling damage was identified failed modules
  - A ‘scrape’ was found on the backside of one COG on the known good LCD assembly
  - Two chip-outs were found at the corners of the front face of the COG on the failed LCD assembly

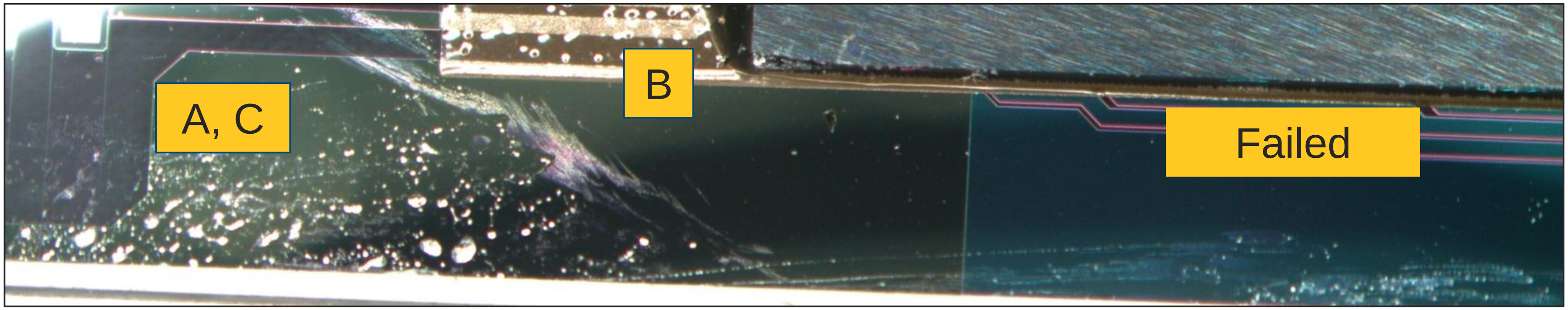


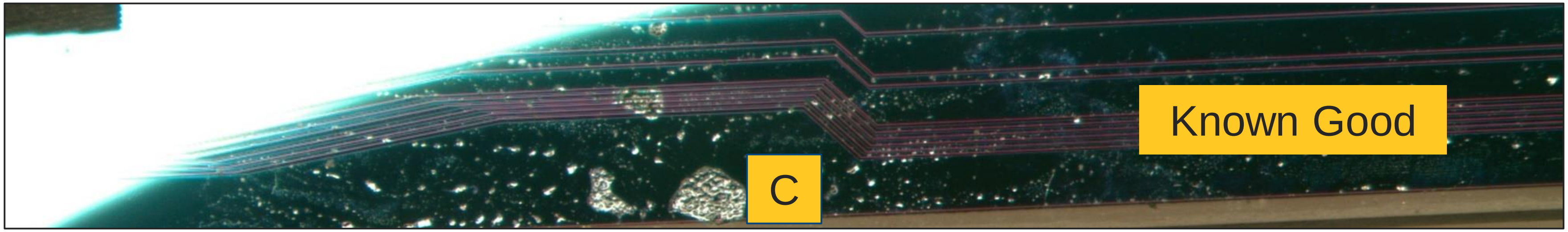
Known Good

Failed

Other Findings (Cont'd)

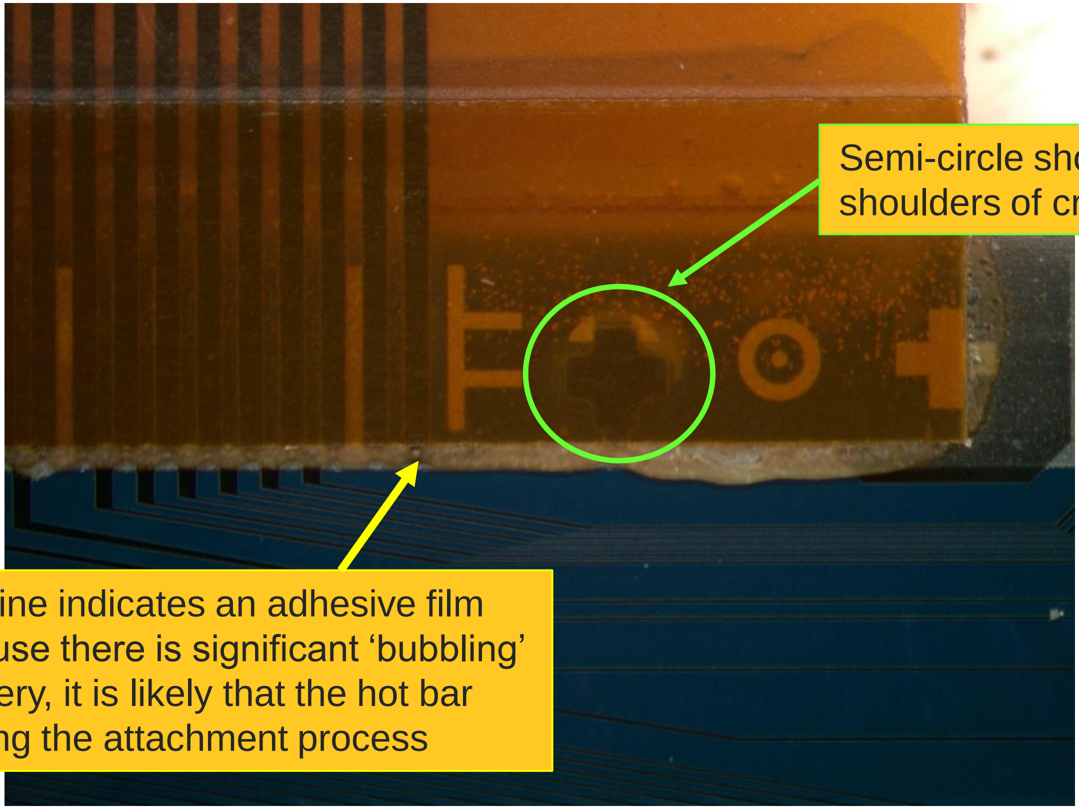
- A general cleanliness observation of both units noted:
  1. Particulate matter trapped in the ledge seal
  2. Excess ACA film near the COGs
  3. Residue on glass (likely a saponifier)





Inspection of Flex on Glass (Cont'd)

- Misalignment of Flex on Glass was noted
- The excess dried out adhesive around the flex cable would be a non-compliance (for both the known good and failed units)

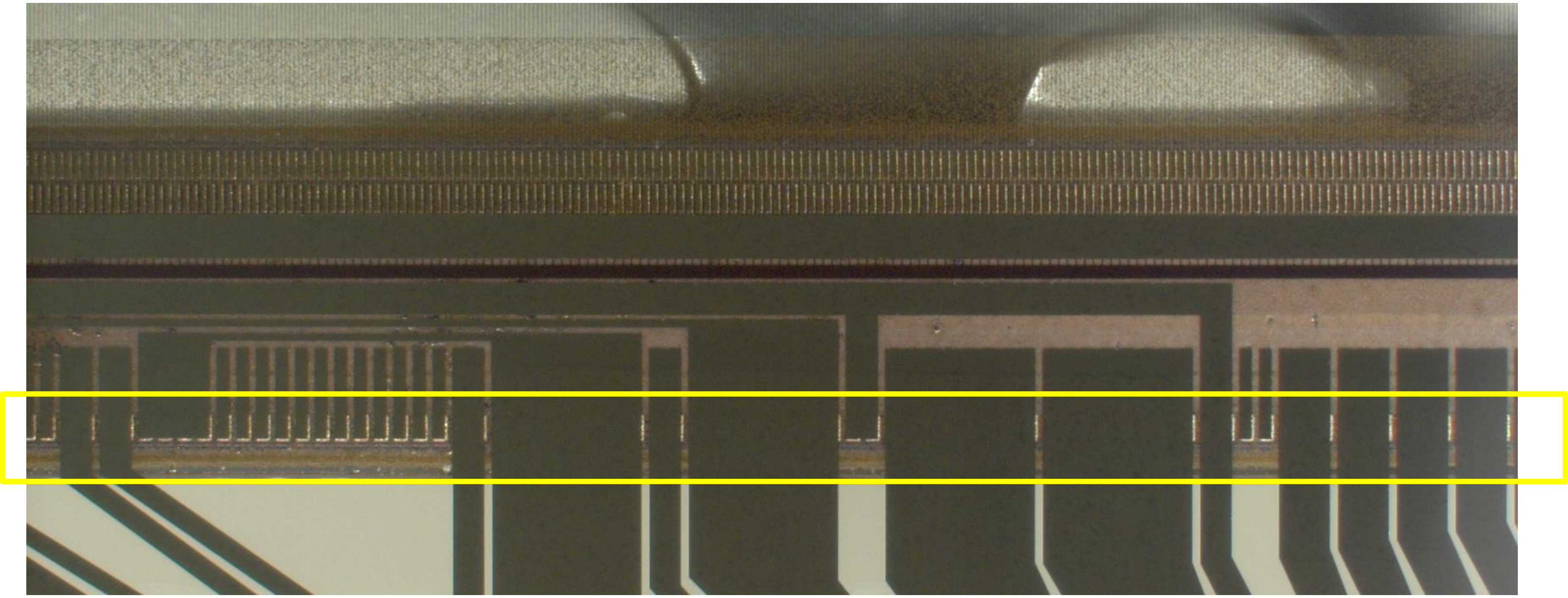


Semi-circle should sit on shoulders of cross

Rectangular outline indicates an adhesive film was used. Because there is significant 'bubbling' along the periphery, it is likely that the hot bar was too hot during the attachment process

Alignment of Chip on Glass

- There is some misalignment with the COG to the glass substrate, this is seen as silvery outline in the lower right hand corner of each pad
  - This characteristic effectively reduces the distance between conductors



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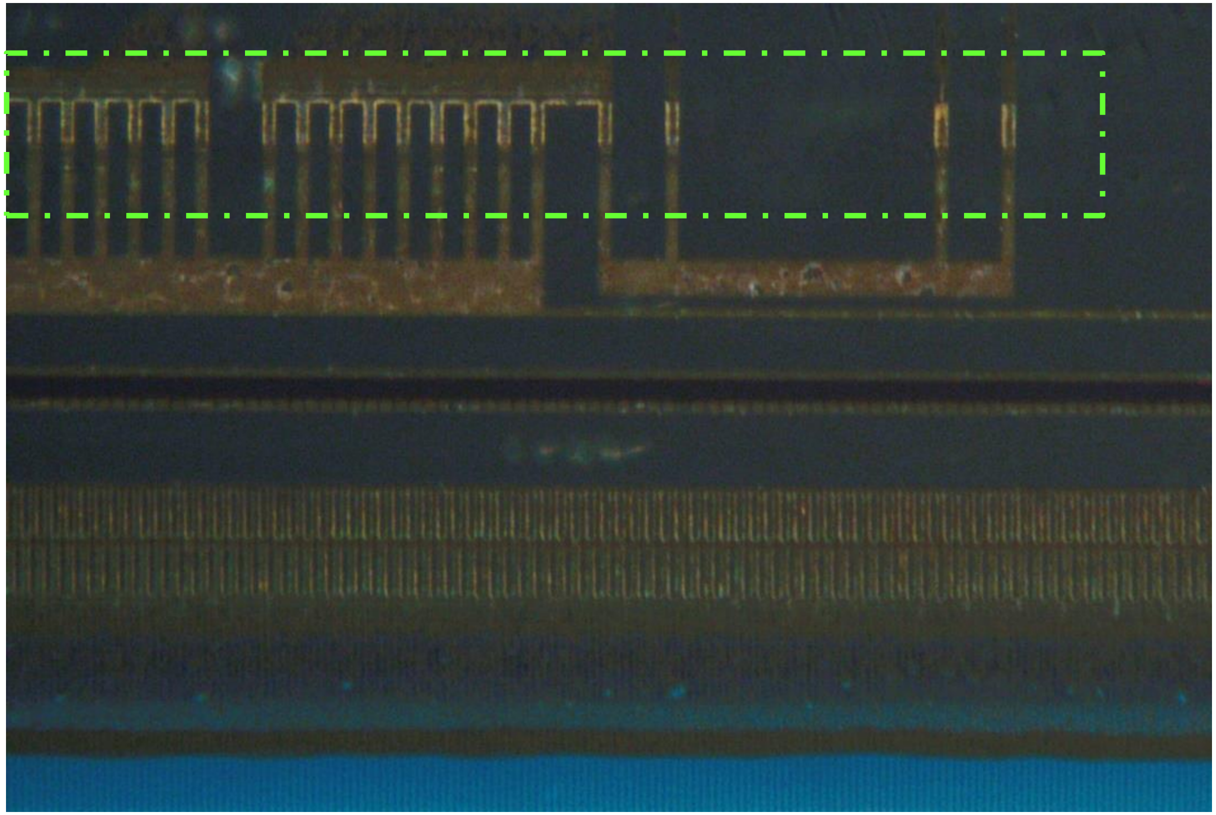
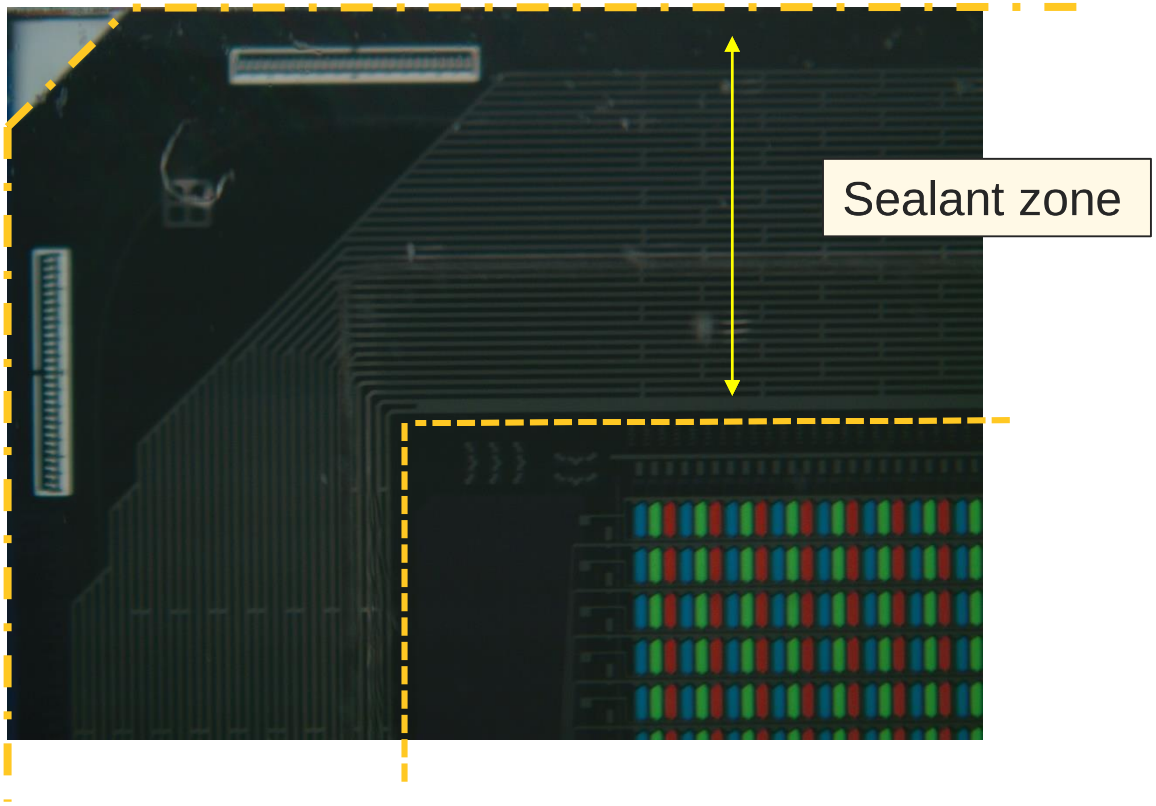
Alignment of Chip on Glass (Cont'd)



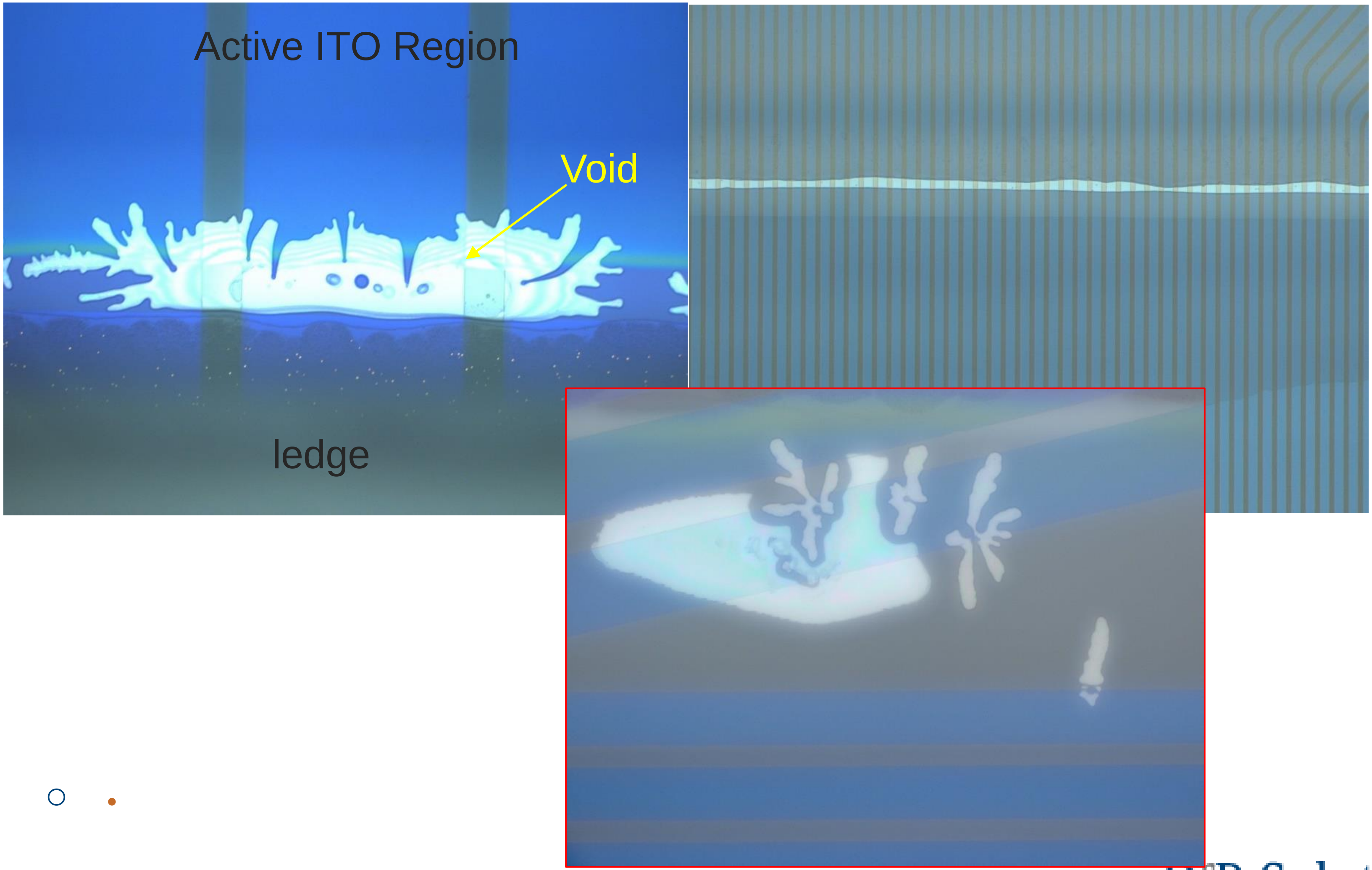
- The chips on glass are concentrically aligned to the bond pads
  - Note the gold-like appearance around each 'black' conductor

Perimeter Sealant

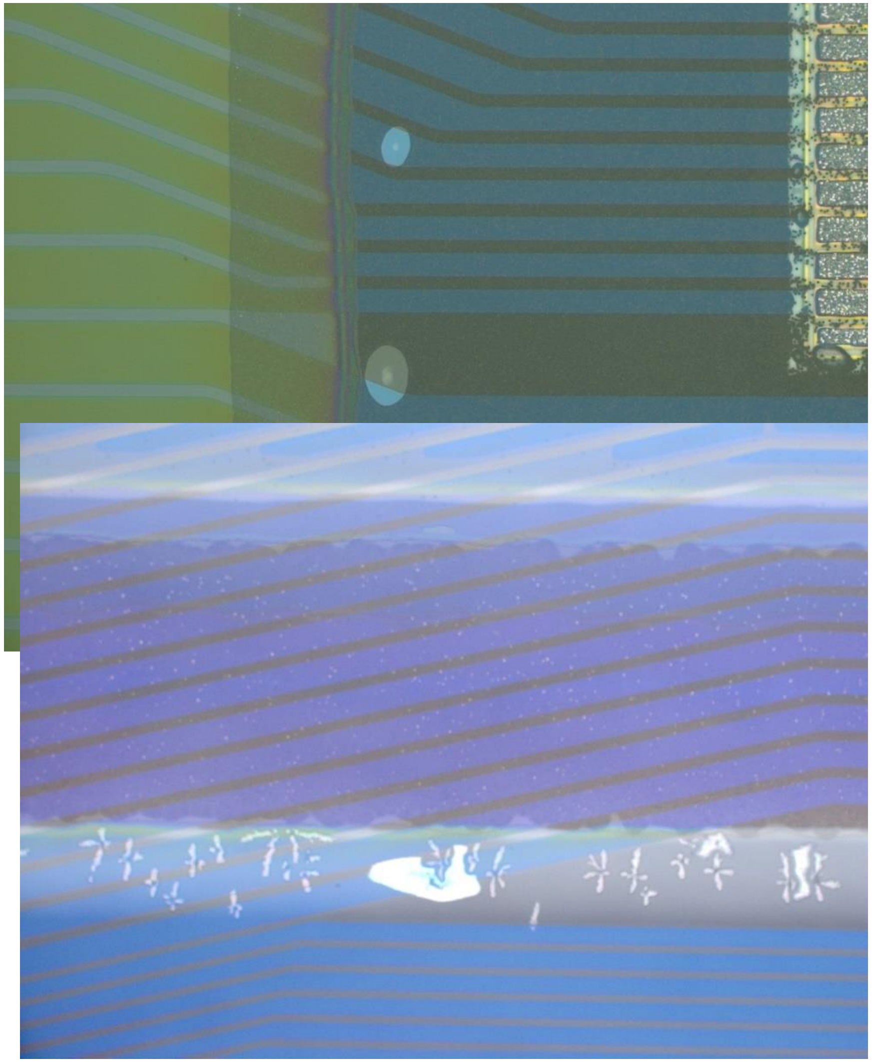


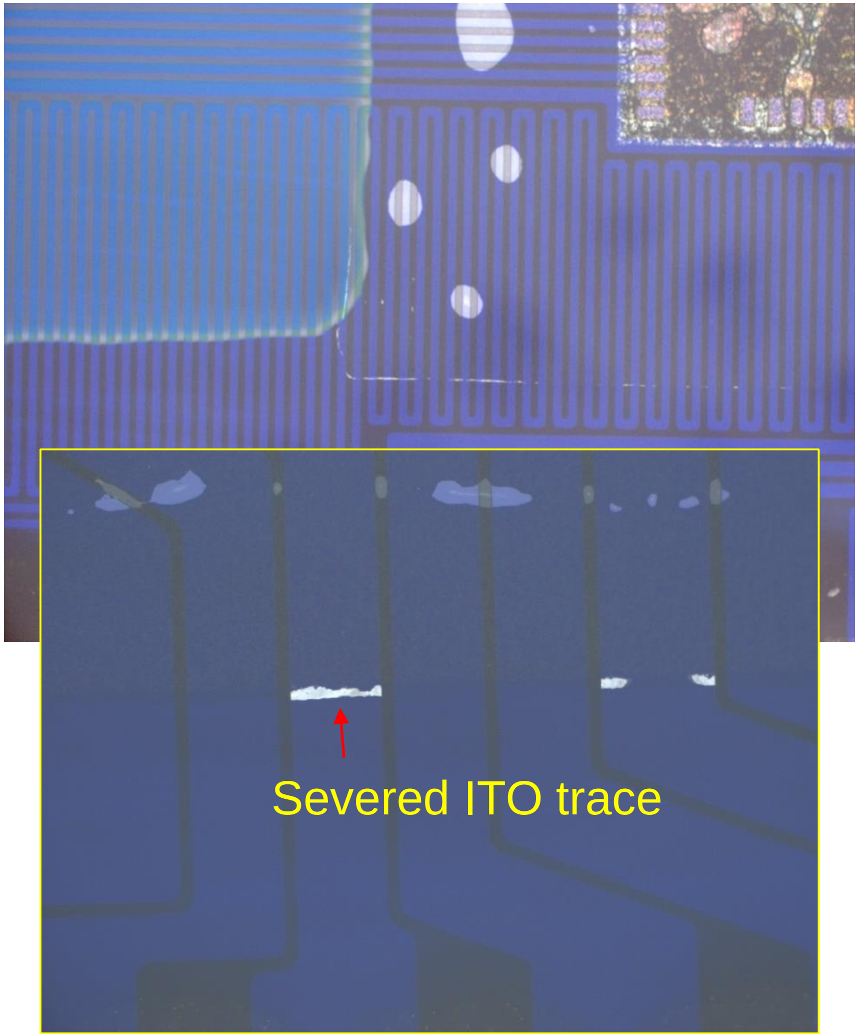
- The perimeter of the glass sandwich is adequately sealed
    - It is worth noting that the particulate matter seen in this image is on the surface of the glass

Images of Irregular Ledge Sealant

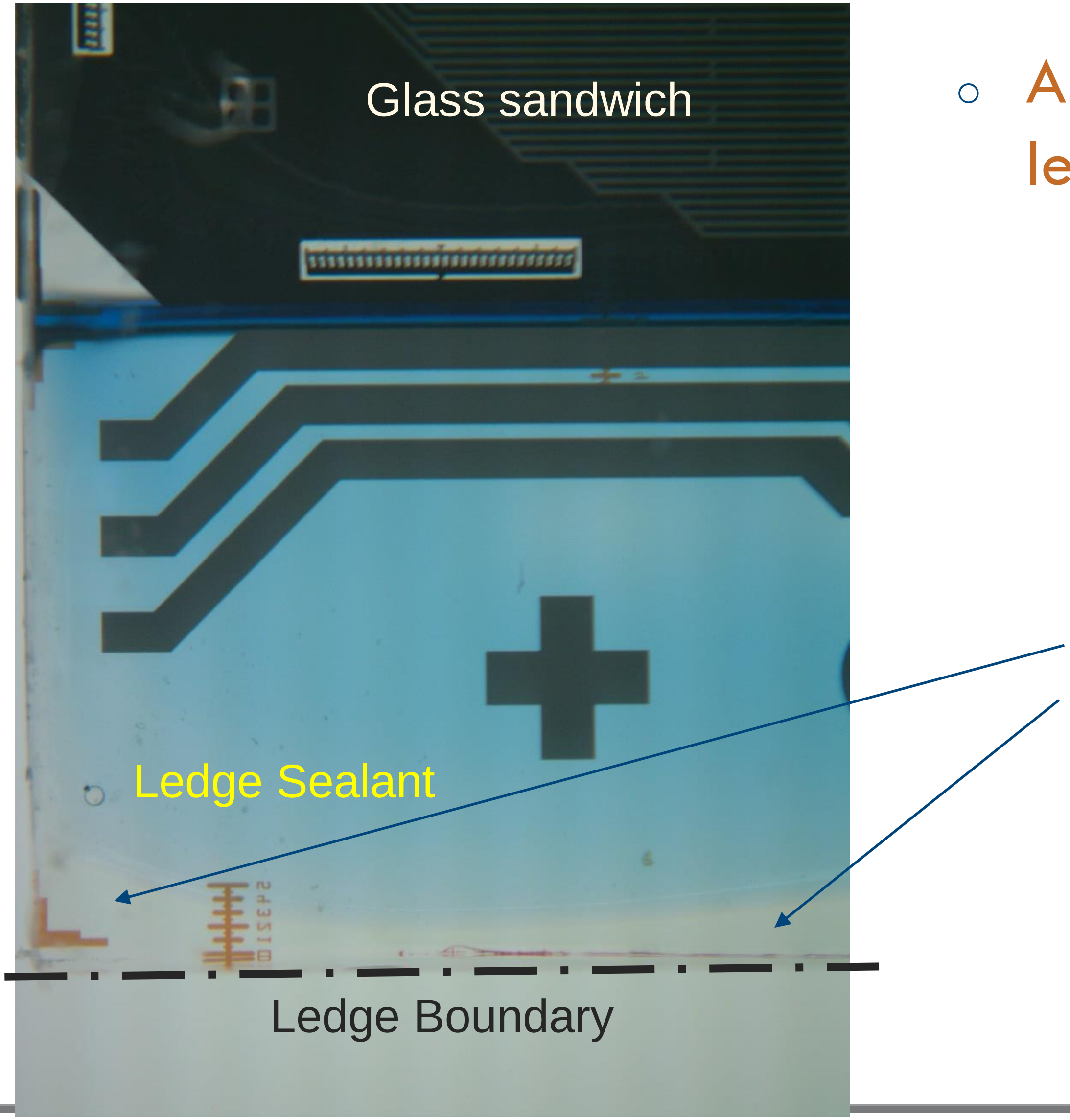


Active ITO Region



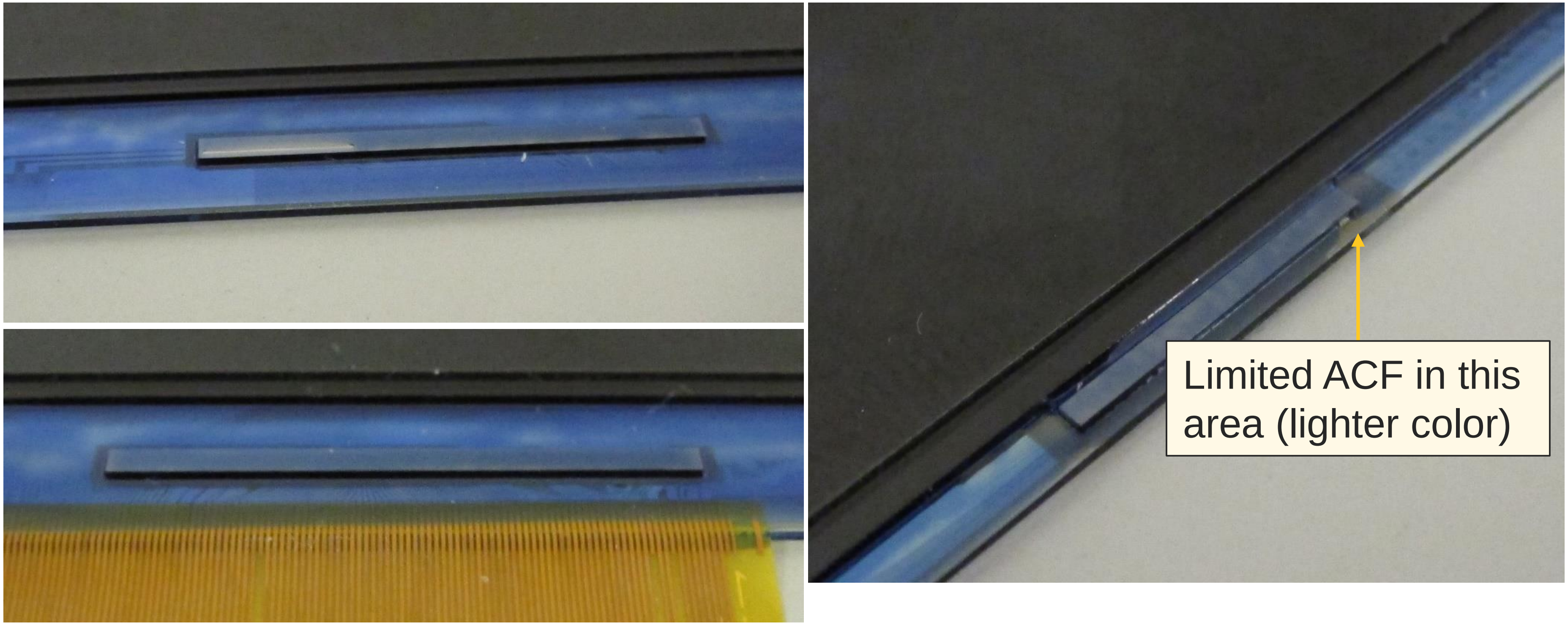


Visual Inspection – Ledge Assembly (Cont'd)



- Another view of the ledge sealant

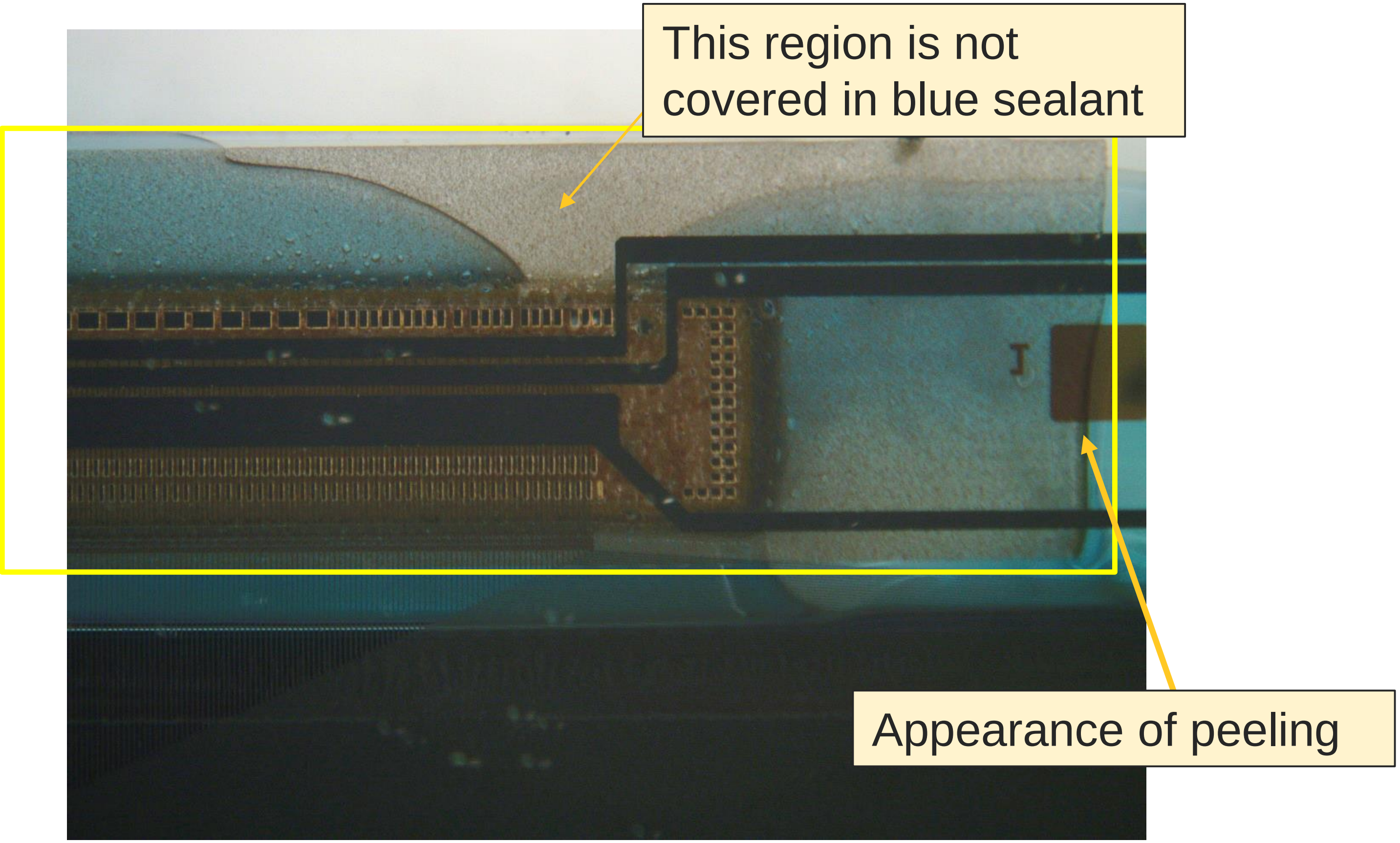
Visual Inspection – Chips on Glass



Limited ACF in this area (lighter color)

- Three driver chips were identified and shown attached to the ledge at the bottom and right sides
- A squeegeed ACA may have been used based on appearance

Optical Microscopy - Chip on Glass Adhesion


This region is not covered in blue sealant

Appearance of peeling

- Though limited, the side ledge chip on glass is not as sufficiently covered with sealant as the bottom ledge chips.
  - Allows for moisture ingress

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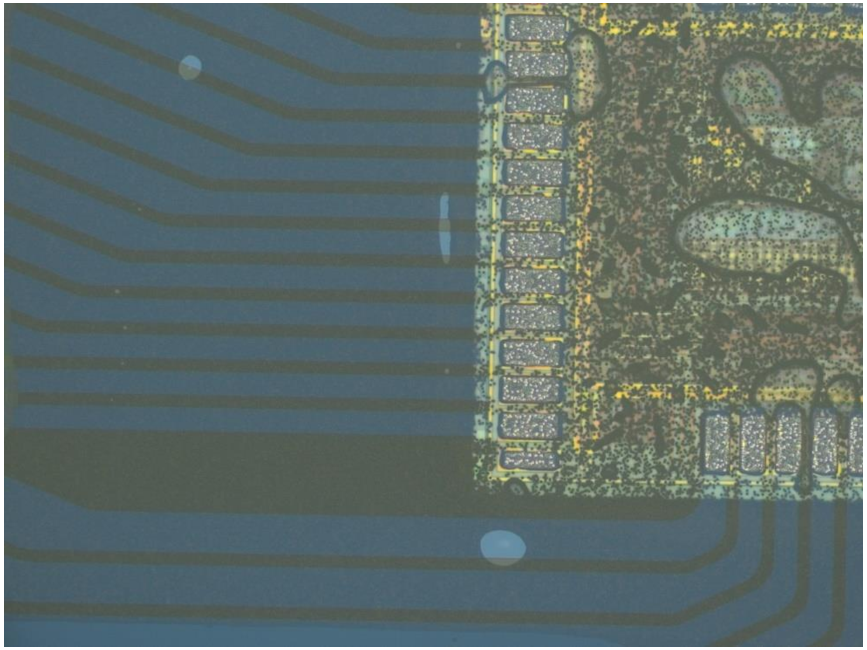
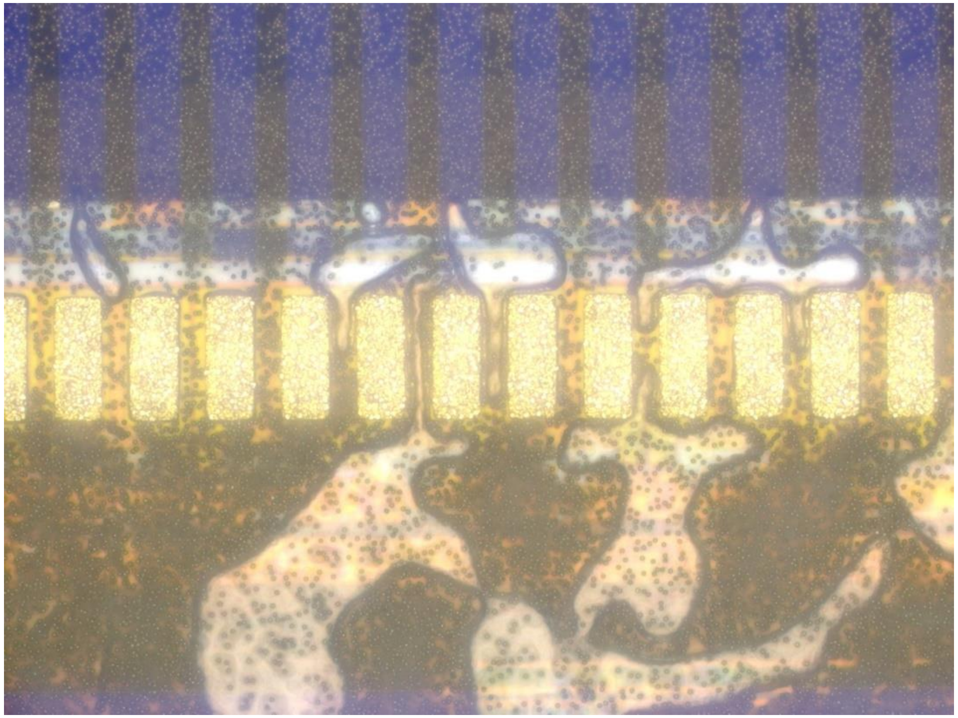
Poor ACA Fill





- Note the voids beneath the COG

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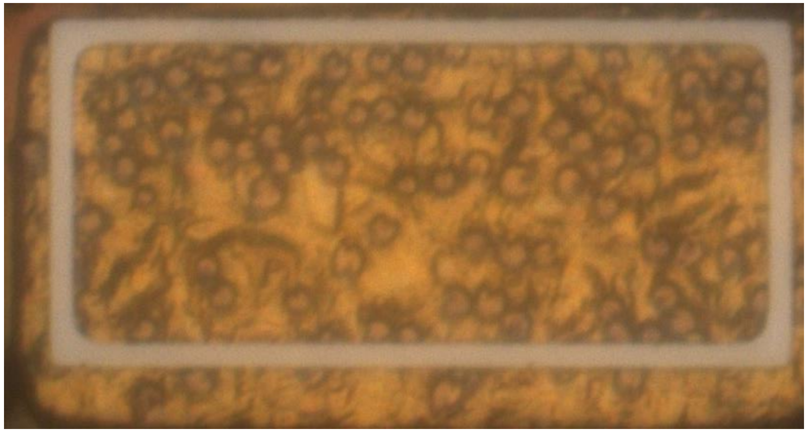
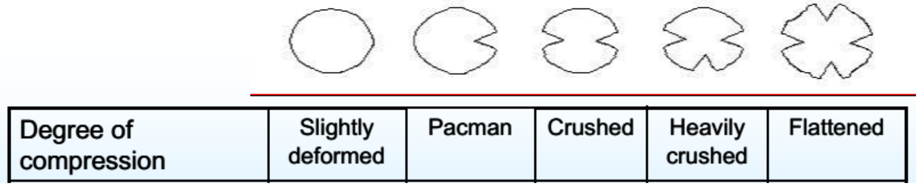
Inspection of ACA on COG

- Anisotropic conductive particles will deform under heat and pressure. The expected shape is a slightly crushed “pacman” with uniformly sized particles.
  - The appearance of particle sizes varies
  - The crush shape of the particles ranges from slightly deformed to completely flattened – indication of fast thermal ramp rates, non uniform heating and high bond force



Misaligned no-connect COG Pad

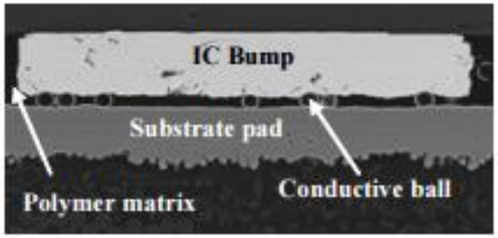


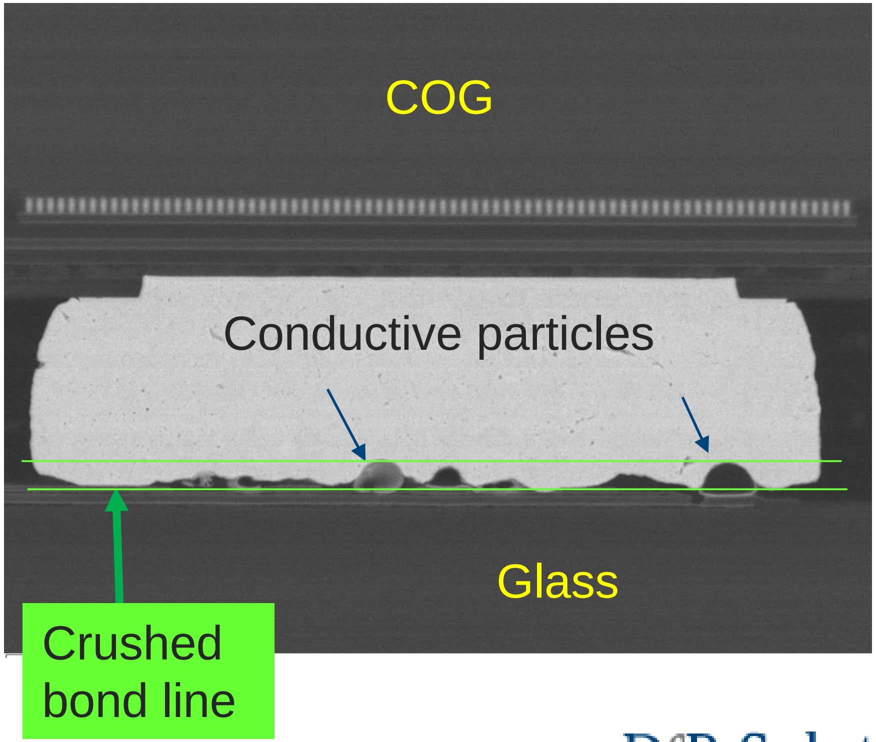
Degree of compression	Slightly deformed	Pacman	Crushed	Heavily crushed	Flattened

Inspection of ACA and COG

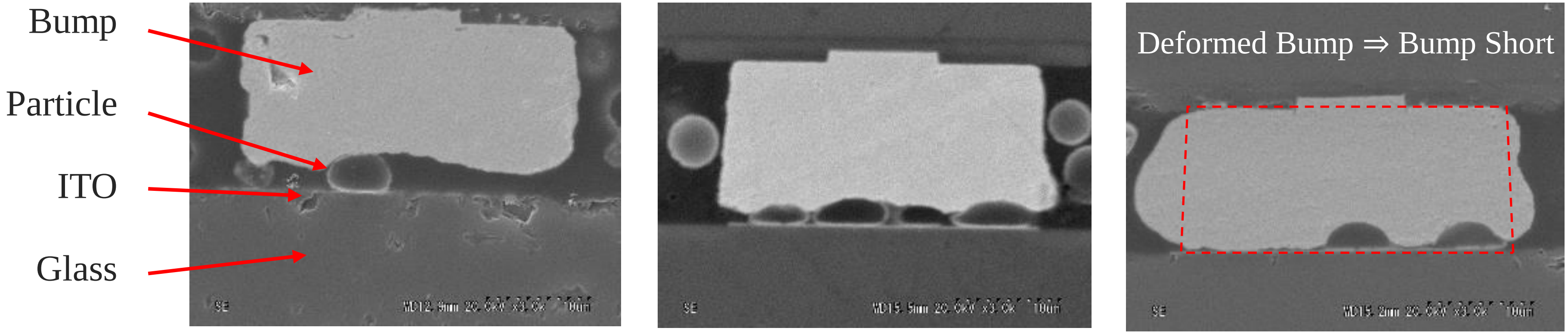
- Cross section of the COG shows deformation of the COG metallization
  - This is an indication of excessive bond force which displaces the conductive particles – references as a function of force are shown on the next slide

Expected appearance





Particle Deformation Examples



Pressure: 6 MPa 40 MPa 100 MPa

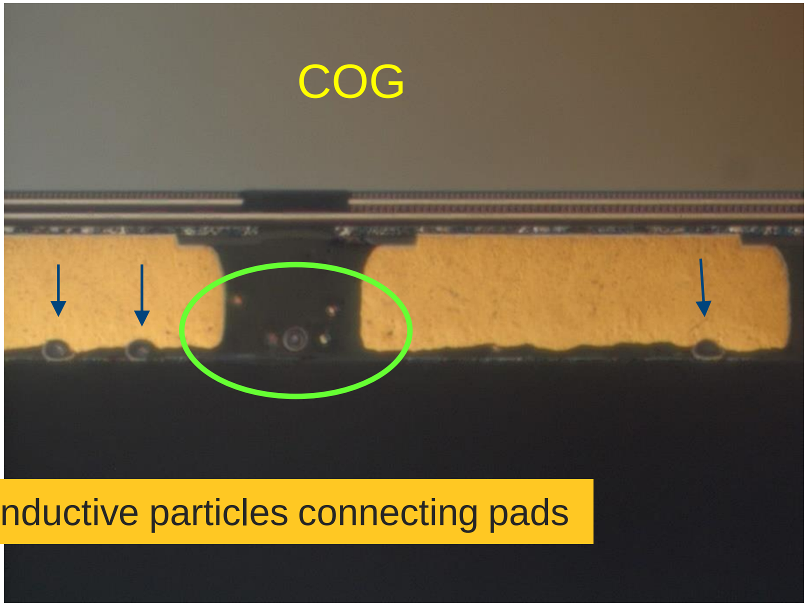
IDEAL

Suspect LCDs

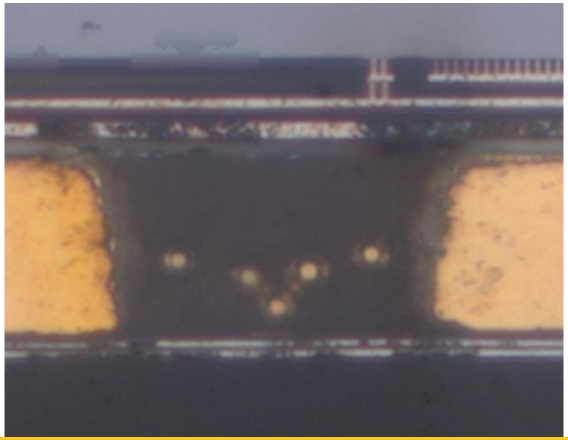
- The metallization bump on the COG is deformed at the interface

Inspection of ACA on COG

- Cross section of the COG shows aggregation of particles between conductors
  - Particle grouping can cause cross talk of the LCD's switching matrix

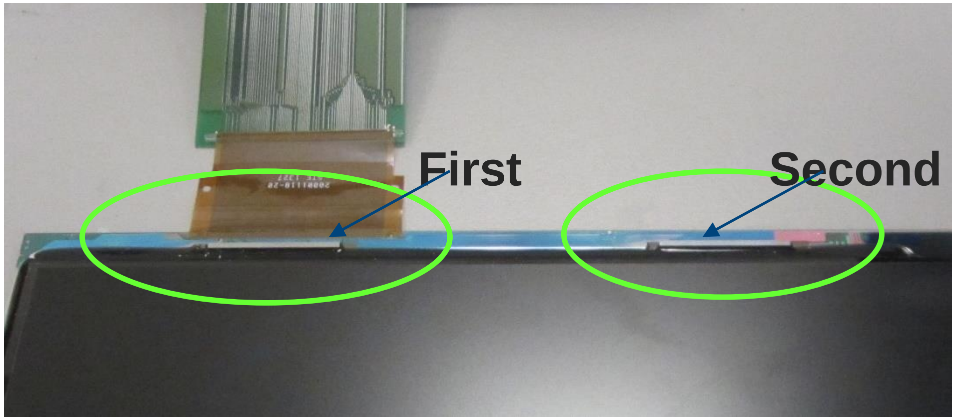


Conductive particles connecting pads



Closer look at particles bridging conductors

Bonding Process Parameters



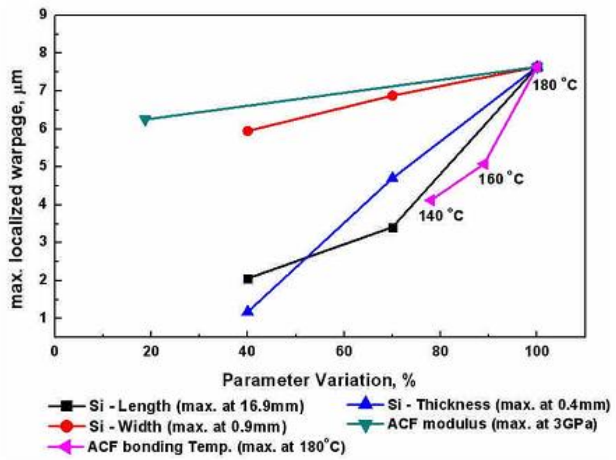


FIGURE 12 —The maximum localized warpage as a function of different parameters: ACF modulus, ACF bonding temperature, and Si dimension (length, width, and thickness) relative to a reference case of 0.3 mm-thick glass and ACF bonding temperature of 180 °C.

- Driver ICs are connected to glass ledge using hot bar process
  - One IC is adhered to the glass at a time, which creates a stress gradient across the glass ledge
- Elevated bonding force coupled with excessive temperature exposure (long dwells, fast ramp rates) will exacerbate the localized warpage stresses created by the thermal mismatch between the glass, conductive film and the silicon chip.
  - A schmoo plot is shown to depict the warpage associated with controllable process parameters

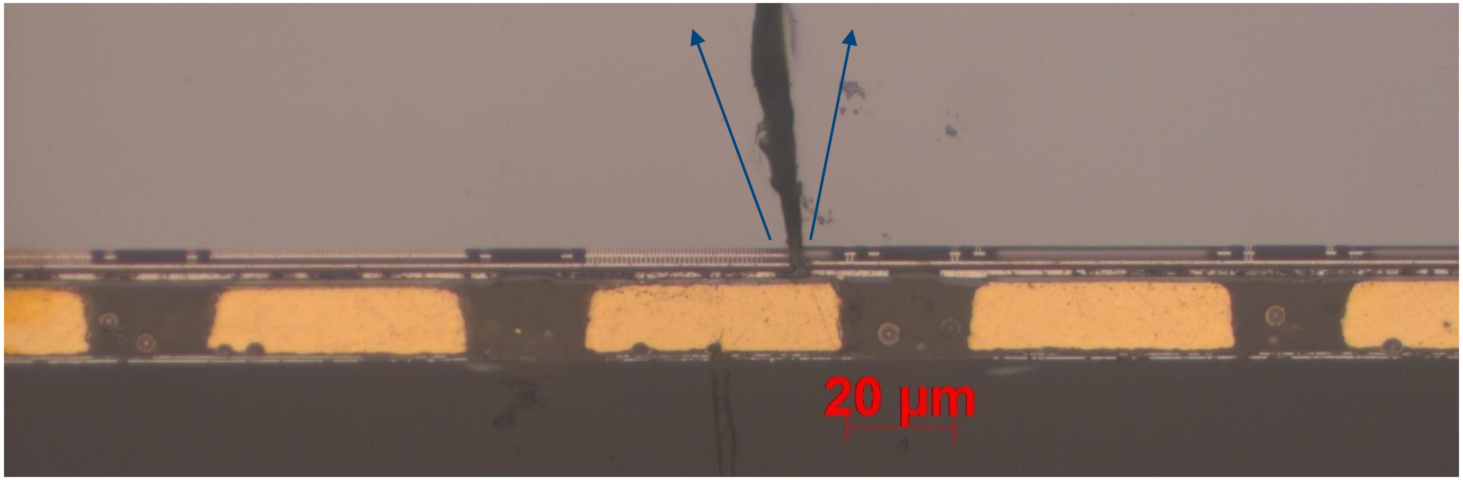
DfR Solutions

Properties of the Materials System

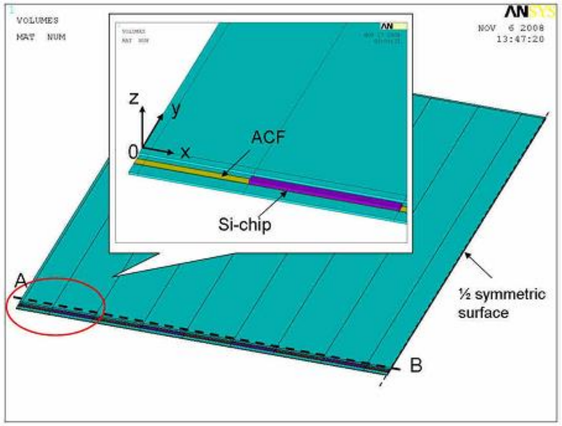
- If the modulus of the ACF is high, the ACF acts as a rigid connector transferring bending moment of the COG to the glass ledge
- If the modulus of the ACF is low, the ACF acts as a stress buffer undergoing plastic deformation
- COG stresses are due to its physical dimensions (L, W, T). If the thickness of the ledge is less than that of the COG, then the bending force from the glass will be transferred to the COG causing it to crack. This force transfer is worse towards the periphery of the ledge.
  - The COG’s thickness can be reduced through backside grinding to make it more compliant.

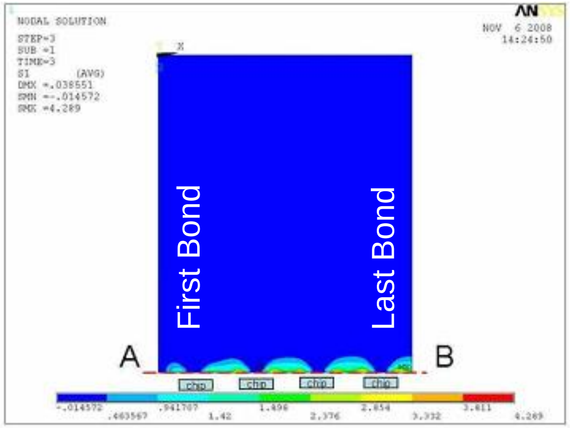
Glass Warpage & Stress Concentration

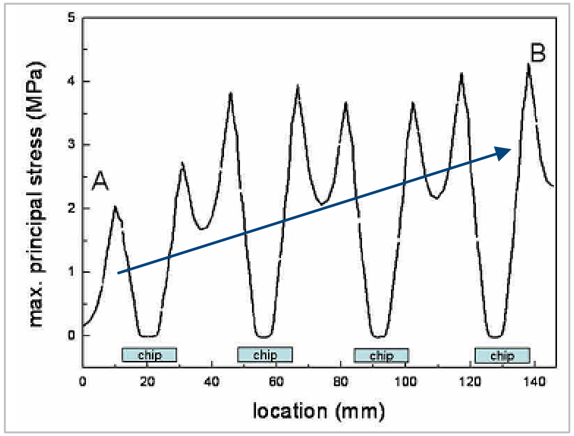
- The fracture direction is through the COG from the bonding interface



Warpage Simulation Reference







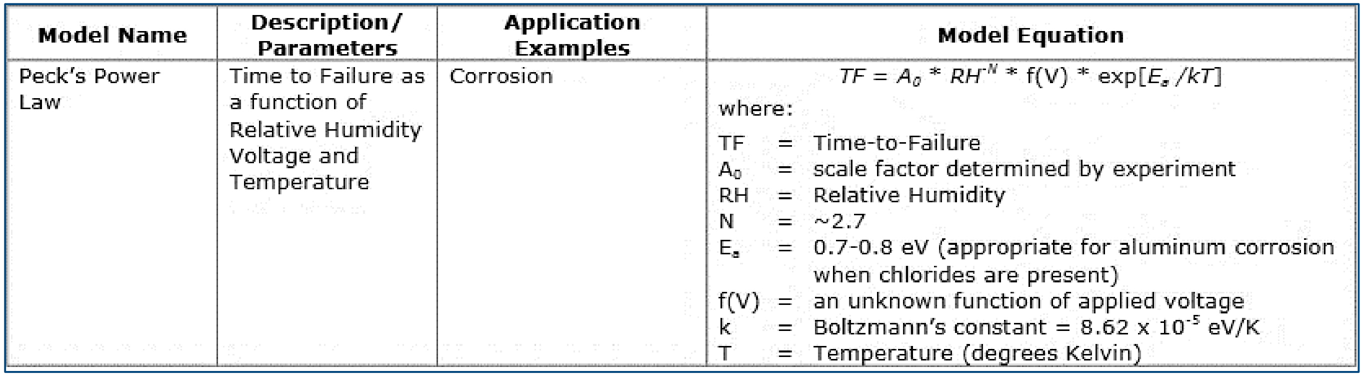
- Stress concentrations exist at the periphery of each COG due to the material system
  - Stress is magnified for each consecutive bond across the glass ledge
  - Stress can be mitigated by placing the LCD panel in a rigid fixture that heats the glass ledge uniformly throughout the bonding process
- The suspect LCDs are most likely assembled with the COG closest to the flex cable bonded first. If sufficient time lapses between hot bar operation, then the second COG will be bonded to a curved surface.

- Let’s Discuss Accelerated Test DoE

DfR Solutions

Lifetime Expectancy

- Lifetime can be assessed using Peck's Power Law



Model Name	Description/ Parameters	Application Examples	Model Equation
Peck's Power Law	Time to Failure as a function of Relative Humidity Voltage and Temperature	Corrosion	$TF = A_0 * RH^{-N} * f(V) * \exp[E_a/kT]$ where: TF = Time-to-Failure A_0 = scale factor determined by experiment RH = Relative Humidity N = ~2.7 E_a = 0.7-0.8 eV (appropriate for aluminum corrosion when chlorides are present) f(V) = an unknown function of applied voltage k = Boltzmann's constant = 8.62×10^{-5} eV/K T = Temperature (degrees Kelvin)

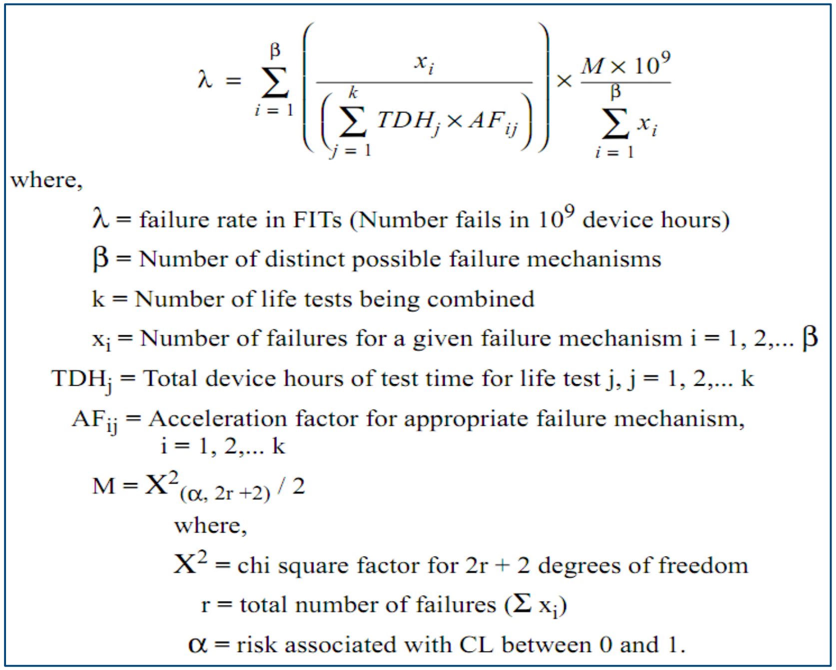
- A complementary acceleration transform can be created using the model equation

$$AF = \left(\frac{RH_{test}}{RH_{field}}\right)^{-2.7} * \left(\frac{V_{test}}{V_{field}}\right)^{1.5} * exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_{test}} - \frac{1}{T_{field}}\right)\right)$$

- Calculation provided on following slides

Lifetime Expectancy (Cont'd)

- Failure rate and MTBF can be calculated using JESD-47 (Stress Test Driven Qualification of Integrated Circuits)



$$\lambda = \sum_{i=1}^{\beta}\left(\frac{x_i}{\left(\sum_{j=1}^{k} TDH_j \times AF_{ij}\right)}\right) \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = Number of distinct possible failure mechanisms

k = Number of life tests being combined

x_i = Number of failures for a given failure mechanism i = 1, 2,... β

TDH_j = Total device hours of test time for life test j, j = 1, 2,... k

AF_{ij} = Acceleration factor for appropriate failure mechanism, i = 1, 2,... k

$M = X^2_{(\alpha,\ 2r+2)} / 2$

where,

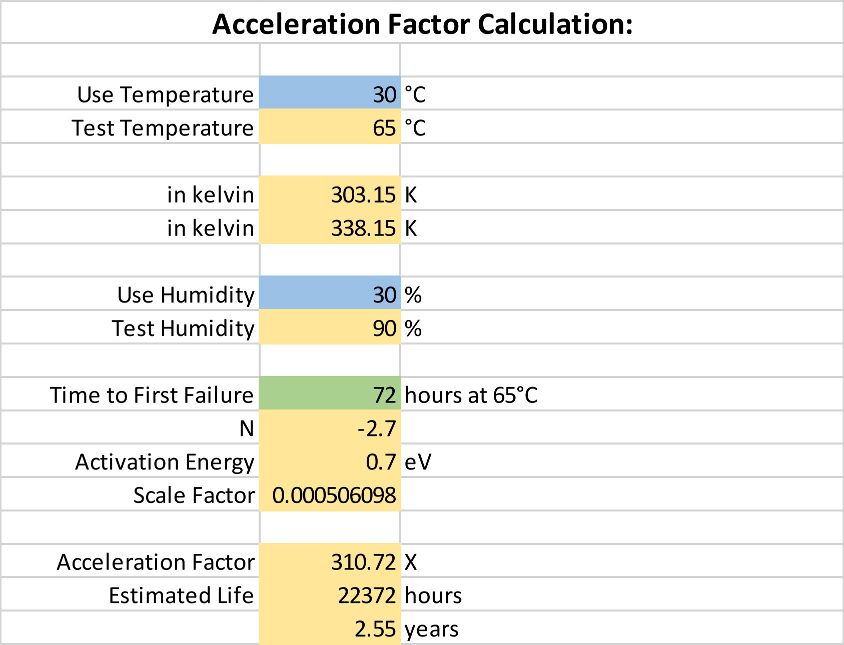
X^2 = chi square factor for 2r + 2 degrees of freedom

r = total number of failures ($\Sigma\ x_i$)

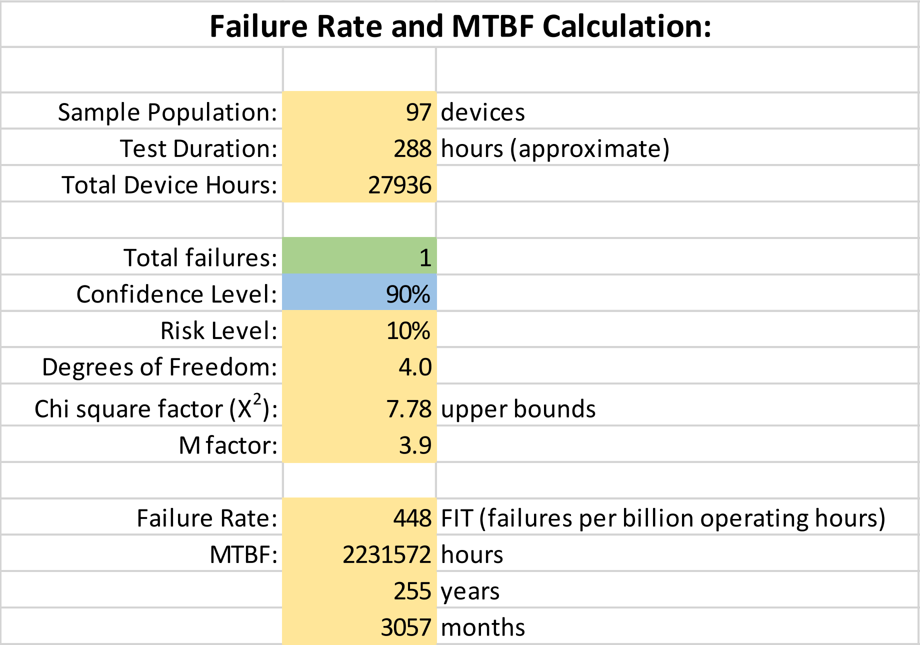
α = risk associated with CL between 0 and 1.

- Calculation provided on following slides

Lifetime Expectancy (Cont'd)



Acceleration Factor Calculation:		
Use Temperature	30	°C
Test Temperature	65	°C
in kelvin	303.15	K
in kelvin	338.15	K
Use Humidity	30	%
Test Humidity	90	%
Time to First Failure	72	hours at 65°C
N	-2.7	
Activation Energy	0.7	eV
Scale Factor	0.000506098	
Acceleration Factor	310.72	X
Estimated Life	22372	hours
	2.55	years



Failure Rate and MTBF Calculation:		
Sample Population:	97	devices
Test Duration:	288	hours (approximate)
Total Device Hours:	27936	
Total failures:	1	
Confidence Level:	90%	
Risk Level:	10%	
Degrees of Freedom:	4.0	
Chi square factor (X^2):	7.78	upper bounds
M factor:	3.9	
Failure Rate:	448	FIT (failures per billion operating hours)
MTBF:	2231572	hours
	255	years
	3057	months

- Company A's lifetime expectation of 5 years was met under the conditions of the THB test
  - Extrapolation using acceleration transform and time to failure under 60°C/90%RH test yields 2.55 years
  - Statistical extrapolation using JESD47 yields 255 years

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Best Regards,
Dr. Craig Hillman, CEO

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