Manufacturability & Reliability Challenges with Leadless Near Chip Scale (LNCSP) Packages in Pb-Free Processes

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ABSTRACT

Leadless, near chip scale packages (LNCSP) like the quad flat pack no lead (QFN) are the fastest growing package types in the electronics industry today. Early LNCSPs were fairly straightforward components with small overall dimensions, a single outer row of leads and small lead counts. However, there is currently a proliferation of advanced LNCSP package styles that have started to approach BGA packages in terms of both size and number of connections. Some of the newer packages have 3 or more rows, pitches as fine as .35mm, lead counts exceeding 200, and dimensions exceeding 12 mm X 12 mm.

While the advantages of these packages are well documented, concerns arise with both reliability and manufacturability in Pb-free environments. So, acceptance of these packages in long-life, severe-environment, high-reliability applications is somewhat limited. One of the most common drivers for reliability failures is the inappropriate adoption of new technologies like LNCSP. Since robust manufacturing and qualifications standards always lag behind implementation, users must carefully select and validate these components for suitability in their use environments and customer applications.

Soldering, flexure, and cleanliness issues have driven many failures seen in production and in the field. All of these areas must be addressed early in the selection and validation processes. In this paper, we will review and discuss LNCSP related reliability concerns and challenges, and propose Physics-of- Failure (PoF) based approaches to allow the successful introduction and failure analysis of LNCSP components in electronics products.

INTRODUCTION

New technologies like LNCSP may initially appear in high volume consumer industries and later migrate to the high reliability products. However, the migration path is not always clear to achieve the necessary reliability confidence. This is especially true for new component packaging technology. Obtaining relevant information can be difficult since data often are segmented and the focus is on design opportunities not reliability risks.

In order to proactively introduce design-in product robustness, the end-to-end reliability program should start with a technology insertion risk assessment. When there is a lack of information, especially due to insufficient industry experiences, a Physics-of-Failure (PoF) approach can be particularly advantageous in identifying risks related to next generation technology.

LNCSP PACKAGES

Leadless, near chip scale packages have been referred to as the poor man's ball grid array (BGA) and are also known as bottom termination components, leadframe chipscale package (LF-CSP), micro-leadframe (MLF), and other names such as QFN, DFN, SON, MLP, LPCC, QLP, and HVQFN.

These packages typically comprise an overmolded leadframe with bond pads exposed on the bottom and arranged along the periphery of the package in one or two rows. Examples of QFN packages are shown in Figure 1. Commonly available in two- or four-sided configurations with either sawed or punched leads, they were developed by multiple component manufacturers in the 1990s and standardized late in the decade by JEDEC/EIAJ.

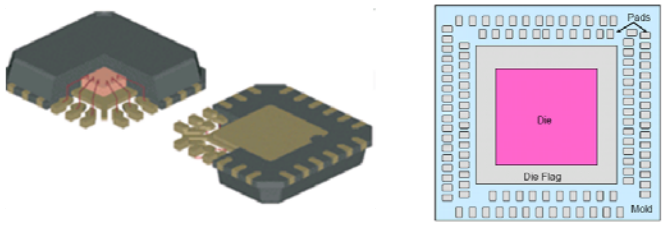

Figure 1: Single & Dual Row QFN Packages

LNCSP RELIABILITY SITUATION

First of all, there are some quality and reliability advantages associated with LNCSPs. They are typically small packages without placement and solder printing constraints like fine pitch leaded devices. Thus, there will be no special handling or trays required to avoid bent or non-planar pins; they are easier to place correctly on PCB pads than, e.g., fine pitch QFPs. They are less prone to bridging defects when proper pad design and stencil apertures are used. The small packages also reduce popcorning related to moisture sensitivity issues. In thermal-related reliability, there is more direct thermal path with larger contact area from Die > Die Attach > Thermal Pad > Solder > Board Bond Pad. The typical LNCSP package thermal impedance is about half of a leaded counterpart.

However, there are major quality and reliability challenges associated with LNCSPs. In a typical thermal cycling test between -40º C to 125º C, a quad flat pack (QFP) package can withstand over 10000 cycles whereas a QFN tends to fail between 1000 to 3000 cycles. Most OEMs have little influence over component packaging; many devices offer only one or two packaging styles. Reliability testing performed by component manufacturers is driven by JEDEC (JESD22 series A & B) and the focus is almost entirely on die, packaging, and first-level interconnections (wire bond, solder bump, etc.) The only focus on second-level interconnect (solder joints) within JEDEC is the JESD22- B113 Cyclic Bend Test, which is driven by the cell phone industry.

There has been some attempt to rectify this absence of information through IPC-9701. Unfortunately, the results have been

limited, as most component manufacturers are not interested in performing thermal cycling or vibration tests of second-level interconnects. This is either because their primary markets (consumer, computer) are not concerned with these stress environments or they view these issues as "application-specific," which can be translated as "this is your problem, not mine."

It is true there are application specific issues, but industry standard acceptance criteria would help in establishing a baseline for new component selection and qualification purposes. Even when there are test "standards" defined, confusions arise due to different test specifications and execution details. For example, JEDEC JESD47 requires ~2300 cycles of 0 to 100ºC, which is typically carried out on thin boards. However, IPC 9701 would recommend 6000 cycles of 0 to 100º C and the test boards should be similar thickness as the end product. Thus, the JEDEC requirements are 60% less than IPC and testing on a thin board can extend lifetimes by 2X to 4X. The problem is if the selection and qualification are based on a "standard" JEDEC test, the components one acquires may only survive 500 cycles of 0 to 100º C in your actual board.

What can one do? In our view, components at risk can be subjected to Physics-of-Failure (PoF) reliability analysis, which starts with failure mechanism understanding.

POF ASSESSMENTS

The PoF approach applies the life-cycle stress and component strength understanding to identify potential failure mechanisms and to prevent operational failures through robust design and manufacturing practices. Reliability assessments based on PoF incorporate reliability into the design process providing a scientific basis for assessing reliability risks under actual operating conditions. For LNCSPs, we will highlight thermal, mechanical, and chemical stresses and evaluate how the packages react under such stresses.

Thermal Stress

One assembly stage thermal stress the LNCSP is exposed to is the reflow profile during the soldering process. Here, the package strength is related to its moisture sensitivity, as there are increasing indications that moisture absorption in the thinner package can drive excessive warpage during reflow. In one case study, a military supplier experienced solder separation under QFNs. The QFN supplier admitted that the package was more susceptible to moisture absorption than initially expected (Figure 2). This resulted in transient swelling during reflow soldering, which induced vertical lift and caused solder separation. This was not a popcorning phenomenon since no evidence of cracking or delamination in the component package was seen. To minimize this potential, larger and thinner QFNs should be treated as an MSL of 3 or higher and reflow profiles should be carefully controlled with a slow, steady ramp rate of 2-3º C/sec max. A similarly controlled cool down is also recommended. If cleaning is performed, the devices should not exit the oven and go directly into a colder cleaning environment. The assembly should be cooler than 60º C before cleaning.

Figure 2: Moisture-related solder fracture

A more challenging thermal issue is the thermal cycling stress these components may experience during their operational life. Multiple package design changes have resulted in the increase in solder joint failure in the current generation of electronic parts. The elimination of leads reduces overall joint compliance. As package sizes shrink, there is more silicon and less plastic, increasing the mismatch in the coefficients of thermal expansion (CTE) between the part and printed circuit board (PCB). Parts are running hotter, which increases the change in temperature (ΔT) at the joint.

QFNs are a good example of reduced robustness of second-level interconnects. For example, under standard thermal cycling environments, QFNs can experience an order of magnitude reduction in time to failure (TtF) from quad flat packs (QFPs) and a 3× reduction from ball grid arrays (BGAs)[1]. This reliability reduction is driven by the die-to-package ratio, package size and I/O count, and the integrity of the thermal pad solder joint. In general, as die size, package size, and number of I/O increase, the number of cycles to fail will decrease — sometimes quite dramatically.

Thermal cycling takes on greater significance when QFNs are conformally coated. When coating material infiltrates under the QFN, the small standoff can result in a high stress state in the solder joint when the conformal coating expands during temperature cycling. A recent study[2] found a significant reduction in mean cycles to failure from a -55° to 125°C cycle, with uncoated QFNs failing in ~2,500 cycles and coated QFNs failing in as little as 300 cycles. A number of companies have responded to this by fencing off QFNs during the conformal coating process.

Mechanical Stress

An assembly related mechanical stress is board flexure. Area array devices like BGAs are known to have board flexure limitations. For SAC alloy attachment, the maximum microstrain can be as low as 500. LNCSPs have an even lower level of compliance and may be more susceptible to flex-induced joint and laminate cracks. Since there is currently limited quantifiable knowledge in this area, be very conservative during board builds. Special focus should be placed on any in-circuit test (ICT) and depanelization processes and on hand assembly operations, since these areas typically induce the most strain.

Another likely mechanical stress is cyclic flexure such as that experienced during bend cycling and vibration, which may result in issues due to the low degree of lead compliance and relatively large footprint of QFNs. For example, International Rectifier tested a 5 × 6 mm QFN to JEDEC JESD22-B113[3]. While the characteristic life demonstrated an extensive number of cycles to failure, the very low beta (~1) suggested brittle fracture, which could be an issue for certain environments. Unfortunately, little test data or analysis is currently available to assess the robustness of LNCSPs in these environments.

Chemical Stress

Large component area, multiple I/Os, a central thermal pad, and low standoff height all combine to entrap flux under LNCSPs post-reflow. When using these devices, soldering process materials should be re-qualified, since particular design and process configurations could result in residual flux residues and/or weak organic acid (WOA) concentrations above a maximum (>150 µg/in2) desired level. Processes using cleanable and no clean fluxes are both vulnerable to dendritic growth. Cleaner variables which should be changed and monitored include deionized (DI) water resistivity, use of a saponifier or surfactant, water temperature, conveyor speed, impingement jet pressure, location, and angle and board loading.

Lack of adequate cleaner maintenance and deionized water control can also contribute to poor cleaning results.

The electric field strength between adjacent conductors (voltage/distance) is also a strong driver for dendritic growth. Digital technology typically has maximum field strength of 0.5 V/mil. Previous generation analog/power technology tended to limit field strength to 1.6 V/mil. The introduction of LNCSPs has increased these maximum electric field strengths, with some components having field strengths as high as 3.5 V/mil. Some component manufacturers are aware of this issue and have modified their designs to maximize the distance between power and ground, while other manufacturers continue to have power and ground on adjacent pins.

Other general factors contributing to dendritic growth include excess solder along with excess flux residues, temperature, and humidity.

IPC-5704, Cleanliness Requirements for Unpopulated Printed Boards, now addresses board cleanliness. It defines the recommended requirements for the cleanliness of unpopulated single, double-sided and multilayer printed boards. However, it does not address *populated* assemblies. Users of LNCSP devices are establishing their own pass/fail limits since no uniformly accepted standard exists. There is currently no obvious trend for weak organic acid (WOA) acceptance limits. What has been seen in the industry appears to be mixtures of absolute maximum acceptable limits and process control limits.

Monitoring and controlling cleanliness throughout the assembly process from start to finish is recommended. Consider cleanliness requirements in terms of IC (ion chromatography) test for assembled printed circuit boards. Establish your own inspection method with accept/reject limits and sampling criteria. Validate compatibility of all new process materials using SIR testing and continue spot check testing of cleanliness using ion chromatography under LNCSPs.

LNCSP Manufacturability Situation

Multiple areas of manufacturing concern regarding the use of LNCSPs have been identified including bond pad design, stencil design, reflow profile control, rework and inspection, and board flexure. For each of these key areas, a brief explanation of the issues and some recommendations are provided.

Bond Pads

Non-soldermask-defined pads (NSMD or copper-defined pads) are preferred since the PCB copper etch process provides for greater dimensional repeatability and control than the solder mask process does. NSMD pads also allow the solder to bond to both the top and the sides of the pad resulting in a stronger, more repeatable joint. If a design does require soldermask-defined (SMD) pads, be aware that the pads can grow or vary in size significantly based on the PCB supplier's capabilities. This may leave the assembly vulnerable to solder bridging. Additionally, consider extending the bond pads 0.2–0.3 mm beyond the package footprint. Solder may or may not wet to the extended edge, but it allows for easier inspection since the outer joints are more clearly visible to an inspector. The extra pad length can also reduce bridging due to excess paste deposition by giving the solder a pathway out from under the component. (Figure 3)

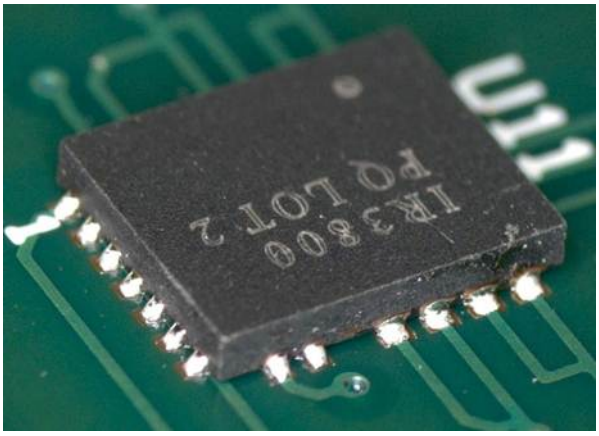

Figure 3 Inspectable Outer Leads

Exercise caution if vias in pads are used. Open vias act as solder drains funneling solder away from the joint down into the via and to the opposite side of the PCB. In the worst-case scenario, there is insufficient solder on the pad and a "solder bump" on the opposing side. This can result in marginal joints on the topside and printing difficulties and solder shorts on the opposing side. Most PCB manufacturers offer several options for closing vias — plugging, capping, tenting — which help keep sufficient paste volume on the pad. Tenting or plugging, the cheaper methods for via closure, are both prone to placement and chemical entrapment issues due to voiding and lack of planarity. Capping is a more robust, more expensive process that eliminates these two concerns. Open vias also result in packages which have less solder joint standoff height from the PCB. This further increases both the entrapment of flux residues under the package and cleaning difficulty.

Stencil Design

Appropriate stencil thickness and aperture design are crucial for reliable soldering of LNCSPs. Begin with the manufacturer's design guidelines when they are provided; the general goal is to provide approximately 2 to 3 mils of solder thickness. (IPC-7093, Design and Assembly Process Implementation for Bottom Termination Components is now released and provides direction for these package styles.) Excessive amounts of paste can induce large-scale voiding of the thermal pad and component float, where the LNCSP is literally lifted off the board. Use multiple, smaller windowpane apertures to avoid large bricks of solder paste that can cause larger and greater numbers of voids. Windowpanes also reduce the propensity for solder balling. For the thermal pad, the general rule of thumb for the ratio of aperture to pad is approximately 0.5:1. (See Figure 4.)

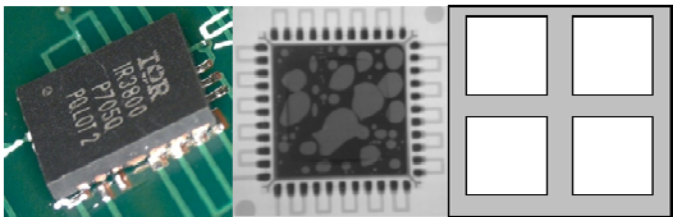

Figure 4: Influence of Stencil Design: Tilt, Voids, Windowpane

Rework and Inspection

LNCSP rework can be difficult, since the thermal pad and any inner row joints are neither accessible nor visible to the repair technician. Mini-stencils, rebumping, or solder performs may be used to replace or add solder volume. Small, portable preheaters can help provide sufficient heat to reliably resolder the larger thermal pad and inner row pads in hand soldering operations.

X-ray inspection equipment is crucial for LNCSPs as this technique allows for inspection for good joints, adequate solder coverage, and void percentage under the package. (IPC-7093 does provide some recommendations for allowable voiding within the thermal pad but there is no rule or specification documenting an acceptable level. It is recommended that producers/manufacturers determine the voids allowable in volume and distribution for respective application requirements.) Robust, concave solder fillets are possible with either sawed or punched LNCSPs. Punched LNCSPs, however, are more prone to concave fillets since more copper is exposed on the component pads. Unfortunately, convex fillets or the absence of fillets are more likely since etching of the leadframe can prevent the bond pads from reaching the edge of the package and the edge of the bond pads are not plated for solderability.

Large, convex fillets also can be an indication of soldering problems such as poor wetting under the LNCSP (Figure 5); tilting due to excessive solder paste on the thermal pad; or elevated solder surface tension, from insufficient solder paste under the thermal pad, pulling the package down.

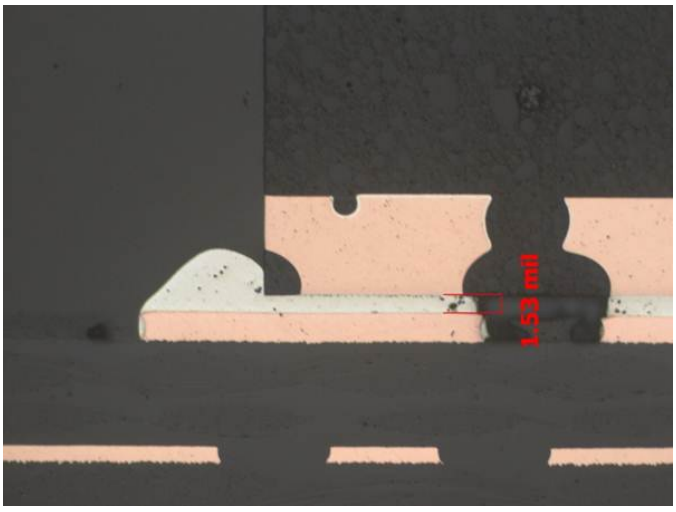

Figure 5: Convex Solder Fillet

CONCLUSIONS

To create a path for the reliable introduction of LNCSP components in high-reliability/severe environment applications, designers, component engineers, and reliability personnel must be aware that heuristic rules may be insufficient and more comprehensive testing and analysis are required such as based on Physics of Failure (PoF). Application-specific reliability analyses and evaluation can be established based on the lifecycle stress and LNCSP strength assessments. Mitigation strategies and guidelines can then be developed to support desired product reliability.

For a successful, reliable introduction of LNCSP components into design and manufacturing, serious assessment is required. At a minimum, the design and manufacturing capability review must include a review of bond pad designs and any design constraints; design of experiment (DOE) on stencil design to optimize thickness and apertures; the degree of reflow profiling control available; assessment of rework and inspection capabilities; and the control of board flexure.

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2. Steve Sytsma and Mark Wrightson, “Lead-free solder durability testing at accelerated thermal excursions for QFN and DFN package interconnects”, SMTA Pan Pacific Symposium, 2007

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