Automated Design Analysis: Comprehensive Modeling of Circuit Card Assemblies

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Abstract

It is widely known and understood that the overall cost and quality of a product is most influenced by decisions made early in the design stage. Finding and correcting design flaws later in the product development cycle is extremely costly. The worst case situation is discovering design problems after failures occur in the field.

Designing for reliability has been "easier said than done" due in large part to the many competing interests involved in a design. For example, the designer is challenged with increasing the product performance while continually reducing the form factor. The reliability engineer may raise concerns about design risks, but without the ability to quantify the potential impact, they are often unable to meaningfully influence the design decisions. Implementing a newly developed reliability prediction analysis tool, Sherlock, will forever change this equation. Before a single product is built, this valuable new tool enables the engineer to import the design files and quantitatively predict the life of the product according to the assumptions made for the user environment. The failure rate is predicted for thermal cycle fatigue of solder joints and plated through hole vias as well as for shorting from conductive anodic filament (CAF) formation. The software also produces a finite element analysis of the circuit boards showing regions susceptible to excessive board strain during vibration or shock events. The greatest value comes from the ability of the engineers to perform various "what if" scenarios to determine the impact of any number of design choices.

- What if I change the mount point locations?
- What if I change the via diameters, the spacing, or the copper thickness?
- What if I change the laminate thickness or material selected?
- What component is at highest risk of failure and what if I change its' format?
- What is the reliability impact of changing from SnPb to SAC305 solder?

Finally, once the design has been optimized to satisfy the many competing requirements, the software can be used to predict the rate of failure over the lifetime of the product. This information can then be used to more accurately plan for the warranty costs. With margins shrinking in the electronics industry, OEMs depend more on profits from extended warranties. Inaccurate life prediction can cut heavily into this income stream. Under-prediction of the failure rate will lead to cost overruns while overestimating failure will mean lost business to competing extended warranty plans and the setting aside of funds that could instead be used for further product development. This paper will illustrate the capabilities and value that this new tool provides to the various functional units within an electronics manufacturing company.

Reliability Assurance

Reliability is the measure of a product's ability to perform the specified function at the customer (independent of environment) over the desired lifetime. Assurance is "freedom from doubt" and confidence in the product's capabilities.

Typical approaches to reliability assurance include 'gut feel', empirical predictions such as MIL-HDBK-217 and TR-332, industry specifications and test-in reliability schemes. Sherlock is reliability assurance software based upon physics of failure algorithms.

The motivation for using the software lies in ensuring sufficient product reliability. This is critical because markets are lost and gained over reliability. Reputations can persist for years or decades and hundreds of millions of dollars are at stake.

Using an automotive example, some common costs of failure:

- Total warranty costs range from $75 to $700 per car
- Failure rates for E/E systems in vehicles range from 1 to 5% in first year of operation (Hansen Report, April 2005).
- Difficult to introduce drive-by-wire, other system-critical components
- E/E issues will result in increase in "walk home" events

Other Costs of Failure Examples

Type of Business	LostRevenue/Hr
Retail Brokerages	$6,450,000
Credit Card Sales Authorization	$2,600,000
Home Shopping Channels	$113,750
Catalog Sales Centers	$90,000
Airline Reservation Centers	$89,500
Cellular Service Activations	$41,000
Package Shipping Services	$28,250
Online Network Connect Fees	$22,250
ATM Service Fees	$14,500
Supermarkets	$10,000

Reliability and Design

The foundation of a reliable product is a robust design. A robust design provides margin, mitigates risk from defects, and satisfies the customer. Assessing and ensuring reliability during the design phase maximizes the return on investment (ROI). For comparison, defects and cost:

- Caught during design: 1x;
- Caught during engineering: 10x;
- Caught during production: 100x
- Caught at the customer: 1000x

Electronic OEMs that use design analysis tools hit development costs 82% more frequently, average 66% fewer re-spins and save up to $26,000 in re-spins.

MTTF / MTBF
Many companies use mean time to failure (MTTF) or mean time between failures (MTBF) calculations as their only means of assessing the reliability of their product while in the design stage. MTTF applies to non-repairable items while MTBF applies to repairable items. They are based on the exponential distribution:

- Distribution: $F(t) = 1 - e^{-\lambda t}$
- Density (pdf): $f(t) = \lambda e^{-\lambda t}$
- Survival (sf): $S(t) = e^{-\lambda t}$
- Failure rate: $\lambda(t) = f(t) / S(t) = \lambda e^{-\lambda t} / e^{-\lambda t} = \lambda$
- MTTF: $= 1 / \lambda$ (Mean Time To Failure)

MTBF is typically calculated through a parts count method. Every part in the design is assigned a failure rate. This failure rate may change with temperature or electrical stress, **but not with time.** Failure rates are summed and then inverted to provide MTBF. Most calculations assume single point of failure while some calculations take into consideration parallel paths

A variety of handbooks provide failure rate numbers. These include MIL-HDBK-217, Telcordia, PRISM, 217Plus, RDF 2000, IEC TR 62380, NSWC Mechanical, Chinese 299B, HRD5. Some companies use internally generated numbers.

MTBF/MTTF calculations tend to assume that failures are random in nature and provide no motivation for failure avoidance. And, it is very easy to manipulate numbers with tweaks made to reach desired MTBF such as modifying quality factors for each component. These calculations are also frequently misinterpreted. Example: A 50K hour MTBF does not mean no failures in 50K hours. Basically these calculations are a better fit towards logistics and procurement, not failure avoidance. Furthermore these calculations do not take into account wear out mechanisms such as solder joint failures, plated through-hole fatigue, or damage due to vibration or shock events.

Process Overview
There are several high levels steps involved in running the Sherlock software. They are:
- Define Reliability Goals
- Define Environments
- Add Circuit Cards
- Import Files
- Generate Inputs
- Perform Analysis
- Interpret Results

Reliability Goals
Desired lifetime and product performance metrics must be identified and documented. The desired lifetime might be defined as the warranty period or by the expectations of the customer. Some companies set reliability goals based on survivability which is often bounded by confidence levels such as 95% reliability with 90% confidence over 15 years. The advantages of using survivability are that it helps set bounds on test time and

sample size and does not assume a failure rate behavior (decreasing, increasing, steady-state).

Defining Environments
Meaningful reliability prediction must take into account the environment in which the product is used. There are several commonly used approaches to identifying the environment. Approach 1 involves the use of industry/military specifications such as MIL-STD-810, MIL-HDBK-310, SAE J1211, IPC-SM-785, Telcordia GR3108, and IEC 60721-3.

The advantages of this approach include the low cost of the standards, their comprehensive nature, and agreement throughout the industry. If information is missing from a given industry, simply consider standards from other industries.

The disadvantages include the age of the standards, some are more than 20 years old, and the lack of validation against current usage. The standards both overestimate and underestimate reliability by an unknown margin. Figure 1 shows an example of such a standard.

Figure 1 Industry standard environmental conditions (IEC 60721-3-3.

Another approach to identifying the field environment is based on actual measurements of similar products in similar environments. This gives the ability to determine both average and realistic worst-case scenarios. All failure-inducing loads can be identified and all environments, manufacturing, transportation, storage, and field, can be included.

In addition to thermal cycle environments, the Sherlock software accepts vibration and shock input as well. Figure 2 shows representation of this input. Identify the number of natural frequencies to look for within the desired frequency range. Single point or frequency sweep loading is available and techniques are also available to equivalence random vibration to harmonic vibration.

Vibration loads can be very complex and may consist of sinusoidal (g as function of frequency), random (g2/Hz as a function of frequency) and sine over/on random. Vibration loads can be multi-axis and damped or amplified depending upon chassis/housing.

shows an example of a PCB stack-up and relevant data for reliability modeling.
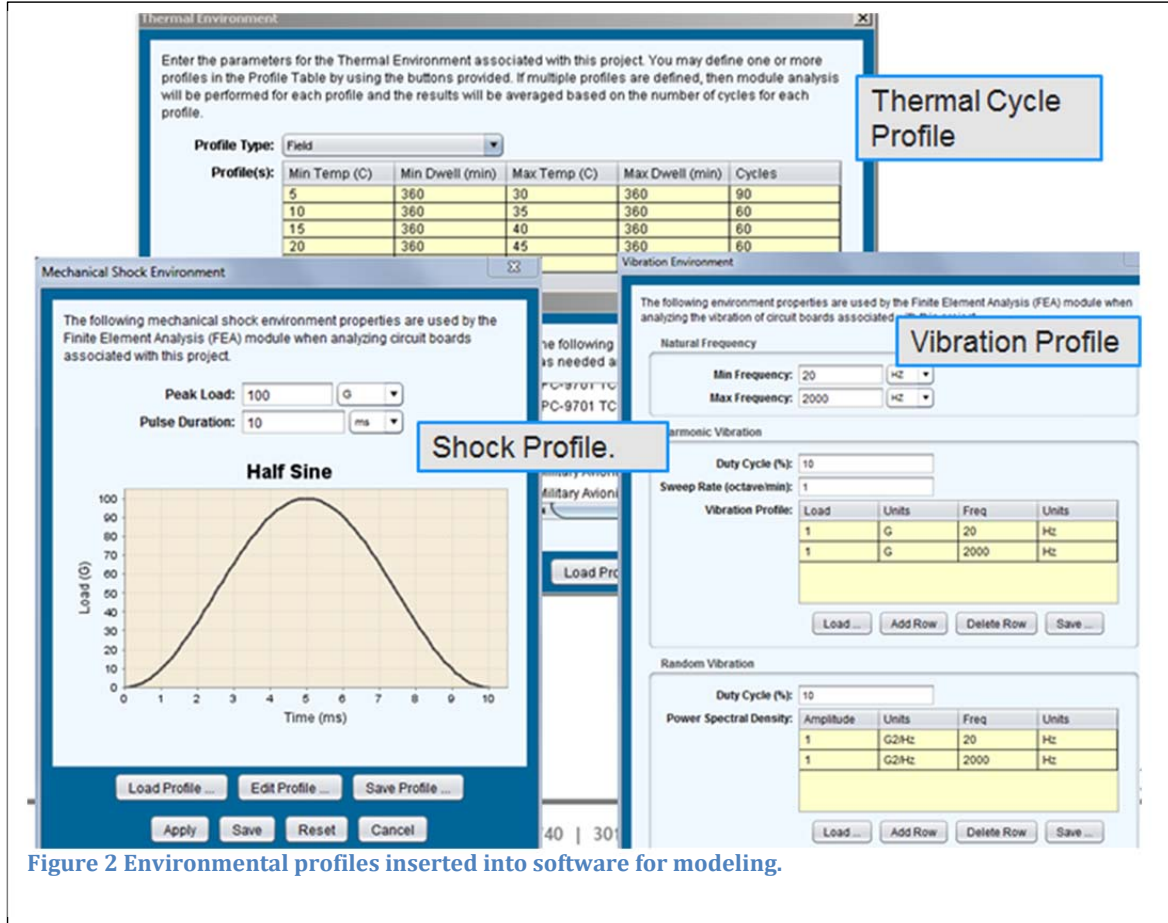

Figure 2 Environmental profiles inserted into software for modeling.

Transmissibility

The response of the electronics will be dependent upon attachments and stiffeners. Peak loads can occur over a range of frequencies including the standard range of 20 to 2000 Hz and an ultrasonic cleaning range of 15 to 400 kHz.

Vibration failures primarily occur when peak loads occur at similar frequencies as the natural frequency of the product / design. Some common natural frequencies:

- Larger boards, simply supported: 60 – 150 Hz
- Smaller boards, wedge locked: 200 – 500 Hz
- Gold wire bonds: 2k – 4kHz
- Aluminum wire bonds: >10kHz

Import Files

The software is designed to accept ODB files which contain all the data for the PCB, the components, and their locations. The data can also be imported with Gerber files and an individual bill of materials. Figure 3
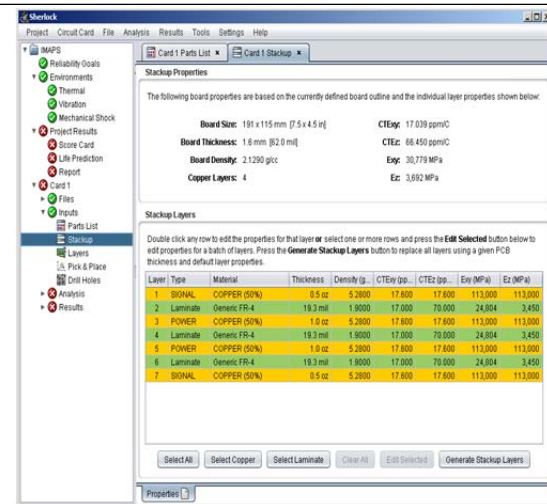

Figure 3. PCB Layer Viewer and relevant data.

Parts List
Individual component data is part of the ODB file; however, modifications to the data can be made manually to ensure the physical characteristics of all the components are accurate. Figure 4 shows the component editor while Figure 5 shows the components laid out on the board.
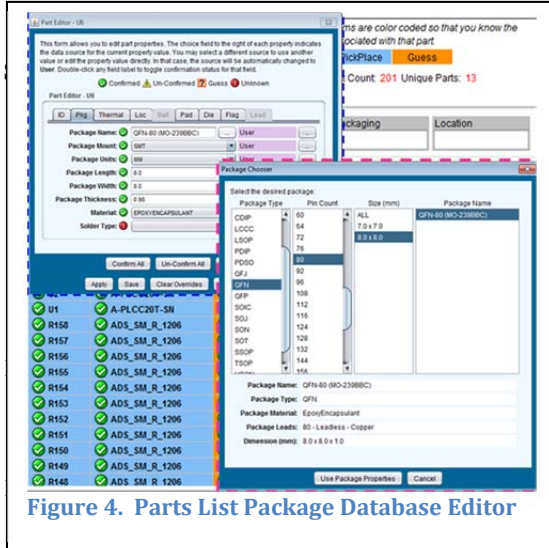

Figure 4. Parts List Package Database Editor

Figure 5. Layer component editor.

Analyses
Six analyses are currently conducted:
- CAF – Conductive Anodic Filament Formation
- Plated Through Hole Fatigue
- Solder Joint Fatigue
- Finite Element Simulations:
  - Natural Frequencies
- Vibration Fatigue
- Mechanical Shock

Conductive Anodic Filament (CAF) Formation
Conductive anodic filament formation is when electrochemical migration of copper occurs between two barrel vias (as shown in Figure 6). The migration occurs through the PCB laminate and not on the surface (which is considered a different defect mechanism).

One factor that drives CAF is damage to the laminate surrounding the drilled via. This can occur from a dull drill bit, excessive desmear etching, or from poorly laminated layers. Environmental factors that can increase the likelihood of CAF formation are the voltage across neighboring vias, the spacing of the vias, and high temperature/humidity conditions. The software evaluates the edge-to-edge spacing of all the vias on the board and estimates the risk of CAF formation based on the damage around each via as well as how well the product was qualified with CAF testing. Such vias can then be assessed to determine if there is a high voltage potential between them or if they could be exposed to high humidity conditions.
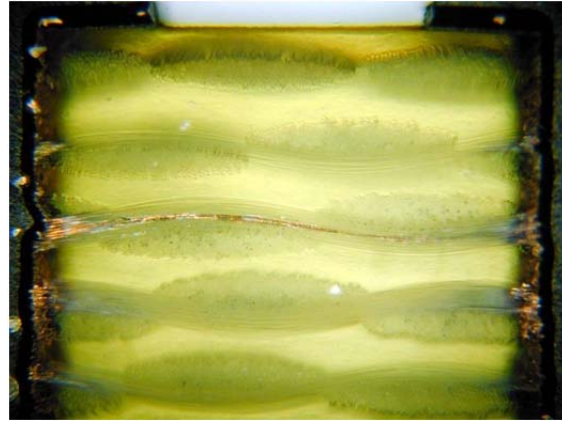

Figure 6. Conductive Anodic Filament formation between vias within the PCB.

PTH Fatigue
Plated Through Hole (PTH) Fatigue occurs when a PCB experiences thermal cycling. The expansion/contraction in the z-direction is much higher than that of the copper which makes up the barrel of the via. The glass fibers constrain the board in the x-y plane but not through the thickness so z-axis expansion can range from $40 - 70$ ppm/C. As a result, a great deal of stress can be built up in the copper via barrels resulting in eventual cracking near the center of the barrel as shown in the cross section photos in Figure 7.
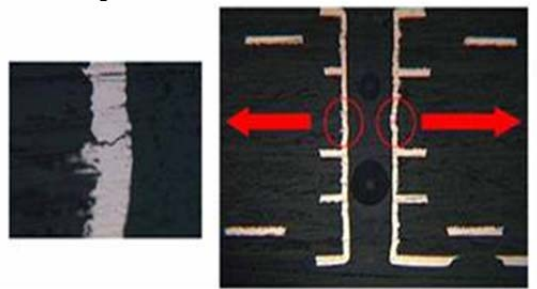

Figure 7. PTH Fatigue Images

A validated industry failure model for PTH fatigue is available in IPC-TR-579, which is based on round-robin testing of 200,000 PTHs performed between 1986 to 1988. This model used hole diameters of 250 µm to 500 µm, board thicknesses of 0.75 mm to 2.25 mm and wall thicknesses of 20 µm and 32 µm. Advantages include the analytical nature in using a straightforward calculation that has been validated through testing.

Disadvantages include the lack of ownership and validation data that is approximately 20 years old. The model is unable to assess complex geometries including PTH spacing and PTH pads that tend to extend lifetime. It is also difficult to assess the effect of multiple temperature cycles. However, this assessment can be performed using Miner's Rule. The PTH equations take into account the expansion coefficient, the thickness of the PCB, the copper thickness, the via diameter, and the glass transition temperature.

In addition to the series of algorithms used to calculate the fatigue life of PTHs, the quality of the copper plating is also taken into account. The "PTH Quality Factor" is a means of estimating the quality of the PTH fabrication process. This is a somewhat subjective determination. Rough edges of the copper wall will provide crack initiation sites and would reduce the quality. On the other hand, smooth copper walls along with a surface finish such as ENIG would improve the quality of the PTH. An example of a failure curve for PTH thermal cycle fatigue is shown in Figure 8 along with a list of vias in order of their expected life.
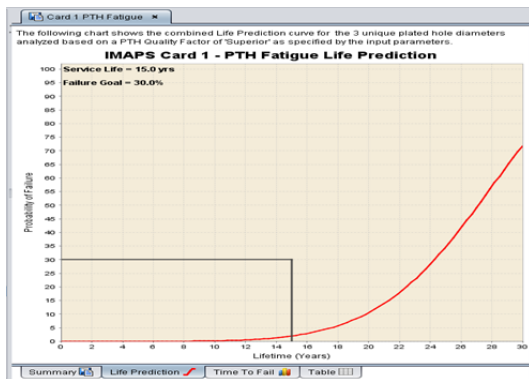

Figure 9. Tabular PTH Fatigue Life Data

Solder Joint Fatigue
Solder joint fatigue failures are becoming more prevalent due to the continued shrinkage of solder joint size and pitch that comes with more advanced packages (Figure 10). The Sherlock software takes into account the physical characteristics of the package and the PCB to calculate the thermal cycle fatigue life of the solder joints. The user can select eutectic tin-lead (SnPb), Lead-free SAC 305 (Sn-3.0%Ag-0.5%Cu) or SN100C (SnCuNiGe). Additional solders may be added in the future and the solder may be specified at the board or at the component level.
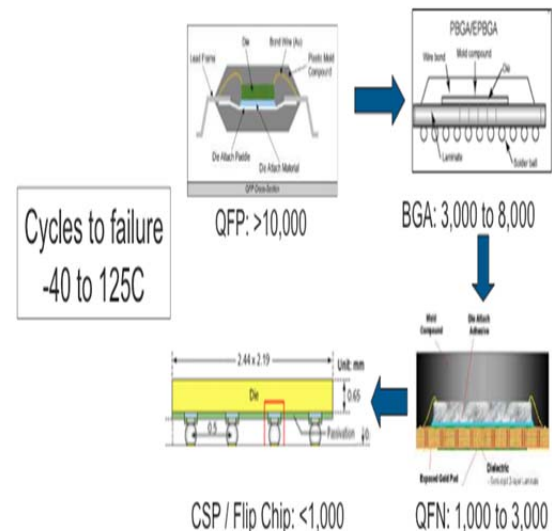

Figure 8. PTH Fatigue Life Prediction

Figure 10. Cycles to Failure for Various Devices

Solder Fatigue Model: Modified Engelmaier
The modified Engelmaier model is used within the software which is a semi-empirical analytical approach using energy based fatigue.

First, determine the strain range, $\Delta\gamma$, using:

$$\Delta\gamma = C \frac{L_D}{h_s} \Delta\alpha\Delta T$$

where C is a correction factor, L_D is diagonal distance, a is CTE, ΔT is temperature cycle, h is solder joint height. C is a function of activation energy, temperature and dwell time. L_D is described further. Da is $a_2 - a_1$ and h_s defaults to 0.1016 mm.

Next, determine the shear force applied to the solder joint using:

$$(\alpha_2 - \alpha_1)\, \Delta T \cdot L_D = F \cdot \left(\frac{L_D}{E_1 A_1} + \frac{L_D}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2-\nu}{9 \cdot G_b a} \right) \right)$$

where F is shear force, L_D is length, E is elastic modulus, A is the area, h is thickness, G is shear modulus, and a is edge length of bond pad. For the subscripts: 1 is the component, 2 is the board, s is the solder joint, c is the bond pad, and b is the board. This model takes into consideration foundation stiffness and both shear and axial loads. Leaded models include lead stiffness.

Area
A1 is thickness of component (h1) x solder joint width and A2 is thickness of board (h2) x solder joint width. As is length of solder joint (Ls) x solder joint width which defaults to 45% of L_D.

Ac is the length of the bond pad (Lc) x solder joint width. Lc defaults to 60% of L_D.

Remaining Parameters (h, G, v, a)
Thickness: h_s defaults to 0.1016 mm and h_c defaults to 0.035 mm

Gs = Es / 2 x (1+v_s) where Es = Temperature dependent modulus of solder and v_s = 0.36.

Gc = Ec / 2 x (1 + v_c) where Ec = 120 GPa and v_c = 0.3.

Gb = Ec / 2 x (1 + v_b) where Eb = 17 GPa and v_b = 0.18.

a = $\sqrt{A_s}$.

Then, determine the strain energy dissipated by the solder joint using:

$$\Delta W = 0.5 \cdot \Delta\gamma \cdot \frac{F}{A_s}$$

Calculate cycles-to-failure (N_{50}), using energy based fatigue models for SAC developed by Syed – Amkor:

$$N_f = (0.0019 \cdot \Delta W)^{-1}$$

and using the energy-based model for SnP

$$N_f = (0.0006061 \cdot \Delta W)^{-1}$$

The software also has user overrides for solder fatigue. These are located in the solder.csv file.

Validation of Modeling Results
A natural question that is asked is how accurate are the Sherlock modeling results compared with actual data? To answer this, over one hundred models were run with individual components and the results compared with reliability data from the literature. The results for QFN, QFP, and BGAs are shown in Figure 11. The predicted results are on the x-axis and the modeled results on the y-axis. A perfect model would result in a diagonal line. Naturally, there is variation in the results; however, for the most part, the predicted results are within a 10% band of the actual data. A larger scatter in data is seen for BGAs, as is typical of experimental results for these components.
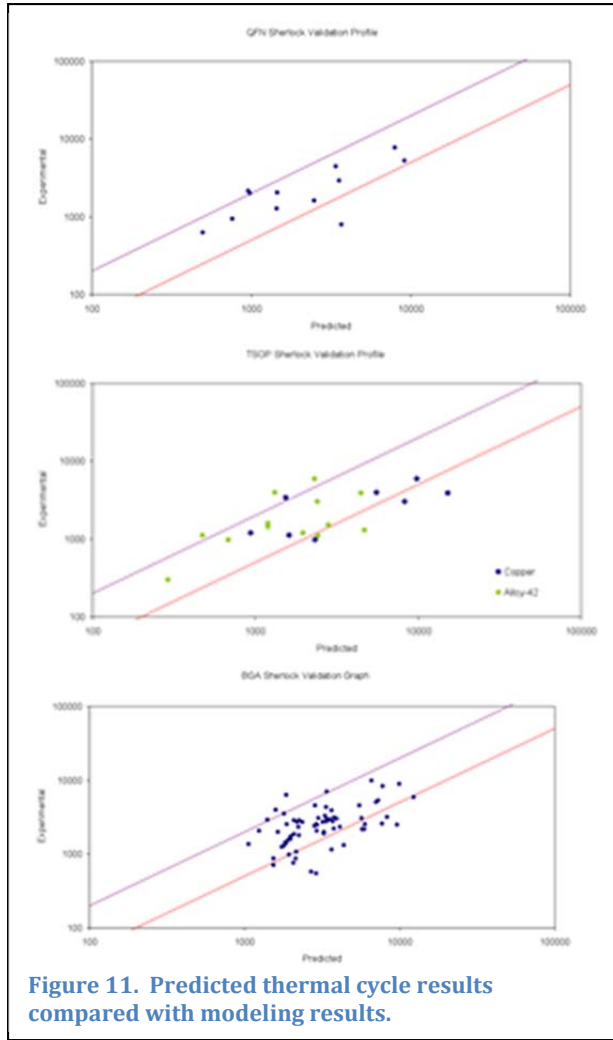

Figure 11. Predicted thermal cycle results compared with modeling results.

Unreliability

Thermal cycle results are provided as an unreliability plot that represents the cumulative reliability of all the components on the circuit card assembly (CCA). An example is shown in Figure 12. The software will go a step further and show the rank order of the individual components and their respective reliability so that the weakest links are determined. Figure 13 shows an example of the results table that is generated. When a product consists of several CCAs, an unreliability failure plot is provided that takes into account all the assemblies.
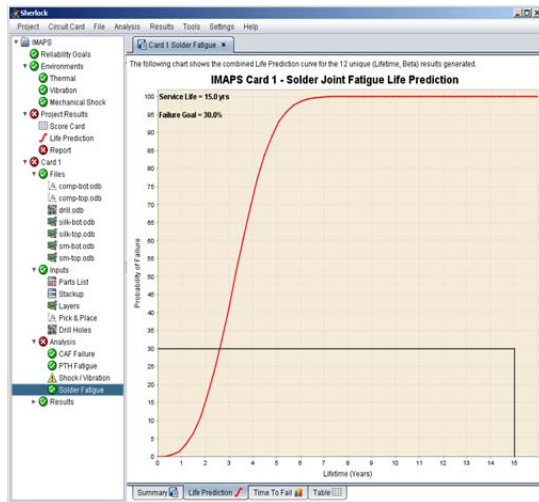
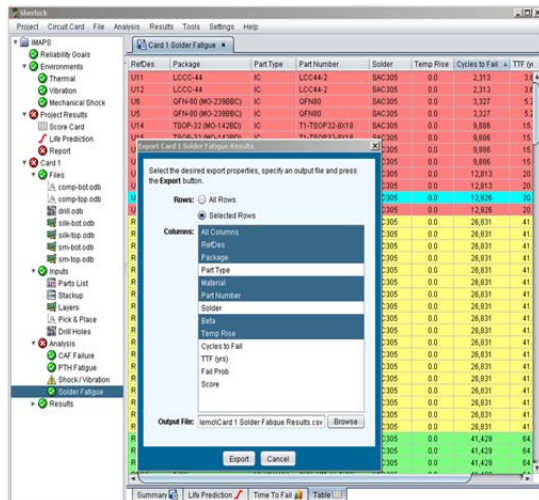**Figure 12 Solder Joint Fatigue Life Prediction (representing a very harsh underhood environment).**

Figure 13. Sherlock Results Table

Natural Frequency Analysis

The Sherlock software contains an embedded finite element modeling tool that allows the user to select the mesh size and angle. The FEA is used to calculate the natural frequencies of the CCA as well as the vibration and shock behavior. An example of the mesh created for a CCA is shown in Figure 14, followed by the 1st natural

frequency generated for the assembly – based off the mount points used for the card.
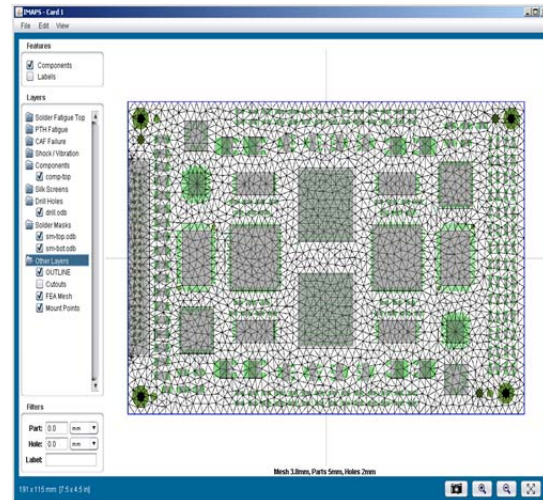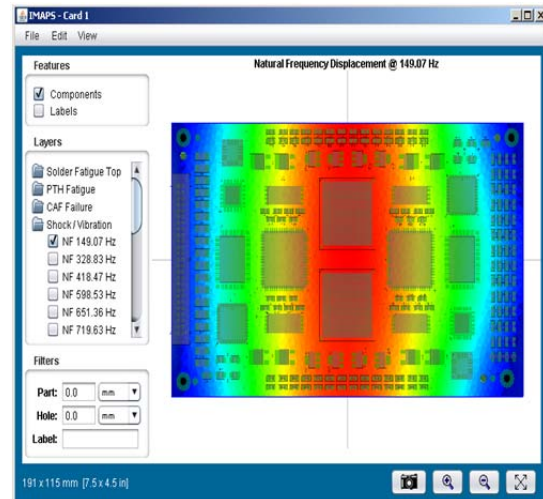

Figure 14. Mesh and Mount Points

Figure 15. Natural Frequency Displacement

Vibration Fatigue

Lifetime under mechanical cycling is divided into low cycle fatigue (LCF) and high cycle fatigue (HCF). LCF is driven by plastic strain and modeled by Coffin-Manson.

$$\varepsilon_p = \varepsilon_f \left(2N_f\right)^c$$

-0.5 < c < -0.7; 1.4 < -^{1}/c > 2

HCF is driven by elastic strain and modeled by Basquin.

$$\varepsilon_e = \frac{\sigma_f}{E}\left(2N_f\right)^b$$

-0.05 < b < -0.12; 8 > -^{1}/b > 20

Mechanical Loads (Vibration)
Exposure to vibration loads can result in highly variable results since:
- Vibration loads can vary by orders of magnitude (e.g., 0.001 g^2/Hz to 1 g^2/Hz)
- Time to failure is very sensitive to vibration loads ($t_f \propto W^4$)
  - Very broad range of vibration environments
  - MIL-STD-810 lists 3 manufacturing categories, 8 transportation categories, 12 operational categories, and 2 supplemental categories

Excessive Vibration (JGPP)
Random Vibration was defined as 9.8 to 28 Grms, 0.07 to 0.5 G^2/Hz with a natural Frequency of 72 Hz. With BGA's, SnPb solder always outperformed lead-free. The results were less conclusive for leadless and leaded parts.

Vibration levels that are too high are more representative of low-cycle fatigue than of high-cycle fatigue. This amount of board strain would crack ceramic capacitors and the information caused quite a stir in the high reliability industries concerning SAC solder.

Realistic High Cycle Fatigue Testing
High cycle fatigue testing can take weeks on an electro-dynamic shaker. Some results of such testing are shown in Figure 16.
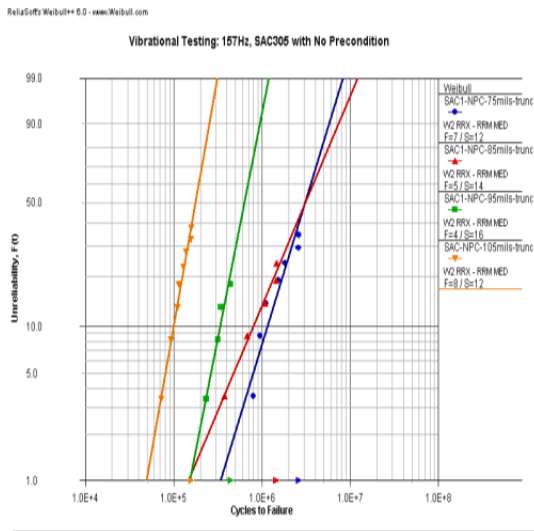

Figure 76. Realistic High Cycle Fatigue Testing for SAC 305

Vibration Interpretation
SAC solder is 'stiffer' than SnPb solder. For a given force per load, SAC will respond with a lower displacement / strain, both elastic and plastic.

Low-cycle fatigue is plasticity driven. Under displacement-driven mechanical cycling, SnPb will tend to out-perform SAC (e.g., chip scale packages, CSP).

Under load-driven mechanical cycling, SAC will tend to out-perform SnPb (e.g., leads of thin scale outline packages, TSOP). High-cycle fatigue is elasticity driven. Stiffer SAC solder exhibits a lower strain range.

Typical Method Vibration: Steinberg
Step 1 is the calculation of maximum deflection (Z_0).

$$Z_0 = \frac{9.8 \times 3\sqrt{\pi/2 \times PSD \times f_n \times Q}}{f_n^2}$$

where PSD is the power spectral density (g^2/Hz), f_n is the natural frequency of the CCA, and Q is the transmissibility which is assumed to be square root of natural frequency.

Step 2 is to calculate the critical displacement.

$$Z_c = \frac{0.00022}{chr} \frac{B}{\sqrt{L}}$$

Where B is length of PCB parallel to component, c is a component packaging constant typically 1 to 2.25, h is PCB thickness, r is a relative position factor and is 1.0 when a component is at the center of the PCB and L is component length.

Step 3 is the life calculation.

$$N_0 = N_c \left(\frac{Z_c}{Z_0} \right)^{6.4} \quad \text{where } N_c \text{ is 10 or 20 million cycles.}$$

Several assumptions made for this calculation are:
- The CCA is simply supported on all four edges. More realistic support conditions, such as standoffs or wedge locks, can result in a lower or higher displacements.
- The chassis natural frequency differs from the CCA natural frequency by at least factor of two (octave) which prevents coupling.
- Vibration occurs at room temperature. Depending upon the configuration and loading, vibration at lower or higher temperatures can increase/decrease lifetime
- The calculation does not consider the influence of in-plane displacement (i.e., tall components).

Vibration Software Implementation
The software uses the finite element results for board level strain in a modified Steinberg-like formula that substitutes the board level strain for deflection and computes cycles to failure. Critical strain for the component is defined by:

$$\varepsilon_c = \frac{\zeta}{c\sqrt{L}}$$

where ζ is analogous to 0.00022B but modified for strain, c is a component packaging constant, 1 to 2.25 and L is component length.

The Miles Equation relates Harmonic vibration to random vibration and must be utilized until the random vibration FEA code is fully tested and released.

$$G_{RMS} = \sqrt{\frac{\pi}{2} f_n Q \ [ASD_{input}]}$$

where f_n = Natural frequency, Q = transmissibility and ASD_{input} = Input spectral density in g^2/Hz.

Sherlock vibration modeling results show the displacement of the PCB at all locations (see Figure 17). The results are plotted for each axis of vibration and the most impacted components are revealed in the component list (Figure 18). Fatigue results are also shown in an unreliability plot over the life of the product, in the case where vibration is an ongoing event.

Mechanical Shock Environments
Mechanical shock requirements were initially driven by experiences during shipping and transportation. Shock became of increasing importance with the use of portable electronic devices and is a surprising concern for portable medical devices.

The basic environmental contributing factors include:
- Height or G levels
- Surface (e.g., concrete)
- Orientation (corner or face; all orientations or worst-case)
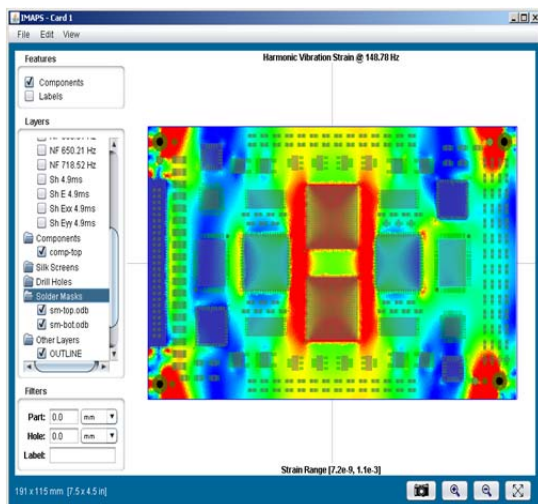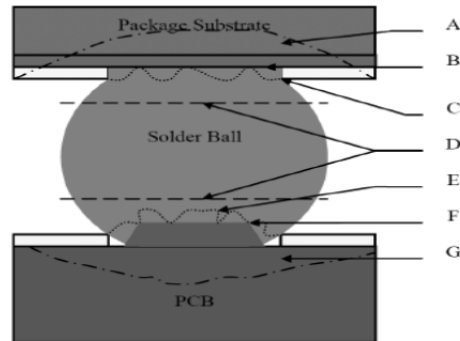- Number of drops

Figure 87 Graphical Vibration Results

Figure 98 Graphical Vibration Results

JEDEC Shock Failure
Failures related to mechanical shock typically cause pad cratering (A,G in the image) and intermetallic fracture (B, F in the Figure 19). This is an overstress failure not a fatigue failure and follows a random failure distribution.

Legend
A Package Pad Lift/Crater
B Pkg Base Metal/IMC Interface Fracture
C Pkg IMC/Solder Interface Fracture
D Bulk Solder Fracture
E PCB IMC/Solder Interface Fracture
F PCB Solder pad/IMC Interface Fracture
G PCB Pad Lift/Crater

Figure 109. JESD22-B110A, Subassembly Mechanical Shock

The software analyzes shock based upon a critical board level strain and will not predict how many drops to failure. Either the design is robust with regards to the expected shock environment or it is not. Additional work being initiated to investigate corner staking patterns and material influences. An example of the modeling showing displacement across a CCA after a shock event is shown in Figure 20. The rank order of components experiencing the largest strain are shown in Figure 21.
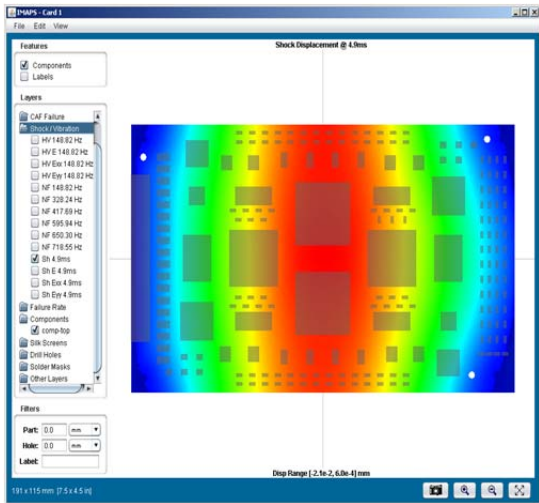
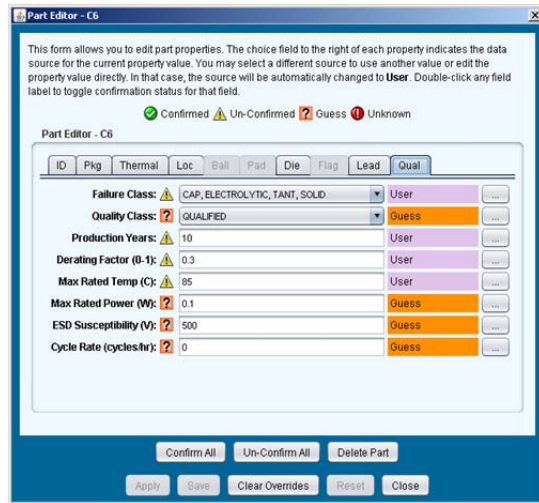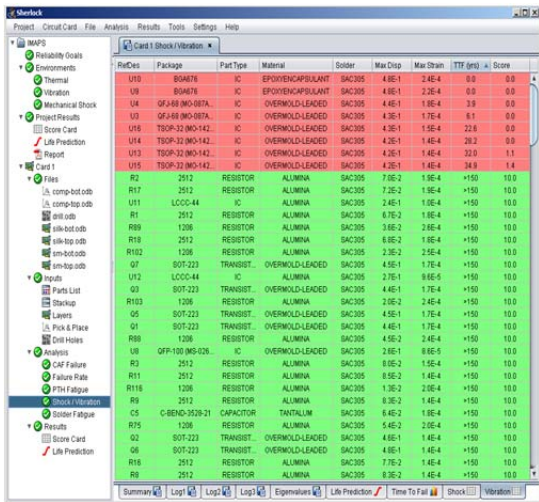**Figure 20. Shock displacement results for a test board.**

Figure 21. Components are listed in order of those experiencing the highest strain.

Constant Failure Rate Module

A recent addition to the software has been the inclusion of a constant failure rate model using MIL-HNBK-217F calculations. Inputs necessary to compute failure rates are located in the parts list (Figure 22). The component failure rate is based off the 217F model and takes into account the temperatures at which the product operates. An example of the unreliability failure plot is shown in Figure 23, along with failure rates from solder joint fatigue and vibration.
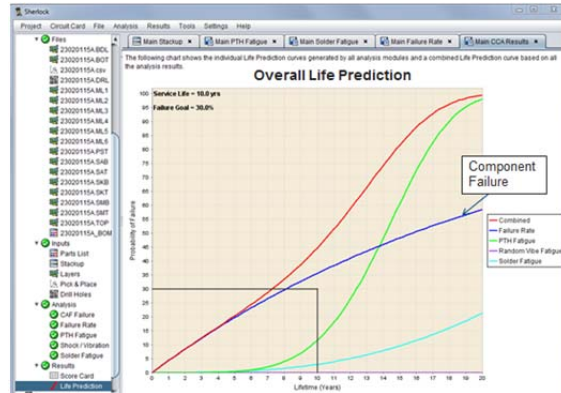

Figure 22. Failure Rate Information Entry

Figure 113. Life Prediction that combines component failure with PTH and solder fatigue.

Discussion

The use of the Sherlock circuit card assembly reliability modeling tool is limited only by the imagination and needs of the user. There are a wide range of problems it can either solve or provide insight to with regards to designing a reliable product. Some of these uses are identified below:

- o   Use Sherlock to determine thermal cycle test requirements needed to replicate the user environment.
- o   Use to modify mount point locations
- o   Use to determine environmental stress screen (ESS) conditions.
- o   Determine impact of component package modifications/changes.
- o   Determine impact of changing to Pb-free solder.
- o   Determine expected warranty costs.

The appropriate test conditions can be determined by first generating a solder joint fatigue model based on the expected field conditions of the product. The percent failure at the required life is then known for the design. The model is then rerun using the desired thermal cycle

test conditions (say 0 to 100°C). The number of cycles required to generate the same percent failure shown in the previous model is how many cycles are required (with no great percent failure). Naturally, the number of cycles may be increased if the sample size is reduced.

Early in the design phase of a product is the best time to run various what-if scenarios for the design. These might include experimenting to determine where the mount point locations should be in order to reduce strain on sensitive components. One may also run thermal cycling modeling using the various package options available for critical integrated circuits. The impact of changing a product from SnPb to Pb-free solder may also be evaluated.

Some high reliability products required 100% ESS to ensure no poorly built products escaped production. A common ESS test is thermal cycling; however, one does not wish to remove more than 5% of the useful life of the product during the ESS. By modeling the total life, one can make sure that the number of cycles selected for ESS is appropriate.

Finally, many consumer electronic companies provide a warranty period for their products. Funds must be set aside for each product shipped to cover the expected field returns within the warranty period. It is important that these costs be roughly accurate and based on data, since money is lost if the retained amount is too large or too small. The results provide by Sherlock can provide a portion of the total expected field returns due to hardware wear-out mechanisms.

Summary
The simple truth is that designing in reliability up front pays off immensely over the life of the product. To date, there has not been a simple to use method of estimating the wear-out life of an electronic product. Sherlock software is designed to fill this need and does so by allowing a rapid assessment of electronic systems reliability utilizing Physics of Failure (PoF).

Sherlock is a powerful reliability tool that can be used by the entire engineering design and management team. It allows the reliability group to get involved in the design process as well, as they now can better quantify tradeoffs before the product is ready for testing. Sherlock is the future of Automated Design Analysis (ADA): the integration of design rules, best practices and a return to a physics based understanding of product reliability.