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GLOBAL TECHNOLOGY AWARD WINNERS

Bruce Moloznik Interview Inside

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Low Tg underfill—The background

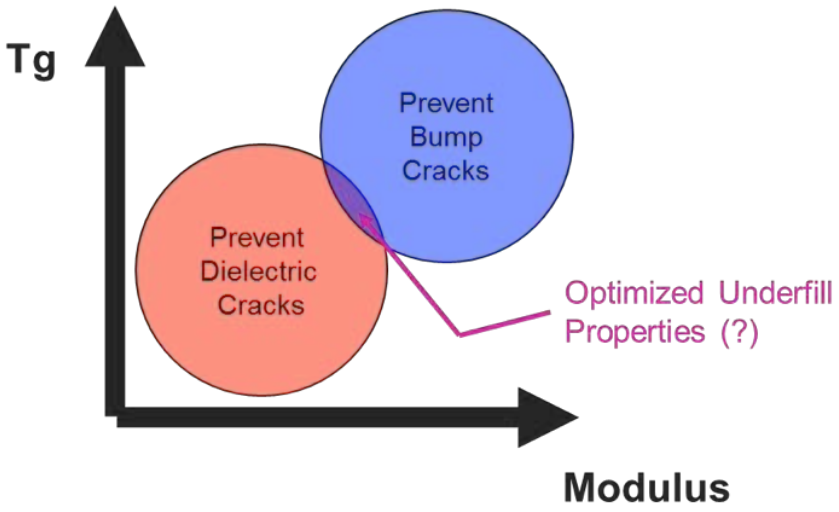
Craig Hillman

Underfill, in some respects, has been an impressive technological advance for component packaging and follows similar historical trends for many innovations. In some respects, the real revolution was the concept of 'flipping' over the die face down and using solderable connections to create a high density array of connections between the integrated circuit and the substrate. This feat is attributed to IBM through the introduction of its controlled collapse chip connection (C4) technology in the 360 Mainframe System in 1964. The C4 was not quite the flip chip we know today, as it had solid copper balls covered in solder. Subsequent work by IBM, DEC, and Motorola eventually drove the adoption of an industry standard flip chip design with high lead solder bumps (97Pb/3Sn).

Amusing thought: Most references acknowledge IBM as the creator of the technology, but the terminology 'flip chip' comes from DEC.

The development of flip chip packaging in 1961 is amazing when one considers that the invention of the integrated circuit only occurred two years before (Jack Kilby of Texas Instruments and Robert Noyce of Fairchild filed their patents in 1959). In fact, it was so early, the initial flip chip packaging was applied to transistor devices, not integrated circuits. And yet while integrated circuit technology went from 10 transistors to 1 million transistors over the next 30 years, flip chip technology, by relative comparison, stagnated. Flip chip packages, while offering substantial density and electrical performance improvements, remained a niche product limited to die below a certain size (distance to neutral point) while wire bonds, the technology it was designed to replace, soared in popularity.

Why the discrepancy? Need, cost, and knowledge. The need was based on the reality that silicon flip devices have a very low coefficient of thermal expansion (approximately 2.5 ppm/°C). To survive the assembly process and any temperature variation in the field, flip chip devices had to be assembled to ceramic substrates. The problem was that ceramic substrates can be 2X to 10X the cost of organic-based substrates (typically FR-4 or Bis-aleimide Triazine (BT)). And there was a lack of knowledge on how to mitigate this restriction. The result was that flip chip technology remained at levels far below 1% of the annual integrated circuit production.



Which takes us back to the original focus of this article: underfill. Like many technologies, the adoption of flip chip was limited until the introduction of an enabler technology. Examples such as LEDs, touchscreen, and composites have all gone through this process. In some respects, the electronic industry was lucky as the enabling technology does not emerge until 40 to 50 years after the initial invention. In the case of underfill, just as with flip chip, there were several companies investigating the technology in the late 1980's. However, Hitachi is often recognized as the first company to publish and patent the concept that is most aligned with the underfill we know today.

With the introduction of underfill, the market for flip chip technology increased rapidly as flip chips could now be bonded to low-cost organic substrates. Through an extensive amount of testing and material design of experiments performed at IBM, the preferred properties of the underfill are a high modulus, low CTE material. Through several iterations, this ends up being primarily an epoxy with an elevated glass transition temperature (between 125°C to 150°C) and highly filled with silica (glass) beads with a 'sufficient' amount of shrinkage. (I'll explain this a little later.) Through tweaking of the polymer chemistry and the size distribution of the filler particles, underfill manufacturers are able to greatly improve manufacturability, expand capillary function, and reduce cure time and temperature.

So far, so good, right? And it potentially gets even better. Several authors stated that since the cost of wirebonding is I/O *dependent* while the cost of solder bumping is I/O *independent*, there would be a crossover point where it would be cheaper to go from wire bond to flip chip. As is usual with these kinds of projections, the reality turned out

to be more complicated, as the predicted threshold went from 100 I/O, to 300 I/O, to 500 I/O, etc. (You get the picture.) A more up to date, fascinating, and nuanced analysis was recently completed by Chet Palesko and Jan Vardaman. As of 2010, the cost cross-over seemed to be around 1000 I/O for gold wire bonds and not until 2000 I/O for copper wire bonds. [Reminds me of the constant prediction that solid state drives will be cheaper than disc drives. These predictions often fail to consider the human element, which is people working on the existing technology do not like to give up their jobs willingly.]

But there were other reasons to migrate to flip chip packaging (size, electrical performance, thermal performance), and the watershed moment for the technology was likely when Intel released the Pentium III in 1999, which was the first flip chip CPU on an organic substrate. This was in the middle of a rapid surge in flip chip packaging, where flip chip as a percentage of integrated circuit packaging went from less than 1% to almost 10% over two decades.

And then, as usual, the market threw a curve ball. Actually, it threw two curve balls. (Apologies for the sport reference for those readers that do not have baseball in their home country.) The first market adjustment was the increasing demand for mobile electronics. As described by Ken Gileo, initial attempts to leverage existing underfill materials for flip chip on board (FCOB) in mobile devices were abject failures because of a dramatic change in environments. Here was an application that could care less about temperature or power cycling, unlike server applications (IBM/Intel), but was extremely sensitive to mechanical loads (specifically bending/handling and mechanical shock).

The second curve ball was the use of porous SiO2 as a low-K dielectric, starting with the 90 nm technology node devices. While porous SiO2 was an elegant solution to the challenging problem of signal delay (due to an ever increasing RC time constant), it simply kicked the can down the road to the packaging level. The result of the weaker dielectric (what else would you expect when you add voids to a material?) was the introduction of the 'white bump' failure mechanism, where the low-K dielectric would crack after underfill cure (depending on bump geometry, under bump metallurgy, die size, etc.).

The solution, to both problems, was to 'soften' (reduce the elastic modulus) the underfill. The most straightforward way to change this mechanical property and not radically change other elements of the material was to lower the glass transition temperature (Tg). However, the Tg could not be reduced too dramatically or its original value would be eliminated. This conundrum led to the 'optimum' low Tg underfill, which prevented mechanical failures, eliminated white bump failures, and still maintained temperature cycling robustness. It was almost too good to be true. And it was… (read my column next month for the what, how, and why).

Craig Hillman is CEO and Managing Member for DfR Solutions. Dr. Hillman's specialties include best practices in Design for Reliability (DfR), Pb-Free strategies for transitioning to Pb-free, supplier qualification (commodity and engineered products), passive component technology (capacitors, resistors, etc.), and printed board failure mechanisms. Dr. Hillman has over 40 Publications and has presented on a wide variety of reliability issues to over 250 companies and organizations.