Chip Scale® REVIEW

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The International Magazine for the Semiconductor Packaging Industry

Volume 18, Number 5

September • October 2014

Suitability of Cu wire bonded ICs for automotive applications

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- Encapsulated WLCSP
- Evolution of wafer dicing
- Lowering the cost of MEMS
- Die attach solutions for thin die applications
- Reliable testing of Cu pillar technology for smart devices
- High-reliability via interconnections in glass wafers for 2.5D

Spring Pins vs. Johnstech Solid Contacts

High Cost of Ownership

Multiple Moving Parts

High Inductance Short MTBA

LOW CCC HIGH VARIANCE

Wildly Varying CRES

High Mean Time to Repair

Lowest Cost of Ownership

EXTENDED MTBA Stable

High CCC New and Innovative Technologies

LOW INDUCTANCE High Performance

Long Life LOW AND STEADY CRES

Wafer and Package Test High OEE

Backward Compatible Load Board Designs

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The demanding and harsh environment in which automotive electronics must operate poses reliability challenges as the industry migrates from gold to copper bond wires. Only optimized package design with well-controlled assembly processes are suitable for this application. Potential solutions for automotive grade electronic components are presented in this article.

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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

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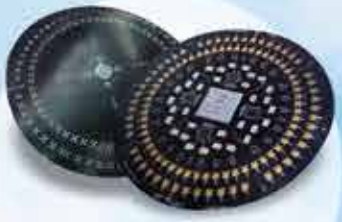
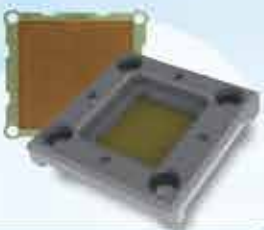


Wafer Level CSP Probe Card

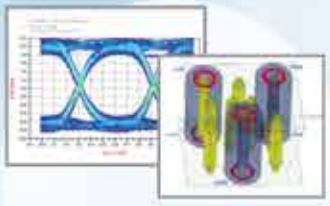
Memory Socket

Spring Contact Probe

SLT Socket



Elastomer Socket



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FROM THE PUBLISHER

Don't forget to pack your copy of CSR before you head off to the cornucopia of conferences the industry is serving up this Fall. Perhaps you are already equipped and picked up your copy at SMTA International, or in Grenoble France at SEMICON Europa. If IMAPS or TSensors Summit is to your liking, perhaps you hopped over to San Diego. Mark your calendar Nov. 11-13 for IWLPC – now in its 11th year – which comes complete with keynote address, plenary sessions, professional development courses, an exclusive 3D panel, and two days of exhibits. IWLPC is the leading industry conference with a 25% increase in registrations over last year. The conference has attracted 19 countries and 31 states from the USA. Be sure to register by October 8 to receive the early bird rate – there is no better time than the present!

See you there!

Kim Newman
Publisher

FEATURE ARTICLES

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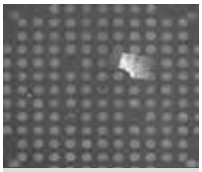
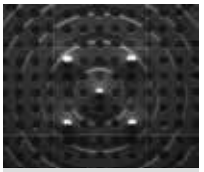
Die Chipout Inspection


Eject Cup F/M


Wafer Ejector Pin Maker Inspection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FLIP CHIP BONDER - S100

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	CHIP ROTATION(θ)	±0.05 °@ 3σ	
BONDING HEAD	BONDING FORCE	1N~20N (Programmable from 1N)	
FOOTPRINT	DIMENSION (Wx Dx H)	1,600mm x 1,230mm x 1,600mm	
	WEIGHT	2,600 kg	

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Calling all chip and system-level designers to IWLPC 2014

3DInCites

By Françoise von Trapp [3D InCites]

For years, the industry has discussed and debated 3D integration technologies, discussing the market drivers, technology challenges, supply chain issues, and above all, the cost. As the roadmaps continued to be pushed out, manufacturers, suppliers, and R&D centers have addressed these concerns, and foundries and outsourced semiconductor assembly and test suppliers (OSATS) have made the necessary capital expenditures and declared themselves ready to ramp production. Still, commercialization lags, waiting for system-level integrators to design 3D ICs into their products.

Why the hold-up? Until very recently, it was believed that performance, power, and cost issues were best solved through continued CMOS scaling to smaller nodes. However, as the cost of scaling continues to rise and the 2.5D/3D manufacturing gaps continue to narrow, 2.5D/3D is emerging as a formidable opponent to node scaling, as well as a preferred solution for heterogeneous system-level integration (**Figure 1**). From a design perspective, until the manufacturing gaps close, it hasn't made sense to design in 3D.

Now that all manufacturing processes are in place, we at 3D InCites decided it was time to bring the system integrators and manufacturers together in a public forum to share their knowledge and concerns by sponsoring a panel at IWLPC that will appeal to both the design and manufacturing communities, and therefore draw attendance from both. As such, system integrators and manufacturers will face-off in a discussion about the system-level advantages of 3D ICs, and whether 3D ICs can solve the issues of SoC design complexity and the cost of CMOS scaling to future nodes. There will be no presentations by the panelists. Rather, the audience will participate in a real-time poll to gauge current industry understanding of these advantages, and the panelists will be invited to present their perspectives on the same polling questions.

Invited panelists include Belgacem Haba, a senior staff member at Google's Data Center Platform; Mike Gianfagna, VP marketing, eSilicon Corporation; Bob Patti, CTO, Tezzaron Semiconductor; Ramakanth Alapati, Package Architecture and Customer Technology group, GLOBALFOUNDRIES; Simon McElrea, CTO of Tessera and president of Invensas Corp.; Rozalia Beica, CTO of Yole Développement; and E. Jan Vardaman, founder and president of TechSearch International, Inc.

Prior to joining Google, Haba was VP and Senior Fellow at Tessera/Invensas. His latest activities while heading the mobile R&D division include developing 3D technologies for mobile devices and servers. So why would Google be interested in 3D technologies? While the company's initial product offering was the Google search engine, it has grown to offer a realm of Internet-based information tools that require a vast number of high-performance data centers to operate. Google has gone so far as to manufacture its own servers, and anecdotally it's been said that although the company doesn't sell servers, it is the fifth largest server manufacturer. So Google stands to benefit greatly from implementing 2.5D and 3D IC devices at the system level.

McElrea noted in a keynote presentation at the BiTS Workshop, March 2014, that the organizations that ultimately take 2.5D and 3D IC to commercialization may not be the traditional semiconductor players, (foundries, OSATS, IDMs, etc.) but rather the end-product owners who are weary of waiting for solutions to their high-performance, low-power needs and will take matters into their own hands—companies like Apple, Google, Microsoft, Facebook and Amazon. "Even while designing innovative bridge technologies to address the current technology requirements, Invensas has had 2.5D and 3D IC in our sights and on our technology roadmap as the ultimate solution for system-level integration," said McElrea.

According to Gianfagna, eSilicon delivers custom integrated circuits and performance-optimized IP to its customers worldwide through a combination of internal resources and management of a global supply chain

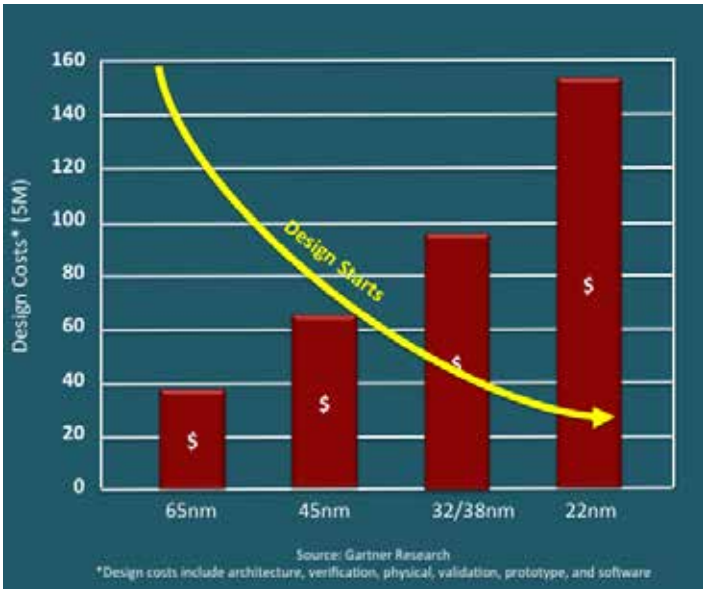

Figure 1: The number of design starts decline as the cost of design increases at smaller nodes. SOURCE: Gartner Research

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Max: 12mm x 12mm

Pin Count:
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Pin Count:
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H-PIN SOCKET

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Pin Count:
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using a fabless model. Similar to many fabless companies, Gianfagna says they are acutely aware of the rapidly growing cost of single-chip solutions at advanced process nodes. “eSilicon views 2.5 and 3D integration as a viable method to bring these costs down and create more custom design opportunities,” he said. “We’re working actively to build the required internal skills and supply chain relationships to address this new and growing market.”

Known throughout the industry as one of the pioneers of 3D technologies, Bob Patti, CTO of Tezzaron Semiconductors, is one of the greatest proponents of 3D integration. He brings perspective from both the chip/system design side and manufacturing to the panels. Explaining how he first decided to investigate the benefits of 3D technologies at Tezzaron, he says, "Back in the 90s we designed gallium arsenide logic. Those transistors were extremely fast, like today’s nanoscale CMOS transistors; so we found our design performance to be entirely dominated by interconnect delay. We realized that further performance improvement required reducing the wire length. That’s when we turned to 3D. Later, we discovered tremendous power reductions, enhanced reparability, and other benefits. We’ve focused on 3D ever since."

Alapati leads the Package Architecture and Customer Technology group focused on delivering package-differentiated solutions, and led the 3D TSV technology startup in GLOBALFOUNDRIES Fab 8 for sub-20nm nodes. Until recently, he was also responsible for sub-20nm CPI qualification. Prior to joining GLOBALFOUNDRIES, Rama was with Micron Technology for 8 years, first as an etch engineer focused on pitch-doubling technology for sub-50nm NAND, and later as an assignee at imec focusing on 3D IC and BEOL integration. “As Moore's Law continues to be challenged at the leading edge, the importance of package architectures to continue node-based scaling and provide energy-efficient solutions has never been more apparent,” he noted. “GLOBALFOUNDRIES continues to invest in advanced packaging technologies to provide such solutions to customers and to meet the growing needs in all product segments.”

In addition to her work at Yole, Beica has been involved in the research, application and strategic marketing of advanced packaging and 3D IC technologies for over 16 years. She recently published a chapter on system-level advantages, market trends and applications for 3D ICs in the latest edition of the Handbook of 3D Integration Volume 3.

Vardaman has also been following the progress of 2.5D and 3D ICs very closely, and has been accurate in her conservative predictions of when it would hit mainstream. In a recent presentation to the GSA 3D IC working group, she indicated that volume shipments of the Hybrid Memory Cube (HMC) will happen in 2015. “That’s what I call high-volume manufacturing,” she said. Her team at TechSearch International has just completed a detailed gap analysis on 3D IC readiness, and she will have interesting data to reference.

During the panel, which is titled “System-level Advantages of 3D Integration,” Haba and Gianfagna will represent the system integrators. McElrea and Alapati represent the manufacturing perspective. Patti brings perspective from both the chip/system design side and manufacturing, and Beica and Vardaman will balance out the panel, providing the market analyst perspective. Get ready for a lively discussion.

Biography

Françoise von Trapp received her BA in communications at the U.of New Hampshire, and is editorial director and Queen of 3D at 3D InCites; www.3DinCites.com; email francoise@3dincites.com

Barriers to the successful commercialization of MEMS

By Roger H. Grace [Roger Grace Associates]

This article provides the results of the recently completed 2013 MEMS Industry Commercialization Report Card Study (Report Card) [1]. The Report Card has been published annually beginning in 1998. For the establishment of the specific topics of the Report Card, market research was conducted on the general topic of technology commercialization and resulted in the selection of a number of critical success factors (aka, topics) that were considered necessary for successful commercialization specific to MEMS and to the MEMS industry.

The purpose of the Report Card is to provide MEMS industry participants with an objective assessment of these critical success factors over time and to act as a tool to help them better understand, respond to and exploit the ever changing dynamics of the MEMS industry. The MEMS Industry Commercialization Report Card has been developed not only to help assess the progress of the commercialization of this technology, but more importantly to serve as a vehicle to help guide industry participants overcome the barriers to the successful commercialization of MEMS.

The Report Card addresses many of the critical components of the MEMS commercialization process model (**Figure 1**) that I created based on extensive research and includes design for manufacturing (DfM) and test, infrastructure, marketing and market research.

The problem

The commercialization process has been researched and tracked for several MEMS products, e.g., pressure sensors, accelerometers, and shows that it takes, on average, approximately 30 years for these products to become totally commercialized [2].

More importantly, however, the total sales of MEMS as reported by numerous groups in 1998 was approximately 1/25th of the sales of ICs at the time of the publishing of the first Report Card. The MEMS market for 2013 has been reported by several organizations to be approximately $10-$12 Billion (US), whereas Gartner Research has reported that the total IC market for 2013 was $315.0 Billion (US)—approximately a 30:1 ratio. The positive news here is that the MEMS market has been reported to be growing over the past several years at a compound annual growth rate (CAGR) in the 10-12% range (primarily fueled by mobile phones/tablets and consumer products). The IC market, however, has recently fluctuated: $299.9B (US) in 2012 and $307.8B (US) in 2011 (per Gartner Research) [3]. The question still remains, however, why is there still such a significant disparity in the market sizes? The Report Card's raison d'être is to help address this seeming paradox.

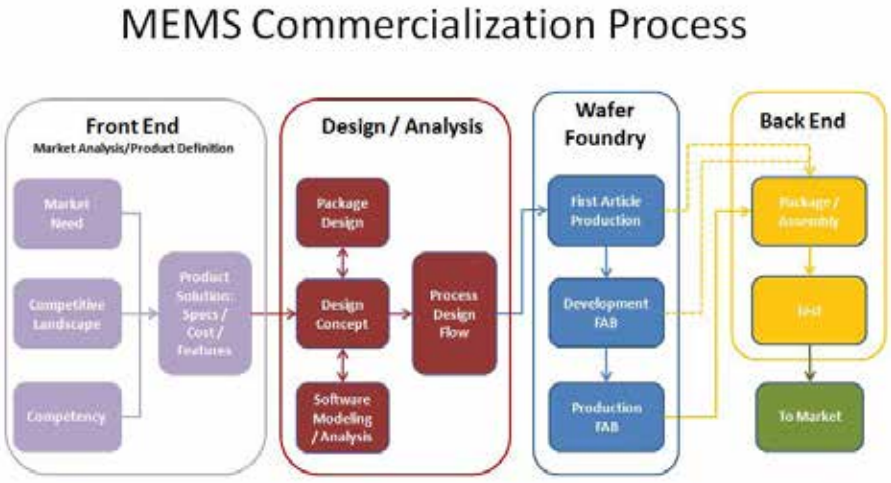

Figure 1: THE MEMS commercialization process model addresses many of the 14 topics included in the MEMS Industry Report Card. Courtesy: Roger Grace Associates

Research methodology

Figure 2 provides the letter grade results of the 2013 MEMS Commercialization Report Card on a yearly basis from 1998 to 2013. It also provides the change in grade from 2012 to 2013, as well as the standard deviation of the responses for each of the 14 topic grades in 2013.

Results

Of the approximately 1200 comments that were submitted, I have reviewed all of these and have attempted to summarize responses that reflect the consensus. (Details are available in ref. #1.) Change from the 2012 to 2013 grades are provided, as well as the standard deviations (SD) of the grades for each of the subjects from 1998 to 2013. The following provides a summary of the results of each of the 14 topics including my interpretations of the consensus overviews of the "verbatims."

R&D: 2013 Grade=B, 2012 Grade=B, Change=0, SD=1.6. R&D has typically received uniformly high grades since the inception of the Report Card in 1998—never falling below a grade of B. The focus of R&D activity

appears to be on "small R" and "large D." There has been a decline in US Federal support, but there is widespread new hope on the expected financial support of the "new players," e.g., Google, Apple.

Marketing: 2013 Grade=B-, 2012 Grade=C+, Change=+1, SD=1.8. The marketing efforts by organizations to support the sales of MEMS devices and services has been hampered by a technology push versus that of an applications/market pull strategy. MEMS marketing has typically received mediocre grades with the lowest being C- and hovering in the C level. I believe that "MEMS marketing" is considered to be an oxymoron [4] primarily influenced by the lack of knowledge and familiarity of basic marketing principles by MEMS industry participants, lack of adequate market research on unfulfilled customer needs, limited budget allocations and "we have a better mousetrap" mentality of MEMS industry management. MEMS marketing plays a vital role in the commercialization process as noted in Figure 1.

Market research: 2013 Grade B-, 2012 Grade B-, Change=0, SD=1.4. While there are several organizations specializing in providing market research vis-à-vis published reports and custom market studies, there appears to be a consensus that existing market research results significantly falls short of client expectations. Current market research is too focused on the mobile market. For example, there is not enough consideration provided on other markets including industrial and military. Furthermore, the market research tends to address the values of the markets based on extrapolation of existing numbers and not on values representative of emerging technologies and/or applications (i.e., shortsighted).

Design for manufacturing (DfM): 2013 Grade=B, 2012 Grade B-, Change=+1, SD=1.6. The focus on the "design solution" includes not only the MEMS element, but also, and at a minimum, the signal conditioning and packaging of the device. Regrettably, and only until recently, has the non-sensor related part of the solution become important especially with software/algorithms. This continues to be a major shortcoming of MEMS developers because the cost of the package, assembly and test of a solution can account from between 60-75 % of the total cost of producing the device. There was consensus that with the emergence of high-volume/low-cost applications presented by the consumer market, DfM is trickling down into many other applications.

Established infrastructure: 2013 Grade=A-, 2012 Grade =A-, Change=0, SD=1.5. Established Infrastructure has historically garnered high grades. After starting off with a C+ in 1998, it has been in the A-region most of the time. Once again, the MEMS established infrastructure is a dominant element on the MEMS commercialization process as noted in Figure 1. The consensus of the "verbatims" support the previous assessment in DfM, i.e., that there needs to be more support of back-end process activities including assembly, packaging and testing. Currently, front-end silicon wafer foundries are abundant and readily available to accommodate all sizes of silicon wafers and all levels of throughput.

Management expertise: 2013 Grade=B, 2012 Grade=B, Change=0, SD=1.8. It is difficult to train managers for the MEMS industry; as a result, many of the entrants to the industry continue to come from the semiconductor industry. There appears to be a lack of sensitivity and awareness as to the difference with MEMS and ICs, especially in the applications sector. Bottom line – there is much room for improvement here.

Venture capital attraction: 2013 Grade=D+, 2012 Grade=D+, Change=0, SD=1.5. Venture Capital Attraction has tended to follow the stock market and overall investment business trends and Report Card results mirror this phenomenon. In the heyday of the "dot com boom" in 2001, it received an A. In the worldwide economic meltdown of 2009, it dipped to D. Since that time, it has only recovered to a level of D+. Consensus is that now VCs are not as interested in hardware companies, but rather biomed, nanotechnology, and now, social media, are in favor. The major opportunity for MEMS entrepreneurs has come from acquisition, e.g., Fairchild (Jyve) and Amphenol (NovaSensor).

2013 MEMS COMMERCIALIZATION REPORT CARD

SUBJECT	98	99	00	01	02	03	04	05	06	07	08	09	10	11	12	13	Δ	SD
R&D	A	A	A	A	A	A-	A-	A-	A-	A-	B+	B	B	B+	B	B	0	1.6
Marketing	C-	C	C+	C+	C+	C	C	C+	C+	C+	C+	C	C	C+	C+	B-	+1	1.8
Market Research	C	B-	B-	B-	B	B	B+	B-	B	B	B	B+	A-	B	B-	B-	0	1.4
Design For Manufacturing	C+	B-	B	B	B	B	B	C+	B-	B	B+	A-	A-	B+	B-	B	+1	1.6
Established Infrastructure	C+	B	B+	A	A	A	A	A-	A-	A-	B+	B+	A-	A-	A-	A-	0	1.5
Management Expertise	C	C	C+	C+	C+	C+	C+	B-	B-	B	B	B	B	B	B	B	0	1.8
Venture Capital Attraction	C	B-	B+	A	C	C-	C	C+	C+	C	C-	D	D+	D+	D+	D+	0	1.5
Creation Of Wealth	C	B-	B+	A	C	C-	C-	C-	C-	C	C-	D+	C-	C+	C+	C+	0	1.9
Profitability	C-	C-	C-	C-	C-	C-	C-	C	C+	C	C-	D+	D	C-	C	C+	+1	1.8
Industry Roadmap	INC	B-	B	B+	A-	A	A	B	B-	C+	C-	C-	C	C	C	C+	+1	1.8
Industry Association	INC	INC	INC	B	B+	B+	B+	B	B	B+	B	B	A-	B+	B+	B+	0	1.6
Standards	INC	INC	INC	INC	C	B-	B-	B-	C+	C	C	C	C+	C	C	C+	+1	1.8
Employment	INC	INC	INC	INC	INC	C	C	C+	C+	C+	C	C-	C	C+	C+	C+	0	1.6
Cluster Development	INC	INC	INC	INC	INC	B	B+	B+	B	B-	C+	C+	C+	C	C+	C+	0	1.8
Overall Grade	C+	B-	B	B	B-	B-	B	B	B-	B-	C+	C+	B-	B-	B-	B-	0	NA

ROGER GRACE ASSOCIATES MARKETING COUNSEL

Figure 2: Since its debut in 1998, the MEMS Industry Report Card has annually addressed the industry's performance critical success factors for MEMS Commercialization. Courtesy: Roger Grace Associates

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- RF / Microwave Modules

Photonic Packaging

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- LED Assemblies
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- Silicon Photonic Packaging

MEMS Assembly

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- Pressure Sensors
- Accelerometers
- MEMS Gyroscope
- Inkjet Assembly

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Creation of wealth: 2013 Grade=C+, 2012 Grade=C+, Change=0, SD=1.9. There have been several instances where there has been significant creation of wealth by MEMS participants. InvenSense alone has reported over 100 multi-millionaires as a result of its very successful IPO. However, the road to riches is expected to continue to come from buyouts, not from the "old fashioned way," i.e., shipping products at a profit. The major news is the acquisition of Nest by Google for $3.2B and Measurement Specialties by TE Connectivity for $1.7B. In addition, several other smaller MEMS companies, e.g., Xsense and Jyve by Fairchild, have been acquired by larger companies. There is widespread major excitement in anticipation that more of this will happen in the near future and that this exit strategy is becoming the approach of favor.

Profitability: 2013 Grade=C+, 2012 Grade=C, Change=0, SD=1.8. It appears that the consensus is that high-volume suppliers, e.g., phone/tablet/automotive suppliers, are under a profit squeeze, but lower volume suppliers, e.g., industrial and military/aerospace are quite comfortable with their margins.

Industry roadmap: 2013 Grade=C+, 2012 Grade=C, Change+1, SD=1.8. Several organizations have attempted creating industry roadmaps. The Micro and Nanotechnology Commercialization Education Foundation created its first MEMS Roadmap in 2002 and has updated it several times [2]. Currently, the Trillion Sensors Roadmap group, headed by Dr. Janusz Bryzek, began its sensor road mapping efforts over 12 months ago [5]. Many of the MEMS industry gurus are on this committee. The jury is still out from the respondents as to the value of a MEMS roadmap. I personally consider road mapping efforts to be laborious, difficult, and drawn out when performed by industry volunteers, but well worthwhile to industry participants when finally completed.

Industry association: 2013 Grade=B+, 2012 Grade=B+, Change=0, SD=1.6. The MEMS Industry Group is considered to be doing an excellent job of serving the needs of the MEMS community based on the consensus of respondents. In "verbatim" mentions, it received the largest number (31). One area that appears to need improvement is in attracting users of MEMS to the group—currently suppliers of devices and equipment/foundry infrastructure providers form the majority of the group.

Standards: 2013 Grade=C+, 2012 Grade=C, Change=+1, SD=1.8. MEMS standards have a long way to go to be able to have any impact on successful commercialization efforts. They are far overshadowed by the standards efforts and resulting success of the semiconductor industry, which has approximately 1000 formal standards vs. approximately a dozen for MEMS. I have personally been involved with MEMS standard development for over 10 years and the progress is rather slow.

Employment: 2013 Grade=C+, 2012 Grade=C+, Change=0, SD=1.6. Employment in the MEMS industry appears to be looking better as a continuous increase of business level from the lows of 2008/2009. Large companies like Google and Apple have hired many MEMS engineers.

Cluster development: 2013 Grade=C+, 2012 Grade=C+, Change=0, SD=1.8. I believe that, based on the "verbatim" responses, the concept and benefits of MEMS technology clusters are not well known – especially by US respondents. Clusters need to have more promotion and demonstrated value creation to become more viable in the minds of the MEMS community.

Summary

The 2013 MEMS Commercialization Report Card provided an overall grade of B- to the 14 critical success factors for MEMS commercialization. The overall grade did not change from the B-grades of 2010, 2011 and 2012. More importantly, however, was the change in the individual grades of the 14 topics. The Established Infrastructure topic had the highest grade of A-, and Venture Capital Attraction had the lowest grade of D+. Five topics increased one grade level, no topics decreased in their grade level, and nine topics remained constant.

Increasing one grade level from 2012 were Profitability (C+), Marketing (B-), Design for Manufacturing (B), Industry Roadmap (C+), and Standards (C+). The standard deviations based on the approximately 85 responses for each topic went from a high of 1.9 for Creation of Wealth, to 1.4 for Market Research. The grades established that Venture Capital Attraction continues to need major improvement and may be the critical item in restraining the industry from realizing its true potential. Venture Capital Attraction has been in the D category since 2009 when the worldwide crisis hit our economy and regrettably, venture capital monies have been targeted to software and social media startups.

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Biography

Roger H. Grace is president of Roger Grace Associates (Naples, FL) which he founded in 1982 as a marketing consultancy serving the sensor, MEMS, IC and capital equipment markets. He holds the BSEE and MSEE (as a Raytheon Company Fellow) degrees from Northeastern U. where he was awarded the "Engineering Alumni of the Year" Award in 2004. He was a visiting lecturer at the U. of California at Berkeley College of Engineering from 1990 to 2004; email rgrace@rgrace.com; www.rgrace.com

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By Chip Scale Review staff editor

Interview with Reinhart Richter,
Chief Technical Officer of Xcerra Corporation

Reinhart Richter is Chief Technical Officer of Xcerra Corporation. He holds a doctorate degree in Solid State Physics from McGill University, Montreal, Canada. After graduation, Reinhart worked for three years in a project on the industrialization of neutron radiography. He then worked several years as a consultant on using statistics and statistics software in quality control, engineering and research, and later moved into an account management position for these products in the semiconductor industry. At KLA-Tencor Corp. he served as account and sales manager, director of a business unit, and director of operations in Central Europe. In 2002 he joined Multitest as Vice President for Sales, Service and Marketing. 2011 he was appointed CEO of Multitest.

Q: How will Xcerra stay competitive with respect to continuing the development of semiconductor/sensor testing?

To the first order, the semiconductor device die is driving the evolution and choice of automated test equipment (ATE); packaging plays a fairly minor role in this. In contrast, however, packaging is driving the evolution and choice of test handling systems; the specifics of the device design and content have limited impact on the handler. The choice of the interface between handler and ATE – i.e., load board and contactor – has to satisfy ATE, handler and device specifics. Advanced packaging – be that wire bonded multi-chip modules (MCMs), wafer-level chip-scale packaging (WLCSP), fan-out wafer-level packaging (FOWLP), or 3D through-silicon via (TSV) die stacks or any variation thereof – is impacting all three elements of the test cell: ATE, tester, and test interface. In the end, the objective is to come up with the best test strategy from wafer probe to final package minimizing cost while ensuring 0 test escapes. Xcerra is able to be deeply involved in all aspects of test – not only the three hardware elements, but also the strategy, test insertion points, etc. I am strongly convinced that we should be able to offer the best solutions to individual customer challenges. In addition, through our atg-Luther & Maelzer PCB test group we are also ensuring the integrity of advanced substrates, be they Si-based or organic. Today, we can configure a test cell for pretty much all automotive/industrial, mobile devices, Internet of Things (IoT) applications and be highly competitive in terms of capability, versatility and cost-of-test. Going forward we will hone our product and solutions portfolio using our insight in the test cell and the business of our customers. So, my concern is not to stay competitive, but rather to prioritize the right projects to make us grow even faster.

Q: How are testing technologies evolving, especially in light of the impact of the Internet of Things?

The IoT does pose many challenges. From a test point of view there are two extremes: 1) the IoT end node providing individual, local, environmental data, the data context engines (servers) providing meaningful information back to the end node or end user based on the data received and stored, and 2) the "stuff" in between that transports all the data.

Advanced packaging is playing an important role in all three areas: combining sensors, MCUs and radios into useful end nodes, transporting the exploding data volumes from end node to context engine, and crunching through those exabytes to provide meaningful and relevant feedback to the user. Each of these three infrastructure elements of the IoT is defining unique test cell requirements.

For IoT end nodes there will be a need for different approaches. Although IoT applications will be very high volume, there will be a strong element of customization or mass customization. This will mean offering more than just the highly parallel (144+) test. In addition, these types of applications are going to demand testing solutions that are much more closely aligned with the assembly and packaging process flow, and can be quickly configured to deal with a much broader range of test parameters. Moore's law describes the evolution of transistor density; you can restate Moore's law as functionality per $ (Euro, Yen, RMB) spent, or number of consumers reached with electronic devices. So, to enable IoT testing, the industry will need to continue to focus on lowering the cost (of test) for the end node and that will mean a mix of high test parallelism, suitable sensor stimulus, and the ability to quickly reconfigure for the broader range of stimulus types.

Similarly, fast data routers will pose a challenge. Integrating optical data transceivers that convert fiber optical data streams into computing devices will be needed to transfer and process exabytes of data effectively at high speeds and minimized power consumption. At this point, I cannot say which challenges in test such devices will pose—this is still to be defined.

On the data context side we will need much more powerful computing chips. Data rates and power consumption of data transfer between cores and memory blocks, as well as the bus to the outside world, seem to be the focus of attention where advanced packaging plays a big role. Test folks will need to come up with very innovative solutions.

Q: How is Xcerra managing the financial challenges that come with its R&D roadmap schedule? (E.g., internal R&D, external R&D, consortia activities, etc.) Can you provide an update on some of these activities?

For Xcerra, the challenge is no different than for any of our peer companies. A certain percentage of our revenue is used for continuing R&D and product development. In doing R&D, we work also with external resources such as institutes, universities, suppliers and sometimes also consortia. Focus areas are – probably not a surprise – test and measurement technology, including algorithms, material and surface technology, high-speed controls, thermal techniques, and software development.

Q: How do you see the semiconductor testing technology roadmap unfolding in the next 2-3 years? What about within the next 5 years? Are there any activities the industry needs to do a better job of evaluating or exploring or funding to meet the evolving needs of its (packaging/testing) technology roadmap?

On the ATE side there are certainly continuing challenges: IoT and mobile applications drive the development of devices consuming lesser power or even no power. In return, devices operate at lower voltage and lower currents and require low-signal precision. The IoT will also drive more low power RF devices, and more RF built-in self test (BIST) will be needed to keep ATE costs down. Also on the RF side, demand for more advanced automotive safety devices has recently triggered the development of a 77GHz integrated test cell. And of course, customers want to test at higher multisite factors with best-in-class efficiency, which poses challenges for instrumentation and architecture. Further, there will be an on-going demand to deal with much higher volumes of test data. This will require ATE architectures that are not just optimized for high units per hour (UPH) and a broad range of applications. This will demand the ability to provide users with these high volumes of test data without impacting the overall productivity of the test cell.

For test handlers there is a continuing trend to even smaller and thinner packages, smaller I/O pitches, more I/Os and the requirement for more precise temperature control of the DUT. And all of that is to be at higher multisite contacting without having the complexity of the handler explode. For lower multisite test cells – say 16x or below – an individual device plunging into the test socket will continue to be the method of choice; however, the industry needs to do a much better job tackling the test cell overall equipment efficiency (OEE) losses inflicted by the handler or contactor. For higher multisite factors, single device plunge needs to yield to DUT array plunging – in strip or carrier – as otherwise the handler will be so complex that its reliability limits (or cost) will destroy any advantage from higher multisite factors. Higher multisite testing of large I/O count, narrow pitch array packages will also drive new contacting technologies offering appropriate electrical performance and yet support narrower pin spacing and less contacting force.

Q: Do you have any other comments or observations about the semiconductor packaging industry you would like to share with our readers?

Packaging is a significant part of the value proposition to our end customers, i.e., the electronics industry or the consumer itself. The end applications drive the choice of packaging and the device form factors. The package and the transport medium not only define the choice of test handler, and thereby cost-of-test, they also have a huge impact on test cell OEE. Great example: micro small-outlined packages (MSOPs) were in vogue for some time. Shipping them in tubes required gravity handling. MSOPs being often wider than long, in conjunction with poor mold quality (mold flash), caused test cell OEEs to be pitiful and made customers lose a lot of money. Today, we have similar challenges: moving to 0.35mm or even 0.3mm I/O pitches with imprecise device singulation (sawing) requires the test handler to align optically the device I/O array to the contactor pin array; significant increases in test handler capex (+10-20%) will be the consequence. More interaction between advanced packaging people and test handler makers is needed similarly to IC designers talking to the ATE makers.

About Xcerra Corporation

Xcerra Corporation is the parent company of four powerful brands that have been supplying products and services to the semiconductor and electronics manufacturing industry for more than 30 years. Xcerra's four brands are atg-Luther & Maelzer, Everett Charles Technologies, LTX-Credence, and Multitest.

Xcerra Semiconductor Test Cell: LTX-Credence Diamondx, Multitest MT2168, Multitest loadboard and Multitest Mercury contactors.

Xcerra Corporation was formed in 2014 following the LTX-Credence acquisition of Everett Charles Technologies (ECT) and Multitest from Dover Corporation in December of 2013. The strategic vision of the LTX-Credence management team in making these acquisitions was to build a company with a greater share of the semiconductor test cell market. A key component of the long term growth strategy for Xcerra is to offer differentiated semiconductor test products and services that include providing customers a fully integrated test cell solution directly to their production floor. This strategy allows customers to procure key components of the test cell such as the tester, handler, contactors and interface boards, from a single supplier and to take delivery of a turnkey solution directly into their high-volume manufacturing environment. This strategy reduces risk for the customer associated with doing the test cell integration and has the added benefit of accelerating the ability to get new products to market faster.

While the semiconductor capital equipment market is the largest driver of Xcerra's business, the acquisition of Everett Charles Technologies expanded the company into vertical markets associated with PCB testing. Within ECT there is another business, atg-Luther & Maelzer, which has been in business for more than 30 years providing test systems for bare-board PCB test.

After a PCB has been manufactured, atg-Luther & Maelzer testers are used to verify point-to-point continuity. There are two different types of test technologies applied to bare-board PCB testing: universal grid and flying probe. atg-Luther & Maelzer has a leadership position in the flying probe tester market.

ECT also provides fixture design, development and fabrication services for the in-circuit and functional test of assembled PCBs and provides these services on a global basis. ECT also markets a wide range of pins and compliant connectors used in many different types of test applications but also in market segments completely outside of test.

The interconnect foundry: a new manufacturing paradigm for WLP

By Garry Pycroft [Deca Technologies]

For the past decade, innovation in advanced packaging processes has launched a metamorphosis in the semiconductor supply chain as traditional wire bond processes have given way to wafer-level packaging (WLP) technologies to meet reduced feature size requirements of shrinking silicon nodes and increased IC pin-counts. WLP technologies require engineering skill sets, equipment, and processes that extend beyond that of many of the traditional packaging providers (aka semiconductor assembly and test service [SATS] providers), crossing over into the domain of wafer foundries. This has led to the market being served by a limited number of suppliers having the financial means to support the significant investments required. An opportunity therefore exists for a supplier with a differentiated approach employing a completely different form of capital.

While they have risen to the challenge of building WLP capability and capacity, the SATS' return on investment (ROI) has been challenged because of the significant capex spending required for traditional wafer fab equipment. The wafer foundries additionally see an opportunity to extend their role in the market by investing or redeploying existing capital to serve the WLP market. Both entities, however, are offering comparable services with similar capital structures, which limits differentiation. The somewhat common approach in the status quo has created an opportunity for a unique entity to serve the specific needs of wafer-level interconnects by adapting proven capabilities from other industries. This article will review the evolving roles of SATS and front-end foundries, and discuss the promise that a unique interconnect foundry holds for the future by driving improvements in several key areas of the supply chain such as cycle time, flexibility and cost.

The semiconductor supply chain evolution

The term "interconnect foundry" captures what's needed in response to the transition happening in the semiconductor supply chain. Prior to the emergence of wafer bumping, the line of demarcation between front-end foundry processes and package assembly and test processes was clearly defined. Foundries manufactured wafers and performed all the lithography and metallization steps to achieve first-level interconnect. These wafers were delivered to the SATS, where singulation, wire bond assembly, package interconnect processes, overmold, and testing was performed. The packaged components were then shipped to the system manufacturer for board-level assembly. Packaging was not typically perceived as value-add—rather, a necessary function adding cost. As such, packaging has always struggled to command the respect it merited within the supply chain.

A number of factors have aligned over the past decade to change the balance of respect. Consumer demand for mobile devices has led original equipment manufacturers (OEMs) to enable more functionality within their systems, which required smaller components and smaller feature sizes in both chip and printed circuit board (PCB) technologies. The front-end foundries have pursued node scaling to accomplish the task. The SATS' solution was the development of processes such as flip-chip, under-bump metallization, redistribution layers, and Cu pillar all performed at the wafer level. The lines between the front-end foundries and packaging houses began to blur. What was traditionally called "packaging," perhaps might have been more accurately defined as "interconnect," because the required processes were increasingly associated with foundry operations.

At this point in time, there was little interest for foundries to compete with SATS for WLP. They continued on their quest of shrinking wafer nodes through advanced (and costly) lithography processes such as double- and triple-patterning, while the talk of a transition to 450mm wafers continues.

Recently, however, the realization that the industry has hit the limits in traditional scaling has led foundries to examine wafer-level interconnect (WLI) technologies as a way to practically achieve cost-performance benefits.

Changing the manufacturing paradigm

WLI has been around for many years, with wafer bump processing being used for flip-chip technology. Significant growth is being driven by wafer-level chip-scale packaging (WLCSP), one of the key interconnect technologies integrated into handsets and tablets. There is also a growing trend toward fan-out wafer-level packaging (FOWLP), which leverages the advantages of WLCSP by enabling higher pin counts beyond the limits of die size, thereby extending the market application space. Currently, the FOWLP market is being served with limited scope by the SATS. The attractiveness of this technology to the end users has wafer foundries viewing this as a potential opportunity to leverage their wafer processing expertise and extend market share.

The high cost of capital for FOWLP is creating a further ROI challenge within the SATS and in many cases, a reluctance to invest. Essentially, the business model may not make sense at the price they can command for the components despite the value added with WLI.

The combination of end market pull and the supply chain's reluctance to invest creates opportunity for a unique approach provided a breakthrough can be achieved in the cost of capital. With a specific focus on WLI technologies and a

heritage inspired by silicon solar cell wafer manufacturing process, Deca Technologies has charted a new course. We have created an interconnect foundry that is capable of delivering breakthroughs in product cycle time, flexibility and cost (Figure 1).

Figure 1: Deca Technologies' wafer-level autoline plating system.

The interconnect foundry in action

An example of the interconnect foundry approach is evident in the case of new product introduction (NPI). Convention holds with using traditional glass masks for lithography processes for wafer processes. Cost, lack of flexibility, and cycle time are all challenges for today's need for rapid NPI. The new approach eliminates the need for traditional glass masks enabling wafers to be processed in the line within hours of design completion. Furthermore, our approach gives the semiconductor company a significant advantage in being first to market with an associated higher likelihood of a design win.

In establishing our interconnect foundry manufacturing paradigm, we selected an industry-proven package type, the WLCSP, to enter the market. With the technology in high-volume production, the company has now started to expand its portfolio by introducing a different approach to FOWLP.

A key part of this differentiated approach to FOWLP, termed M-Series™, is the inclusion of Cu pillars along with a fully molded structure providing a highly reliable package (Figure 2). The benefits of the fully molded structure include: separation of the discontinuity at the die edge from the buildup structure; better panel warpage control because of the balanced material around the die; and improved board-level reliability as a result of the molded layer separation between the chip and PCB connections.

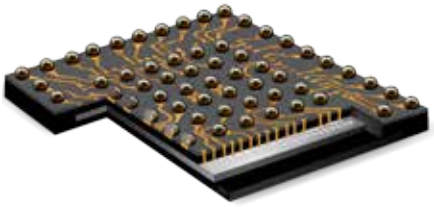

Figure 2: Deca's M-Series™ fan-out wafer-level package is a fully molded structure.

Another key FOWLP enabling technology we have developed is Adaptive Patterning™, born of the need to compensate for the inherent die shift within a molded structure. Every device on every panel has exactly the right design through the manufacturing process. This approach enables both cost reduction and yield improvement compared with current industry methods.

The combination of Adaptive Patterning, a fully molded structure, and the new manufacturing approach may finally provide the industry with a cost-effective, highly capable FOWLP process that can rapidly scale to serve growing OEM demand.

Summary

As the interconnect roadmap trend continues to call for increased metal layers and finer line and space resolution—which drive foundry-level services for WLI—it is clear that providers with a unique capital structure are well positioned to deliver on these requirements. By breaking with the conventional approach we expect focused interconnect foundries to set new levels of performance in terms of cycle time, flexibility and cost for WLCSP, FOWLP, and future WLI technologies.

Biography

Garry Pycroft received his Diploma in Engineering in Wirral, Merseyside, UK and is VP of Sales and Marketing at Deca Technologies; email garry.pycroft@decatechnologies.com

Ensuring suitability of Cu wire bonded ICs for automotive applications

By James McLeish, Randy Schueller [DfR Solutions]

The transition to replace gold with copper bond wires in semiconductor components, primarily driven by the ever increasing price of gold wire, has been under way for several years. Cu wire bonds (Cu-WBs) are technically more challenging than gold to produce, requiring improved designs, processes and equipment. After introduction in consumer products, their use is now migrating to automotive electronics where product integrity for quality, reliability and durability (QRD) and safety over 10-15 years in a demanding harsh environment is paramount, in addition to managing cost in the highly competitive global automotive market.

Reliability issues with some Cu wire bonded components detected during the rigorous product validation durability–reliability tests of automotive electronics, however, are starting to appear. The indications are that only optimized package design with well-controlled assembly processes are suitable for high reliability (hi-rel) harsh environment applications such as automotive, military and aerospace. A concern is that non-optimized Cu-WBs and package materials issues are being detected in module-level durability validation tests in parts that were qualified as automotive grade per AEC Q-100 or AEC-Q101. This article will explore the issues and discuss potential solutions as the Automotive Electronics Council (AEC) – the organization that defines requirements for automotive grade electronic components – works to update qualification procedures for evolving Cu-wire bond technology.

Cu-WB delamination issues

Mold compound delamination in a semiconductor component has been a potential failure issue that has needed to be managed since plastic encapsulated packages were invented. Delamination can occur rapidly during soldering if excessive amounts of moisture were absorbed by the mold compound resulting in popcorning fractures or interfacial fractures during soldering. Delamination can also occur slowly because of swelling from gradual absorption of moisture while in service or thermal expansion mismatch stresses. Delamination can cause fractured or lifted wire bonds that result in open circuits. It can result in cracks in the package that can allow contaminants to enter, leading to corrosion of copper wires or bond pads that also results in open circuits, or it can cause current leakage due to the presence of mobile ions.

IPC/JEDEC J-STD-020 revision D on Moisture/Reflow Sensitivity Classifications only applies to identifying moisture-sensitivities and related protective measures needed to avoid package popcorning or internal delamination damage during assembly soldering. However, there are no industry standards on delamination limit requirements after environmental stress testing of loose components, after board mounting, or after reliability testing with components mounted on circuit boards. J-STD-020 allows delamination if the component passes reliability testing, however, such testing may not correlate to a long life hi-rel application.

Because copper is less ductile than gold, copper is more sensitive than gold to package delamination induced wire fracture. Failures of some ICs during module-level durability tests have been related to soldering delamination issues that weaken the bond, resulting in the inability to endure module-level automotive durability requirements.

Thermal cycling-related Cu-WB issues

Recently, there have been cases of copper wire separation near the stitch bonds without package delamination. These issues occurred during automotive module-level thermal cycle validation testing and were not detected during component-level thermal cycle testing. The testing challenges are discussed below.

Module-level thermal cycling testing. These are accelerated life tests calibrated to focus on structural integrity of the assembled circuit board with its components and housing. This testing places emphasis on component-to-circuit board coefficient of thermal expansion (CTE) mismatch-driven attachment solder fatigue.

Component-level thermal cycle tests. These tests are focused on the CTE mismatch issues within a component such as between the die, lead frame, wire bond attachments and the package. These tests are performed using loose components and only assess the stresses generated within the component. CTE mismatch and elastic modulus of the mold compound against leads, and bond wires are important factors that create internal mechanical stress as temperature changes. Internal dimensions and geometries are important because serpentine internal package lead shapes can have different mechanical behavior than straight shapes.

Mold compound and lead frame materials, however, will also stretch, compress, and bend because of the additional externally applied thermal cycling forces on the leads resulting from the components being mounted to a circuit board and perhaps potted. If externally applied forces are added to the internal component generated forces, their addition can be sufficient to cause failure of non-optimized Cu wire or their bonds during module-level testing.

Some recent module-level thermal cycling issues have included wire heel breaks that have occurred at the point where the wire transitions out of the stitch bond, instead of a separation of the actual stitch bond (**Figure 1**). In these type of wire breaks,

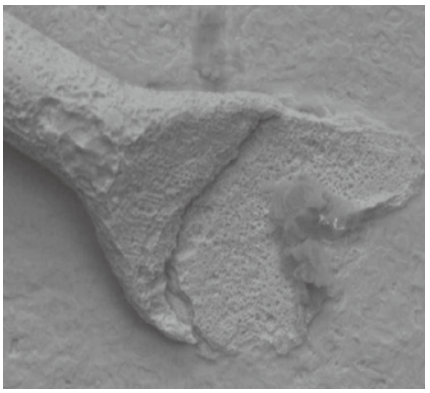

Figure 1: Example of a copper bond wire broken at the heel point where the wire exits from the stitch bond. The break occurred during module-level thermal cycle test, from-40°C to +120°C, and package delamination was not a factor.

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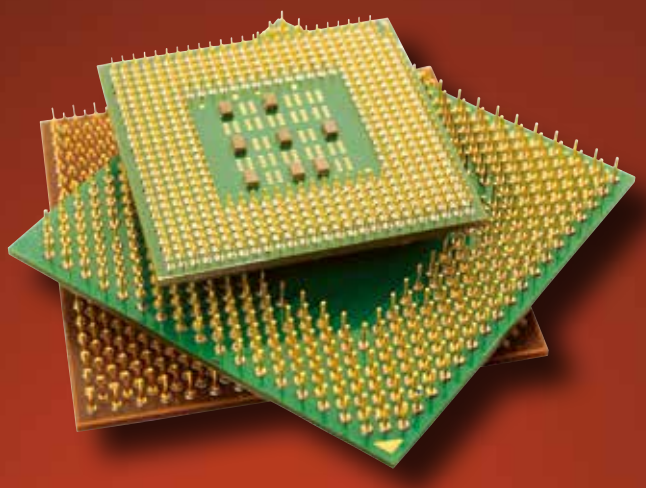

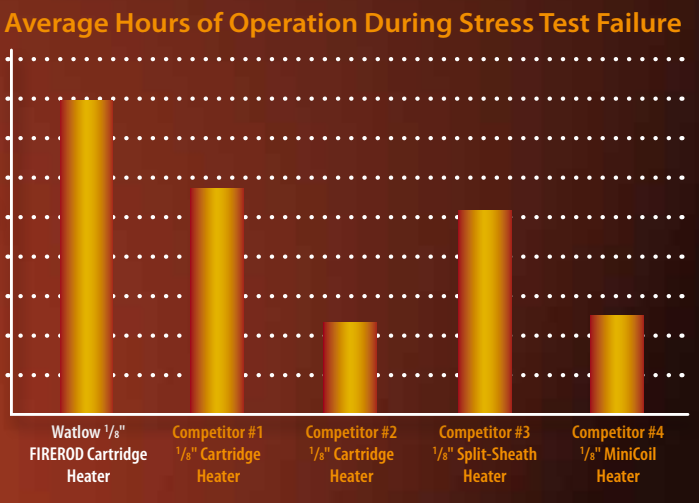

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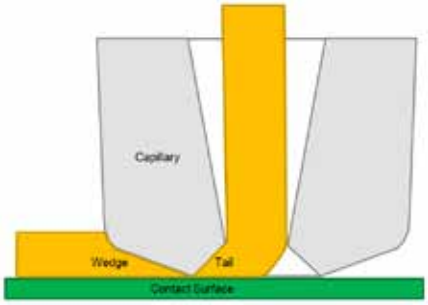
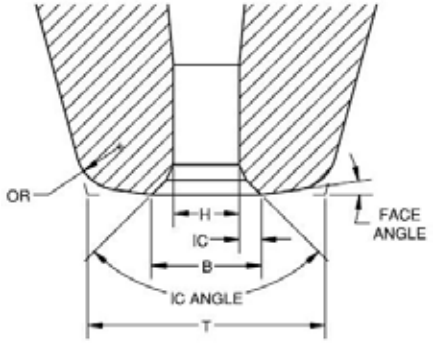


Figure 2: An optimized, non-worn wire bonding capillary head that is sized and shaped to provide an adequate heel weld and a gradual transition back to the wire diameter applied with proper calibration and wear monitoring/maintenance is required to prevent excessive flattening and pinch points.



T – Tip Diameter (Influences Bond Size)
H – Hole Diameter (Sized to Wire Diameter)
B – Chamfer Diameter (Affects Ball Bond Shape)
IC – Inner Chamfer (Affects Ball Bond Shape)
ICA – Inner Chamfer Angle (Affects Ball Bond Shape)
FA – Face Angle (Defines Transition Slope)
OR – Outer Radius (Defines Heel Thickness)

Figure 3: Bonder capillary head geometry determines the size and shape of the wire bonds, which affect bond durability and robustness.

the root causes are typically: 1) Excessive capillary force resulting in a thin pinch point where the break occurs; 2) A worn capillary head that produces an insufficient transition back to the wire diameter (Figure 2); 3) A non-optimized capillary head will produce an undersized weld width and/or an undersized heel bond (Figure 3).

The strongest stitch bonds are produced by using a capillary head with a large tip diameter, which produces a larger bond. A face angle, of 8 degrees, combined with a large outer radius produces a gradual transition slope with a large heel weld needed to avoid the type of pinch point that resulted in the wire break shown in Figure 1.

While module-level thermal cycling tests have also occasionally resulted in gold bond wire failures, the reduced ductility or copper wire and the challenges of copper bonding makes understanding the capabilities of copper wire and copper bonding under long-life harsh environmental conditions a priority in hi-rel industries. While most Cu-WB components can pass both automotive component- and module-level validation, the few that do not have resulted in efforts to identify the critical to quality (CTQ) reliability physics characteristics that ensure robustness and durability. Additional efforts are ongoing to develop ways of consistently validating good components and screen out weak components at the components level.

Automotive OEM expectations

Ensuring the performance suitability, QRD, and safety of an automotive electrical/electronics (E/E) module is a primary objective of automotive module-level validation procedures. Before validation test failures result in extra cost and time to identify the root cause and correct problems, automotive OEMs desire that products be designed right on the first attempt so that validation is achieved on the first attempt. This allows budgets and schedules to be maintained, which results in fast and efficient product development processes. OEMs do not want to find what they see as component-level issues, discovered during module-level validation tests, they want component-levels issues resolved down the supply chain. They also desire to get more potential board- and module-related design and assembly problems designed out, prior to validation testing. This tactic is known as the "design for reliability" (DfR) approach to product development. It is an improvement over the traditional "reliability growth/design-build-test-fix, trial and error" approach to product development. The DfR approach is becoming even more essential under the current safety critical atmosphere in the auto industry related to the recent increase of global vehicle safety recalls for E/E issues that have been accompanied by significant media coverage, record fines and congressional investigations and proposals for new legislation and regulations. Furthermore, the development of robotic self-driving vehicles is well under way. Cars with limited camera aided self-parking and emergency braking features are already here. Fully autonomous vehicles are expected between 2020 and 2025 [1].

The safety-critical issues of self-driving vehicles demand a quantum leap in the QRD performance of vehicular E/E systems and components. In Europe, the release of the new ISO-26262 Standard for Vehicle System – Functional Safety is driving increased emphasis on E/E QRD and safety for comprehensive product integrity throughout the entire E/E supply chain.

WB design and CTQ characteristics

The primary Cu-WB QRD issues are related to ball bond separation, pad or die damage, corrosion, and stitch bond separation, which are related to Cu being a harder material than gold that is more prone to oxidation. Primary critical to QRD characteristics for Cu-WB are:

Formation of the Cu ball bond. To prevent damage to the ball bond pad and IC die and to ensure a good bond – a very symmetrical, spherical ball, of precise dimensions, that is oxide free – has to be consistently formed at the tip of the bond wire during the electronic flame off (EFO) process. Copper oxide on the ball surfaces will make bonding difficult. Misshaped spheres can damage the pad or result in weak, partial bonds that may fail either after molding, or in the field under usage stresses. Because copper readily oxidizes, it has a short shelf life; Cu bond wire must therefore be used within one week of package opening. At the elevated temperatures of the EFO sphere creation process, oxidation occurs rapidly. To prevent this situation, Cu spheres were initially formed in a nitrogen (N_2) inert atmosphere. It was later found that a mixture of 95% nitrogen and 5% hydrogen (called forming gas) is more effective at preventing Cu oxidation (Figure 4).

Preventing pad and die damage and Cu ball bond failure. Because copper wire is harder than gold, more force is required during thermosonic bonding. Excessive force can displace bond pad aluminum and sometimes damage die material or features under the pads.

Aluminum splash occurs when bonding forces cause pad aluminum to flow out from under the ball bond or the ball can punch through the pad and damage the die. The bonding process must be controlled so that ≥0.2µm of the original aluminum pad thickness remains for the pad to maintain the strength needed to prevent pad fractures or tearing. This can be mitigated with pads that are thicker than the typical 1µm Al thickness used with gold wire bonds. It is also essential that the CuAl inter-metallic compounds that form the bond are created over at least 70% of the ball contact area.

Die cracks and cratering damage to the die or circuitry under the pads from excessive bonding or probing forces can disrupt circuit functions or undermine pad attachment strength, ultimately resulting in bond separation. Using very pure Cu, which is softer, is one way to reduce these risks. Robustness against die damage can also be

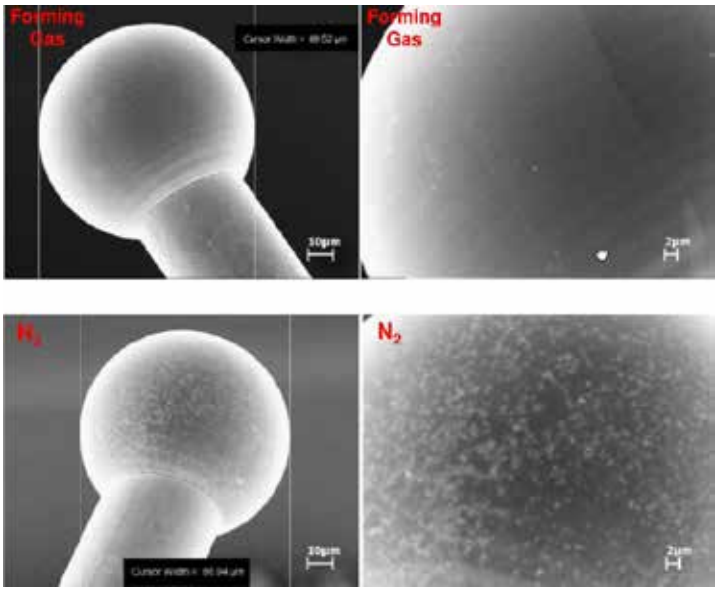


Figure 4: The use of forming gas during Cu wire bonding (upper images) reduces Cu oxide formation more than an inert N_2 atmosphere (lower images) [2].

improved by up front design considerations for components that will be using Cu bond wires. Circuit features and vias should not be routed in die layers under Cu bond pads. If this is not possible, very careful calibration and control of the Cu bonding process is required to reduce die damage risks. The use of silicon-doped aluminum bond pad metallization should be avoided because it results in silicon nodules that act like grit under the bond pad. Barrier layers are a preferred method to prevent contact spiking and produce a more robust pad structure. Finally, the use of low-k dielectric materials should be avoided because they are more fragile and more prone to cracking than high-k dielectrics.

Chlorine corrosion of the Cu-WBs can occur from high chlorine (Cl^-) content and high pH in the package encapsulant molding material. Humidity, temperature and electrical bias drive this failure mechanism. When a forward bias is applied, Cl^- ions are attracted to the positively-charged pad causing corrosion that can eventually result in bond separation. This mechanism is accelerated by the high humidity and temperature conditions automotive electronics are required to endure. Using a molding compound with a low pH (between 4-6) and a low chlorine content <20ppm, (preferably <10ppm) is essential for alleviating failure risks. It is also important to minimize voids or irregularities in CuAl IMC bonds that would allow moisture ingress that could hasten corrosion degradation and separation stresses within the bond.

Preventing 2nd stitch bond failure. The stitch bond is created by impressing the wire against the bond surface of the terminal lead frame. Oxidation of the wire is again a concern because the wire was not freshly formed in an EFO process as the ball head was. The main concern is that the harder Cu wire may not deform enough to expose fresh metal for the bond. Enhanced ultra-sonic action known as stitch bond enhancement (SBE) features have been proven to produce stronger stitch bonds [4]. A thin palladium coating over the copper wire also produces a stronger stitch bond. However, this further increased wire hardness might increase risk for pad/die damage during ball bonding, so this trade off needs to be carefully managed.

During the introduction of Cu-WBs, retrofitted conversion kits were developed to adapt existing gold bonding equipment for producing Cu bonds. As experience grew, enhancements to IC die design and material issues were identified and new bonding equipment systems were developed to account for the differences and needs of copper wire bonding. When these design features and properly calibrated equipment are used, the optimized Cu-WBs discussed in the previous sections can be produced.

Qualification of automotive semiconductors with Cu-WBs. The challenge now is to further optimize qualification procedures for automotive grade semiconductors to enable distinction between marginal Cu-WBs and the optimized Cu-WBs needed to survive in automotive applications. The AEC is developing a new automotive industry specification to be used when qualifying components that have copper wire. A document has been drafted that will add additional requirements over and above what is specified in the AEC-Q100 and AEC-Q101 documents when copper wire is used. The document is under discussion, but will likely include mold compound delamination requirements before and after environmental stress testing, and physical analysis requirements after environmental stress testing. Under consideration is a requirement for a circuit board-mounted thermal cycle test.

One OEM has suggested that semiconductor suppliers perform thermal cycle testing to 3X the AEC requirement in order to catch the failures that 1X testing at the component level has not detected. However, extending AEC testing to more cycles on loose components may not correlate with module-level thermal cycle performance because the stresses experienced by the component are significantly different when mounted to a substrate. Performing a board-level stress test followed by physical analysis to validate package robustness may be a more effective approach to catch package weaknesses early in the package development phase.

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Reliable testing of Cu pillar technology for smart devices

By Amer Cassier, Lily Zhao, Ahmer Syed, Steve Bezuk, William Miller [Qualcomm] and *Amy Leong, Mike Slessor [FormFactor Inc.]*

The relentless drive for greater functionality and performance in smart phones, tablets and other consumer devices requires a higher level of chip integration, which in turn, requires increasing the bump density in monolithic ICs. As a result, scaling of flip-chip (FC) bump pitch is imperative in order to successfully connect all the I/Os on die, and to meet area and performance constraints.

While solder bump technology is a reliable interconnect for flip-chips, it is not easily scalable to pitches under 130µm. On the other hand, Cu pillars, which are typically fabricated using photolithography and plating techniques, enable the fabrication of smaller diameter bumps scalable down to 20µm pitch. In addition to pitch scalability, Cu pillars also offer significant performance advantages over solder bumps, including higher electrical and thermal conductivity, as well as improved electromigration reliability. As a result of these benefits, Cu pillar flip-chip packaging is rapidly becoming the interconnect technology of choice for advanced ICs, especially for highly integrated applications such as smart phones and tablets.

There are currently two types of Cu pillars in use. The first is a bare Cu column (**Figure 1**). The second incorporates lead-free (SnAg) solder caps on the top of the column (**Figure 2**). The lead-free cap version is gaining in popularity because this type is more compatible with existing flip-chip solder bonding processes. This article will look at the four main probing challenges involved in testing fine-pitch Cu pillars with solder caps (CuP).

Probe mark damage

As pitch is reduced, the diameter of the Cu pillar shrinks accordingly. At a typical solder bump pitch of 150 to 200µm, the solder bump diameter is in the range of 75µm to 100µm. For a Cu pillar at a pitch below 100µm, the Cu pillar diameter is generally less than 50µm. This significant reduction in diameter of pillars, and the corresponding lead-free solder caps of **Figure 2**, make them much more susceptible to damage during wafer probing.

For Cu pillars with solder caps, acceptable probe mark criteria are generally a ratio of probe mark diameter (d) to Cu pillar diameter (D) as shown in **Figure 3**. Typically, the maximum acceptable d/D ratio is approximately 50% (equivalent to an affected-area ratio of 25%), although this depends on specific details of packaged-part reliability requirement. Probe mark is a strong function of probe force and number of touch downs, as a consequence, probe force must be reduced at smaller pitches to meet the d/D specification. However, maintaining reliable and stable electrical contact with small probe forces presents a significant challenge.

In a production environment, multiple touch downs on the same die are not uncommon, for example, to test at different temperatures, retest failures, or to optimize prober stepping pattern and test time in the case of multi-DUT (device under test) cards. Therefore, the effects of additional touchdowns (TDs) must be characterized and factored into the probe mark specification such that production

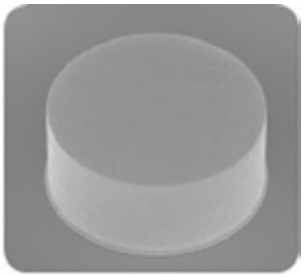

Figure 1: Cu pillars with no solder caps.

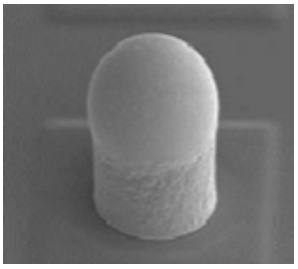

Figure 2: Cu pillars with lead-free solder cap.

Figure 3: d/D ratio of probe mark to pillar diameter.

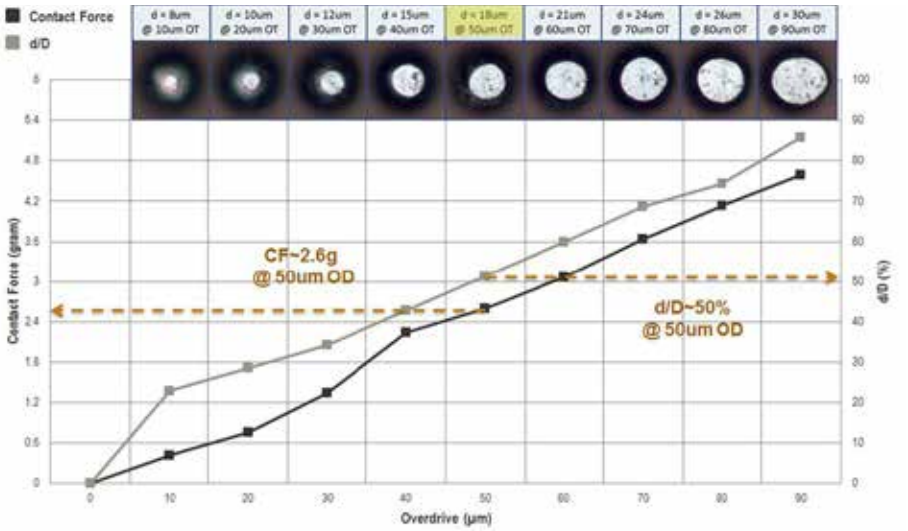

Figure 4: Relationship between probe mark size and probe force.

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As discussed above, a low probe force is critical to controlling the probe mark size. Figure 4 shows a study of the relationship between probe mark size and probe force. The Cu pillar diameter (D) used in this study is 40µm. At a typical production overdrive of 50µm, with a probe force of 2.6 gram, a probe mark d/D ratio of 50% was demonstrated.

As shown in Figure 4, for Cu pillars, around 40µm diameter, probe force needs to be in the range of 2-3 grams in production. Figure 5a shows an example of a bump with large and out-of-spec probe mark because of high probe force and multiple touch downs. Figure 5b shows the same bump after reflow.

Figure 5: Failed probe mark resulting from high probe force a) post robing b) reflow the same probed bump.

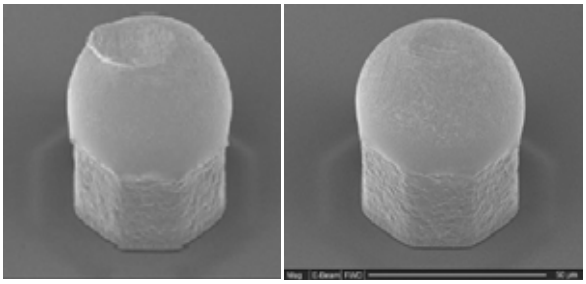

Figure 6: Probe mark comparison between a) a mechanically stamped vertical 2.0mil probes, and b) a low-impact vertical MEMS probe MF100.

Probe force tolerance control is also critical. As shown in Figure 4, when the probe force increases from 2.6g to 3.6g—just 1g difference in probe force—the d/D ratio changed by about 20% from a single touchdown. At 6 TDs per bump, that change constitutes a significant portion of the 50% probe mark specification window. Mechanically stamped vertical probes, made from a pre-curved wire rod, simply cannot deliver the individual probe force control needed to meet required probe force tolerances.

Low-probe force control is certainly not limited to force in vertical probe direction. Low lateral force is also desired to minimize bump damage due to shear forces in the x/y direction. Figure 6 illustrates that 2 mil probe, with a similar z-force but higher lateral force, induces much more solder cap disturbance compared to a low-impact vertical MEMS probe (FormFactor's MF100) [1].

Contact-resistant stability when using low-force probes

Maintaining stable and low contract resistance (C_{res}) is essential in wafer probing to ensure acceptable wafer probing yields. Contact resistance quality relies on the contactor's ability to penetrate any contaminants or non-conductive oxides on the bump materials and form metal-to-metal contact areas that establish efficient conduction paths between the probe tip and the bump. Traditionally, a high-force probe (≥10g probe force) was used to ensure this good metal-to-metal contact in probing lead-free solder bumps. This approach is clearly out of the question, however, when it comes to meeting d/D specifications in the case of sub-100µm pitch CuP.

When using the 2-3g of force required for volume production, probe tip materials and geometry must be carefully optimized to guarantee the stable contact resistance needed for accurate results. Figure 7 illustrates the differences in contact resistance behavior that varying combinations of probe tip designs and materials can have on lead-free solder and Cu columns.

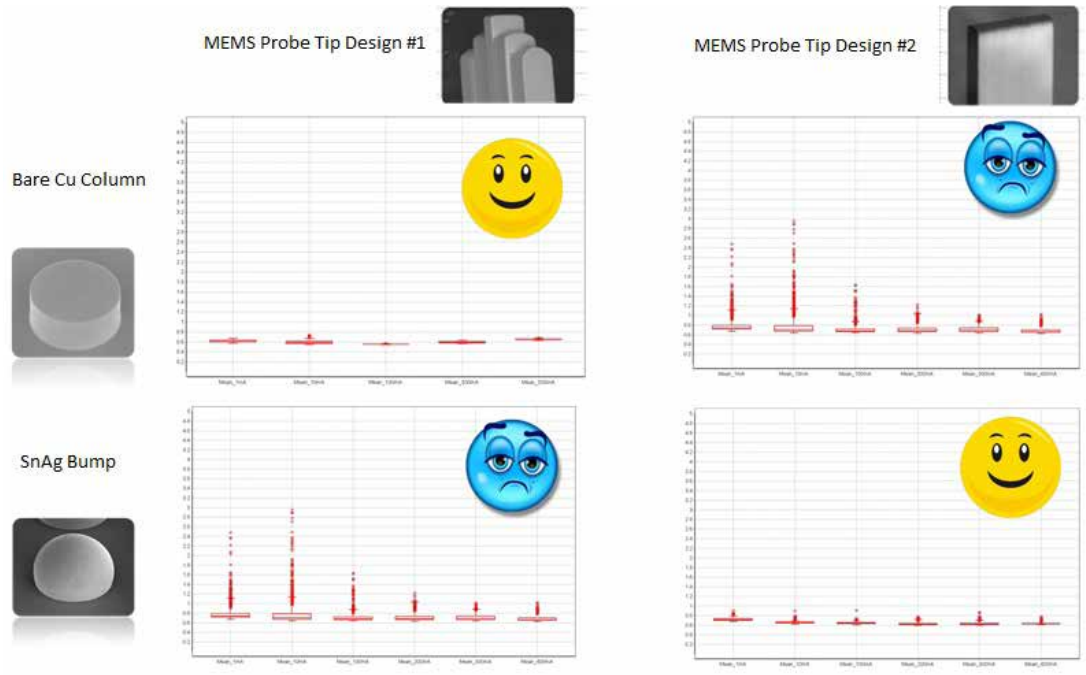

Figure 7: Contact resistance results from varying combinations of probe tip materials and design.

Bare Cu columns tend to form oxidation layers. Probe tip design #1 with a narrow skate can help to increase the probing pressure on the bump material, and has proven to be very effective in penetrating the oxidation layers on bare Cu columns. When used to probe solder material, however, the probe tip material on design #1 couldn't form a good metal-to-metal contact with SnAg

solder bumps, and very poor contact resistance performance was observed.

Probe tip design #2, with the right metallurgy, on the other hand, can achieve excellent contact performance on SnAg bumps even at sub-3g probe force. This type of flat-tip design and tip material is commonly used to probe Cu pillars with a SnAg cap.

It is easier to sustain stable contact resistance on bigger bumps than smaller bumps, given the same probe tip design and bump material, because of the physical metal-to-metal contact area differences (or scrub mark size) to achieve d/D of 50%.

Overall cost-of-test or probe card usable lifetime

Overall cost-of-test (CoT) is strongly influenced by the selection of probe tip design and material. During production, the probe tip will experience wear from routine probe tip cleaning cycles. The usable vertical probe card life-time is fundamentally influenced by the length of the effective usable tip and how quickly it will be worn away.

As the bump pitch is reduced, probe tips must become more slender in order to fit the required number of vertical probes into the dense grid-array bump patterns. During normal cleaning processes, probe tips with smaller cross sections degrade more quickly than do larger ones with more material. Using traditional cleaning sheet or recipe probes with small cross sections will lead to a much shortened probe card usable lifetime.

Figure 8 shows a benchmark study of 100µm grid-array pitch-capable vertical probes, comparing a traditional Cobra-style 2mil vertical probe with Pallany 7 probe material, with two other MEMS probes. As **Figure 8** shows, by optimizing tip geometry, tip metallurgy and tip surface finish, the MEMS-Type 2 probe offers three times the usable lifetime of the Cobra-style probe [2].

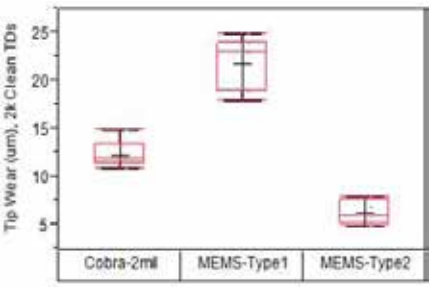

Figure 8: Comparison of probe tip lifetimes.

Figure 8 clearly demonstrates that careful design of probe tip geometry for the targeted Cu pillar bump and associated tip material are essential to minimize probe tip wear and extend probe card lifetimes. Close collaboration between end users and probe card suppliers to optimize in-line cleaning recipes for these novel MEMS probe tip materials will also help to maximize probe card lifetime in production environments.

Probe tip to Cu pillar alignment

The allowable probe-tip to Cu pillar alignment tolerance is a function of the probe tip size relative to the Cu pillar diameter. Typically, as the pillar diameter decreases with pillar pitch, the allowable alignment budget will shrink as well. As a result of this trend, probing sub-100µm pitch Cu pillars requires significant improvement on probe tip aiming accuracy compared to that required to probe 150µm pitch solder bumps.

To use a probe card of 10,000-20,000 probes daily in a high-volume production environment, the probe tip needs to be well aligned to every one of them. The aiming accuracy this requires is the equivalent to expecting an archer to shoot 20,000 arrows simultaneously with every one of them hitting the bull's-eye every time (Figure 9).

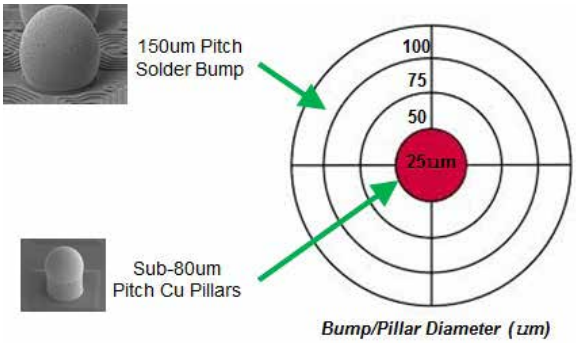

Figure 9: Typical bump diameter of a 150µm pitch solder bump is approximately 75µm. In contrast, a typical Cu pillar diameter with sub-100µm pitch can be as small as 25-30µm. To align a fine-pitch probe card tip to a 25µm Cu pilliar, it's equivalent to hitting a bull's-eye on a target practice.

When a probe tip is perfectly aligned with a pillar, a nicely rounded probe mark results. When tip and pillar are misaligned, the probe tip damages or removes the solder cap materials and induce downstream packaging reliability or yield loss. Figure 10 shows the comparison of passing and failed probe marks.

The alignment challenge does not end with probe card fabrication. This level of accuracy must be maintained throughout the probe card's lifetime. Figure 11 shows the result of a probe positional accuracy study over touchdowns of a 2mil probe card [1]. The card showed excellent results at the beginning, but after 40 to 50k touchdowns, the alignment starts to drift outside the allowance window. The probes that are outside the acceptable level of accuracy will be more likely to have unacceptable probe mark illustrated in Figure 10.

From a probe card fabrication standpoint, to get optimal alignment by design, the dimensional control of probe and guide plate fabrication processes must be good at the start. Figure 12 shows the raw dimensional errors that can occur in the production of a mechanically formed probe head vs. a MEMS-fabbed one [2]. The mechanically produced probes and guide plates have more than three times the errors of the MEMS-fabbed guide plates and probes.

If probe card suppliers are to support the increasingly stringent testing demands of advanced IC production, they must design and fab their guide plates and probes to maintain their initial x/y

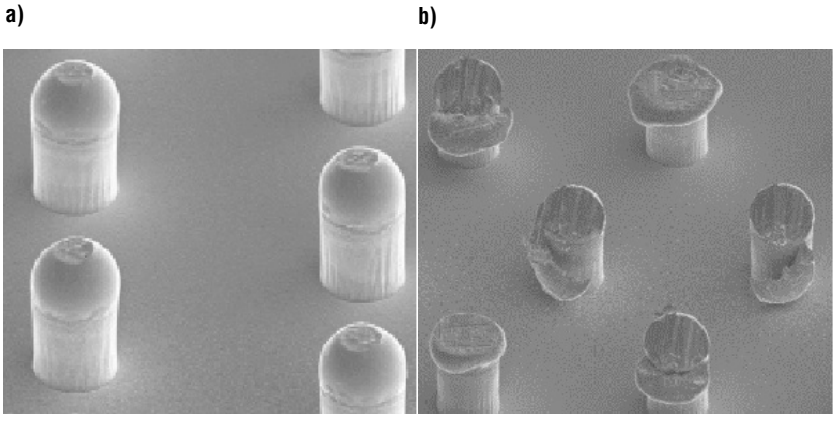

Figure 10: Examples of circular passing probe marks and severe bump damage observed on 25µm Cu pillars because of poor x/y alignment error in the range of 12 to 15µm.

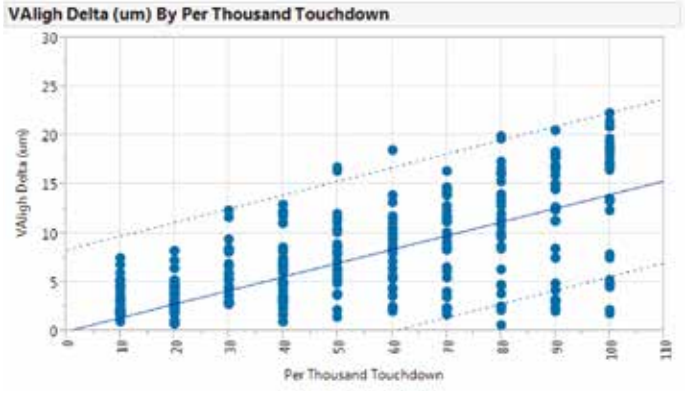

Figure 11: Probe positional accuracy over lifetime using Cobra 2 mil probe.

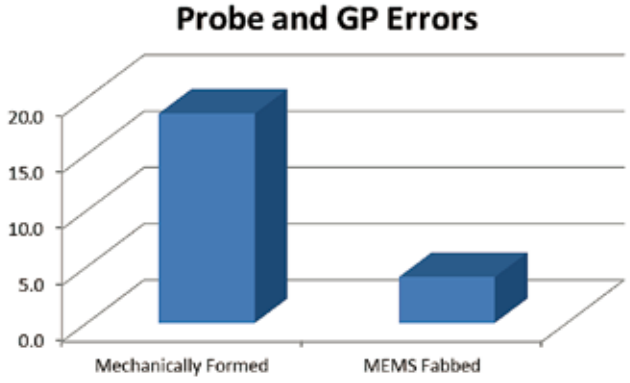

Figure 12: A comparison of errors occurring in mechanically formed and MEMS-fabbed probes and guide plates.

positioning throughout the probe card's lifetime. To do so, they must not only ensure good "as fabbed" dimensional control when their product is shipped to the end user, but must also make the right probe/guide plate material choices during probe fabrication that will minimize probe wear and misalignment during regular use.

Summary

Smart mobile devices have upended the once static packaging pitch landscape. The Cu pillar technology required to support the expanded functionalities and I/O density used in these appliances are driving grid-array pitch to sub-100µm, and migrating to sub-50µm in 2.5D and 3D packaging.

Mechanically formed Cobra-style probes that have been used for flip-chip bump probing in the last decade cannot support sub-100µm pitch requirements reliably in production. They have been replaced with vertical MEMS probe cards that are more cost-effective and robust in terms of mechanical precision, electrical contact stability, and overall cost. Close cooperation among end users and test cell suppliers is essential for the industry to "hit the bull's-eye" and maximize the full benefits of Cu pillar technology.

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eWLCSP: a new path for WLCSP packaging

By Rajendra D. Pendse, Seung Wook Yoon, Kang Chen, Linda Chua, Yaojian Lin [STATS ChipPAC]

The wafer-level chip-scale package (WLCSP) was introduced in the late 1990s as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin-film metals and solder bumps applied directly on the surface of the die with no additional packaging [1]. The basic structure of WLCSP comprises an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides. The WLCSP provides the smallest possible package size because the final package is no larger than the die itself. The volume of WLCSP packages used in the industry has experienced steady growth since its introduction driven by the small form factor and high performance requirements of mobile consumer products.

Despite the indisputable benefits of WLCSP, there are a number of concerns that have continued to plague the adopters of this technology since its inception. These issues are as follows:

WLCSP is essentially a bare die with exposed Si surfaces. The package suffers mechanical damage in the form of chipping and cracking in the course of processing, shipping and during surface mount technology (SMT) operations. This necessitates additional processing (e.g., back side coating or lamination) for partial die protection and inspection steps to ensure outgoing product quality, leaving the product still exposed to potential field failures because of the risk of marginally damaged parts being shipped that may not be "caught" by inspection.

The manufacturing infrastructure for WLCSP is entirely dependent on the incoming wafer diameter. As designs migrate to larger wafer diameters (as in the 200mm to 300mm transition or the future transition from 300mm to 450mm), new investments become necessary to support the capacity requirements, while investments in the existing infrastructure may be rendered obsolete.

From a design perspective, WLCSP is effectively a "fan-in only" package. The input/output (I/O) must be accommodated on the area of the die at the desired terminal pitch; hence, there is a threshold of I/O density above which the WLCSP package becomes unusable and a change to a completely different packaging solution becomes necessary. Such situations often arise with node transitions that result in die shrinks. For example, a change from WLCSP to fine-pitch ball grid array (FBGA), flip-chip ball grid array (fcFBGA) or quad flat no leads (QFN) is not uncommon and entails a radical change in package footprint, form factor, performance, and cost structure.

Enter the encapsulated Wafer Level Chip Scale Package, or eWLCSP™, which is a simple variation of the broader fan-out wafer-level packaging (FOWLP) platform (trade named eWLB for embedded wafer-level ball grid array). eWLCSP retains the benefits of WLCSP packaging while addressing many of the key concerns mentioned above. The unique structure of the package, the fabrication process, the advantages and preliminary product/reliability assessment are discussed here.

eWLCSP with sidewall protection

A new process has been developed to provide five-sided protection for the exposed silicon in a WLCSP. The formation of a protective polymer coating on the back and four sides of the die surfaces is accomplished using the existing high-volume manufacturing flow developed for eWLB (**Figure 1**). The first step in eWLB manufacturing is to thin and singulate the incoming silicon wafer. Following singulation, the diced silicon wafers are reconstituted into a standardized carrier for subsequent processing.

The reconstitution process, as depicted on the left in **Figure 1**, comprises four main steps: 1) lamination of an adhesive foil onto a carrier; 2) accurate face down placement of the die onto the carrier; 3) encapsulation of the die by a compression molding process with the active face of the die protected; and 4) removal of the carrier and foil, resulting in a reconstituted wafer with only the active face of each die exposed. The eWLB process is unique in that the reconstituted wafer does not require a carrier for subsequent processing.

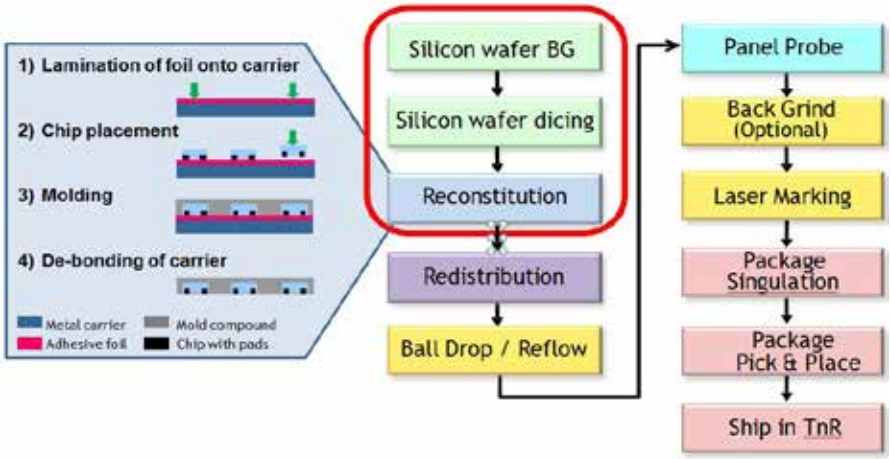


Figure 1: eWLB process flow

The implementation of this process in the 300mm reconstituted wafer format has been described in detail in previous work [2, 3].

The eWLB manufacturing process seamlessly accommodates multiple silicon wafer diameters in the same manufacturing line and produces both fan-out and fan-in devices as illustrated in **Figure 2**. In view of this universality and flexibility of the manufacturing line, the term FlexLine™ was coined to describe it. The basic process is essentially identical and fully fungible with the fabrication process for standard WLCSP. It entails the usual steps of applying and patterning dielectric layers, thin film metals (redistribution) and under bump metal (UBM).

It is easy to see that the formation of a polymer coating on the exposed Si surfaces is a natural part of the basic process and requires no additional processing. To implement the sidewall feature, a thin layer of molding compound, typically 30µm, is left on the side of the die after singulation. The back of the die remains protected with molding compound. The result is the new eWLCSP™ [4].

The typical structure of eWLCSP is shown in **Figure 3** with micrographs of

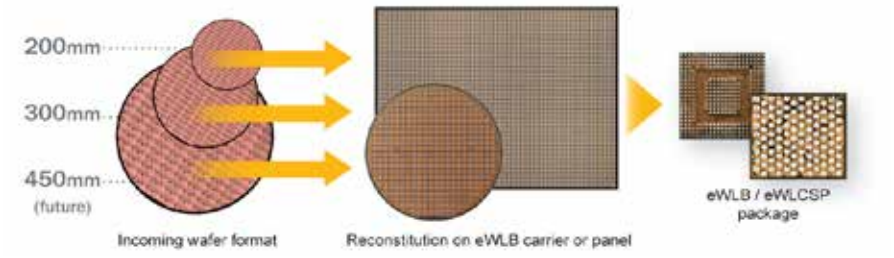


Figure 2: FlexLine™ processes multiple silicon wafer diameters on the same manufacturing line to produce both fan-in and fan-out packages.

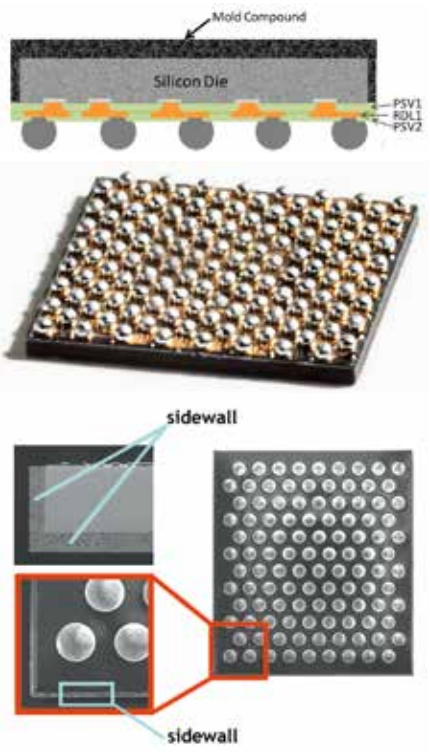


Figure 3: eWLCSP™ structure.

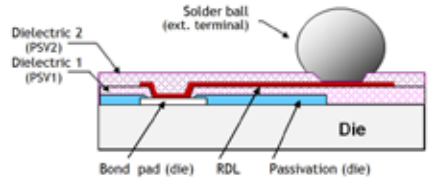
Figure 4: Micrographs of X-section view of eWLCSP™: standard overmolded and thin versions.

the cross section view in **Figure 4**. While the typical structure is shown in **Figure 3**, many variants of the base structure have been demonstrated – e.g., the backside molding compound can be removed with an optional back grind operation and the body made thinner while retaining the protective sidewall layer (**Figure 4**).

While there is considerable flexibility in the choice of metal and dielectric thicknesses in eWLCSP, a "1L RDL structure" (**Figure 5**) is most typical. Note that in the typical case, no UBM layer is necessary; the terminal solder balls are attached directly to the RDL metal layer through a suitably designed dielectric (PSV2) opening. This unique feature, which essentially amounts to the elimination of one lithography step, is made possible with the use of carefully engineered dielectric materials and has been proven through extensive board-level reliability (BLR) testing on eWLB packages with very high volumes of product shipped for various mobile applications.

Advantages of eWLCSP

The structure and manufacturing process for eWLCSP bring a number of advantages that address the primary areas of concern associated with the traditional WLCSP solution as referred to earlier.



PSV 1 (um)	7.0 - 11.0
RDL (um)	7.0 - 10.0
PSV 2 (um)	7.0 - 11.0
Ball pitch (mm)	0.4
S'ball size (um)	250

Figure 5: Dielectric and metal layer stack-up for a typical 1L RDL structure.

Cost. As described above, eWLCSP is fabricated using reconstitution. Good die from the parent wafer are picked and transferred to a (larger) reconstituted carrier. Since the majority of WLCSP products use 200mm wafers, reconstitution enables the scaling of the manufacturing process from the 200mm wafer to the size of the carrier in eWLB technology. This carrier size ranges from 200/300mm, to a larger format like high-density (HD) with ~20% greater area or ultra high-density (UHD) with >300% greater area. The HD format is currently in mass production. The scaling of the manufacturing process with reconstitution far outweighs the cost of reconstitution itself, thereby enabling large net cost reductions. Additionally, the ability to selectively pick good die from the parent wafer presents an additional net cost benefit as most wafers have a less than 100% wafer sort yield. Last but not least, the ability to pool the volume of traditional fan-out eWLB packages seamlessly together with eWLCSP packages on the same FlexLine™ provides important economies of scale. With the three factors stated above, net cost reductions up to 40% over traditional WLCSP front end processing are achievable depending on the original wafer diameter, the carrier format used for reconstitution (300, HD or UHD), and the yield of incoming wafers.

Quality. The polymer sidewall structure of eWLCSP all but eliminates mechanical damage such as chipping and cracking that is commonly encountered in traditional WLCSP processing. This serves to eliminate many expensive steps such as back side coating or lamination and complex inspection steps that are currently necessary for standard WLCSP to manage mechanical damage and ensure product quality. More fundamentally, the eWLCSP allows end users to build in quality by design vs. using inspection to weed out defects. This has implications for reducing the risk of field failure caused by the shipment of marginally defective parts that may escape inspection. As is shown in a later section, the encapsulated eWLCSP structure has also helped to increase the overall die strength by ~100% in addition to the mitigation of cracking and chipping defects, making for an overall more robust package.

Investment and infrastructure: wafer agnostic processing. In traditional WLCSP processing, the investment and infrastructure for manufacturing are based on the diameter of the incoming wafer. This creates a financial burden to re-tool the manufacturing lines to provide the needed capacity (to meet market demand) as wafer transitions occur (e.g., from 200mm to 300mm, or from 300mm to 450mm in the future) while also having to obsolete the existing manufacturing assets. The FlexLine approach for eWLB and eWLCSP effectively decouples the packaging process from the incoming wafer altogether obviating the above-described financial burden resulting from wafer diameter transitions.

Design friendly: allows seamless transition from fan-in to fan-out within the same basic package platform. As noted previously, the standard fan-in WLCSP only works below a certain threshold of I/O density, based on the minimum allowable terminal I/O pitch. The threshold is ~ 4 I/O /mm^2 for a 0.5mm terminal I/O pitch and ~ 6 I/O /mm^2 for a 0.4mm terminal I/O pitch. Small changes in I/O density that commonly occur with changes in Si design, or die shrinks resulting from Si node transitions, may lead to a given design exceeding the WLCSP threshold, causing the design to "fall off" the WLCSP application space envelope, necessitating a change in the packaging plan of record (POR) to traditional substrate- or lead frame-based packages like FBGA, fcBGA, QFN, etc. These packages are fundamentally different than WLCSP in terms of footprint, form factor, performance and cost, resulting in a major "reset" in the packaging POR. In contrast, the eWLCSP may be viewed as part of the more universal eWLB platform wherein the aforementioned I/O density transitions can be seamlessly accommodated within the same packaging platform. For designs whose I/O density falls marginally outside the threshold, an additional row of terminal solder balls can be added without fundamentally altering the package structure, form factor or performance.

Increased quality and reliability of eWLCSP™

The protective polymer sidewall feature not only helps prevent Si chipping and cracking, but also provides protection against mechanical breakage during socket insertion for electrical testing. While multi-site probe testing at the reconstituted wafer level is common for

many applications, eWLCSP enables the prospect of conventional socket testing, often a more simple and cost-effective alternative especially for larger die sizes. The viability of socket testing without mechanical damage to the part has been demonstrated through multiple insertion tests. To quantify this effect, it was shown through 3-point bend testing that the break strength of a typical eWLCSP package (4.7 x 4.7mm body size with a 30µm side wall and exposed Si structure) had comparable back side Si surface roughness, but approximately 2x the break strength (Figure 6).

The eWLCSP™ process has passed standard reliability tests used in wafer-level packaging, which includes component-level reliability (CLR), temperature cycle on board (TCoB), and drop test [5]. CLR was completed on a 4.7 x 4.7mm package with 1L RDL structure as illustrated in Figure 5, and the test conditions as shown in Table 1. The response variables were electrical continuity, delamination, solder ball shear strength, and visual/mechanical damage with measurements performed pre- and post-stressing.

BLR testing comprising TCoB and drop testing was also performed. TCoB passed 500 cycles to first failure and drop test passed the JEDEC requirement of 30 drops (Table 2).

Preliminary predictive modeling has shown that the BLR reliability of eWLCSP should far exceed that of WLCSP in view of the mechanically balanced structure of the polymer encased configuration. Systematic comparative studies of BLR of eWLCSP and WLCSP packages using a combination of finite element analysis (FEA) and empirical TCoB and drop testing are currently under way.

Summary

There is a growing demand for WLCSP packages in a wide range of advanced mobile products. Despite the successful adoption of WLCSP technology in the industry, there continues to be a number of areas of concern, notably: 1) the risk of cracking, chipping and other forms of handling damage before or during the SMT assembly operations and the associated quality implications; 2) an investment structure that is exposed to changes in wafer transitions, e.g., from 200mm to 300mm and to 450mm in the future; and 3) a "fan-in only" package architecture that dictates migration to other packaging solutions with small changes in the I/O density of the device.

A new encapsulated WLCSP (eWLCSP) package has been developed that features a unique polymer sidewall structure. It can be used as a drop in replacement for standard WLCSP packages, yet addresses the major concerns of WLCSP stated above. In addition, eWLCSP provides a lower cost structure and a scalable path to wafer-agnostic wafer-level packaging.

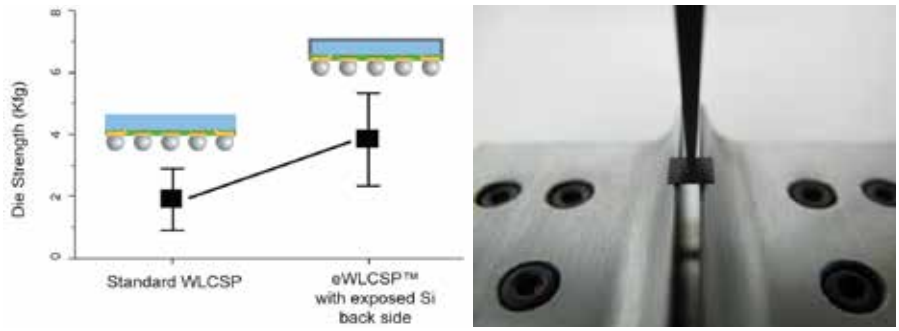


Figure 6: Dielectric and metal layer stack-up for a typical 1L RDL structure.

Component Level Test	Condition		Status
MSL1	MSL1, 260C Reflow (3x)	-	Pass
Temperature Cycling (TC) after Precon	-55°C to 125°C	1000 x	Pass
HAST (w/o bias) after Precon	130°C / 85% RH	192 hrs	Pass
High Temperature Storage (HTS)	150°C	1000 hrs	Pass

Table 1: Component-level reliability results.

Tests	Conditions	Failure Rate	Characteristic life (η)	Weibull slope β)	First Failure
TCoB (Cond B)	-40°C to 125°C	0.635	1219.4	10.13	864x
Drop Test	JEDEC	0.635	1553.5	5.97	772x

Table 2: Board-level reliability (BLR) test results.

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Silicon interposers with integrated passive devices—an ultra-miniaturized solution for 3D integration

By Stéphane Bellenger, Laëtitia Omnès, Jean-René Tenailleau [IPDiA]

A common theme with articles that address progress in the electronic components world is the search for form factor reduction and high performance. Since the 90s, designers have been working on 3D integration (multi-chip package, stacked die, system-in-package), which brings highly efficient solutions to achieve these goals. Several products have been developed to enable solutions, one in particular, is the interposer. The interposer can be assimilated to a packaging platform serving as a high-density substrate with a redistribution layer and offering, unlike traditional packages, the reduced pitch capabilities required by advanced IC technology nodes [1]. In other words, the interposer plays the role of a space transformer from the IC to the applicable module. It also allows usually incompatible technologies to be mixed on the same platform, therefore leading to heterogeneous integration (system-in-package on interposer) [2]. Combined with through-silicon vias (TSVs), it opens the doors to an optimized form factor world (system volume, weight and footprint) with improved performance (higher transmission speed, lower power consumption and RF parasitic reduction).

From an application point of view, interposers were first imagined to be used as a pure packaging platform dedicated to dies with large numbers of I/O (high-density ball grid array [BGA]). They have evolved towards 3D structures to meet the demands of CCD imager, mobile phone, and consumer applications. Now, an additional range of applications can be reached with the so-called 2.5D interposers. This new approach offers an economic model perfectly adapted to related portable products, implantable medical devices, avionics, and defense.

Several types of materials can be considered for interposer substrates, each offering intrinsic properties that need to be seriously weighed prior to any other considerations. Silicon is one, and is chosen for the following reasons: first, silicon is a stable base substrate that presents a very small coefficient of thermal expansion (CTE) mismatch with attached external ICs. Because the active parts are in fact often made of silicon themselves, the thermo-mechanical stresses encountered during processing and lifetime applications are minimized, thereby increasing the reliability. Silicon therefore offers a very good trade-off between thermal conductivity and thickness. It is also perfectly adapted to via or micro-via technology (including via-last technology) and provides wider possibilities in terms of pitch, via diameter and via density. Lastly, it enables passive devices to be integrated (IPD technology) and is compatible with ICs and MEMS.

Now that some general points about interposers have been described, we will explore what has been developed so far to optimize the performance and density of these structures. For a better understanding of the results presented, the TSV process flow set up by our R&D experts will first be detailed. Comparison tables will then be given, followed by characterizations. The reliability model tested will also be described. Finally, some application examples involving 2D interposers and 2.5D interposers will be detailed. The IPD process will not be developed here, however numerous articles are available on the subject [3, 4].

TSV key process steps

The introduction of through-silicon vias has had a tremendous positive impact on new 3D packaging architectures. TSVs enable higher density and shorter connection lengths compared with wire bonded solutions, and are perfectly suited to face the increasing demand for faster signals and lower power use. We are providing TSVs for interposers with or without IPDs. In past years, we have worked with our main technological partner, CEA-Leti, on TSV process optimization to bring it to the right level of maturity and cost for markets where high added-value products are needed (medical devices, aerospace, professional electronics, and telecom infrastructures). Of the three TSV process options (via-first, via-middle and via-last), IPDiA endorsed the via-last approach, in which vias are formed after the die has been manufactured. This choice is mainly driven by co-integrating TSV with passive integration connecting substrate (PICS) technology. Moreover, this solution brings the potential of making TSVs on pre-existing CMOS wafers or on a 2.5D IPD interposer [5]. The TSV key process steps are listed below (Figure 1):

Bonding process. Temporary wafer bonding carried out on a glass substrate is necessary to make thin-wafer handling possible through the next steps at process temperatures up to 250°C.

Deep silicon etching. Because of the bonding process, silicon etching is made from the back side to the first dielectric on the front side. During this step, the undesirable notching effect at the bottom of the via is minimized and the thickness variations are absorbed, preparing the ground for functional and efficient vias.

Insulation deposition. An SiO_2 layer is deposited to provide the insulation needed between the lateral parts of the vias and the substrate. At this stage, a thickness ratio of 0.25 between the bottom corner and the top plane and a relative permittivity of 5 are

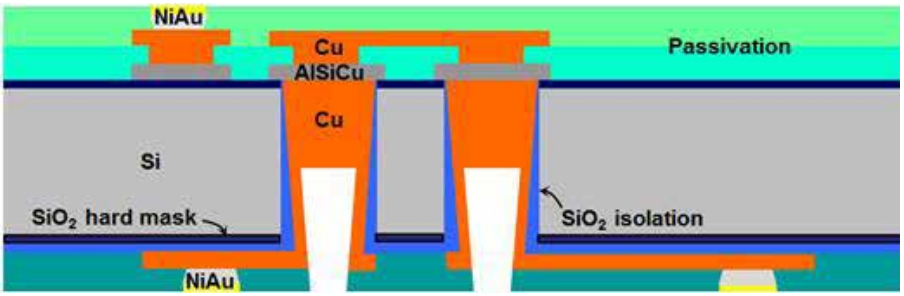

Figure 1: Schematic view of the via final architecture.

measured, which leads us to conclude that conditions are right for the propagation of RF signals through the TSV with limited attenuation.

Etch back. The insulation film and the first silicon dielectric are removed from the bottom of the cavities with an etching step using a gas mixture consisting mainly of Ar for an efficient vertical etch. Cooling steps are necessary to preserve the wafer bonding glue.

Barrier and seed deposition. The efficiency of the copper filling depends on the characteristics of underlying barrier and seed layers. Ti is used as an adherence layer and TiN as a barrier against Cu diffusion into the interposer silicon structure.

Copper via filling and back side metallization. At this stage, both copper via filling and back side metallization (tracks) are carried out. In order to modulate the copper thickness at the bottom of vias while limiting the thickness at the surface, we have developed a "super-filling" process, which is achieved with electrochemical deposition and pulsed current. The "super-filling" facilitates the final module assembly.

Passivation and finishing. After the seed layer etching, a final passivation step using organic material is performed to complete the wafer back side and clog the via holes to prevent corrosion. Finishing prepares the assembly step with micro-bumps made at the back side of the interposer.

Substrate	Printed Circuit Board (PCB)	Thick/thin flex	Ceramic	Silicon Interposer
Line width / Spacing	90 µm down to 65 µm for advanced PCB technologies	75 µm down to 50 µm for advanced thin flex technologies	75 µm to 50 µm for advanced LTCC technologies	5 µm
	Accuracy around 25 µm	Accuracy around 15 µm	Accuracy around 15 µm or less for LTCC	Less than 1µm
Metal layers for signal & routing management	One metal layer in between 2 thick laminated layers	Two layers for advanced flex technology	One layer	No limitation (2 to 3 layers)
Via diameter	200 µm or less for advanced PCB	150 µm for the best in class	120 µm for advanced LTCC	75 µm or less

Table 1: Comparison with several substrates of dimensional features.

Substrate	Printed Circuit Board (PCB)	Thick flex	Ceramic	Silicon Interposer
CTE1	~ 20 ppm/K	~ 20 ppm/K	~ 10 ppm/K	~ 2 ppm/K
	Big CTE mismatch with Silicon based ASIC	Big CTE mismatch with Silicon based ASIC	Slight CTE mismatch with Silicon based ASIC	No CTE mismatch with Silicon based ASIC
Temperature	Limited to 250 °C with warpage	Lower than 200 °C with polymer degradation	Higher than 400 °C for HTCC. Lower than 300 °C for LTTC	Higher than 300 °C
Packaging Process Compatibility	Very good with SMD	Good with SMD	Good with SMD	Good with SMD
	Specific adjustment with silicon die set	Good with silicon die set	Specific adjustment with silicon die set	Very good with silicon die set

Table 2: Comparison with several substrates of thermal and thermo-mechanical features.

Dimensional comparison table. Main dimensional characteristics for different types of substrates are summarized in Table 1.

Thermal and thermo-mechanical comparison table. Main thermal and thermo-mechanical characteristics for different types of substrate are summarized in Table 2.

Electrical characterization

All the results presented in the electrical characterization and the reliability model

sections refer to reference #5 [5]. Based on the process described above, wafers have been processed and characterized in HF mode from which a π-shape equivalent model is validated. The results of the TSV performance are measured at high-frequency (HF) on a specific test structure called a dual via chain (DVC) including a co-planar waveguide (CPW) adapted access, two TSVs, and a back side layer. HF results are presented in Figure 2. The graphs represent the transmission and reflection of a 250µm length DVC.

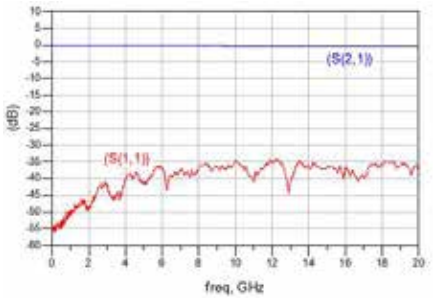

Figure 2: HR measurement result; transmission (S21 in blue), and reflection (S11 in red).

The results in Figure 3 show a rejection between transmission and reflection of more than 35dB throughout the frequency range (up to 20GHz), and a very low loss in transmission – better than 0.35dB. This performance is obtained thanks to control of the process, particularly with efficient contact between the copper in vias and the first metal layer on the front side, and the insulation of the TSV even on its critical corner in the bottom. As shown in Figure 3, we can conclude that the use of high resistivity (HR) silicon has consistently reduced conductive loss in DVC of TSVs. The high value of resistance introduced by the use of an HR substrate makes it less sensitive to the effects of noise.

Reliability model

In order to test the ability to withstand cyclical exposure and introduce mechanical stress to TSV structures, they were subjected to thermal cycling (TMCL) as recommended by JEDEC standard [6] (cycling: -40°C to 125°C with a 10°C/min ramp, during 200, 500 and 1000 cycles). The DC resistance of a daisy chain made of 50 TSVs is measured by a 4-point probe system. Figure 4 shows the electrical results after this thermo-mechanical stress. Preconditioning was made on a full wafer (74 DVC structures) and TMCL reliability tests on ¼ wafer (16 DVC structures).

The normal distribution of DC resistance on a full wafer test (blue bar chart) and the cumulative distribution function (red curve) validates a good uniformity on a full wafer for a TSV chain structure. Note that the TMCL reliability test has been done on a ¼ wafer having the structure with the higher resistance. Moreover, the low number of structures induces a non-normal distribution. However, the low confidence interval on them reveals good uniformity and therefore good process maturity. The small and successive decreases in DC resistance can be interpreted as a crystalline rearrangement of copper introduced by successive cycling. This statistical approach allows us to estimate single TSV resistance to 124mΩ with a very high accuracy, i.e., error less than 2%.

Application examples

The application examples given below come as a conclusion of this article and illustrate the benefits of the different types of interposers in three specific areas (implantable medical devices, vision care devices, and aerospace).

1/2D silicon interposer with IPD for implantable medical devices. In this first example, major improvements were made using the interposer discussed in this article with integrated passive devices for a medical sensor module including RF communication (Figure 5). The module is to be used in an implantable defibrillation system. The main concerns of the customer are miniaturization (impact of size and weight), stability, and reliability. The silicon not only serves as a redistribution layer, but also allows the integration of passive components within the substrate. It enables a size reduction (35% area saving) and a decrease of the total system weight. Additionally, the PICS technology used for integration of the passive components results in very stable high capacitor integration.

2/2D silicon interposers with IPD for vision care devices. The final application of this second example is linked to the medical field, more precisely to preventive treatment for vision care. The first advantage the method we have developed has brought forward is miniaturization of the final device

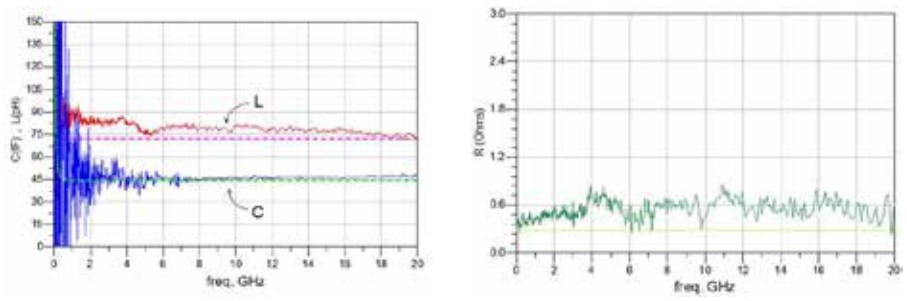

Figure 3: Simulation (dashed line) and measurement (solid line) of extracted TSV π-shape elements. Parallel capacitance and series inductance (left), series resistance (right).

Statistics	Before Precond.	0 cycles	200 cycles	500 cycles	1000 cycles
Average	6,193	6,886	6,721	6,516	6,240
error deviation	0,073	0,126	0,119	0,110	0,101
median	6,172	6,869	6,714	6,520	6,236
standard deviation	0,630	0,487	0,459	0,440	0,404
sample variance	0,396	0,237	0,211	0,194	0,163
number of samples	74	16	16	16	16
Confidence interval(95.0%)	0,146	0,270	0,254	0,235	0,215

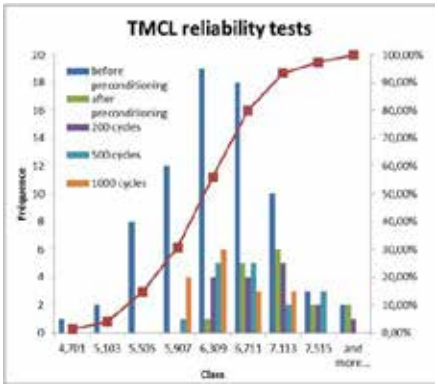

Figure 4: Statistic chart and table on DC resistance results after TMCL reliability test.

Figure 5: RF module for medical application using IPDiA 2D interposer technology [7-8].

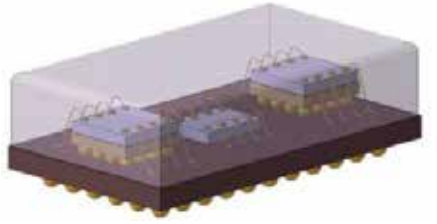

Figure 6: Motor controller device for avionic application using IPDiA 2.5D interposer technology [9].

in the x, y and z axes. We have also adapted this technology to the customer's product environment and have developed a module with four 2D silicon interposers including IPD and active components—the complete system being mounted on a 100µm thick flexible organic substrate.

3/2.5D silicon interposer with IPD for aerospace. The third example combines integrated passive devices with a TSV 2.5D interposer combined with a 3D packaging technology, suitable for motor control in the aerospace domain (Figure 6). This time, miniaturization and decrease of the total weight of the device is optimized thanks to the combination of IPD, TSV and 3D packing. Reliability is achieved by the silicon-silicon compatibility. The complete module is finalized by using a stacked-die technology on the 2.5D interposer.

Acknowledgments

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High-reliability via interconnections in glass wafers for 2.5D packaging

By Tim Mobley, Roupen Keusseyan [Triton Microtechnologies, Inc.]

Semiconductor devices are constantly responding to the market demand for faster, smaller and less expensive devices. Devices are expected to deliver more functionality at greater speeds in smaller dimensions and with interconnecting electrical and optical signals between them. This demand requires a new packaging scheme that can integrate heterogeneous devices such as logic, memory, power, graphics, optics, displays, sensors and other integrated circuits and components in a single package; improved electrical performance is also achieved by having these devices in close proximity in a hermetic environment.

For the past decade, work has focused mainly on silicon interposer technology using through-silicon vias (TSVs), seemingly driven from a convenience factor, as existing equipment, processes and materials for IC technology can also be used for passive silicon-based interposer processing. Although silicon is a convenient choice in the field of 2.5D and 3D packaging technologies, critical material properties fall short when considering silicon for passive interposers, such as high-speed routing, hermeticity and cost reduction considerations. Table 1 summarizes the critical differences between silicon, glass and organic laminate-based interposer materials. These differences will be highlighted and discussed in the following sections.

Recent technical advances in processing of borosilicate glass wafers for interposer applications have enabled a new technology with superior characteristics and material properties in critical areas and needs for next-generation material systems. The primary argument is why should a designer sacrifice performance when higher performance can be achieved over silicon at lower cost simply because the wafer foundries are using silicon when it is convenient for them to process passive silicon interposers? The path to scalability and low cost lies within panel processing, which cannot be achieved with silicon. The maturity of glass has reached a point that is ready for the market and panel processing is being addressed by major partnerships in the industry. The present article will focus on unique characteristics of high-reliability through-glass via (TGV) metallizations that are hermetic, with high electrical conductivity (close to that of bulk copper), low cost, thermal coefficient of expansion (TCE) matched with the borosilicate glass (3.2ppm/°C) and having no plating solution remnants or ions that are normally known to cause system reliability and high-humidity bias test (HHBT) issues between metallization interfaces of vias and planar traces.

The borosilicate glass used in this application is the same material used for liquid crystal display (LCD) front panel displays; thus, it is available as a reliable high-volume source of substrate material, possesses excellent optical transparency, and is manufactured in large panel sizes (up to 2160 x 2460mm for Gen 8). For the current application, glass panels that are 550 x 650mm (Gen 3) or smaller are used as a starting point, taking advantage of under-utilized older display glass production lines, and scribed/cut down to standard semiconductor wafer sizes of 100, 150, 200, 300 and 450mm that are subsequently processed to generate holes and via filling. Standard semiconductor wafers are cut from the panels in order to accommodate today's downstream processing such as metal coating, photo resist depositions, imaging, and developing for generation of circuit patterns. The major advantage of the authors' position is that the processes used for standard circular wafers can be eventually eliminated and large panels can be utilized with the same process line enabling a multitude of interposers on the same panel; this is nearly impossible for silicon-based interposer platforms—now and in the future.

As shown in Table 1, borosilicate-based glass interposer platforms have superior material characteristics compared to silicon; dielectric, high-frequency performance and digital module capabilities for the type of borosilicate glass used are discussed in detail in reference [2]. The applications driving these key care-abouts are 2.5D packaging, life science glass slides, microfluidics, and displays, which now can be enabled with new designs and electrical functions because reliable vias are integrated into the glass, all while processed in large-panel format. Today, TGV wafers are produced in wafer format in order to be easily utilized in downstream processing, and may be temporarily bonded to sacrificial wafers in order to handle thin glass wafers, which can be transitioned to large panels as depicted in Figure 1.

	Desired Properties	Glass	Silicon	Organic Laminate
TTV	<5µm			
Warp	<2µm/20mm			
Insulation Resistance	High			
Optical Transparency	Optical I/O			
Surface Roughness	<5nm			
TCE	3.2ppm/C			
Hermetic Vias	Mil-Spec.			

Table 1: Critical material characteristics for interposer material systems.

Process

One of the challenges in producing glass interposer technology is generating small diameter through-holes in borosilicate

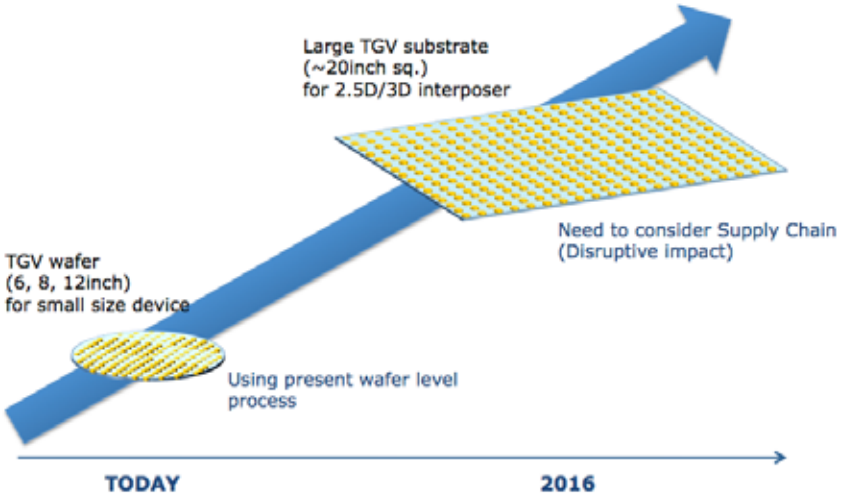

Figure 1: Transition to glass panel processing.

glass with pitches less than 150µm and diameters of 70µm or smaller in 700µm thick glass or thinner; this is critical for electrical designers that have high count I/O systems. The shape of the hole from top to bottom depends on the through-hole drilling method and approaches. Figure 2 shows a side view of typical non-metallized though-holes generated in glass, while Figure 3 shows a cross section of the filled through-hole with copper. The copper is processed at elevated temperatures for ideal conductivity to achieve hermeticity and a TCE match with that of the borosilicate glass. While the authors have not definitively described TCE of a single Cu via in glass, a via does not change its characteristics during or after thermal cycling, which is indicative of the via being closely matched in thermal expansion to that of the glass substrate.

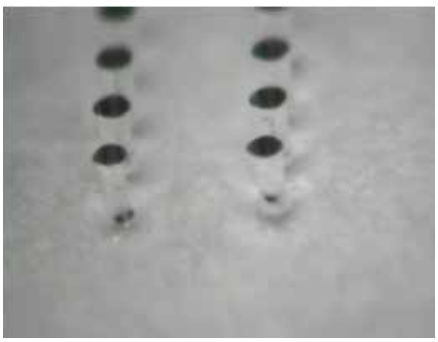

Figure 2: Non-metallized through-holes in borosilicate glass.

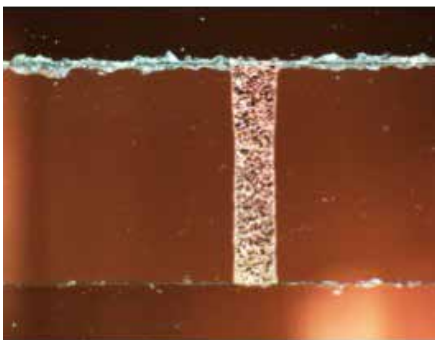

Figure 3: Copper-filled via in borosilicate glass interposer.

Figure 3 shows a cross section of the filled through-hole with copper, which is currently obtained by destructively testing from each lot of glass wafers, providing confidence that there are no voids in the via and adhesion is achieved by processing at elevated temperatures while relaxing the glass wafer from stresses. The top and bottom surfaces in Figure 3 are roughened from the scribing affect in order to quickly perform cross sections on the production line and inspect quickly, and is not indicative of the final wafer surface roughness.

Thermal cycling reliability and low warp of the system are optimized when the TCE of the copper via is matched to the borosilicate glass substrate, using high processing temperatures, and by not approaching the softening point of the borosilicate glass (typically between 815°C and 830°C). A critical feature mentioned in Table 1 is the warp or bow across a wafer. Measurements are performed on a 3D laser profilometer and typical results in a 20mm square area are less than 2µm, and over a 150mm wafer is less than 20µm as shown in Figure 4. The X-axis is the diagonal distance across the wafer that the laser scan travelled and the Y-axis is the change in height over the 150mm scan length. This solution is in contrast with other solutions that plate into blind vias and require back side grinding from one side in order to reveal the via thereby resulting in extremely high stresses and large warp. The impact of this new process is that breakage of wafers is reduced during handling and increases reliability of large I/O die with fine pitch, ensuring that all the interconnects can be attached to the pads on the glass interposer due to the low warp at the die level.

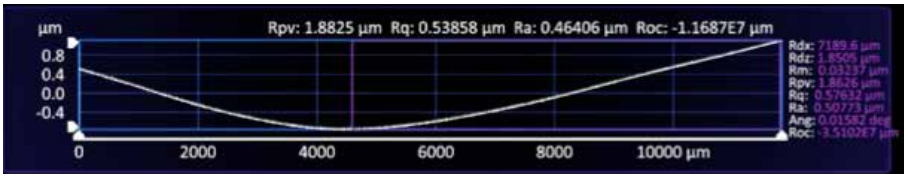

Figure 4: 3D profilometer scan of a 150mm wafer post-processing.

Hermeticity is extremely critical in any future interposer system design for two primary reasons: first, subsequent process fluids can become entrapped in voids or non-hermetic regions of the via and released during later thermal events to the wafer, causing metal delamination and eventual circuit failure. Figure 5 shows a generalized system designs cross section for typical interposers available in literature, used here to as a common reference of terminologies to highlight the regions to discuss hermeticity.

A second reason that hermeticity in an interposer system is critical is that ICs should be protected from the environment from all sides of the package in order to ensure the highest reliability. The ICs are "presumably" protected by using a hermetic enclosure. However, if the vias in the interposer are not hermetic, the system as a whole is not hermetic, even though the spacing between the printed wiring board (PWB) and the interposer is filled with an organic material. This approach will protect

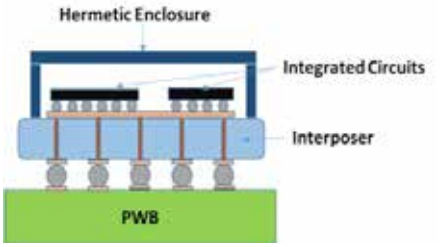

Figure 5: Cross section of a generalized interposer system.

the IC to a degree and having hermetic vias in the interposer is critical for the reliability of the total system. Thus, why sacrifice hermeticity if you can have it at a lower cost compared to that of silicon?

Finally, referring to Table 1 in regards to material property differences: silicon has much higher thermal conductivity (150W/m/K) compared to borosilicate glass by itself. However, systems have been designed using thermal vias (Figure 6) that strategically improve the thermal conductivity of glass interposer

Figure 6: Cross sectional view of thermal vias in a borosilicate glass interposer.

by designing in vias to remove the heat away quickly and through the substrate by use of the copper-filled vias. The thermal vias can be used for logic, power or other applications where thermal issues are critical.

Summary

A new core packaging technology using borosilicate glass interposers has been developed and is undergoing intensive investigation for 2.5D packaging solutions by many designers. The inherent ability to process the Cu vias discussed in this article overcomes several technical hurdles and provides users a path to scalability with hermetic vias. Electrical conductivity, TCE matching and hermeticity of the copper-based vias have been emphasized and demonstrated as critical achievements in the current work. Glass is well poised, now and far into the future, to enable designers to realize ideas that have never before been able to be achieved by integrating the circuit designs into the glass for 2.5D packaging, displays, life science slides, and microfluidic applications. A strong glass core with low cost, highly reliable vias provides a platform of integration of nearly any type of process on the glass core.

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Error-free assembly operation through recipe management

By Didier Chavet [SanDisk Inc.] and Shekar Krishnaswamy [Applied Materials, Inc.]

Semiconductor assembly and test has traditionally been a manual operation with a legacy of simple and rudimentary approaches for decision making and execution. However, the recent advances in technology coupled with complex product requirements have induced great complexity in assembly and test. Legacy manual approaches cannot provide the required efficiencies necessary for a cost-effective operation. In fact, they can be expected to worsen the cost equation due to increased scrap arising from errors in manual methods. Automation methods can certainly minimize scrap and improve product quality. One such approach using recipe management has been implemented at SanDisk and this paper provides some of the key elements of recipe management that has helped SanDisk achieve phenomenal results.

Some of the noteworthy devices using SanDisks' flash memory storage solutions include smartphones, tablets and solid-state drives in the personal computing and enterprise computing segments. The significant growth of this market has led to many innovations in flash technology that have continuously generated the demand for sophisticated integrated circuit (IC) packages. These innovations include products manufactured using 2.5D and 3D packaging technologies.

Because of the rapid adoption of advanced technologies in the packaging segment of semiconductor processing, there is a significant need for tighter management and control of the manufacturing operations. Some of the challenges generally seen in the semiconductor fab operations are now being seen in assembly and test. Some examples are product re-entrance in the manufacturing process wherein the same product is processed at the same machine-type multiple times, the need for increased adherence to procedures in manufacturing execution systems (MES), effective use of statistical and advanced process controls, equipment automation, automated error-proof processes, etc.

The application of the techniques listed above and the addressing of the relevant challenges in assembly and test have been spotty at best. A major cause for the continued inefficiency is the reliance on manual methods and procedures, which is a legacy of traditional assembly and test technologies. In such complex environments, these manual approaches generally induce many procedural errors in the execution of the manufacturing process leading to product scrap and quality issues. This had been a large problem in fab operations and was reported to account for 40% of process holds in one fab [1]. Fabs, however, have been able to effectively use automation techniques and seem to have the problem under control.

The manufacturing operation at SanDisk's Shanghai assembly and test facility involves processing at multiple machines. Hundreds of different part numbers can be processed at each machine. In addition, each part number could be processed at the same machine but under different processing conditions. The processing parameters for each operation and each part type are encapsulated into a "process recipe." Because of the large number of part numbers and the different processes in the process flow, there could be hundreds of different recipes qualified on any particular machine. It is becoming intractable to use manual methods of recipe selection and recipe usage because of this complexity. The use of an incorrect recipe invariably causes product scrap leading to higher manufacturing costs and issues with customer satisfaction.

As part of the SanDisk's lean management and six-sigma programs, a major objective was to increase productivity, quality and reliability of the production operation at the Shanghai assembly and test facility. A key opportunity for scrap reduction and quality improvement existed in the adoption and deployment of an automated recipe management system (RMS) that eliminates human-induced processing errors caused by the use of wrong process recipes. This paper will provide more details on the implementation of such a system and the benefits seen as a result.

Industry efforts in recipe management

Though semiconductor assembly and test operations are increasing in complexity, there are very few documented implementations of a comprehensive RMS. Most of the literature is focused on the application of RMS in semiconductor fab processing.

Tseng, et al. [2], describe the implementation of a recipe control and management system (RCMS) in their high-volume fab at United Microelectronics Corporation (UMC). Their system has a comprehensive method of recipe parameter uploads, comparison and usage. They have multiple supporting sub-systems that include job cancellations, alarm disposition, pre-checking, change management and reporting. Incorrect recipe usage is classified as a major abnormal event (MAE). The occurrences of MAE across a four-year time period have dropped to nearly zero as the coverage of RCMS has spread across all the fabs in UMC.

Baweja, et al. [3], describe the importance of a central recipe management system. Their work mainly focused on the data flow and the functional design of such a system. They describe the different formats that can be used in representing recipes and the challenges with each of the formats.

Approach and design

The SanDisk team outlined the key basic functions required for effective

recipe management as follows:

- Requesting a recipe based on product and process from MES;
- Request for <checking in> a recipe based on the recipe-ID received from MES;
- Validating the equipment unit recipe ID;
- Receiving the content and parameters of the recipe for the operation (if required);
- Downloading of the recipe to the equipment unit (if required);
- Validating the download process (if required); and
- Performing pre-execution checks.

Other SanDisk functions required for effective quality management have included:

- Checking for alerts and status of equipment units;
- Performing equipment unit parameters and process variables threshold analysis;
- Creation of equipment unit quality incidents;
- Automated lot holds before processing in response to a quality incident;
- Quality Incident Resolution Process;
- Quality Incident Disposition Process;
- Automation of MES operation start and end transactions; and
- Automated key product attributes error-proof process.

In addition to the compilation and mapping of requirements and functions, the generic design included the activity mapping diagrams that detailed all the relevant activities, the key players and their sequence of execution.

A key component of the design was to provide a user interface to capture the sequence of automated and manual events. Initially, this was meant for configuration and diagnostics. It was felt, however, that there was enough value for the manufacturing operator that it eventually turned out to be the single operator interface to the manufacturing process step across all process steps, providing strong consistency and rapid manufacturing operator education.

Another important component of the design was alarm management. Prior to the deployment of RMS, many unnecessary and non-value added steps were performed by the operators. These activities were never exposed, but the RMS alarm management captured all these events along with their frequencies. These were, in turn, used to educate the operators on such non-value added activities and the need to eliminate them. A schematic diagram of all the interacting components is shown in **Figure 1**.

Deployment and results

The Applied Materials E3™ RMS was the chosen solution that satisfied the SanDisk requirements. The E3™ framework coupled with the E3™ Equipment Automation Platform (EAP) provided the necessary functionality along with the required integration capabilities to the other systems such as MES. The key functionalities provided by E3™ RMS are shown in **Figure 2**.

The site has more than 800 equipment units. Based on the criticality, the decision was made to deploy RMS across 90% of the equipment set in four phases over a span of three years. Nearly 15% of this set was targeted for phase 1. The project is currently in the final phase that will cover the last 10% of the targeted equipment set.

Some of the key results seen from the project deployment so far are: 1) Product cycle-time reduction (throughput improvement); 2) Streamlined equipment monitoring and alert management; and 3) Drastic reduction of product quality incidents related to equipment unit issues.

While the main objective of the project was scrap prevention and quality enhancement, significant benefits were seen in other areas such as alarm management and incident resolution, unauthorized parameter changes, and most importantly, equipment throughput improvement by way of efficiencies gained through automating recipe downloads and MES transactions. In fact, the throughput improvement and MES transactions automation alone provided a payback for phase 1 to just under 30 days per machine. This justified the project propagation to the remaining phases and similar improvements have been realized across the remaining equipment sets.

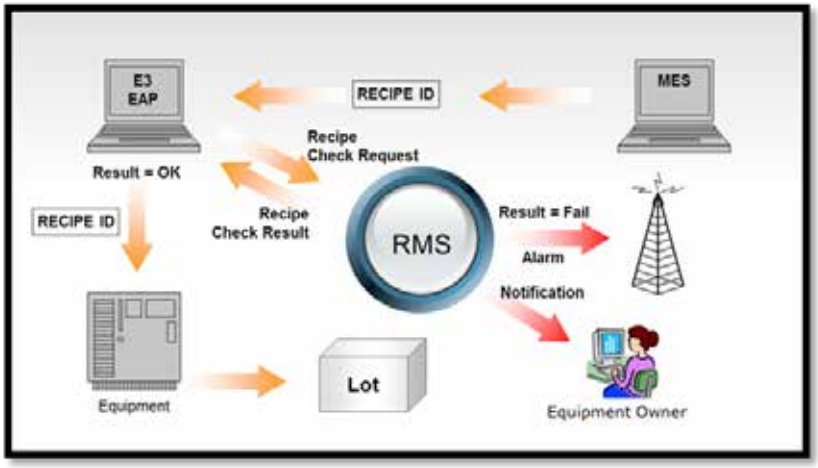

Figure 1: Schematic diagram of all the interacting components in the RMS.

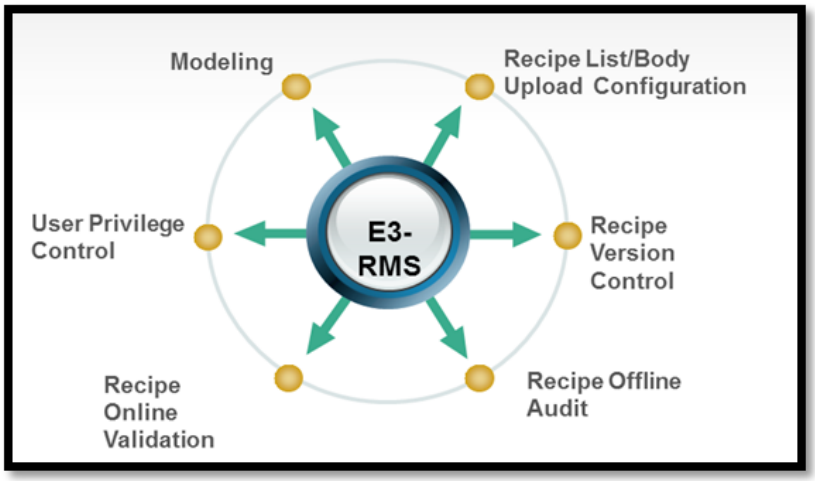

Figure 2: Key functionalities provided by E3™ RMS.

Future direction

While the RMS has provided a basic foundation for factory automation, more remains to be done to extract further improvements in the factory. The remaining improvements include: 1) Automated material handling; 2) Single die traceability; 3) Going totally paperless in the factory; and 4) Real-time dispatch and scheduling.

Summary

Lean manufacturing principles drive productivity improvements through a variety of strategies. Two key elements of lean manufacturing are the elimination of errors and consistency in decision making. SanDisk embarked on the main objective of elimination of human-induced errors through the implementation of recipe management. This paper has detailed some of the activities that have led to achieving this objective. More importantly, this project has also helped achieve productivity through improvements garnered by cycle-time reduction by elimination of wasteful sub-activities and quality improvements through alarm management and issue resolution.

Acknowledgements

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Lowering the cost of MEMS through improved process control

By Erwan Le Roy [Solid State Equipment LLC]

At the dawn of the Internet of Things (IoT) and in the age of smart wearable devices, microelectromechanical system (MEMS) components are becoming critically important as a result of their ability to sense and report on the environment around them; to provide micro-actuating functions such as RF switching; and to provide robust, silicon-based timing solutions in a move to replace quartz-based legacy products. Consumer electronics continue to drive the need for smaller, high-performance, lower-cost MEMS solutions.

MEMS packaging drivers

The need for new MEMS packaging configurations is forcing a reduction in MEMS device thickness to decrease overall package height, as has been the recent trend in the broader CMOS IC industry. According to STATS ChipPAC, "Market demand for advanced, multi-functional portable electronic devices is driving the need for semiconductor packages with higher thermal and electrical performance, increased bandwidth and speed in an ultra-thin package profile [1]."

Additionally, the forecast for significant increases in the number of MEMS devices and the need for continued cost reductions in MEMS manufacturing call for a larger wafer format for MEMS fabrication, as has also been the case for CMOS ICs. Yole Développement, a market research firm covering the MEMS space, estimates that approximately 40% of the total number of processed MEMS wafers by 2018 will be 8" wafers, compared to the emphasis on 6" – and smaller – MEMS wafer processing today. The trend will be to continue to increase wafer size, to 12" wafers, as the number of MEMS sensors fabricated per year reaches the 1 trillion mark [2]. These cost and miniaturization requirements are driving MEMS technology toward wafer-level packaging (WLP) methods that can be applied to a wide range of MEMS devices.

A variety of processes and technologies characterize MEMS device fabrication (the result of the Yole Développement MEMS Law of "one product, one process, one package"), and MEMS as a device family is a technology supporting a wide range of nonstandard wafer thicknesses. To address the need for thinner MEMS sensors for mobile applications, the individual elements of a stacked MEMS product—for example, the wafer cap, the MEMS sensing elements, and the paired application specific integrated circuit (ASIC)—will need to become thinner, particularly for inertial MEMS products.

MEMS fabrication is characterized by a wide range of photoresist thicknesses, from thin photoresists used for standard imaging applications, to thick photoresists that may or may not be intended to become a permanent part of the final structure of the MEMS device as a protective material. In the event that the thick resist needs to be completely removed, the thick resist poses a challenge to conventional stripping methods.

The MEMS industry is taking many different actions to meet the changes noted above head-on. One example is the industry's transition from batch-wafer processing to single-wafer processing in many of the unit operations found in typical wafer fabs to achieve better process control, better process uniformity, and higher device yields.

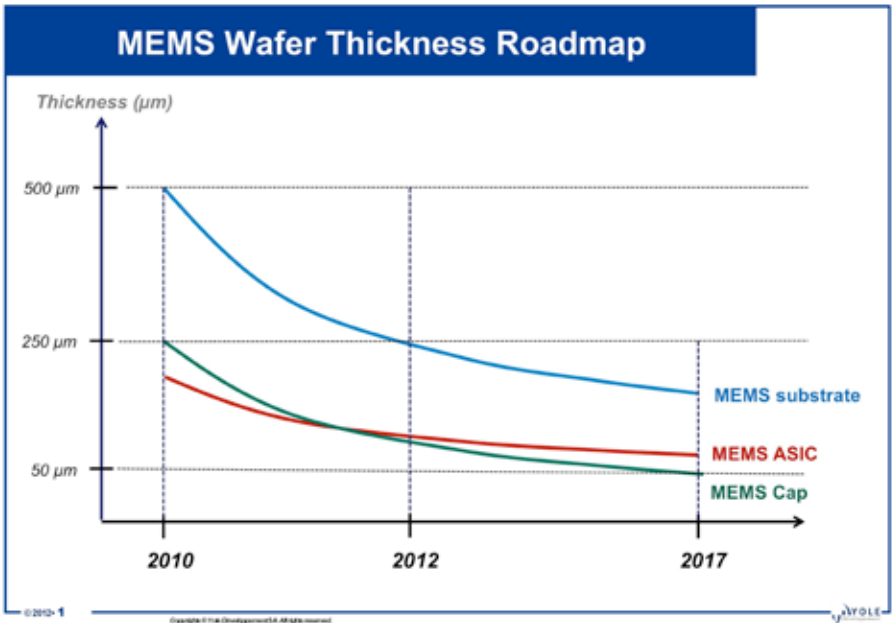

Figure 1: MEMS wafer thickness roadmap. (Courtesy of Yole Développement.)

MEMS manufacturing challenges

To achieve some of the important processing goals listed above, we will consider two key single-wafer wet processes for MEMS packaging: wafer thinning and photoresist removal.

Wafer thinning challenges. In general, a packaged, fully integrated MEMS product is comprised of a sensing (or actuating or resonating) element, a protective cap (silicon, glass or quartz), and a paired ASIC. Each of these elements is expected to decrease in thickness in the near future (Figure 1).

In the continuum of MEMS device processed-wafer thicknesses, RF MEMS are typically the thinnest devices. Resonator wafers are also very thin (100µm) and require temporary bonding for handling because of the mechanical fragility of thin silicon. The standard starting thickness for 6" silicon wafers is 675µm, and for 8" wafers, it is 725µm. Cap thickness ranges can also be on the order of 100µm for MEMS resonators.

As wafer thicknesses decrease below 100µm, wafers are less mechanically stable and more vulnerable to stresses, and die can be prone to breaking and warping—not only during the wafer thinning process, but in subsequent processing steps.

Depending on the MEMS product, wafer thinning will be performed on the MEMS device wafer itself, the capping wafer forming the MEMS cap, and/or the paired ASIC. There is a wide range of wafer-thinning processes and technologies for silicon removal after the grinding process. Key post-grinding wafer thinning processes include stress relief in order to remove mechanical damage to the wafer (incurred during the bulk thinning process), wet cleaning to remove polishing particles, and a final thinning process to reach the target thickness (wet, dry or chemical mechanical polish [CMP]).

To produce wafers less than 100µm thick, the thinning process becomes more challenging, and often requires special handling, for example, using dedicated wafer carriers. Such thin wafers are subject to increased risk of warpage and fractures as a result of the decreased mechanical strength of the thinned silicon. This can impact MEMS fab line yields, and can also affect long-term device reliability [3].

An alternative solution for wafer thinning. To respond to the emerging industry need for thin wafers, post-grinding wafer thinning using single-wafer wet etch is a viable alternative. Using wet etch with integrated metrology reduces processing and capital equipment costs by improving and simplifying the process based on only one platform—the wet etch tool—instead of the four separate tools (CMP, Si thickness measurement, Si etch, and wet cleaning) associated with standard wafer thinning practices. This single-wafer etch processing equipment can achieve less than 1.5% remaining silicon thickness uniformity by controlling the chemical dispense arm, the chemistry flow rate, and the wafer rotation speed.

A critical step for silicon wafers

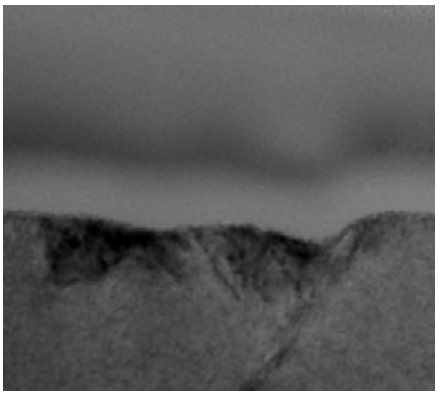

Figure 2: Surface damage resulting from mechanical grinding.

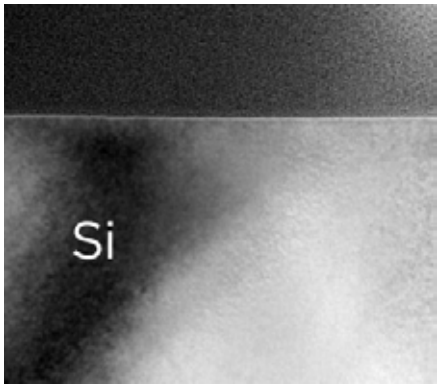

Figure 3: Damaged silicon removed and surface smoothed by isotropic wet etch.

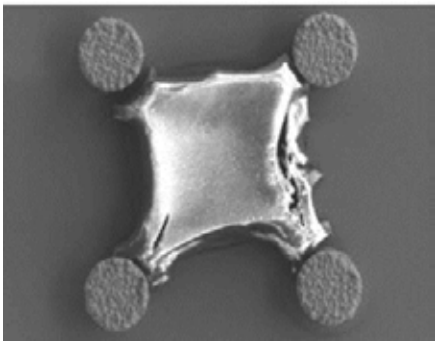

Figure 4: Thick-film residues left after using only batch immersion.

Figure 5: A cassette of wafers soaking in heated solvent.

Figure 6: The four-step process flow using a soak-and-spray wet process platform.

thinned to 100µm is residual stress removal (Figures 2 and 3). Isotropic wet etching of silicon can be used to smooth silicon surface roughness, and hence, reduce stress, induced by mechanical wafer thinning. Further, this method effects a high etch rate of over 10µm/min, for improved productivity. The wet etchant used for silicon wafer thinning contains a mixture of nitric and hydrofluoric acids as the active etch ingredients. The nitric acid acts as an oxidizer to convert the exposed silicon surface into silicon oxide, and then the HF acid etches the oxide. For use in a single-wafer spin processor, the addition of chemicals with higher viscosities is needed to provide a more uniform etch of the wafer surface. Phosphoric and sulfuric acids are added to increase the viscosity of the wet etch solution, but they do not chemically participate in the silicon etching reaction. The addition of these acids does not alter the chemical kinetics of the silicon etch, but does favorably increase the mass-transfer resistance as a result of the increase in viscosity. Process conditions can be selected to tailor the silicon etch rate for creating a smoother silicon surface, and to compensate for thickness nonuniformities of the post-grind wafer (Figure 3) [4].

Thick photoresist film removal challenges. Another key packaging process step for MEMS component fabrication is resist removal, including photoresists and dry patterning films. Due to their chemical composition and significant thicknesses, completely removing these materials tends to be particularly challenging in terms of the required defect-free quality of the final result. Achieving reasonable throughputs poses an added burden.

There is a wide variety of photoresists and dry films used in front-end MEMS processing and in MEMS wafer-level packaging to accommodate the diversity of MEMS device structures. Further, photoresist thicknesses encountered in MEMS fabrication can range from a few microns to a few hundreds of microns [5,6].

Positive resists that are processed at room temperature typically pose no great resist-stripping problem. However, resists that have undergone elevated process temperatures, or that have been exposed to plasma etch environments, may be difficult to remove. Ultrasound agitation, applied in conjunction with photoresist removal using wet processing, can hasten resist removal. However, with resonating MEMS structures and other fragile elements potentially subject to damage from ultrasonic energy, its use is limited [7].

SU-8, a negative photoresist, is commonly used in MEMS device fabrication because the resist is highly transparent in the ultraviolet region, allowing for fabrication of relatively thick (hundreds-of-microns) structures with nearly vertical sidewalls. However, SU-8 is notoriously difficult to remove once processed. For example, the highly cross-linked epoxy remaining after development is difficult to remove reliably from high-aspect-ratio structures without damage or alteration to electroplated metals [8]. One approach is to use a sacrificial polymer layer and lift off the SU-8 resist [9,10].

For these hard-to-remove resists, use of a batch wet-processing tool can potentially negatively impact device yield as a result of incomplete photoresist removal, especially as wafer size increases. Using solely batch immersion to remove thick-film resists results in only partial removal of the film (Figure 4).

Using spray tools for resist removal could potentially negatively impact

throughput. Also, spray tools have a tendency to consume more chemistry than other wet processes.

An alternative solution for thick photoresist film removal. As a viable alternative to batch or spray wafer-processing systems used for thick photoresist removal, a two-step single-wafer wet stripping platform can be substituted. In the first part of the resist removal process, cassettes of wafers are loaded onto a wet stripping tool. The cassettes are then placed in an immersion tank to soak in a heated solvent (Figure 5).

After being softened by this soak step, the wafers are transferred one by one to the single-wafer spray station, where they are exposed to high-pressure fan sprays with heated solvents optimized for rapid removal of thick-film residues (Figure 6).

This single-wafer equipment configuration optimizes device yield by completely removing the resist (Figure 7). Resist residues left on the surface can impact subsequent process steps. For example, during solder reflow, the bumps would now have residual organics as well as unwanted oxide layers. They can also cause furnace contamination and particle issues [11].

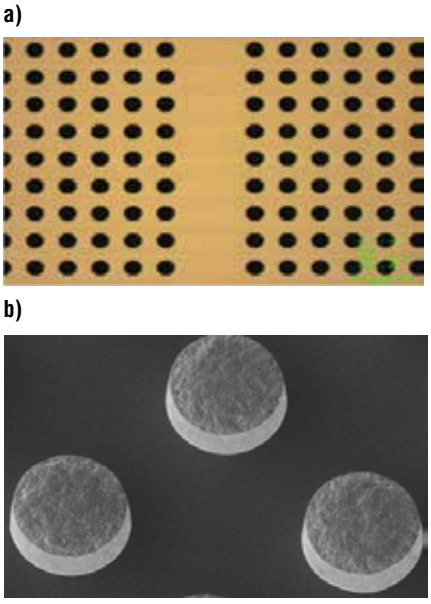

Figure 7: a) Thick-resist film completely removed after stripping using soak-and-spray; and b) Residue-free vias after using soak-and-spray approach for thick-film resist removal.

Single-wafer resist removal reduces the overall cost of MEMS processing and, hence, the final cost of the MEMS product compared to other resist removal techniques. Traditional methods such as wet bench allow for high throughput, but do not completely remove the residue, while spray methods remove more materials, but have a lower output rate. The soak-and-spray technique

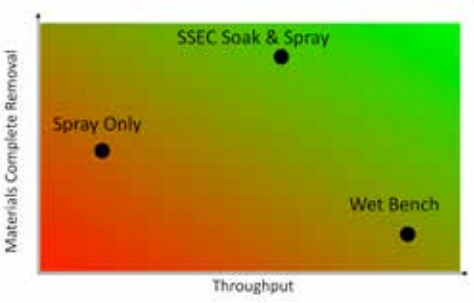

Figure 8: Comparison of soak-and-spray vs. spray-only or wet-bench.

performed in a single tool produces optimum throughput while solving the issues of safely handling very thin wafers and completely removing thick resist (Figure 8).

Summary

As MEMS device fabrication volumes increase from today's healthy level toward the visionary goal of a 1-trillion-sensor future, the MEMS industry is transitioning to larger wafer sizes while continuing to work on improving MEMS fabrication process control and yields, both in front-end MEMS fabrication and in back-end packaging.

Two of the key processes for MEMS packaging are wafer thinning and thick-resist removal. Single-wafer wet etch and resist-stripping-process technologies will enable continued device and line yield improvements on advanced MEMS devices to create a fundamentally lower cost base for MEMS development and production. Failure to address yield and production flexibility issues while attempting to improve process throughput to satisfy increasing MEMS demand will not allow MEMS industry participants to successfully realize the full market potential of increasingly sophisticated MEMS devices—to the detriment of the industry and to its customers. Single-wafer wet etch systems for bulk silicon etch and for thick photoresist film removal offer an attractive means of achieving device yield and quality goals for current and future MEMS front-end and back-end processes.

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Biography

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The evolution of wafer dicing

By Devin Martin [DISCO Hi-Tec America]

The push to achieve increasingly smaller and thinner die as well as the emergence of new products with unique cleanliness and sidewall requirements has led to significant innovations in dicing over the past 10 years. Stacked memory has pushed final die thicknesses below 50µm, and although everyone can imagine the difficulty of thinning wafers to 50µm, perhaps more challenging is dicing wafers this thin. Additionally, RFID and other small devices are pushing die dimensions below 0.5mm x 0.5mm resulting in the need to increase die per wafer by reducing dicing street widths. The migration to low-k dielectric and copper has necessitated the addition of laser surface grooving prior to blade dicing. MEMS that are packaged on the die level typically require very clean surfaces making wet dicing methods very difficult, or impossible. These diverse requirements have driven the development of numerous laser-based processes as well as significant innovation in diamond blade dicing. For device makers looking to optimize yield while reducing cost, the available options can seem daunting. Choosing the wrong dicing process can result in lost time and opportunity. This article will clarify the current benefits and limitations of the various approaches to wafer dicing.

Blade dicing

Blade dicing may be less exciting than laser dicing, but in the majority of cases it is the most flexible and cost effective process for wafer dicing. The ability to change blades and process parameters to cut a wide variety of products and materials has enabled blade dicing to remain the preferred process for many device assemblers. Moreover, the existing install base of dicing saws allows for a great deal of operational flexibility with the ability to allocate production between in-house capacity and multiple subcontractors.

There have been several new developments in diamond blade processing over the past several years including ultrasonic dicing, ultra-thin blades, new bond types, and grit size control. Some of these are enabling innovations while others reduce process cost or improve cut quality. Ultrasonic dicing, where ultrasonic–wave oscillation is transmitted to the blade through the spindle can improve cutting speed and quality for hard to dice materials like SiC and glass. The oscillating motion of the blade reduces loading, which results in better removal of cutting swarf and improved delivery of cooling water to the cutting area (Figure 1). A SiC wafer which, depending on thickness, might be cut at 0.3mm/sec without ultrasonic-wave assistance can now be cut at 3mm/sec with less topside and backside chipping.

In the past, the thinnest blades that could be considered production worthy were about 20µm and could achieve a kerf width of less than 25µm. However, with advancements in blade manufacturing techniques, 10µm-wide dicing blades are now available. The limiting factor for blades is the aspect ratio of thickness to exposure (the usable portion of the blade that extends beyond the aluminum hub). For nickel bond blades, this is typically 20:1, so a blade that is 10µm thick can have 200µm of exposure. This exposure is not enough to cut a full thickness silicon wafer, but sufficient to cut thin wafers or to make very narrow grooves.

Dicing blade bond materials have also evolved that enable higher quality cutting of hard materials. Vitrified bond blades used to only be available in wide format, but are now available in blade widths as thin as 100µm. Vitrified bond blades have excellent rigidity and dimensional accuracy for processing hardened ceramics, sapphire, SiC, and other hard materials.

Vitrified bond blades are also widely used for silicon wafer edge trim. This process uses a flat dressed dicing blade and dicing saw to create a step in the topside of the wafer around the perimeter, typically about 1mm in from the edge of the wafer (Figure 2). This is done so that when wafers are ground very thin, the edge bevel of the wafer will not become a knife edge and result in wafer edge chipping, which can be crack initiation

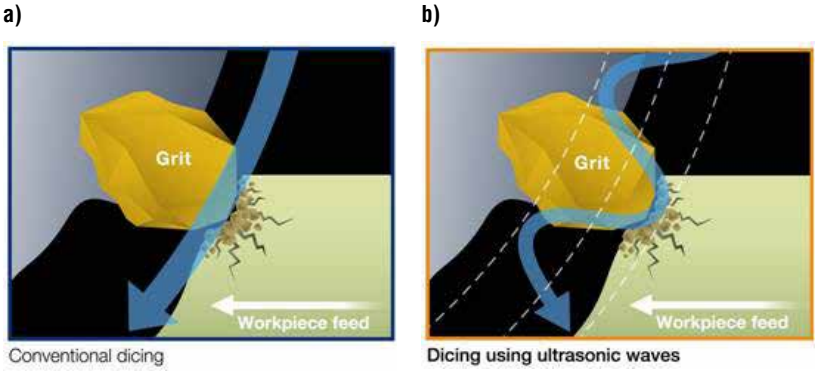

Figure 1: a) Conventional dicing, and b) ultrasonic dicing.

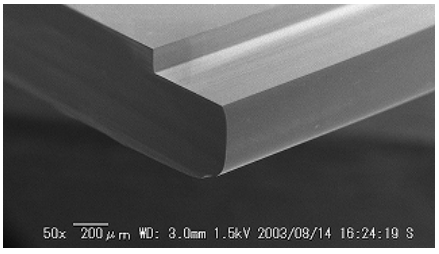

Figure 2: An edge of a trimmed wafer.

points leading to wafer breakage. A high rigidity blade is necessary to maintain the proper edge profile and vitrified bond blades are ideally suited to this.

Nickel bond blades, the most common blade type for dicing silicon, are also now available with porosity. Standard nickel blades are electroplated and therefore do not have any air pockets. This type of blade is suitable for cutting silicon, but as silicon and glass bonded wafers have become more common, a blade that can cut both materials was needed. Silicon shatters into small pieces when cut, but glass tends to shatter into larger pieces during blade dicing. Normally, small diamond grit is used to cut silicon and larger grit is used to cut glass. Prior to the development of porous nickel blades, two blades were used to cut silicon and glass: a resin bond blade with a larger diamond grit to cut glass followed by use of a nickel bond blade with small diamond size to cut the silicon. To use a single blade to cut both materials the self-sharpening effect must be maintained so that it does not load up with material and become dull while using smaller diamond grit to reduce topside and backside chipping. Adding pores to the nickel bond enables self-sharpening to be more uniform with smaller diamond grit so cut quality is consistently maintained (Figure 3).

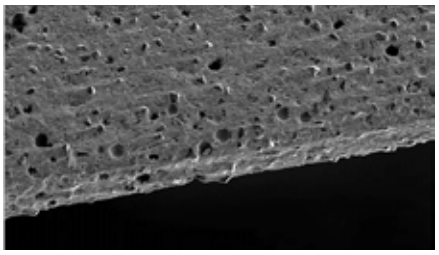

Figure 3: A porous nickel bond blade.

Laser grooving

While blade dicing remains the preferred process for most applications, there are specific cases where the current blade technology cannot overcome material properties. As design rules continue to shrink and inter-layer dielectric materials become more porous and brittle, the abrasive blade dicing process has become incompatible with the surface materials. Topside de-lamination and sub-surface cracking of the dielectric material, in particular at 45nm and below, has necessitated the adoption of laser grooving. The purpose of laser grooving is two-fold. First, the edge of the die must be isolated by creating train track grooves through the surface layers and just into the silicon using a laser. This isolation step is followed by subsequent passes of the laser to remove the material in the street between the train tracks. Once the streets have been "cleaned," the wafer is then diced with a blade that only has to cut through the silicon and not any of the surface materials. Laser grooving eliminates damage to the surface layers but creates another problem: redeposition of ablated material onto the wafer surface. To protect the wafer from the debris, it is coated with a water soluble film prior to laser grooving so that the ablated material lands on the film and not the wafer surface. After laser grooving is completed, the wafer is washed with DI water and the debris is removed along with the coating material leaving a pristine surface.

Laser grooving of low-k wafers has been in practice for over 10 years, but the process has evolved to improve topside quality and increase throughput. Two developments are beam splitting and beam shaping. In the past, a single beam with a round spot size was used to isolate the edges of the die as well as remove material from the street. The round spot size was well suited to die edge isolation, but required several passes to remove the material in the street. The trend lately has been to split the beam in two so that you can isolate the die on either side of the dicing street simultaneously, and then re-shape the beam into a rectangle or oval resulting in a wide beam to clear the street. This technique has greatly reduced the number of passes it takes to achieve the desired street condition.

Stealth dicing

With the rapid growth of specialized MEMS that are packaged on the die level, an extremely clean method of wafer singulation is needed. Stealth Dicing satisfies many of the requirements for dicing MEMS wafers with exposed structures, thin membranes, or other highly sensitive surface features. While laser ablation focuses at or near the surface of the wafer, Stealth Dicing focuses the beam below

the surface. The wavelength of the laser is specific to the material being cut so that the laser light passes through the material at the surface where the energy density is low, but is absorbed at the focal point at a specific depth below the surface. The absorption of the energy below the surface results in a void in the wafer. This void is created in the X and Y direction below the desired dicing lanes and at different depths depending on the wafer thickness. For example, a silicon wafer that is 200µm thick may have linear voids in X and Y at three different depths. The bottom layer acts as a crack initiation point with the voids above guiding the crack to the top surface, essentially acting as vertical perforations. The force to initiate the crack from the lowest void layer can come from tape expansion, a guillotine breaker, or a tape side (backside) scanning bar. For most silicon wafers, the backside is mounted to dicing tape that is stretched in all directions after Stealth Dicing, thereby forcing the wafer to singulate into die along the void planes (Figure 4).

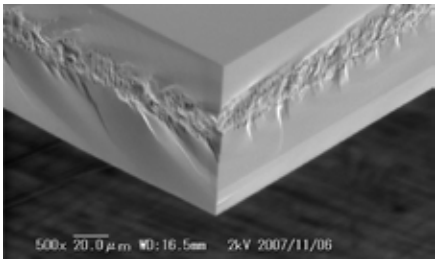

Figure 4: Die sidewall after Stealth Dicing.

The Stealth Dicing process has several advantages. It is an entirely dry process, which means that you do not have the turbulence and contamination that comes with a wet dicing process. This is particularly appealing for MEMS devices that are sensitive to contamination or surface forces. Kerf loss, the material in the dicing streets that is lost because of blade thickness, is also eliminated. This allows for dicing street width to be reduced, thereby increasing the number of die per wafer in the case of very small die. Stealth Dicing also results in stronger die than blade dicing because of the near elimination of topside and backside chipping. Because chipping due to diamond blade dicing can be a die crack initiation point resulting in die breakage, the elimination of it increases average die strength.

Stealth Dicing does have some limitations. The surface from which one irradiates, must be relatively smooth, at least a #2000 mesh ground surface finish. The surface must also have a clear path with no metal or reflective coatings that is 40% of the wafer thickness. So a 400µm-thick wafer requires a 160µm-wide dicing path at the surface. In cases where dicing streets need to be reduced below 50µm, the typical process is to irradiate from the backside.

Dicing thin wafers below 50µm

As the number of die vertically stacked into a single package keeps increasing, as well as ultra-thin die for conformal/wearable devices becomes more widespread, there is a push to create strong die that are very thin. The typical process of thinning wafers and then dicing them becomes very difficult below 50µm, and therefore, alternative processes have been developed. One of these is Stealth Dice Before Grind (SDBG). In this process, a modified layer is created just above the final thickness of the die using Stealth Dicing. The wafer is then ground to the final thickness and in the process, the Stealth Layer propagates to the frontside to singulate the wafer into die. The resulting die have nearly zero topside, backside, or sidewall damage, and are therefore flexible and less prone to breakage. Tests have shown that SDBG can achieve die thicknesses of 25µm and below with considerably less risk than the conventional process flow.

Summary

Wafer dicing is as old as the semiconductor industry itself, but over the past 10 years it has seen several new technologies emerge. Innovation in laser technology coupled with the development of products that are not compatible with blade dicing has led to new processes including laser grooving and Stealth Dicing. And as exciting as these new developments are, the mainstay for over 40 years, blade dicing, continues to be the primary method of singulating wafers into die. Perhaps in another 10 years there will be a replacement technology. But then again, the engineers developing the diamond blades of tomorrow might have some surprises for the industry.

Biography

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Die attach options and challenges with going thin

By M. Todd Wyant [Texas Instruments]

In back end semiconductor manufacturing, the die attach process is a critical step in the operation of transitioning the silicon wafer into the final unit configuration. In simple terms, the die attach is picking a singulated integrated circuit, or passive component, from a wafer and placing it onto a metal lead frame or substrate surface. The method of attachment truly defines the process and complicates the simple picking and placement. Epoxy, die attach film, spin coat epoxy, screen print epoxy, eutectic, and flip-chip are the main driving die attach methods today and the most commonly used methods in high-output production. Die attach processing is being continually challenged by both shrinking silicon size and by shrinking thickness requirements, and each material type directly impacts manufacturing and its associated risks. This article will discuss the different methods along with the pros and cons of material selection as it relates to the equipment and downstream processes.

Die attach process flow utilized on metal lead frames

The basic die attached steps used for metal lead frame packages are similar regardless of equipment manufacturer and type used, and most are adaptable to the materials we'll discuss in this article. The steps of operation are described below.

The input vacuum arm picks up a lead frame from a stack and places it on the input track or loading system. The lead frame is then shuttled to the dispense position, which can also be used as a preheat station, or it can also have an additional first step preheat station to be used independent of the dispense station. This process step is also highly dependent on the attachment material being utilized. For some material application, the dispense station is not utilized. The alignment is typically performed with a vision system for high accuracy of the material placement in the case of dispense applications.

Post alignment, the machine will dispense a set pattern based on the chip characteristics being mounted. After material is placed, the equipment's vision system will inspect the dispensed pattern to assure correct volume is placed. This inspection is also only applicable to the characteristics of the material used.

The lead frame is then moved to the next position where die placement is completed from a singulated wafer, as shown in Figure 1. The bonding process has many

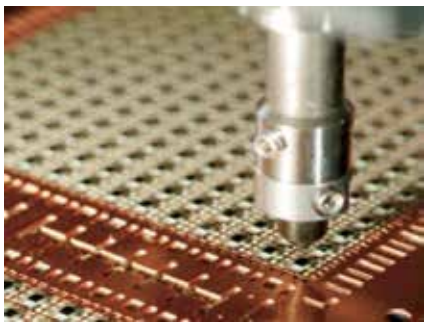

Figure 1: Die placement is completed from a singulated wafer.

variables based on the material set and material utilized for die placement. The main inputs are bond force, dwell timing, and on some machines today, scrubbing at frequency is available.

Another machine inspection can then confirm placement position and tolerance, in addition to placement material defect reasons. The bond pads can be inspected for damage associated with the process, in addition to placement inspections. In some process/material cases, an output station can also be utilized for UV cure or additional post-placement heating of the units to complete the attachment process.

Once the lead frame is populated, inspected and finalized on output (as shown in Figure 2) it is typically placed back into a strip carrier and ready for the next operations.

Figure 2: After population, inspection, and finalization on output, a lead frame is placed back into a strip carrier.

The most common die attach material processes

There are five major die attach materials processes used today in analog semiconductor packaging. The next sections will outline the types used and some of the associated benefits and drawbacks for use today.

Epoxy die attach. Epoxy die attach is the most common process used today and has been the longtime standard for die attach or die bond operations. The process always utilizes an adhesive material to attach the die to the metal substrate. On the initial lead frame input, the adhesive is dispensed in paste form on the lead frame before the die is placed on top. The wide varieties of pastes make it possible to mount a thermally conductive material or electrically isolated material between the die and the pad for mounting. The epoxy composition allows for variations of properties to achieve targeted final design needs and variations. This allows for epoxy die attach processing to be the most flexible and widely used form of attachment utilized. Figure 3 shows typical dispense patterns.

The disadvantages for epoxy die attach revolve around a few common factors: processing time, silicon size, bond line thickness control, and cost. These common factors are interrelated and can contribute to selection of another process or material for use in many applications.

The typical problems encountered with processing time revolve around cost and epoxy drying. The industry push today is to enable full line entitlement by maximizing the number of units on a strip. As lead frame sizes grow toward 100mm by 300mm and silicon and package sizes for analog shrink to 1x1mm and below, we are creating situations that enable 23,000-25,000 packages on a lead frame strip. This situation has created many problems from an equipment and materials process window standpoint. The equipment industry first started to add multiple dispense heads to account for the need for quicker processing, but the problem of the epoxy drying before die placement still is a common, material-dependent challenge that has had very little materials adaptability.

The second time factor is equipment throughput. As dispense times increase, it

Figure 3: Typical epoxy die attach dispense patterns.

frequently reaches a point where the placement station is waiting for the dispense station to complete its operations. When this occurs, the equipment output takes a dramatic hit on sprint parts per minute. This directly ties to factory efficiency, number of machines needed, and ultimately to operational cost for producing the product.

These two factors discussed above have driven development and implementation of new materials focused on eliminating drying on small die as well as the output impact that develops when we have large lead frames and small components.

Lastly, as die size and thickness decrease, process controls become more challenging with dispense epoxies. The placement and rotation of small units combined with parallelism create downstream problems that significantly impact line quality. The new materials target bond line thickness variation, as well as rotation problems between placement and die attach cure processing.

Eutectic die attach. The eutectic die attach process is also one that has been around the industry for a very long time. It was used in semiconductor processing for the first transistors and semiconductor devices. It is also used for high-volume output on products because of its ease of use and process efficiency. The eutectic process utilizes a high temperature (up to 460°C) to form a silicon-gold eutectic bond. The bond process typically uses a high-frequency scrubbing motion during placement to increase the development of intermetallic formation between the chip and the substrate. This is a strong bond that eliminates the need for a post-die attach curing step.

The disadvantage of using the eutectic die attach process is typically experienced on cost-sensitive parts and temperature-sensitive products. In most cases, the backside metal is applied to the wafer and this process greatly increases the die cost. The second cost factor is use of highly specialized bonding equipment. In some cases, the process requires forming a gas atmosphere (nitrogen/hydrogen combination) to prevent oxidation at the high bonding temperatures of the lead frame, or, as in the case of metallized backsides, the wafer material as well.

Output of this process combination can be high on the specialized die attach machines, and many utilize reel-to-reel set-ups to additionally increase factory capacity and to reduce process labor cost on highly cost-sensitive devices. This high-volume, low-cost operation with little device changeover can quickly recover the additional cost-of-use for wafer backside metal treatments and benefit bottom line cost numbers.

Spin coat die attach. The spin coat die attach process, outlined in Figure 4, uses a material that is sprayed or poured onto the wafer backside during a spin process with UV cured in place. The equipment takes a wafer from the grind cassette, performs application and UV cure, and then places the wafer back into the cassette for the next processing step. The materials for this process have been noted to be cheaper in cost to other materials and processes today. Many people are strongly looking at this application, its advantages, and how it fits into the strategy for cost reductions and ongoing die size reductions.

The advantages gained with spin coating is that the cure or "c-stage' process is completed on the spin tool and eliminates the need for bake cycles and equipment. Yet another advantage is the ability to utilize back grind tape to enable handling of thin wafers during processing in/

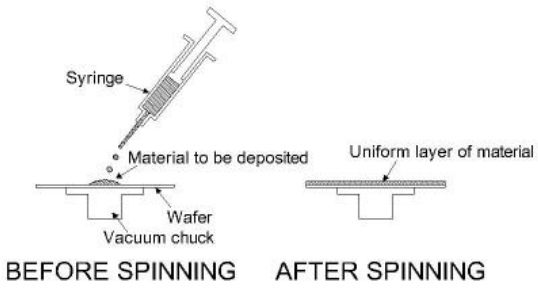

Figure 4: A typical spin coat die attach process.

out of the wafer cassette. This eliminates complications with other material choices and the utilization of very thin wafers for processing. It enables a roadmap for even thinner die development and handling to minimize cost and warpage concerns.

The disadvantages of spin coating include the need for back grind tape to be in place for spin coating, as the spindle system must make contact with the active side of the wafer in order to expose the backside to the coating process. If tape was not in place, the risk for damage to circuitry would be high. Another disadvantage is uneven coating created by material and process interactions that are very difficult to control and establish. Material control and coating evenness is affected by material shelf life, equipment capabilities and environment inputs. All inputs make this technology difficult to control on a long term production basis. When materials and standards are in place, this method will be more widely adopted.

Screen print coat die attach. The screen print coat die attach process uses a material that is stencil-printed onto the backside of the wafer with specialized circuit board screen printing equipment adapted for use with wafers. The equipment takes a wafer from the grind cassette with/without back grind tape still applied. The material is screen-printed onto the backside and put back into the wafer cassette wet. The printed wafers are put into a bake oven to partially cure or 'b-stage' the material onto the backside.

The advantages with screen print materials are that they can be applied in thick, even coatings and enable good bond line control on a long-term basis. They also offer ease of material selection, as both conductive and nonconductive materials are readily available for screen printing in many formulations and material compositions.

The disadvantages of using screen printing include uneven material cure and flow on the backside. A perimeter ring of uncoated wafer for wafer handling, as shown in Figure 5, can create issues during later processes; additionally, wet handling during the cure process step is a major concern. The handling for very thin wafers is a challenge because back grind tape must be removed, in most cases, to allow for bake processing. Adding a heat resistant back grind tape is an option for processing issues, but it adds cost

Figure 5: A perimeter ring of uncoated wafer being used in a screen print coating die attach process.

to the process flow. As specialized transport improves and wafers become thinner, this may be a future roadmap process for use.

Die attach film (DAF) coat die attach. The die attach film (DAF) coat die attach process uses a material that is integrated into the dicing tape and is typically applied using an inline back grinding system after the grind process. This material is in a laminated sheet, and it is typically cut to wafer diameter or is provided in precut format. New materials development enables both conductive and non-conductive versions for use in semiconductor processing.

The advantages of DAF include the ability to handle wafers down to ultra-thin levels with an inline type back grinding system with output on saw-ready frames. Additional advantages include reduction in handling between processing steps (including yield loss and labor), increased line throughput eliminating bake cycles, and a slight capital cost advantage of purchasing an inline back grind system eliminating the need for other processing equipment purchases and more floor space.

The disadvantages have been limited to a few areas. The first disadvantage is the shorting issues caused post-placement due to silicon splintering from the wafer dicing operations. The splinters that are generated attach themselves to the corner of the chips and cause a short from the die backside to ground, thereby creating electrical leakage within the parts. The second disadvantage is the decreased wire bonding process window on parameters. This window is even tighter on copper wire bonding processes, with the key contributor being lead bouncing during the bonding process.

Is cost really a factor?

Cost is always a topic of discussion. The inputs are more than just a material selection method. The material cost varies greatly among the various solutions mentioned above, but selection based merely on material cost may actually end up putting you in the situation of highest cost process flow. Direct materials, equipment, labor, indirect materials, yield, and finally, factory space, must be taken into account for determining the best path forward on any selection process.

In a few cases, the highest cost material enables a lower overall cost of process. This is justified by labor elimination and equipment depreciation reduction upon capital purchased for the factory. This situation proves it is important to weigh all options and understand materials, equipment and flows before making any materials decisions.

Summary

Die attach processing and material selection are critical to small/thin die challenges that continue to evolve. Many choices have grown out of the need for improvement and to solve problems from going smaller and thinner. This article provides information needed to understand the options and paths that enable a well informed selection. The pros and cons of each particular material selection need to be weighed against the factory operating cost to obtain the best selection path. Unfortunately, the analysis cannot be generally applied to all cases and each factory must look at all options to make the best selection possible.

Biography

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INDUSTRY NEWS

3D Architectures for Semiconductor Integration and Packaging

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Nov. 13	Professional Tutorials **T1:** Wafer Level Packaging for MEMS and Microsystems Challenges and Opportunities, **T2:** Wafer Level-Chip Scale Packaging (WL-CSP), **T3:** 3D IC Integration and Packaging, **T4:** Achieving High Reliability for Lead-Free Solder Joints — Materials Consideration

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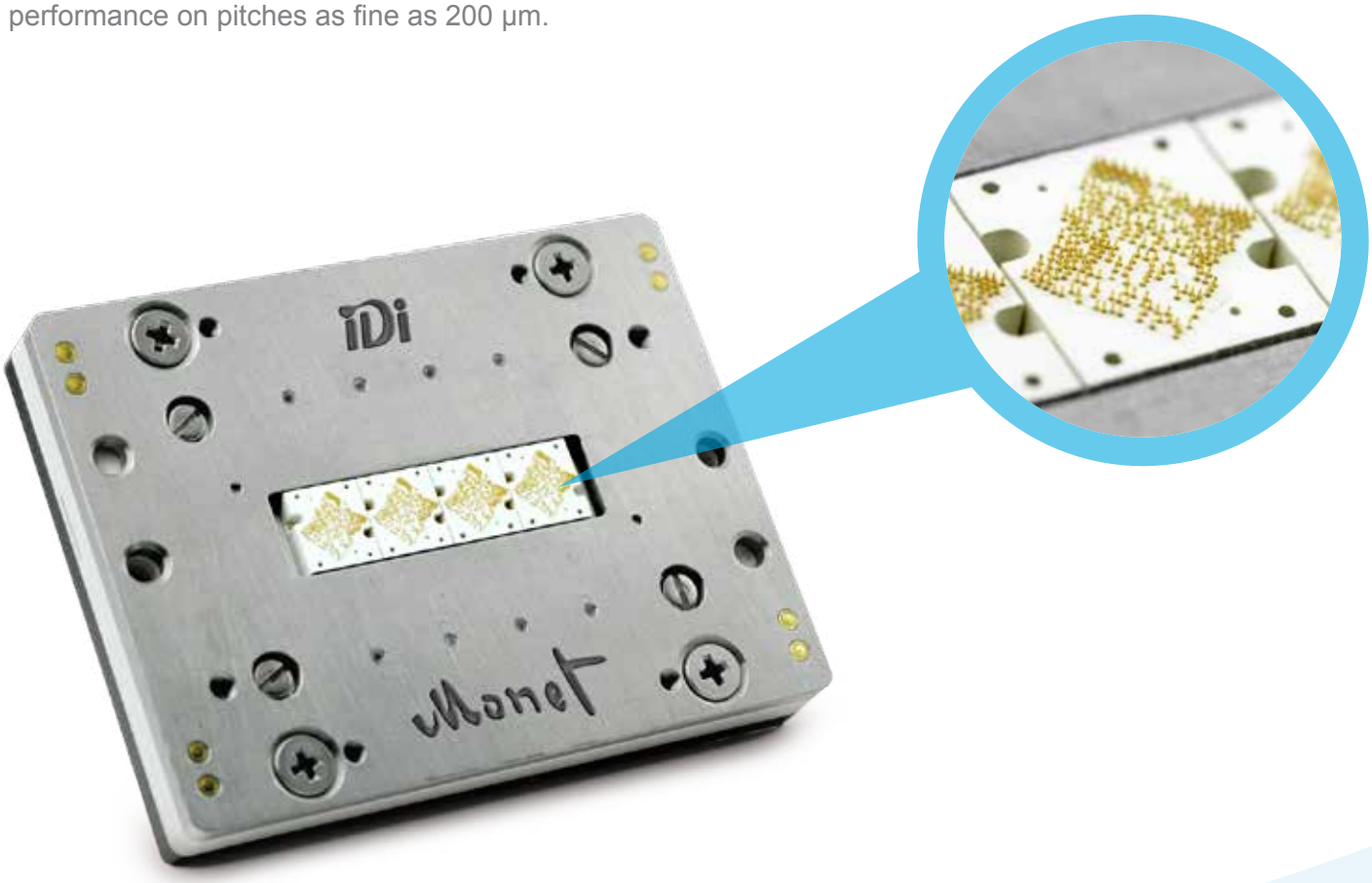

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