DfR Solutions
reliability designed, reliability delivered

Thermal Cycling and Fatigue

Gil Sharon

9000 Virginia Manor Rd Ste 290, Beltsville MD 20705 | Phone: (301) 474-0607 | Fax: (866) 247-9457 | www.dfrsolutions.com

Introduction

The majority of electronic failures are thermo-mechanically related by thermally induced stresses and strains. The excessive difference in coefficients of thermal expansion between the components and the board cause a large enough strain in solder and embedded copper structures to induce a fatigue failure mode. In this paper we will present the solder fatigue failure mechanism and the PTH fatigue failure. The solder fatigue failure is more complicated due to the many solder materials and different solder shapes. One example of solder fatigue occurrence is a ball grid array (BGA) solder ball. The following figure shows a cross section of a solder ball with the corresponding finite element model. The predicted location of maximum strain corresponds to the same location of solder fatigue crack initiation.

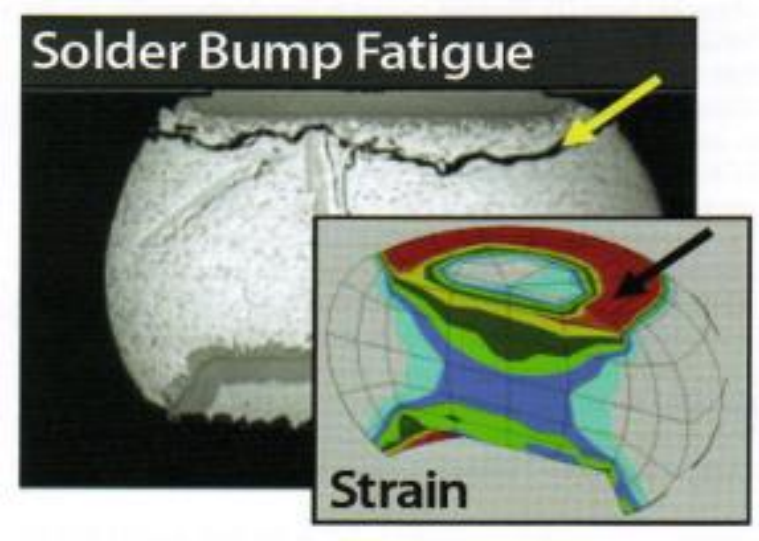

Figure 1: BGA solder ball fatigue fracture and corresponding FEA model of fracture

Any time two materials are connected to one another there is a potential for CTE mismatch to occur in electronics assemblies. Some of these CTE mismatch interactions can be quite complicated due to the changing properties of material, complex geometries, competing material behaviors and so on. For example, the 1st level interconnects called C4 "bumps" connect a flip chip die to substrate. They have many options that affect the solder fatigue behavior. They can be underfilled, corner depopulated and shaped by solder mask to name a few. In this case both the global CTE mismatch between the die and substrate need to be considered as well as the local CTE mismatch between the underfill and C4 solder bump. This failure mode is part of the "package level" reliability prediction and is separate from "board level" reliability.

All the packages components or structures that are soldered directly to the board can be considered 2nd level interconnects. In the BGA example discussed above, this would relate to the C5 "Balls" that connect the bottom of the substrate to printed circuit board (PCB). Here too, the

board level reliability predictions are complicated by several mitigation techniques, conformal coatings, heat sinks etc. While BGAs are some of the more complicated components that can suffer from solder fatigue, other components that are much simpler are not immune.

The simplest form of CTE mismatch can be considered in order to illustrate the effect on solder fatigue. In the following figure the component is connected to the board with two solder joints. The component and the board are infinitely rigid, the solder joins are symmetric to the component and the CTE of the board is larger than that of the component. In the stress free or "neutral" state, the solder joint is not subjected to any strain. If the temperature is elevated from the neutral state then the board (higher CTE) will expand more than the component (lower CTE) and the solder joints will be have a strain applied to them. If the temperature is decreased from the neutral state then the board will contract more than the component and the solder joints will again have a strain applied to them. It is clear than any time the temperature changes the solder joint is being stretched one way or another. The neutral point remains at the line of symmetry of the component. The distance from the neutral point to the solder joint is called the "distance to neutral point" (DNP). For most cases, the global CTE mismatch will have a larger effect on components with larger DNP

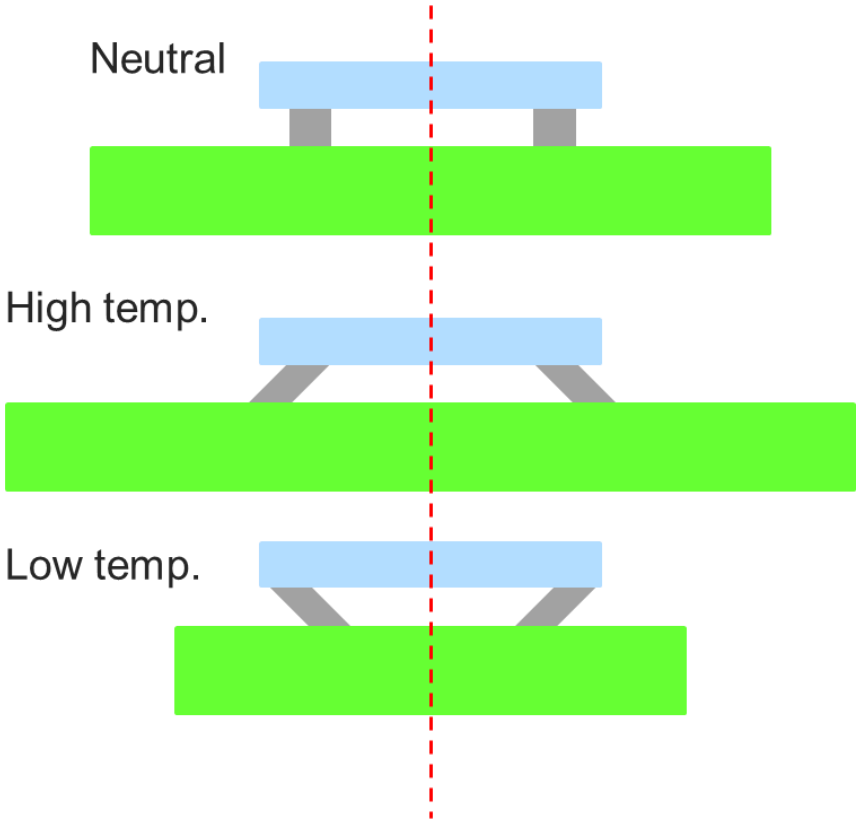

Figure 2: Effect of CTE mismatch on solder joint strains.

Field Conditions

The figure above shows that the temperature changes in electronics assemblies are a critical part of the fatigue prediction and not just the component shape or quality. To understand the types of loads that an assembly might go through in its intended life we should consider the various temperature cycles in the field. Field conditions can be different for different usage and applications even for the same product. Every industry segment has a characteristic service life and usage conditions as shown in the following table.

	Temp range	Cycles/year	Service time	Failure rate
Consumer	0 to 60 °C	365	1 year	1 %
Computer	15 to 60 °C	1460	5 years	0.1 %
Telecom	-40 to 85 °C	365	7 to 20 years	0.01 %
Aircraft	-55 to 95 °C	365	20 years	0.001 %
Automotive	-55 to 95 °C	100	10 years	0.1 %

Table 1: Field conditions for various industries

The list in this table is far from comprehensive. Specific applications will have detailed specifications. In some products there will be different requirements for different life phases. The acceptable failure rates in each industry segment also vary widely and can cause a significant difference in product design. It is also possible that in the same product there will be electronics assemblies with different thermal loads for eexample: the LCD touch panels, voltage regulators and networking module of a laptop can be at different temperatures at the same time. In some cases it is possible for special field conditions to exist. Some products will see a long period of storage followed by short period of usage, such as: smart munitions, launch platforms, AEDs and airbags. In these products, the majority of life is spent in an inactive state punctuated by short usage periods of critical importance. The electronics would need to survive for many years and be reliable at the end. A good design would need to consider all the life phases of the product.

Accelerating life tests

It is prohibitively expensive to test an electronics assembly for 20 years at 1 cycle/day. It is better to validate the product reliability in some way as early as possible in the design phase. The life test time can be contracted from several years to several weeks or days. For example: a product that sees one cycle per day for 1000 days can be tested in six weeks (15 minute ramps and 15 minute dwells = 24/cycles per day). Life tests can also be accelerated by applying stresses that are beyond normal life while maintaining the same dominant failure mode. The elevated stress can be achieved by applying a higher temperature and higher load. There can be some limitations

to how much a life test can be accelerated because competing failure modes can exist in an assembly. Accelerating the test can result in different failure modes to appear. An accelerated life test may be valid even if another failure mode appears side by side with the desired one. The following table shows an example of a JEDEC standard with equivalent conditions that far exceed the use conditions.

Use Condition	Use Condition Requirement	Equivalent Condition B -55 °C to +125 °C 700 cycles	Equivalent Condition G -40 °C to +125 °C 850 cycles	Equivalent Condition J 0 °C to +100 °C 2300 cycles
Desktop 5 yr Life	ΔT 40 °C 2000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15 °C 1500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr Life	ΔT 40 °C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr Life	ΔT 25 °C 5500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr Life	ΔT 6 °C 5500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year Life	ΔT 30 °C 3000 cy	25,200 cy	25,712 cy	25,557 cy

Table 2: Table of equivalent conditions examples used in accelerated tests (JEDEC standard 47G)

There are limits on how much a temperature cycle can be accelerated. These limits can be related to melting temperature of the solder alloy, glass transition temperatures of the laminate or underfill and others. Performing accelerated life tests may add complications and may require additional steps to validate that the failure mode in the accelerated test is the same as the usage condition.

Controlling the Coefficient of Thermal Expansion

It is unlikely that the designer or end user will be able to influence the component properties because component packaging is typically driven by package level reliability. Complex components may also need to pass package level qualification tests. There may also be a limited number of options for materials at the component level. It is more likely that a board designer will be able to control the PCB properties such as: glass style, laminate type, copper thickness and board thickness.

Printed circuit boards in the past had effective CTE values close to that of copper (17.6 ppm/°C). The components that are connected to the PCB can have a wide range of effective CTEs. The prevalence of leadless packages with stiffer leads means that more components are susceptible to CTE mismatch. There are also an increasing number of larger packages that have a larger CTE mismatch effect. The CTE of laminates is decreasing, but the PCB laminate manufacturers do not make it easy to determine the CTE of their laminate. Low CTE laminates have their own set of problems. There is also a tradeoff between low CTE and cost.

A realistic target for board CTE is between 15 and 17 ppm/°C. Most laminate suppliers only provide CTE values for the in-plane direction as shown in the following table.

370HR	
Property	Typical Value
Glass Transition Temperature (Tg) by DSC, spec minimum	180
CTE, Z Axis Pre-Tg	45
CTE, Z Axis Post-Tg	230
CTE, X, Y Axes Pre-Tg	13-14
CTE, X, Y Axes Post-Tg	14-17

Table 3: Example of laminate properties provided by manufacturer

These values are typical for a low resin content laminate (46%-50% resin content by weight, 7628 glass style) however the most popular laminates have much higher resin contents. Higher resin content corresponds to a higher CTE and lower modulus. It is possible to calculate the laminate modulus by taking the resin modulus and adding the glass content in the calculation. For example: FR-4 boards have fibers oriented in both X and Y direction as shown in the figure below.

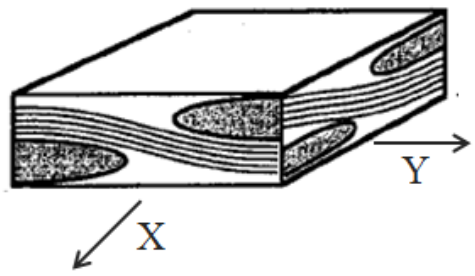

Figure 3: Glass fiber weave illustration showing the X and Y fiber orientation

We can back calculate the resin Modulus (Em) from the in-plane Moduli (Ex and Ey) assuming that half the fibers are oriented in the X direction and half in the Y direction. The in-plane modulus is calculated in the following equation.

$$E_{x,y} = \frac{V_f E_f}{2} + V_m E_m + \left(\frac{V_f}{2E_f} + \frac{V_m}{E_m} \right)^{-1}$$

Equation 1: In-Plane Modulus calculation for FR-4 laminate

In the equation shown above we can solve for Em as shown below. The positive value for Em from the equation corresponds to the resin modulus.

$$E_m = \frac{-\left(V_f{}^2 E_f + 4V_m{}^2 E_f + 4E_f - 2V_f E_{x,y}\right) \pm \sqrt{\left(V_f{}^2 E_f + 4V_m{}^2 E_f + 4E_f - 2V_f E_{x,y}\right)^2 - 4(2V_m V_f)(2\,V_m V_f\; E_f{}^2 - 4V_m E_f E_{x,y})}}{2(2V_m V_f)}$$

Equation 2: Resin modulus value calculated from in-plane modulus values

These two equations show that the glass style has an effect on the resulting material properties. We can consider a variety of glass styles and consider their resin content by weight percent and volume percent as shown in the table below.

Glass Style	Resin Content [Weight %]	Resin Content [Vol %]
1027	75%	86%
1037	75%	86%
106	72%	84%
1067	71%	84%
1035	70%	83%
1078	68%	82%
1080	64%	79%
1086	63%	78%
2313	57%	74%
2113	55%	72%
2116	54%	71%
3313	54%	71%
3070	50%	68%
1647	48%	66%
1651	48%	66%
2165	48%	66%
2157	48%	66%
7628	48%	64%

Table 4: List of glass styles and their resin contents

Using the previous calculations for each of these glass styles we can identify a couple of trends. Modulus decreases and CTE increases as resin content increases, as shown in the chart below.

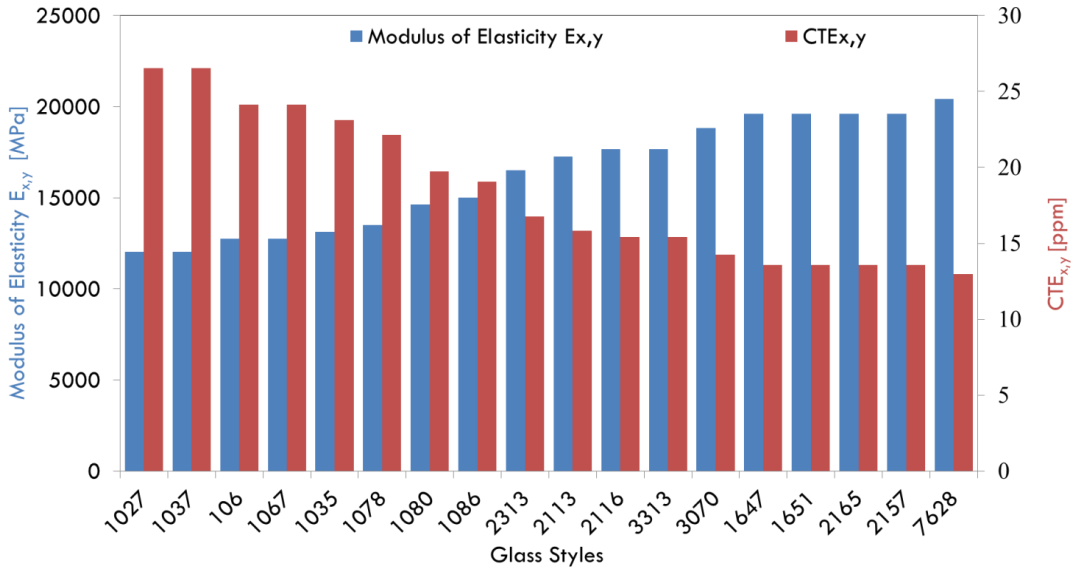

Table 5: Calculated Moduli and CTEs for different glass styles

Copper content can also play a significant role in PCB properties. The board designer can take the layer stackup with the copper content in each layer and calculate the effective CTE for the board. The original model shown in
Figure 2 can be modified to add the board and component properties. These properties can be used in solder joint fatigue predictions.

Solder Fatigue and Grain Structures

Solder joints are made of more than solder. Solder joints are connected to the PCB with a solder pad that can be made of several alloys and have various finishes. The component termination can also have different types of materials. A basic solder joints construction once the joint is completed will have:

1. Base metal at PWB
2. IMC solid solutions between the solder and the PWB base metal
3. Layer of solder that has been depleted due to IMC formation
4. Bulk solder grain structure
5. Layer of solder that has been depleted due to IMC formation
6. IMC solid solutions between the solder and the component base metal
7. Base metal at component termination

Each part of the solder joint will be affected by the thermos-mechanical loads in a different way. Solder fatigue in thermal cycling in caused by grain growth. When the solder joint is formed at high temperature it is in a stress-free state. Some residual stresses will build in the solder due to the CTE mismatch as the assembly cools. These residual stresses will relax by creep mechanism. Stresses from the CTE mismatch during thermo-cycling will contribute to grain growth. At higher temperatures the grains will grow faster.

The amount of stress in the solder will vary according to the lead and solder shape. The three types of leads are typically “super compliant”, “compliant” and “non-compliant” leads. There is less stress in the solder joint for components with more compliant leads. Leadless components can have solder joints with or without a fillet. Examples for components with a fillet are chip resistors, chip capacitors Metal Electrode Leadless Face (MELF) and leadless chip carriers. Examples of components without a fillet are Flip-Chip C4 (Controlled Collapse Chip Connection), BGAs C5 (Controlled Collapse Chip Carrier Connection) and CGA (Column Grid Array). The different surface mount attachment types can have significantly different failure modes depending on how the load is distributed in the joint. In the case of uniform load distributions (For example: BGA) the crack formation mechanism is shown in the following figure.

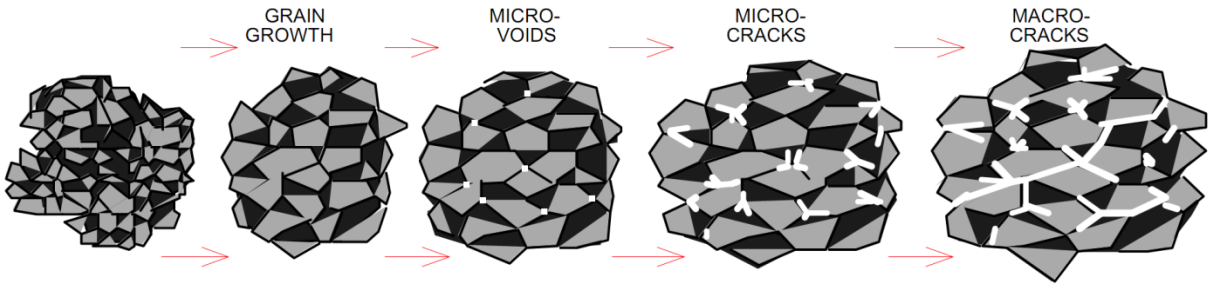

Figure 4: Solder fatigue crack formation in solder joints with uniform loads

From the original solder joint (left) the grains will grow as the solder joint is stressed. The growing grains will cause micro-voids to appear on the grain boundaries. The micro-voids will connect with each other to create micro-cracks and eventually macro-cracks. If the load is distributed evenly across the joint this will happen everywhere at the same time. In BGA balls this will happen in an entire layer of the bulk solder. If the load is not even then the grain growth and micro cracks are formed in the stress concentration and the micro-crack is advancing along a crack path.

The speed of crack formation and propagation in the solder can be modeled. One way to predict the solder fatigue is to use a modification of the Engelmaier model. The Engelmaier model is a semi-empirical analytical approach that calculates fatigue using energy method. The following equation gives the calculation to determine the strain range ($\Delta\gamma$) where C is a correction factor (function of activation energy, temperature and dwell time), $\Delta\alpha$ is the CTE difference, h_s is solder joint height (defaults to 0.1016 mm or 5 mils), ΔT is the temperature cycle and L_D is the maximum diagonal distance between solder joints

$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T$$

Equation 3: Strain range ($\Delta\gamma$) equation for solder fatigue model

Next we use the following equation to determine the shear force applied to the solder joint. The equation considers the PCB and bond pad stiffness and both shear and axial loads. It also considers the lead stiffness for leaded components. Where F is the shear force L_D is length, E is elastic modulus, A is the area, h is solder thickness, G is shear modulus, and a is edge length of bond pad and the subscripts are: [1] for component, [2] for board, [s] for solder joint, [c] for bond pad, and [b] for board

$$(\alpha_2 - \alpha_1)\cdot\Delta T\cdot L_D = F\cdot\left(\frac{L_D}{E_1A_1}+\frac{L_D}{E_2A_2}+\frac{h_s}{A_sG_s}+\frac{h_c}{A_cG_c}+\left(\frac{2-\nu}{9\cdot G_b a}\right)\right)$$

Equation 4: Equation to determine the shear force applied to the solder joint

Using the strain range and shear force we can calculate the strain energy dissipated by the solder joint using
Equation 5 and calculate the number of cycles-to-failure (Nf), using energy based fatigue models for SAC developed by Ahmer Syed (Amkor technology) or the model for SnPb

$$\Delta W = 0.5\cdot\Delta\gamma\cdot\frac{F}{A_s}$$

Equation 5: Strain energy dissipated in the solder joint

$$N_f = \left(0.0019\cdot\Delta W\right)^{-1}$$

Equation 6: Syed model for SAC solder fatigue model

$$N_f = \left(0.0006061\cdot\Delta W\right)^{-1}$$

Equation 7: Energy based fatigue models for SnPb solder fatigue

Using this method we can compare the fatigue behavior calculations for an example component. The following figure shows the fatigue life of a 2512 Resistor using the different glass styles from
Table 4 and two thicknesses of boards. The resistor is a low CTE part (Alumina 5.6 ppm/°C) mounted with filleted solder joints. The predicted fatigue life of the component is higher for thinner boards. This highlights why some component manufactures prefer to test on thin laminates

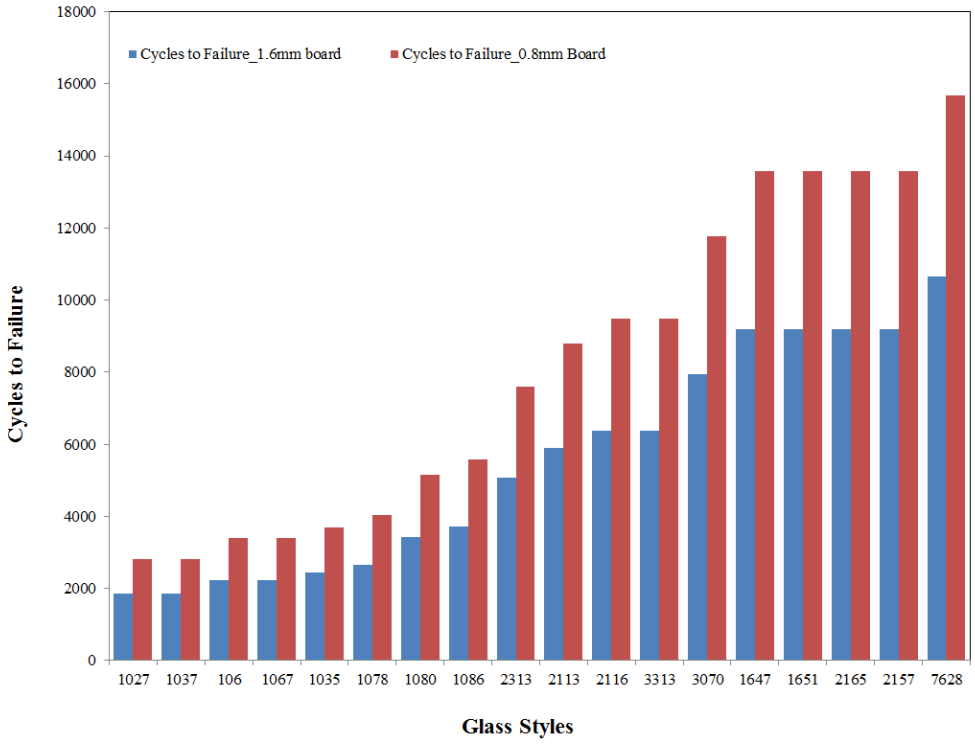

Figure 5: Fatigue life of a 2512 resistor mounted on a PCB with different glass style and two thicknesses

This method also works to predict the life of leaded components as shown in the following figure. In this example: TSOP type devices with two different lead alloys (Copper and Alloy 42) were tested to failure. A comparison is made to the calculated number of cycles to failure.

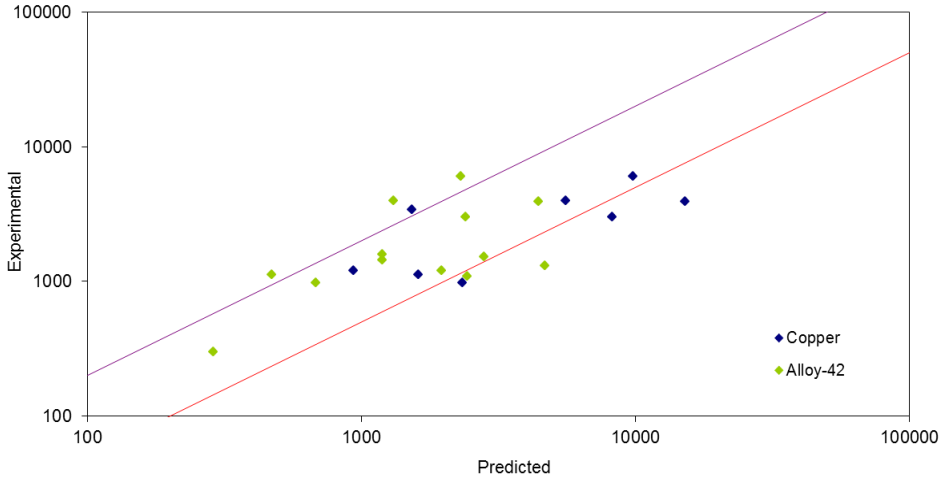

Figure 6: Correlation between solder fatigue model and experimental results

It is possible to use analytical energy based methods to predict some solder fatigue behavior. The solder fatigue model is far from comprehensive. The model does not account for complex mounting conditions such as underfilled components.

SnPb and SAC Solder Alloys

There are many solders that can be used in electronics. The two most common ones are Tin-Lead (Sn63Pb37) and Lead-Free (SnAgCu or SAC) solders. They have different grain structures and different fatigue behavior. Tin Lead solder typically performs better under high stress conditions found in large ceramic devices (stiffer parts) and large changes in temperature (higher strains). Due to RoHS regulations most high performance parts are manufactured with Pb-free alloys. SAC alloys tend to do better for moderate thermal cycles. The following chart shows a comparison of SnPb and Pb-free solders for different components.

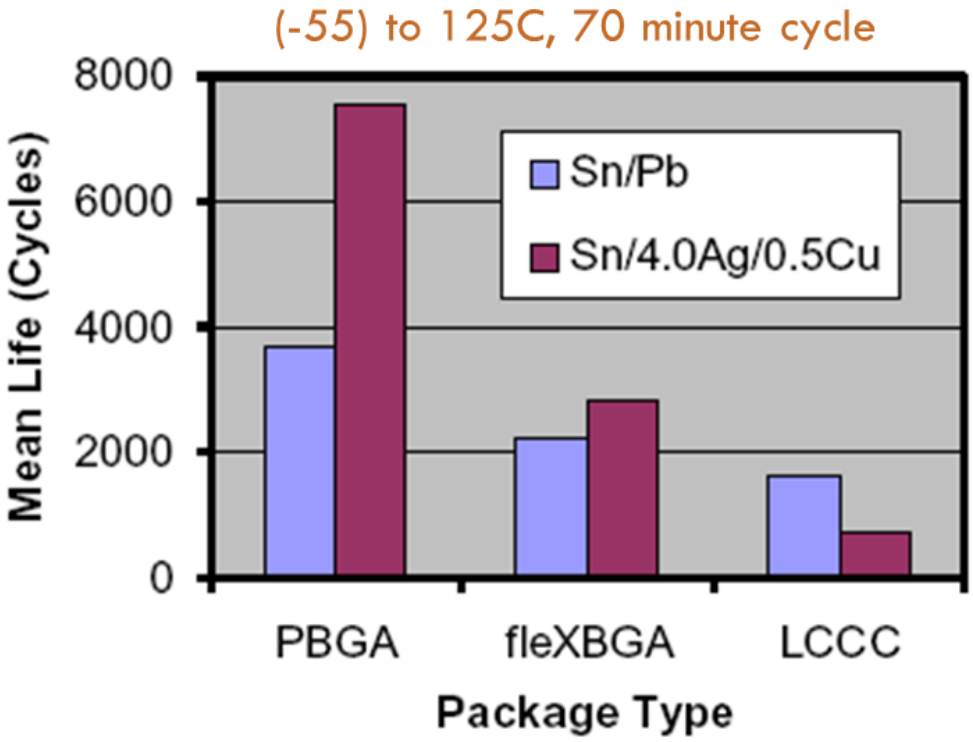

Figure 7: Comparison of SnPb and Pb-free solder performance of three components

The Pb-free solder will perform better than SnPb for the more compliant components. The performance of both solders is decreased for stiffer components but the Pb-free solder suffers a larger decrease in life than the SnPb solder. The dependence of solder performance on the ΔT is not captured because in this example the temperature difference for all three components was

from (-55)°C to 125°C. At smaller temperature differences the Pb-free solder seems better if we look at the same component with bot solder types and vary the ΔT. In the next two figures we plot the time to 1% failure of resistors and TSOP devices attached with SnPb solder (shown in red) and two types of Pb-free solders (dashed lines).

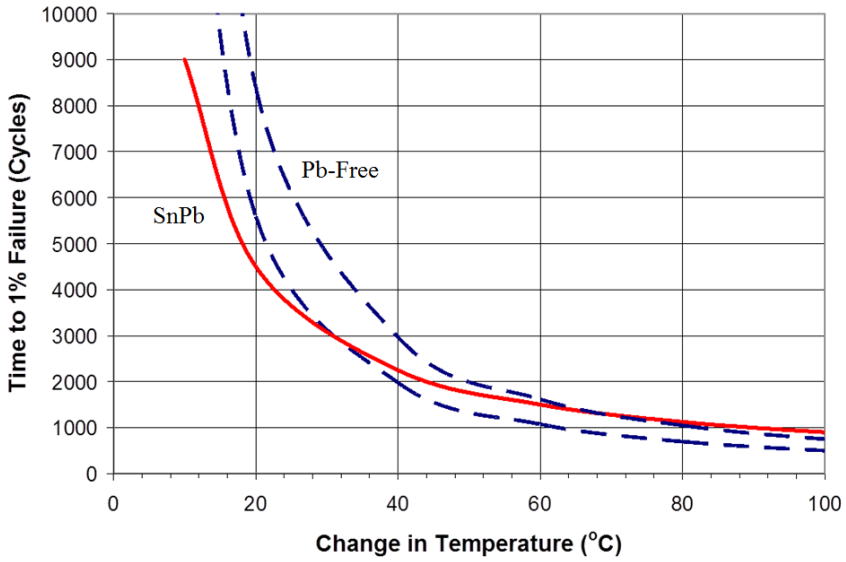

Figure 8: Time to 1% failure for 2512 resistors attached with SAC and SnPb solder with long dwells (~8 hours)

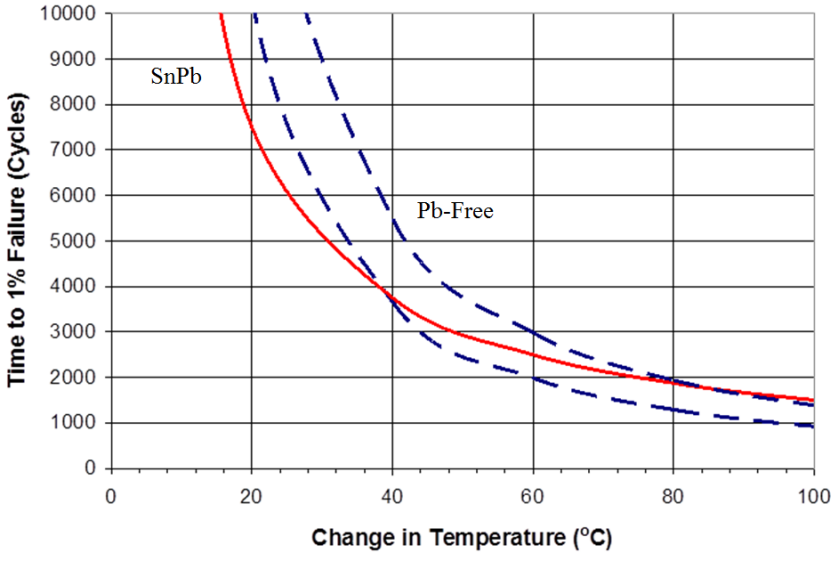

Figure 9: Time to 1% failure for TSOPs attached with SAC and SnPb solder with long dwells (~8 hours)

It can be seen that at small changes in temperature the SnPb will fail first but perform better at higher temperature changes. The solder fatigue failure mode is one of the most dominant ones in electronics. The RoHS legislation and the move to Pb-free solders means that board designers need to account for solder fatigue at the design phase.

Plated Through Hole Fatigue

Choosing the correct laminate material is also critical to the performance of embedded components not just soldered components. The most common embedded component in a PCB is a plated through hole (PTH) or plated through via (PTV). PTHs serve as conductive conduits from one layer of the board to another. They are created by drilling a hole in the board and plating a conductive material inside the hole. There are many flavors of drill diameters, plating thicknesses and materials that can be used in PCBs.

In temperature cycling, the expansion and contraction in the out of plane (z) direction is much higher than that in the in-plane (x-y) direction. The glass fibers constrain the board in the x-y plane but not through the thickness. As a result, stress can be built up in the PTH barrel and eventually cracking occurs near the center of the barrel. The picture below shows a cross section of a PTH without a failure.

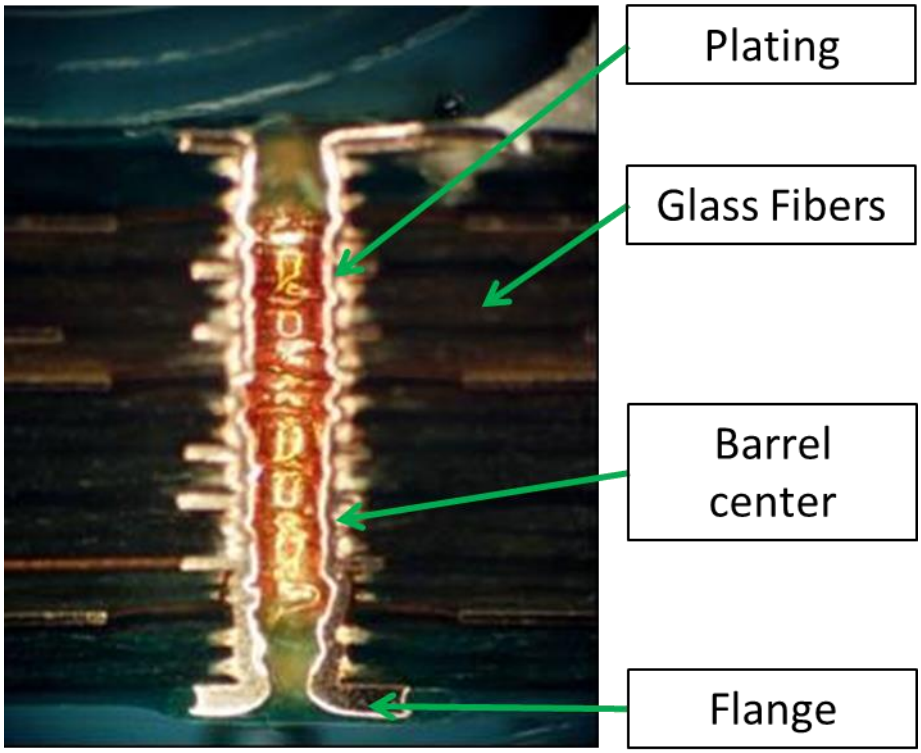

Figure 10: Anatomy of a plated through hole

While there is a tendency for plating to crack towards the center of the barrel it is possible for cracks to appear in other places in the PTH. Several cross sections of cracks in PTH are shown in the following figure. One of the difficult aspects of finding a PTH crack is that the failure is detected when the board is at high temperature. When the board is then tested for faults at room temperature the fault is not found because the board has shrunk and the two sides of the crack are touching.

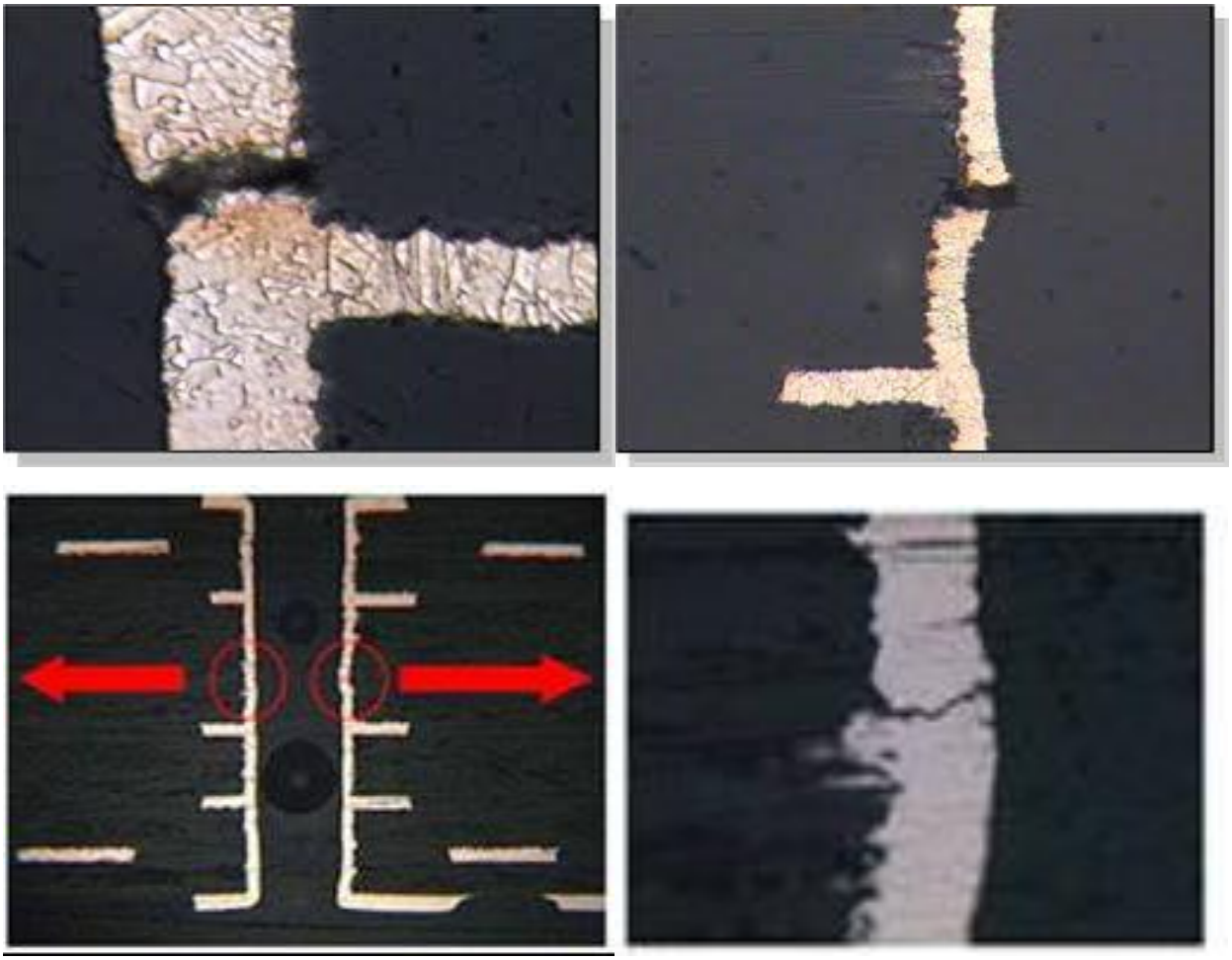

Figure 11: Cross sections showing cracks in plated through holes

There is an industry accepted failure model outlined in IPC-TR-579 (Round Robin Reliability Evaluation of Small Diameter Plated-Through Holes in Printed Wiring Boards) in order to predict the appearance of cracks in PTH. This model assumes perfectly elastic deformation when below yield strength (σ_y or S_y) and a linear stress-strain relationship during the failure occurrence. The following equations are used to determine stress applied (σ). The plating material used in this example is Copper but any plating material that follows the assumptions will work as well.

$$\sigma = \frac{(\alpha_E - \alpha_{Cu})\Delta T A_E E_E E_{Cu}}{A_E E_E + A_{Cu} E_{Cu}}, \text{for } \sigma \le S_y$$

$$\sigma = \frac{\left[(\alpha_E - \alpha_{Cu})\Delta T + S_y \frac{E_{Cu} - E'_{Cu}}{E_{Cu} E'_{Cu}}\right] A_E E_E E'_{Cu}}{A_E E_E + A_{Cu} E'_{Cu}}, \text{for } \sigma > S_y$$

$$A_E = \frac{\pi}{4}\left[(h + d)^2 - d^2\right]$$

$$A_{Cu} = \frac{\pi}{4}\left[d^2 - (d - 2t)^2\right]$$

Equation 8: Determination of applied stress according to IPC-TR-579

We then use the stress value to determine strain range ($\Delta\varepsilon$) as shown in the equations below.

$$\Delta\varepsilon = \frac{\sigma}{E_{Cu}}, \text{for } \sigma < S_y$$

$$\Delta\varepsilon = \frac{S_y}{E_{Cu}} + \frac{\sigma - S_y}{E'_{Cu}}, \text{for } \sigma > S_y$$

Equation 9: Strain rage equations according to IPC-TR-579

A calibration factor is applied based on the quality index (K_Q~0 to 10) and strain distribution factor (K_d~2.5-5.0) to find the "effective" strain range.

$$\Delta\varepsilon_{eff} = \Delta\varepsilon\left(K_d \frac{10}{K_Q}\right)$$

Equation 10: Effective strain rate calculation

The number of cycles-to-failure (N_f) can be calculated

$$N_f^{-0.6} D_f^{0.75} + 0.9\frac{S_u}{E}\left[\frac{\exp(D_f)}{0.36}\right]^{0.1785\log\frac{10^5}{N_f}} - \Delta\varepsilon = 0$$

Equation 11: Number of cycles to failure of a PTH

The IPC-TR-579 standard is based on round-robin testing of 200,000 PTHs performed between 1986 to 1988 with hole diameters ranging from 250 µm to 500 µm, board thicknesses from 0.75 mm to 2.25 mm and plating thicknesses from 20 µm to 32 µm. The advantage of this standard is that it is a straightforward analytical calculation that is validated through extensive testing. The main disadvantage of this standard is that the validation data is 20 years old. It also can't handle complex geometries of PTH spacing and PTH pads that can change the lifetime. It can be a bit difficult to assess the effect of multiple temperature cycles but using Miner's rule it is possible.

It is impossible to eliminate PTH fatigue completely. Better reliability can be achieved if the board laminate and PTH plating material have a close CTE value for the out-of-plane direction. The board glass style and resin can be modified to some degree. Increasing the glass content can help reduce the CTE mismatch but it will be harder to drill the holes into the board. The plating material ductility will also affect the life of the PTH. The predicted numbers of cycles to failure are plotted in the figure below for different glass styles. The plating material, plating thickness, temperature profile and drill diameters are kept the same.

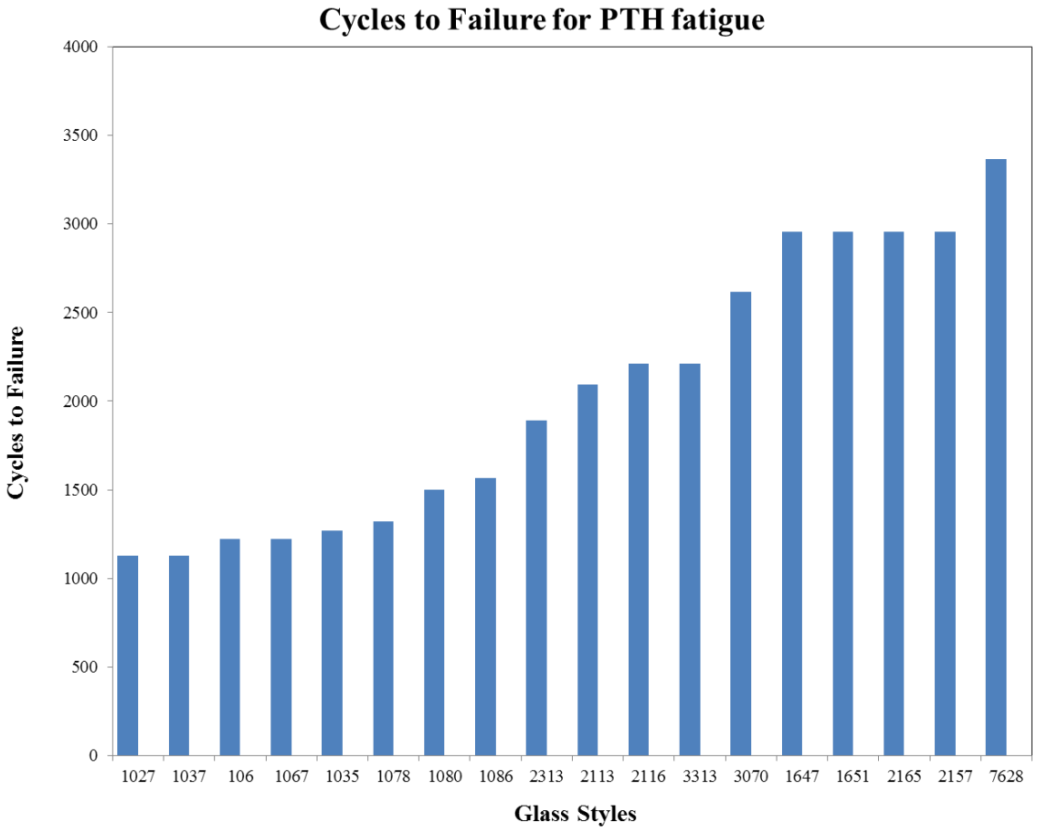

Figure 12: Effect of glass style on PTH fatigue performance

There is a clear trend for the PTH fatigue performance to improve for low CTE and high modulus glass styles but the use of underfills, potting compounds and thick conformal coatings can greatly influence the failure behavior under thermal cycling. Underfills designed for enhancing shock robustness do not tend to enhance thermal cycling robustness. Another consideration that can complicate the calculations is any time a material goes through its glass transition temperature. The analytical computational method will work for most cases where PTH are not soldered or potted.

Summary

The majority of failures in electronics are caused by thermos-mechanical loads. The CTE mismatch between the board, component and attach materials causes stresses in solder and plating material. Solder fatigue is a major failure mechanism. There is a lot of experimental data for solder fatigue predictions. Basic models can be used to predict solder fatigue for surface mount components. Board designers can change component placement and board laminate material to alleviate this problem because component level design is usually not an option. The board laminate design will also affect PTH reliability. PTHs are components that are embedded in the board. The board designer can influence PTH reliability by modifying the drill diameters, laminate material, and plating parameters. Solder and PTH fatigue are just two of the many effects of thermo-mechanical loads but they can be predicted.