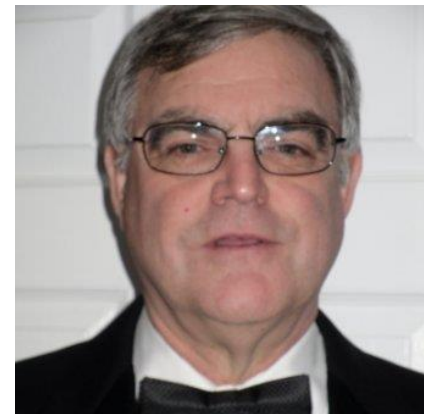


# Test Plan Development: How to do it – Sherlock

Dr. Gil Sharon, [gsharon@dfrsolutions.com](mailto:gsharon@dfrsolutions.com)

# Speaker Bio:

- **Research focus:**
  - Mechanical reliability of electronic systems and components
  - Multidisciplinary reliability of complex electro mechanical systems
  - Characterization and modeling of material behavior
  - Physics of failure of electromechanical and MEMS system
  - Mechanical performance of flip chip packages
- **Doctoral research**
  - Solder reliability
  - MEMS structures characterization
  - Embedded components failure analysis
  - Particle beam accelerator mechanical fatigue.
- **Experience at Amkor technology**
  - Advanced product development group as senior engineer
  - Analysis of chip-package interactions
- **Ph.D, Mechanical Engineering (University of Maryland)**
- **Sales contact: Tom O'Connor [toconnor@dfrsolutions.com](mailto:toconnor@dfrsolutions.com)**



# Question Everything

“I want you to remember that everything I am saying may be wrong and I want you to question everything that I’m saying.”

-Nathan Myhrvold

Formerly Chief Technology Officer at Microsoft

# Agenda

- What is a test plan
  - Test plan strategies
- Physics of failure
  - Field failures
- Test plan elements
- Reliability goals
- Wear out and overstress
- Use environment
- Choosing a test board
- Test methods
  - Temperature cycling
  - Plated through hole fatigue
  - Mechanical vibration
  - Mechanical Shock
  - CAF resistance
- Failure analysis
- Summary and questions
  - But feel free to ask questions in the middle

# What Is A Test Plan?

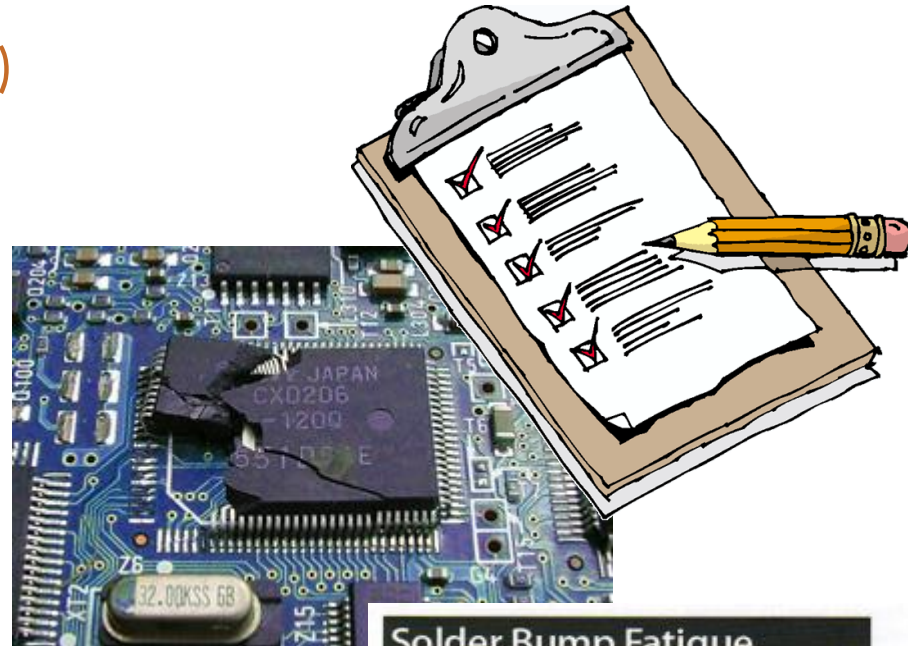
- Test plans are a central part of implementing any new technology
- Test plan is the strategy used to identify the board's ability to succeed
  - For the intended use environment
  - For a specified reliability goal
  - Known failure modes
- Trade off between:
  - Cost of test and simulation
  - Risk
- There are many specifications



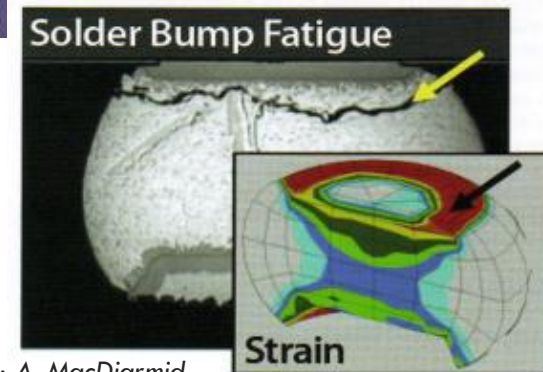
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# Test Plan Strategies

- **Test to “Spec” (Industry standards)**
  - Pass/Fail: Clipboard engineering
  - Uses best practices and previous success
  - Design by similarity
  - Different requirements for every manufacturer or industry
- **Physics of failure (POF) testing**
  - Test to failure
  - Failure analysis for failure mode verification
  - One test per failure mode
  - Creates prediction models that feed back to industry standards
- **Combined approach**
  - Physics of failure prediction
  - Industry standards



Source: nationalparts



Source: A. MacDiarmid,  
“Thermal Cycling Failures”,  
RIAC Journal, Jan., 2011.

# Physics of Failure

- The use of science (physics, chemistry, etc.) to capture an understanding of failure mechanisms and evaluate useful life under actual operating conditions
- Using PoF, design, perform, and interpret the results of accelerated life tests
  - Starting at design stage
  - Continuing throughout the lifecycle of the product
- Start with standard industry specifications
  - Modify or exceed them
  - Tailor test strategies specifically for individual board design and materials
  - Consider the use environment and reliability needs

# Clipboard Engineering Is Not Enough

- **Limited failure mechanism specific testing**
  - Only performed at transition to new technology nodes
  - Mechanism-specific coupons (not real boards)
  - Test data is hidden from end-users
- **Questionable JEDEC tests are promoted to OEMs**
  - Limited duration (1,000 hrs) hides wearout behavior
  - Use of simple activation energy
    - Incorrect assumption that all mechanisms are thermally activated
    - Constant failure rate calculation is outdated



# Field Failure of Devices

- **Field failures rates of hardware**
  - Gradual material degradation
  - Rapid or immediate failures
- **Environment stressors**
  - Thermal, Chemical, Moisture, Electrical, Shock...ETC
  - Combination of stresses
  - Probabilistic vs. deterministic
- **Premature failures**
  - Shipping, manufacturing, installation, test ...
- **Gradual failures**
  - Long product life, high cycle count, long term storage...
- **Erratic failures**
  - Mechanical shock, accidental misuse, electrical overstress ...

# Test Plan Elements

- **Type of test objective**
  - Comparison test
    - Option A,B,C ...
  - Qualification
    - Pass/ Fail
  - Validation
    - Sanity check
  - Research
  - Compliance and regulatory
  - Failure analysis
    - Verify failure mode
    - Can be difficult
- **A test without an objective is doomed before it even started**
- **Justification checklist**
  - Define reliability goals
  - Experiment design
  - Materials availability
  - Defined use environment
  - Budget
    - Time and money
  - Sample availability
  - Practicality of test
  - Risk
- **Every test has a risk associated with it**
- **Have a plan for failure**

# Reliability Goals

## ○ Lifetime

- How long does the customer expect the device to perform?
- How long is the warranty? Extended warranty?
- Cost of replacement.
- Should be used in all phases of product qualification

## ○ Performance

- Define the probability of failure during product life
- Actively monitor field returns: perform failure analysis
  - Feedback to refurbishing/redesign
- MTBF and MTTF
  - Only if customer requirement
  - Do not use for design

# Examples of Product Lifetimes

- Low-End Consumer Products (Toys, pedometers, gadgets etc.)
  - Do they ever work?
- Consumer electronics
  - Cell Phones: 18 to 36 months
  - Laptop Computers: 24 to 36 months
  - Desktop Computers: 24 to 60 months
  - Home appliances: 7 to 15 years
- Commercial electronics
  - Medical (External): 5 to 10 years
  - Medical (Internal): 7 years
  - High-End Servers: 7 to 10 years
  - Industrial Controls: 7 to 15 years
- Highly regulated
  - Automotive: 10 to 15 years (warranty)
  - Avionics (Civil): 10 to 20 years
  - Avionics (Military): 10 to 30 years
- Telecommunications: 10 to 30 years
- Solar: 25 years (warranty)

- Can we really define a “standard” use case for an entire industry?
  - Or product?
  - Or board?

# Wear Out and Overstress

- **Wear out mechanisms are the usual culprit for failures**
  - Fatigue and creep are hard to test for correctly
  - Perform failure analysis to verify failure mode
  - We are getting much better at doing this but you can't rush physics
- **What if an overstress failure is detected**
  - Audit suppliers
  - Reevaluate field environments
  - Combined stresses can have an unexpected effect
  - Redesign the test
    - Must be effective for desired failure mode
    - Must be effective for expected use environment

# Defining the Use Environment

- **Shipping**
  - How well is the product protected during shipping?
- **Assembly, test, manufacturing, storage ...**
  - All the things that happen before the product is even turned on
- **Do you have a good understanding of how your customer uses the product?**
  - What about the corner cases?
- **Opinioneeering: Engineering without data**
  - Measured temperatures. Thermal simulation. Previous experience.
  - Mechanical loads: Accelerometer data. Strain gauge. Extensometer
  - Cycle rate data: Software and hardware interaction

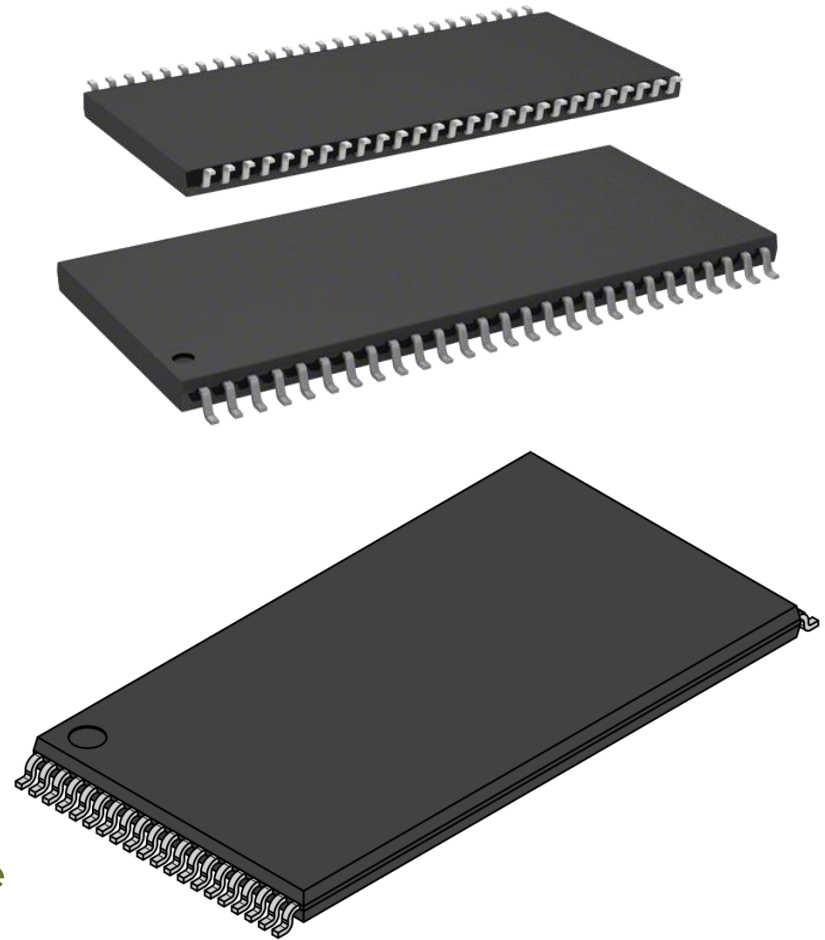
# Test Plan Development

- **Develop a comprehensive test plan**
  - Have specific goals in mind
- **Assemble boards at optimum conditions**
  - Manufacture test boards in similar environment as production boards
- **Visually inspect and electrically test**
  - Per lot ?
  - 100% inspection ?
  - Per product line ?
- **Non destructive inspection of critical components**
  - C-SAM, X-ray
- **Destructive reliability testing**
  - Test to failure: No failure = no data
- **Perform failure analysis**
- **Compile results and review**
- **Recommended actions**

The test or analysis is worthless without a recommendation based on the result

# The Test Board: Case study

- Comparing two different components
  - TSOP-I and TSOP-II
  - Both are surface mounted
  - Similar size
- Do we really need a production board?
  - Expensive materials
  - Similar failure mode
- Cheaper board with dummy components
  - Failure analysis to verify failure mode

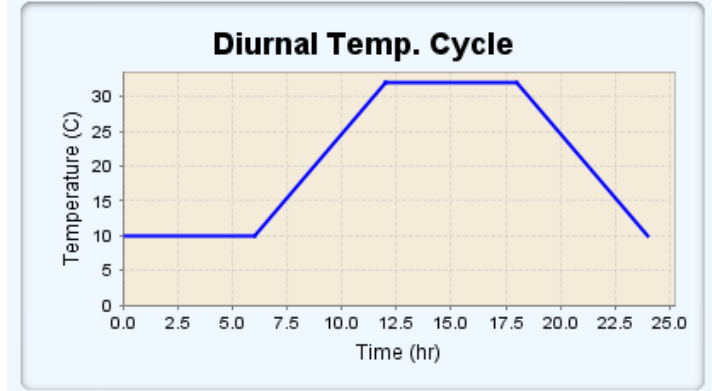




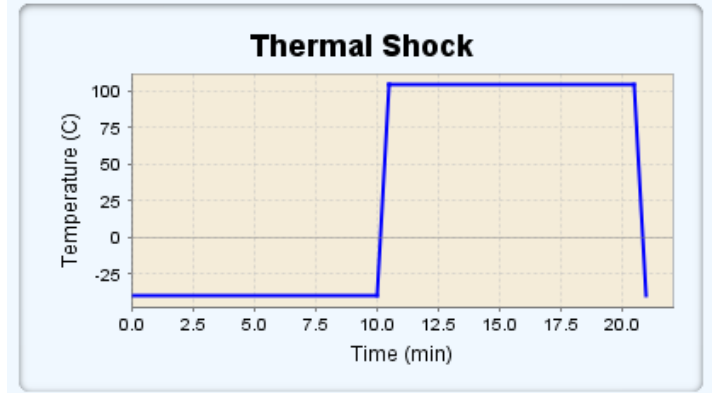
# Test Methods: Temperature Cycling

- **Key parameters:**
  - Number of cycles
    - Qual vs. test to failure
  - High and low temperatures
    - Glass transition temperature ( $T_g$ )
  - Dwell time
    - Critical dwell time can be different for different solders
  - Ramp rates
    - Thermal shock vs. Thermal cycling
- **Monitoring during test**
  - Most desirable: in situ monitoring with event detector
  - Usual: Spot check every number of cycles
  - Least desirable: Functional check at beginning and end
  - Thermocouple data
    - Temperature should be measured on components
    - Chamber settings do not include self heating or thermal lag effects
- **Verify failure mode**
  - The whole test can be worthless

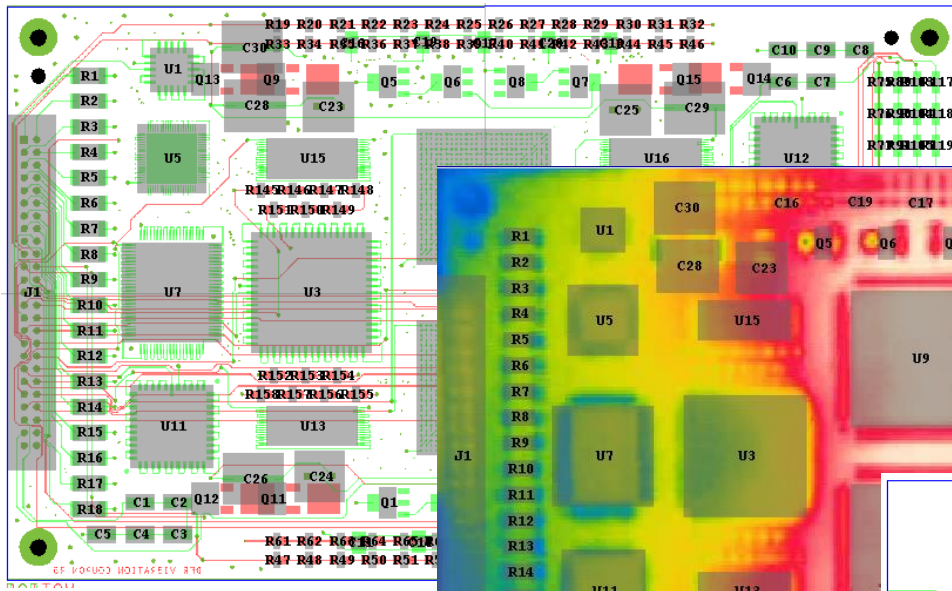
Thermal Profile



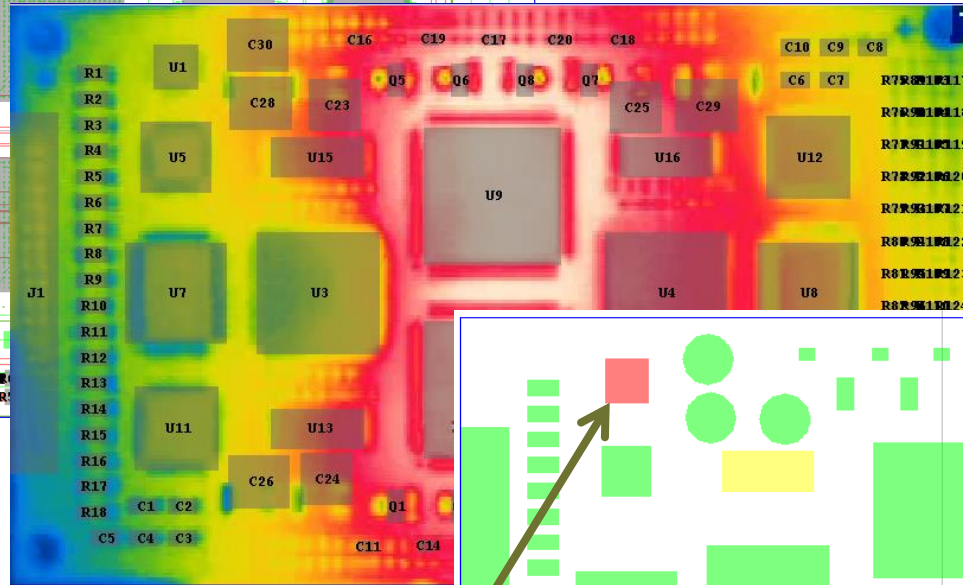
Thermal Profile



# Temp. Cycling: Reliability Prediction Software

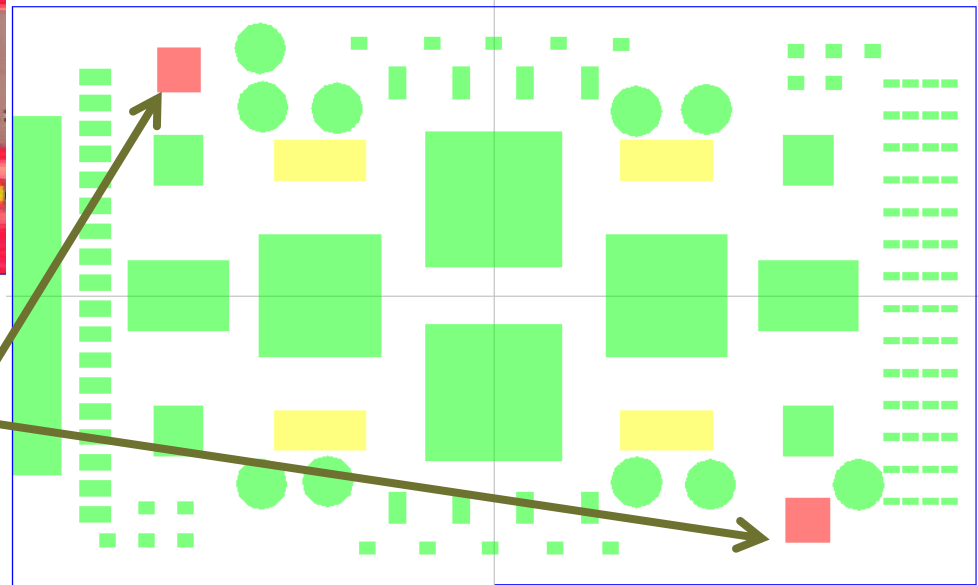


Design the board



Apply the temp. cycle

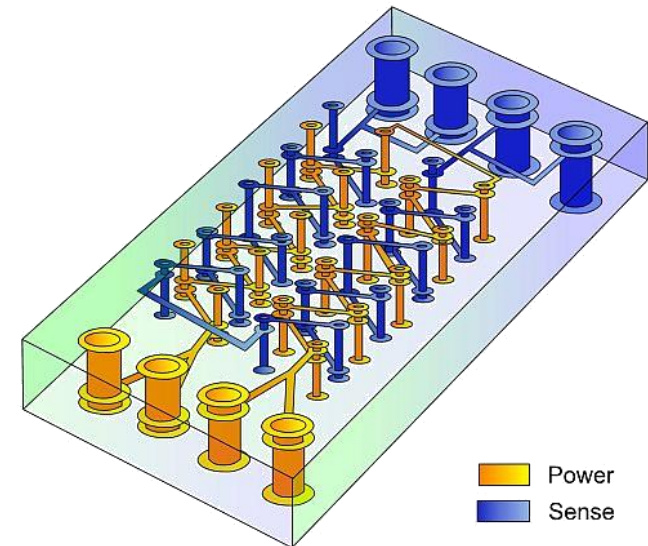
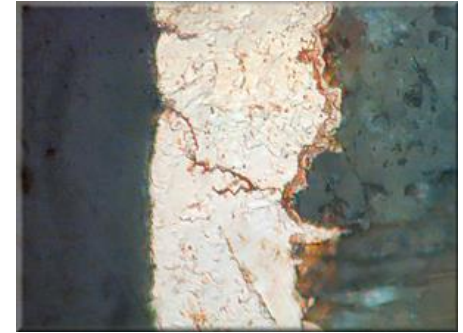
Find the failed components



# Test Method: Plated Through Hole Fatigue

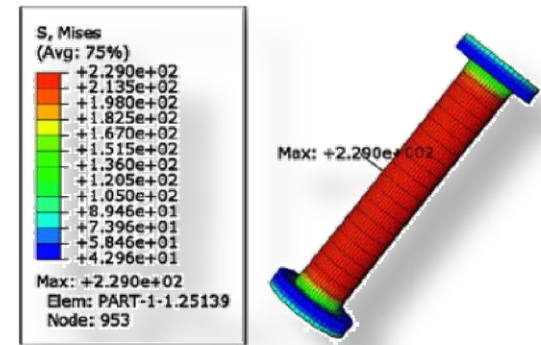
- Expansion/contraction in the z-direction is higher than that in the x-y plane.
  - The glass fibers constrain the board in the x-y plane
- Smaller holes fail faster
  - Higher aspect ratio
- More plating is better
  - Up to a point
- Lower CTE of PCB is better
  - Hard to do in reality

Source: Paul Reid, "The Impact of Lead-Free Processing on Interconnect Reliability", Printed Circuit Design & Fab,

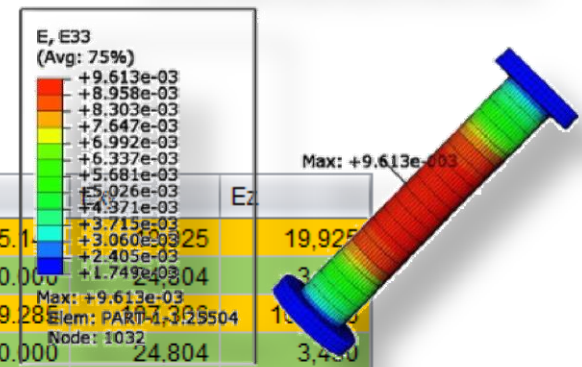


# Plated Hole Fatigue: Reliability Prediction Software

- Use the same temperature map from the solder fatigue input
- Calculate barrel stress
  - Use board stackup in the calculation
  - Modify calculations to account for qualification tests and quality control



(a) The Mises stress field of PTH at 150°C

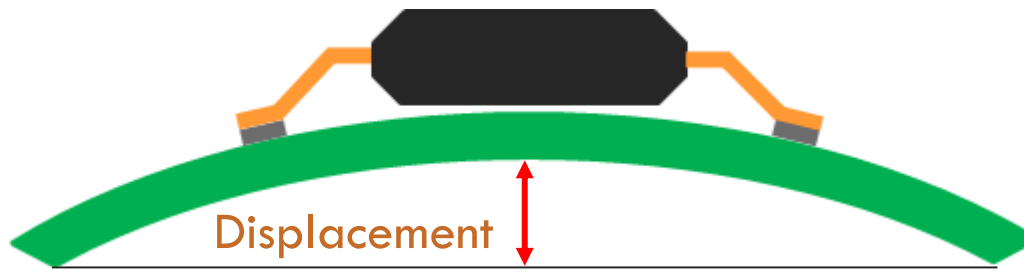


(b) The residual strain field of PTH after 3 cycles

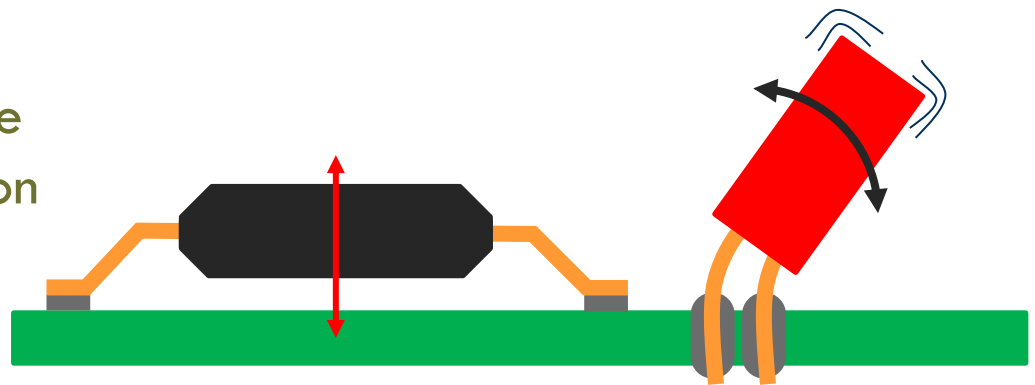
Layer	Type	Material	Thickness	Density	CTExy	CTEz	Ez
1	SIGNAL	COPPER (15.0%) / COPPER-RESIN	0.5 oz	2.8650	45.140	45.140	19,925
2	Laminate	Generic FR-4	51.26 mil	1.9000	17.000	70.000	24,804
3	SIGNAL	COPPER (94.8%) / COPPER-RESIN	0.5 oz	8.5308	19.285	19.285	107,306
4	Laminate	Generic FR-4	51.26 mil	1.9000	17.000	70.000	24,804
5	SIGNAL	COPPER (1.7%) / COPPER-RESIN	0.5 oz	1.9207	49.449	49.449	5,252
6	Laminate	Generic FR-4	51.26 mil	1.9000	17.000	70.000	24,804
7	SIGNAL	COPPER (1.6%) / COPPER-RESIN	0.5 oz	1.9136	49.482	49.482	5,252
8	Laminate	Generic FR-4	51.26 mil	1.9000	17.000	70.000	24,804
9	SIGNAL	COPPER (94.8%) / COPPER-RESIN	0.5 oz	8.5308	19.285	19.285	107,306
10	Laminate	Generic FR-4	51.26 mil	1.9000	17.000	70.000	24,804
11	SIGNAL	COPPER (9.9%) / COPPER-RESIN	0.5 oz	2.5029	46.792	46.792	14,340

# Test Method: Vibration

- Board close to resonance
  - Components can shake off due to fatigue in leads or solder



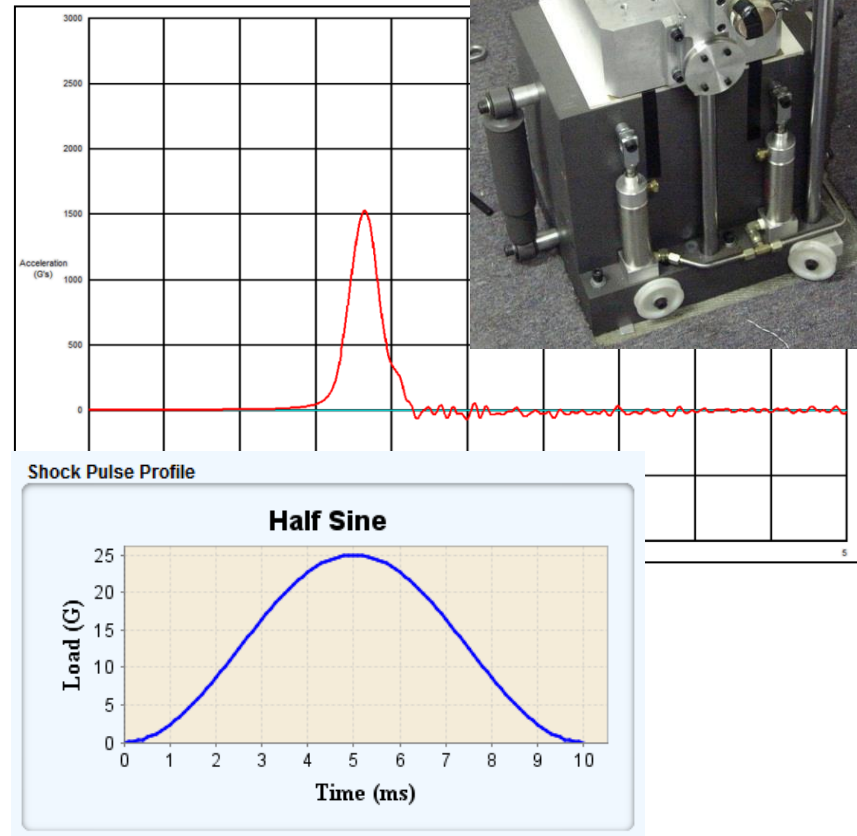
- Time to failure is determined by intensity and frequency of stress
- Component resonance
  - Lead and solder fatigue due to component motion



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# Test Method: Mechanical Shock

- Happens as random events
- Failure mechanism
  - Sensitive to intermetallic layer thickness
  - Brittle failure
- Board failures
  - Pad cracking
- Lead failures
- Probabilistic
  - Equally likely to fail at event #20 as event #200
  - Stress to probability of failure

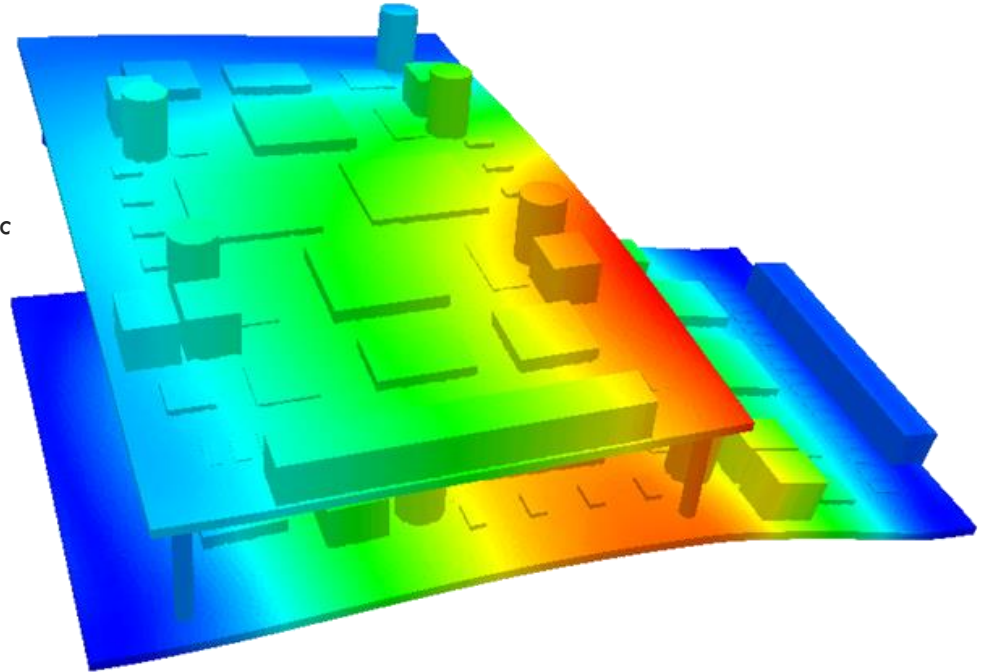


# Shock and Vibration: Reliability Prediction Software

- Calculate board strain during mechanical shock or vibration
- Use the strain to predict probability of failure

$$Z_0 = \frac{9.8 \times G_{in} \times Q}{f_n^2}$$

Source: Steinberg D.S. "Vibration analysis for electronic equipment". John Wiley & Sons, 2000.



# Test Method: CAF Resistance Test

- CAF: Conductive Anodic Filament
- Inadequate dielectric for the applied voltage
- Exceeding the maximum operating temperature of the laminate
- Manufacturing process

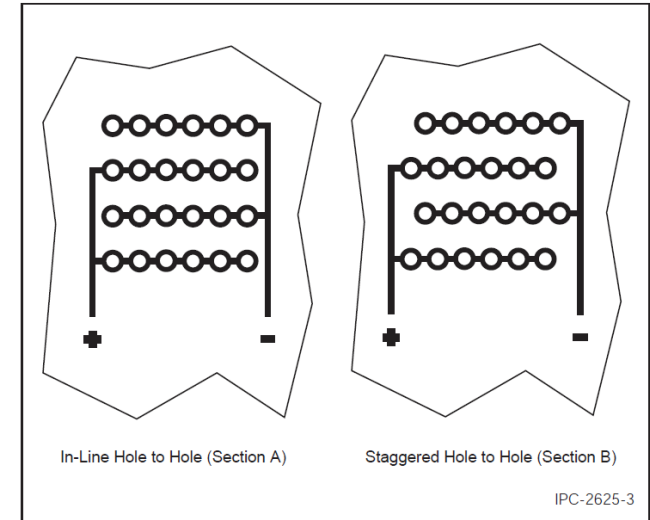
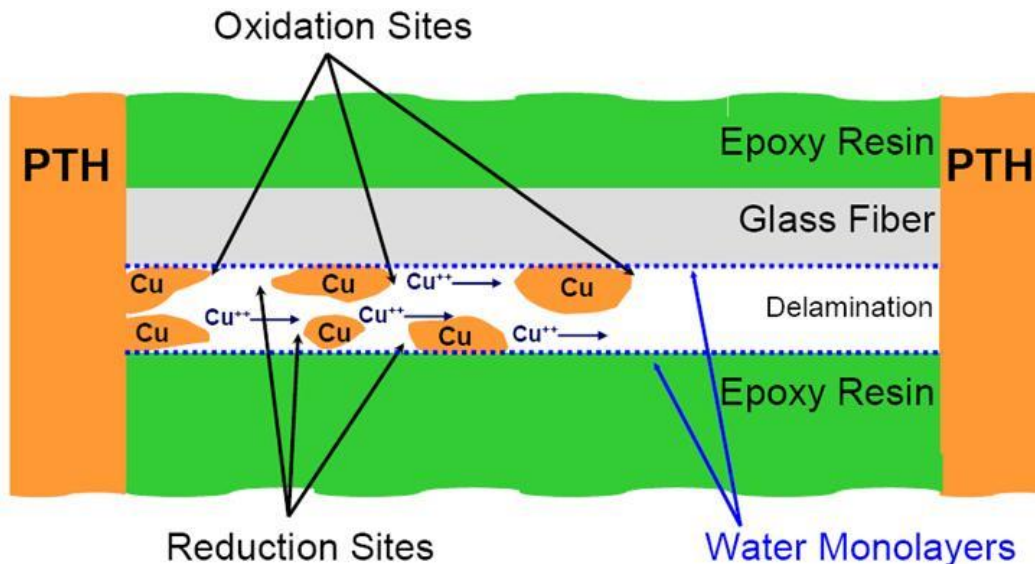
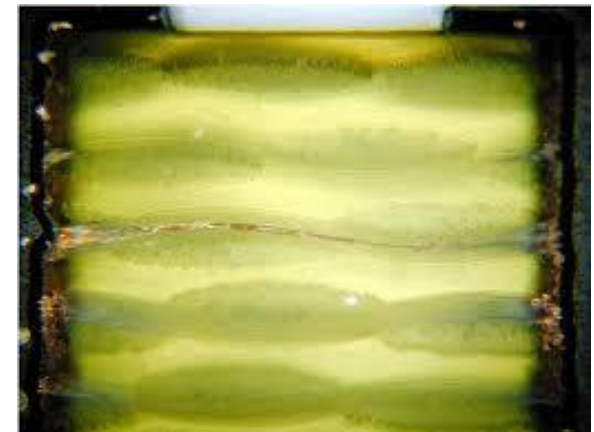


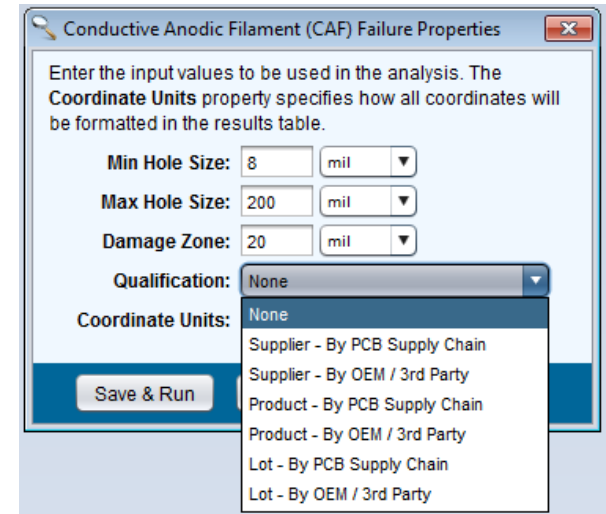
Figure 3 CAF Test Board PTH-PTH Spacing Design





# CAF: Reliability Prediction Software

- Input the drill hole locations and diameters
  - From drill files
- Set the “Damage zone”
  - Maximum distance between a pair of holes to be considered for analysis
- Qualification process
  - Better qualification process will decrease the number of failures
- Filter by hole size



Highlighted CAF Results

# Failure Analysis

- Effective failure analysis is critical to reliability!
- Without identifying the root causes of failure, true corrective action cannot be implemented
  - Risk of repeat occurrence increases
- Use a systematic approach to failure analysis
  - Proceed from non-destructive to destructive methods until all root causes are identified.
- Techniques based upon the failure information specific to the problem.
  - Failure history, failure mode, failure site, failure mechanism

# Summary

- **If you remember nothing else:**
  - A test plan without an objective is doomed before it even started
  - Testing to pass has no failure data
  - Root cause failure analysis is worth it
- **Some tests can be simulated in software**
  - Solder fatigue
  - Plated Through Hole fatigue
  - Mechanical shock and vibration
  - Conductive anodic filament resistance
- **Every test or analysis must have a recommended action as a result**
  - And every recommended action should have test data or analysis as justification

**Questions?**

# **Test Plan Development**

Dr. Gil Sharon, [gsharon@dfrsolutions.com](mailto:gsharon@dfrsolutions.com)

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