

OZDSP3000 Test Application Software

User's Manual UM-0019

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Date and Revision July 2011 Rev B

Part Number UM-0019

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1. Introduction

This document is intended to briefly describe the simple test application that was developed to exercise the various interfaces on the Oztek 10741 DSP Control Board. This test application was developed to support initial bring up of the 10741 board. It is also intended to be used as a basic template for the various software routines needed to interface with the on-board resources.

1.1 Referenced Documents

Ref.	Document	Description	
[1]	FS-0044	OZDSP3000 FPGA Functional Specification	
[2]	UM-0015	Oztek TMS28x CAN Bootloader Users Manual	
[3]	UM-0018	OZDSP3000 User's Manual	
[4] SPRS439 Texas Instruments: TMS320F28335, TMS320F28335, TMS320F28234, TMS320F28232, TMS320F28232, TMS320F28234, TMS320F28232, DSCs		Texas Instruments: TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232 DSCs	

1.2 Definitions

AFE	Active Front End
CAN	Controller Area Network
DSP	Digital signal processor
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro-magnetic compatibility
EMI	Electro-magnetic interference
GND	Ground, low side of input power supply
GTI	Grid Tied Inverter
GUI	Graphical User Interface
HMI	Human Machine Interface
IPM	Intelligent Power Module
N.C.	Not connected
PCB	Printed Circuit Board
PCC	Power Control Center
PLC	Programmable Logic Controller
PLL	Phase Locked Loop
POR	Power On Reset
PWM	Pulse width modulation
SVM	Space Vector Modulator

2. Communications Configuration

The test application software is controlled via a standard RS-232 link from a host computer. The HyperTerminal settings necessary to communicate with the Test Board are shown in the figure below:

COM1 Properties		? 🔀
Port Settings		
<u>B</u> its per second:	19200	•
<u>D</u> ata bits:	8	¥
Parity:	None	~
Stop bits:	1	~
Elow control:	None	~
	<u>R</u> estore	e Defaults
	Cancel	

Figure 1 - HyperTerminal Settings for Test Application

There is one serial port and one CAN port on the DSP control board. The serial port is located at connector P1, which is shown in the following diagram:



Figure 2 – Location of RS232 Port

3. DAC Outputs

The test application configures the four debug Digital to Analog Converters (DACs) to always update. The output for each DAC channel is a 4 Hz saw tooth wave form that varies in amplitude from 0 V to 3 V. The DAC outputs are located at TP29, TP27, TP24, and TP21. There is a 90° phase shift between each of the signals (TP27 to TP29, TP24 to TP27, TP21 to TP24, and TP29 to TP21).

4. Test Menu Description

When turning on the power while the board is connected to the host PC with an RS232 cable, the following menu will appear on the HyperTerminal Screen:

OZDSP3000 DSP CONTROL BOARD TEST MENU: a - Report ADC Results in Counts b - Repeat Single ADC Result c - Report ADC Results in Volts d - Clear Fault bits e - Report the Fault bits f - Run EEPROM Test

g - Run SRAM Test h - Run Expansion Test i - Turn Debug LEDs on/off j - Get Digital Input Pin State k - Set Digital Output Pin State 1 - Set Relay Driver State m - Display this menu n - Boot Enable Pin State o - Run CAN Test p - Read QEP Input Bits q - Toggle Inverter A Output on/off r - Toggle Inverter B Output on/off s - Toggle Half Bridge Output on/off u - Real Time Clock v - Watchdog Control w - Test Interrupt Lines x - Read HALLs y - Test FPGA Read/Write

z - Report Software/FPGA Revs

Each of the menu items is discussed in the following sections.

4.1 a- Report ADC Results in Counts

The test application configures the DSP's internal ADC to make conversions at the 10 KHz PWM rate. Because the PWM outputs and timers are free running, the ADC results are constantly updated at the PWM rate; executing this command displays the result of the last conversion. The analog MUX on board is used to cycle through 11 additional inputs to the DSP's internal ADC. As such, these values are only updated every 11 PWM cycles, or at 909 Hz.

When executed, this command will display the following screen dump:

INVA_ISENSE_U	(Q15)	=	0xFFFFEF42	INVB_ISENSE_U (QI	15)	=	0xffffef68
INVA_ISENSE_V	(Q15)	=	0xFFFFEF3C	INVB_ISENSE_V (Q)	15)	=	0xFFFFEF56
INVA_ISENSE_W	(Q15)	=	0xFFFFEF43	INVB_ISENSE_W (Q)	15)	=	0xFFFFEF61
INVA_UDC	(Q15)	=	0x00000021	INVB_UDC (QI	15)	=	0x0000030
INVA_TEMP		=	0x0000073	INVB_TEMP		=	0×00000071
HB_ISENSE	(Q15)	=	0xFFFFEF43	HB_TEMP		=	0x0000072
AUX_ISENSE_U	(Q15)	=	0xFFFFDD19	AUXA_TEMP		=	0×00000071
AUX_ISENSE_V	(Q15)	=	0xFFFFDD19	AUXB_TEMP		=	0×00000071
AUX_ISENSE_W	(Q15)	=	0xFFFFDD19	AUXC_TEMP		=	0×00000071
VLINE_AB	(Q15)	=	0xFFFFFFF0	VOUT_AB (QI	15)	=	$0 \mathbf{x} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} 0$
VLINE_BC	(Q15)	=	0 xFFFFFFFFFFFFF	VOUT_BC (QI	15)	=	$0 \mathbf{x} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} 0$
VLINE_CA	(Q15)	=	0 xFFFFFFFFFFFFF	VOUT_CA (QI	15)	=	$0 \mathbf{x} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} \mathbf{F} 0$
REF_1P5V		=	0x000080E0	REF_2P5V		=	0x000087E0
VSENSE_POS_24	7	=	0x0000CD50	$VSENSE_POS_15V$		=	0x0000AD60
VSENSE_POS_5V		=	0x0000C7D0	VSENSE_POS_3P3V		=	0x0000CD80
NET_ANALYZER		=	0xFFFFDD19	TEST_POINT		=	0xFFFFDD2C
ADC_CAL_STATUS		=	0 (OK)				
CAL_GAIN (Q12)		=	0x00000FFE	CAL_OFST (Q16)		=	0x00000050

Upon power-up, the DSP's ADC is calibrated to improve the overall ADC accuracy. The raw calibration gain and offset values are shown in the displayed output.

The numeric format of the various measurements depends on the measurement type as follows:

- The current sense measurements are displayed in Q15 format and are normalized to range from -1 to +1 (where 1 is full scale and -1 is negative full scale), and take into account the internal ADC calibration.
- The VOUT/VLINE measurements are also displayed in normalized Q15 format and range from –1 to +1. These are read from the external isolated ADC and are not calibrated.
- The UDC measurements from the two 3-phase inverter drivers are displayed in Q15 format and range from 0 to +1. These take into account the internal ADC calibration.
- The measured temperatures are given as unsigned 16-bit values that represent calibrated ADC data.
- The auxiliary analog input values are displayed in normalized Q15 format and range from 0 to +1, and take into account the internal ADC calibration.
- The supply (+3V, +5V, +/-15V) and reference (2.654V, 1.5V) voltages are merely the raw ADC results without any calibration correction (unsigned 16-bit data)

4.2 b - Repeat single ADC Measurement

This command allows the user to constantly monitor one particular ADC input. Upon executing this command, the user will see:

Enter one of the 2-o	character channel IDs shown below:
00 - INVA_ISENSE_U	11 - INVB_TEMP
01 - INVA_ISENSE_V	12 - HB_TEMP
02 - INVA_ISENSE_W	13 - AUXA_TEMP
03 - INVA_UDC	14 - AUXB_TEMP
04 - HB_ISENSE	15 - AUXC_TEMP
05 - 1P5V_REF	16 - 24V_VSENSE
06 - 2P5V_REF	17 - 15V_VSENSE
07 - NET_ANALYZER	18 - 5V_VSENSE
08 - INVB_ISENSE_U	19 - 3P3V_SENSE
09 - INVB_ISENSE_V	1A - TEST_POINT
0A - INVB_ISENSE_W	1B - VLINE_AB
0B - INVB_UDC	1C - VLINE_BC
0C - AUX_ISENSE_U	1D - VLINE_CA
0D - AUX_ISENSE_V	1E - VOUT_AB
0E - AUX_ISENSE_W	1F - VOUT_BC
10 - INVA_TEMP	20 - VOUT_CA

By entering the 2-digit ID of the desired ADC input, the application will continuously update the latest 'live' value for that ADC channel, such as:

INVB_ISENSE_U (Q15) = 0xFFFFEF57

This mode can also be used to hold the analog MUX on a certain channel so that the voltage can be measured at TP18. This mode is exited by hitting any key.

4.3 c - Report ADC Results in Volts

Executing this command dumps the results of the last conversion in human-readable decimal values. When executed, the user will see the following screen dump (of course, user's actual output might be different and will reflect actual inputs):

=	1.59v	INVB_ISENSE_U	=	1.09v
=	1.09v	INVB_ISENSE_V	=	1.09v
=	1.09v	INVB_ISENSE_W	=	1.09v
=	0.01v	INVB_UDC	=	0.00v
=	0.01v	INVB_TEMP	=	0.01v
=	1.09v	HB_TEMP	=	0.01v
=	1.09v	AUXA_TEMP	=	0.01v
=	1.09v	AUXB_TEMP	=	0.01v
=	1.09v	AUXC_TEMP	=	0.01v
=	2.49v	VOUT_AB	=	2.49v
=	2.49v	VOUT_BC	=	2.49v
=	2.49v	VOUT_CA	=	2.49v
=	1.51v	REF_2P5V	=	2.49v
=	24.02v	VSENSE_POS_15V	=	15.00v
=	5.06v	VSENSE_POS_3P3V	=	3.27v
=	3.33v	TEST_POINT	=	0.01v
		= 1.59v = 1.09v = 0.01v = 0.01v = 1.09v = 1.09v = 1.09v = 1.09v = 2.49v = 2.49v = 2.49v = 1.51v = 24.02v = 5.06v = 3.33v	<pre>= 1.59v INVB_ISENSE_U = 1.09v INVB_ISENSE_V = 0.01v INVB_ISENSE_W = 0.01v INVB_UDC = 0.01v INVB_TEMP = 1.09v AUXA_TEMP = 1.09v AUXA_TEMP = 1.09v AUXB_TEMP = 1.09v AUXC_TEMP = 2.49v VOUT_AB = 2.49v VOUT_BC = 2.49v VOUT_CA = 1.51v REF_2P5V = 24.02v VSENSE_POS_15V = 5.06v VSENSE_POS_3P3V = 3.33v TEST_POINT</pre>	= 1.59v INVB_ISENSE_U = = 1.09v INVB_ISENSE_V = = 0.01v INVB_UDC = = 0.01v INVB_TEMP = = 0.01v INVB_TEMP = = 0.01v INVB_TEMP = = 1.09v HB_TEMP = = 1.09v AUXA_TEMP = = 1.09v AUXE_TEMP = = 1.09v AUXC_TEMP = = 2.49v VOUT_AB = = 2.49v VOUT_CA = = 1.51v REF_2P5V = = 24.02v VSENSE_POS_15V = = 5.06v VSENSE_POS_3P3V = = 3.33v TEST_POINT =

For the HV ADC voltage values (VLINE, VOUT) the value reported is the voltage at the input to the ADC, not the input to the board.

4.4 d - Clear Fault bits

This routine is used to clear all active fault bits.

4.5 e - Report the Fault bits

This command returns the present state of the various board faults as read from the FPGA. When executed, the user will see the following display:

INVA_ERR_U	= 1
INVA_ERR_V	= 1
INVA_ERR_W	= 1
INVB_ERR_U	= 1
INVB_ERR_V	= 1
INVB_ERR_W	= 1
INVA_OVT	= 1
INVB_OVT	= 1
HB_ERR	= 1
HB_OVT	= 1
GPIN_INT	= 1
RELAY_FAULT	= 1

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```
RELAY_0 = 0
RELAY_1 = 1
RELAY_2 = 2
RELAY_3 = 3
```

Any bit that is reported as a '1' indicates that the corresponding fault has occurred. Any bit that is reported as a '0' indicates that the corresponding fault has not occurred.

The **RELAY_FAULT** indicates the relay driver chip has a fault, **RELAY_X** specifies the fault conditions for a particular output. Fault conditions only occur if **RELAY_FAULT** is a '1'. Below are the fault conditions that can be reported.

Fault Condition	Value
Over-voltage	0
Open-load	1
Over-current	2
Short-to-ground	3

4.6 f - Run EEPROM Test

This test is used to verify the three EEPROM devices on the control board. The user must select which of the devices to test. When executed, the user will see the following output:

```
Select EEPROM to test.

'0' - Boot EEPROM

'1' - Config EEPROM

'2' - Data EEPROM

Testing EEPROMs...

Test Passed!
```

If a failure occurs, the test stops executing immediately, and the user will see the following output:

Test FAILED at address: 0x02

4.7 g – Run SRAM Test

When executed, the SRAM test will display:

```
SRAM Test IN PROGRESS ... Hit any key to quit.
```

The test performs a series of writes then reads to the external memory. If data is read back that does not match what was read, the test will stop immediately and display:

SRAM Test Failed in block XX

Where xx is the block that failed. If no failures are detected, the output will be:

SRAM Test Passed.

4.8 h – Run Expansion Test

This test is used to stimulate IO to the Oztek Expansion bus. The test simultaneously writes data on both the SPI bus and Parallel bus. The test has no validation testing, it is up to the user to verify that the signals are toggling.

4.9 i - Turn Debug LEDs on/off

This is a simple routine that simply turns the three debug LEDS (D22, D27 and D34) on or off. When executed, the user will see the following prompt:

Enter '1' to turn LEDs ON, '0' to turn LEDs OFF:

Any character entered other than '0' or '1' will result in the operation being aborted.

A fourth LED, D38, is used as a heart beat signal, and is not affected by this test.

4.10 j - Get the Digital Input Pin State

This command returns the state of the 4 opto-isolated digital input lines to the control board. The values are represented as a single HEX digit, with bit 0 representing the state of the LSB, and bit 3 representing the state of the MSB. Additionally, the states of the SPARE GPIO pins to the DSP are displayed. The data is displayed as follows:

General Purpose Digital Inputs = 0xF

Additionally, the states of the SPARE GPIO pins to the DSP are tested by forcing them to a known pattern from the FPGA. If the pattern matches, the following will be displayed:

General Purpose SPARES: = 0x2A Pattern matches FPGA

If the pattern does not match, the following will be displayed:

General Purpose SPARES: = 0x3C Pattern DOES NOT match the FPGA

4.11 k - Set the Digital Output Pin State

This routine is used to drive the state of the 4 opto-isolated digital output lines on the control board. When executed, the user will see the following prompt:

Enter 4-bit Digital Output State (in HEX):

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A single HEX digit must be entered to set the outputs. Bit 0 will drive the LSB of the digital outputs; bit 3 will drive the MSB of the digital outputs. Setting a bit to a '1' will assert the output (i.e. turn on the open-collector output). Setting a bit to a '0' will turn off the output.

Additionally, the ability of the FPGA to receive the SPARE GPIO pins as inputs is tested automatically. The DSP forces a pattern then checks to see if the same pattern is observed by the FPGA. If the test passes the following output will be shown:

General Purpose SPARES: = 0x15 Pattern matches DSP

Otherwise, the output will be similar to this:

General Purpose SPARES: = 0x2E Pattern DOES NOT match the DSP

4.12 I - Set Relay Driver Output

This command is used to set the relay driver state. When executed, the user will see:

```
Enter 4-bit Relay Output State (in HEX):
```

A single hex digit must be entered. The hex digit represents the state of the 4 relay driver outputs (bit 0 represents the GATE1 output, bit 3 represents the GATE4 output). Setting a bit to a '1' will assert the relay driver output (i.e. close the relay); setting a bit to a '0' will turn off the relay driver (i.e. open the relay).

4.13 m - Display this menu

This selection will display the main menu.

4.14 n – Boot Enable Pin State

This routine displays the state of the Boot Select pin state. It will display one of the following two messages:

Boot pin state is: 0 (SPI BOOT). Boot pin state is: 1 (FLASH BOOT).

4.15 o - Run CAN Test

The CAN test verifies the CAN transmitter and receiver on the DSP Control Board. The user is prompted at each step of the CAN port configuration and selections are echoed before the test

is run. For the CAN tests to run successfully, correct termination resistors must be connected to the bus lines.

For the transmit test, the user selects either a standard or extended Message ID format along with transmitted byte order and BAUD rate. Once the test is launched, the transmit test continuously sends a fixed Message ID and data for easy verification at the receiving CAN port.

For the receive test, the user selects either a standard or extended Message ID format along with the BAUD rate and Message ID match and mask values. For a message to be received, the each *mask value* bit must be set to '1' (ignore) or the incoming Message ID bits must match the corresponding bits of the *match value*. Once the receiver test is launched, receive messages are reported as in the following example: RCVD EXT MSG ID: 0x16100020, BYTES: 2, DATA: 0x1 0x0

4.16 p - Read QEP Input Bits

This routine returns presents the user with two test options:

```
Select an Encoder Test:

'0' to Check Logic Levels

'1' for Encoder Operation
```

Choosing option '0' will simply display the logic level of the three inputs:

```
Encoder Logic Levels:
Input A: = 1
Input B: = 0
Index: = 0
```

Option '1' allows the user to read actual encoder counts after entering some configuration data:

Enter Line Count as 16-bit Hex: 0x0100 Enter Pole pairs as 4-bit Hex: 0x02

After the data has been entered, the encoder data below will be continuously updated.

POSCNT: 255 MECH_THETA: 90 ELEC THETA: 0

To stop this test, press any key.

4.17 q - Toggle Inverter A Output on/off

The test application configures the DSP's 3-phase Inverter A PWM outputs, labeled INVERTER A on the board silkscreen by connectors J11, with a 100us PWM period (10 kHz) and unique duty cycles. The table below shows the unique duty cycles for all the pins.

This test simply toggles all the Pulse Width Modulated (PWM) signals at Inverter A output on/off. The user needs to connect a scope probe at the inverter output to verify that the Software is behaving properly.

Connector	Pin	Signal Name	Duty Cycle
	4	INVA_TOP_U	10 %
	2	INVA_BOT_U	90 %
14.4	7	INVA_TOP_V	20 %
JII	5	INVA_BOT_V	80 %
	10	INVA_TOP_W	30 %
	8	INVA_BOT_W	70 %

 Table 1 - Inverter A Output Duty Cycles

4.18 r - Toggle Inverter B Output on/off

The test application configures the DSP's 3-phase Inverter BPWM outputs, (labeled INVERTER Bon the board silkscreen by connectors J13) with a 100us PWM period (10 kHz) and unique duty cycles. The table below shows the unique duty cycles for all the pins.

This test simply toggles all the Pulse Width Modulated (PWM) signals at Inverter Boutput on/off. The user needs to connect a scope probe at the inverter output to verify that the Software is behaving properly.

Connector	Pin	Signal Name	Duty Cycle
J13	4	INVB_TOP_U	25 %
	2	INVB_BOT_U	75 %
	7	INVB_TOP_V	35 %
	5	INVB_BOT_V	65 %
	10	INVB_TOP_W	45 %
	8	INVB_BOT_W	55 %

Table 2 – Inverter BOutput Duty Cycles

4.19 s - Toggle Half Bridge Output on/off

The test application configures the DSP's Half Bridge PWM outputs (labeled HALF BRIDGE on the board silkscreen by connector J14) with a 100us PWM period (10 kHz) and an 85% duty cycle signal. The table below shows the unique duty cycles for all the pins.

This test simply toggles all the Pulse Width Modulated (PWM) signals at the Half Bridge outputs on/off. The user needs to connect a scope probe at the inverter output to verify that the Software is behaving properly.

Connector	Pin	Signal Name	Duty Cycle
J14	4	HB_TOP	85 %
	2	HB_BOT	15 %

Table 3 – Hal	f Bridge O	utput Dut	y Cycles
---------------	------------	-----------	----------

4.20 u – Real Time Clock

This routine provides access to the on board real time clock. The user can read the Real Time Clock or change its value. Upon selecting the routine, the current time is displayed as time, date, day of week:

Real Time Clock Value: 14:45:37 07/31/09 5 Waiting 10 seconds to verify clock...

The Test Application will automatically wait 10 seconds to verify operation of the Real Time Clock by reading it again. If the elapsed time is between 9 and 11 seconds (inclusive), the following message will be displayed:

```
Elapsed time PASSES.
Real Time Clock Value: 14:45:47 07/31/09 5
```

If the elapsed time is out of range, the message displayed will be:

```
Elapsed time FAILS.
Real Time Clock Value: 14:45:52 07/31/09 5
```

The user is then allowed to update the entire Clock value:

```
Enter '1' to change value: 1
Enter 8-bit Hour Value: 0x0E
Enter 8-bit Minute Value: 0x2D
Enter 8-bit Second Value: 0x00
Enter 8-bit Month Value: 0x07
Enter 8-bit Date Value: 0x1F
Enter 8-bit Year Value: 0x09
Enter 3-bit Day of Week Value: 0x5
```

The clock has now been updated, and can be checked by selecting 'u' again from the main menu.

4.21 v – Watchdog Control

This routine can modify the watchdog circuit on the board. Selecting this test will first display the current settings:

```
Watchdog Enable Status
SW Enable: 1
HW Enable: 0
```

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Key: 0xAA

When SW Enable is selected, the DSP is responsible for keeping the DSP out of reset. When HW is selected, it assumes the presence of the HW jumper at J21. With HW selected, and the jumper removed, the DSP should reset, presenting the main menu again.

4.22 w – Test Interrupt Lines

This test forces several interrupt events to occur, and then looks at the logic level for the interrupt lines that come into the DSP. The interrupt lines tested are Inverter A, Inverter B, and Half Bridge. The test assumes that nothing is plugged in to connectors J8, J11, J13, and J14 on the board. If all tests pass, the following will be the output:

INV_A_N PIN is LOW. PASS. Visually check D44 and a press a key to continue. INV_B_N PIN is LOW. PASS. Visually check D50 and a press a key to continue. HB_INT_N PIN is LOW. PASS. Visually check D52 and a press a key to continue. SYS_INT_n PIN is LOW. PASS.

If any of the tests fail, or a device is connected to J11, J13, or J14, the following will be the output for the associated pin:

INV_A_N PIN is HIGH. FAIL. Visually check D44 and a press a key to continue.

4.23 x - Read Hall Input Bits

This test will return the present state of the three HALL sensor inputs to the DSP. Upon executing, the user will see the following return data:

HALL Read Data = 0x0

4.24 y - Test FPGA Read/Write

This test performs a series of writes and reads to a register on the FPGA. If the value written is always read back correctly, the following message will be displayed:

FPGA test PASSED.

Otherwise, a failure message will be displayed, indicating the data line that failed:

FPGA test FAILED on data line: 2

4.25 z - Report Software/FPGA Revs

This test displays the corresponding versions for the following elements:

Test Application Firmware Version MM.mm

```
Driver Library Firmware Info:
 DSP
           SW90077-0100 Rev MM.mm
 ADC
           SW90078-0100 Rev MM.mm
 CAN
          SW90080-0100 Rev MM.mm
 QEP
         SW90084-0100 Rev MM.mm
 PWM
          SW90083-0101 Rev MM.mm
 RING_BUF SW90087-0100 Rev MM.mm
          SW90081-0100 Rev MM.mm
 SPI
 TIMER
          SW90079-0100 Rev MM.mm
         SW90082-0100 Rev MM.mm
 UART
 XINTF
         SW90086-0100 Rev MM.mm
 CAP
           SW90114-0100 Rev MM.mm
FPGA Hardware Revision MM.mm
Board Model Revision m
AnyBus Model Info
                  xxxxxxxx
 Serial Number:
 Bootloader Version: MM.mm
 API Version:
                 MM.mm
 Fieldbus Type:
                     XXXX
 Fieldbus FW Version: MM.mm
 Module Type:
                     XXXX
 Module Version:
                     MM.mm
```

Where "MM" represents the major version and "mm" the minor version.

The user needs to consult appropriate documentation to verify that the numbers displayed are appropriate.

Warranty and Product Information

Limited Warranty

What does this warranty cover and how long does it last? This Limited Warranty is provided by Oztek Corp. ("Oztek") and covers defects in workmanship and materials in your OZDSP3000 controller. This Warranty Period lasts for 18 months from the date of purchase at the point of sale to you, the original end user customer, unless otherwise agreed in writing. You will be required to demonstrate proof of purchase to make warranty claims. This Limited Warranty is transferable to subsequent owners but only for the unexpired portion of the Warranty Period. Subsequent owners also require original proof of purchase as described in "What proof of purchase is required?"

What will Oztek do? During the Warranty Period Oztek will, at its option, repair the product (if economically feasible) or replace the defective product free of charge, provided that you notify Oztek of the product defect within the Warranty Period, and provided that through inspection Oztek establishes the existence of such a defect and that it is covered by this Limited Warranty.

Oztek will, at its option, use new and/or reconditioned parts in performing warranty repair and building replacement products. Oztek reserves the right to use parts or products of original or improved design in the repair or replacement. If Oztek repairs or replaces a product, its warranty continues for the remaining portion of the original Warranty Period or 90 days from the date of the return shipment to the customer, whichever is greater. All replaced products and all parts removed from repaired products become the property of Oztek.

Oztek covers both parts and labor necessary to repair the product, and return shipment to the customer via an Oztek-selected non-expedited surface freight within the contiguous United States and Canada. Alaska, Hawaii and locations outside of the United States and Canada are excluded. Contact Oztek Customer Service for details on freight policy for return shipments from excluded areas.

How do you get service? If your product requires troubleshooting or warranty service, contact your merchant. If you are unable to contact your merchant, or the merchant is unable to provide service, contact Oztek directly at:

USA Telephone: 603-546-0090 Fax: 603-386-6366 Email techsupport@oztekcorp.com

Direct returns may be performed according to the Oztek Return Material Authorization Policy described in your product manual.

What proof of purchase is required? In any warranty claim, dated proof of purchase must accompany the product and the product must not have been disassembled or modified without prior written authorization by Oztek. Proof of purchase may be in any one of the following forms:

- The dated purchase receipt from the original purchase of the product at point of sale to the end user
- The dated dealer invoice or purchase receipt showing original equipment manufacturer (OEM) status
- The dated invoice or purchase receipt showing the product exchanged under warranty

What does this warranty not cover? Claims are limited to repair and replacement, or if in Oztek's discretion that is not possible, reimbursement up to the purchase price paid for the product. Oztek will be liable to you only for direct damages suffered by you and only up to a maximum amount equal to the purchase price of the product. This Limited Warranty does not warrant uninterrupted or error-free operation of the product or cover normal wear and tear of the product or costs related to the removal, installation, or troubleshooting of the customer's electrical systems. This warranty does not apply to and Oztek will not be responsible for any defect in or damage to:

a) The product if it has been misused, neglected, improperly installed, physically damaged or altered, either internally or externally, or damaged from improper use or use in an unsuitable environment
b) The product if it has been subjected to fire, water, generalized corrosion, biological infestations, or input voltage that creates operating conditions beyond the maximum or minimum limits listed in the Oztek product specifications including high input voltage from generators and lightning strikes
c) The product if repairs have been done to it other than by Oztek or its authorized service centers (hereafter "ASCs")

d) The product if it is used as a component part of a product expressly warranted by another manufacturer

e) The product if its original identification (trade-mark, serial number) markings have been defaced, altered, or removed

f) The product if it is located outside of the country where it was purchased

g) Any consequential losses that are attributable to the product losing power whether by product malfunction, installation error or misuse.

Disclaimer

Product

THIS LIMITED WARRANTY IS THE SOLE AND EXCLUSIVE WARRANTY PROVIDED BY OZTEK IN CONNECTION WITH YOUR OZTEK PRODUCT AND IS, WHERE PERMITTED BY LAW, IN LIEU OF ALL OTHER WARRANTIES, CONDITIONS, GUARANTEES, REPRESENTATIONS, OBLIGATIONS AND LIABILITIES, EXPRESS OR IMPLIED, STATUTORY OR OTHERWISE IN CONNECTION WITH THE PRODUCT, HOWEVER ARISING (WHETHER BY CONTRACT, TORT, NEGLIGENCE, PRINCIPLES OF MANUFACTURER'S LIABILITY, OPERATION OF LAW, CONDUCT, STATEMENT OR OTHERWISE), INCLUDING WITHOUT RESTRICTION ANY IMPLIED WARRANTY OR CONDITION OF QUALITY, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE TO THE EXTENT REQUIRED UNDER APPLICABLE LAW TO APPLY TO THE PRODUCT SHALL BE LIMITED IN DURATION TO THE PERIOD STIPULATED UNDER THIS LIMITED WARRANTY. IN NO EVENT WILL OZTEK BE LIABLE FOR: (a) ANY SPECIAL, INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING LOST PROFITS, LOST REVENUES, FAILURE TO REALIZE EXPECTED SAVINGS, OR OTHER COMMERCIAL OR ECONOMIC LOSSES OF ANY KIND, EVEN IF OZTEK HAS BEEN ADVISED, OR HAD REASON TO KNOW, OF THE POSSIBILITY OF SUCH DAMAGE, (b) ANY LIABILITY ARISING IN TORT, WHETHER OR NOT ARISING OUT OF OZTEK'S NEGLIGENCE, AND ALL LOSSES OR DAMAGES TO ANY PROPERTY OR FOR ANY PERSONAL INJURY OR ECONOMIC LOSS OR DAMAGE CAUSED BY THE CONNECTION OF A PRODUCT TO ANY OTHER DEVICE OR SYSTEM, AND (c) ANY DAMAGE OR INJURY ARISING FROM OR AS A RESULT OF MISUSE OR ABUSE, OR THE INCORRECT INSTALLATION, INTEGRATION OR OPERATION OF THE PRODUCT. IF YOU ARE A CONSUMER (RATHER THAN A PURCHASER OF THE PRODUCT IN THE COURSE OF A BUSINESS) AND PURCHASED THE PRODUCT IN A MEMBER STATE OF THE EUROPEAN UNION, THIS LIMITED WARRANTY SHALL BE SUBJECT TO YOUR STATUTORY RIGHTS AS A CONSUMER UNDER THE EUROPEAN UNION PRODUCT WARRANTY DIRECTIVE 1999/44/EC AND AS SUCH DIRECTIVE HAS BEEN IMPLEMENTED IN THE EUROPEAN UNION MEMBER STATE WHERE YOU PURCHASED THE PRODUCT. FURTHER, WHILE THIS LIMITED WARRANTY GIVES YOU SPECIFIC LEGAL RIGHTS, YOU MAY HAVE OTHER RIGHTS WHICH MAY VARY FROM EU MEMBER STATE TO EU MEMBER STATE OR, IF YOU DID NOT PURCHASE THE PRODUCT IN AN EU MEMBER STATE, IN THE COUNTRY YOU PURCHASED THE PRODUCT WHICH MAY VARY FROM COUNTRY TO COUNTRY AND JURISDICTION TO JURISDICTION.

Return Material Authorization Policy

Before returning a product directly to Oztek you must obtain a Return Material Authorization (RMA) number and the correct factory "Ship To" address. Products must also be shipped prepaid. Product shipments will be refused and returned at your expense if they are unauthorized, returned without an RMA number clearly marked on the outside of the shipping box, if they are shipped collect, or if they are shipped to the wrong location. When you contact Oztek to obtain service, please have your instruction manual ready for reference and be prepared to supply:

- The serial number of your product
- Information about the installation and use of the unit
- Information about the failure and/or reason for the return
- A copy of your dated proof of purchase

Return Procedure

Package the unit safely, preferably using the original box and packing materials. Please ensure that your product is shipped fully insured in the original packaging or equivalent. This warranty will not apply where the product is damaged due to improper packaging. Include the following:

- The RMA number supplied by Oztek clearly marked on the outside of the box.
- A return address where the unit can be shipped. Post office boxes are not acceptable.
- A contact telephone number where you can be reached during work hours.
- A brief description of the problem.

Ship the unit prepaid to the address provided by your Oztek customer service representative.

If you are returning a product from outside of the USA or Canada - In addition to the above, you MUST include return freight funds and you are fully responsible for all documents, duties, tariffs, and deposits.

Out of Warranty Service

If the warranty period for your product has expired, if the unit was damaged by misuse or incorrect installation, if other conditions of the warranty have not been met, or if no dated proof of purchase is available, your unit may be serviced or replaced for a flat fee. If a unit cannot be serviced due to damage beyond salvation or because the repair is not economically feasible, a labor fee may still be incurred for the time spent making this determination.

To return your product for out of warranty service, contact Oztek Customer Service for a Return Material Authorization (RMA) number and follow the other steps outlined in "Return Procedure".

Payment options such as credit card or money order will be explained by the Customer Service Representative. In cases where the minimum flat fee does not apply, as with incomplete units or units with excessive damage, an additional fee will be charged. If applicable, you will be contacted by Customer Service once your unit has been received.