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# Implementing Metric Driven Methodology that Accelerates Verification Predictability and Automation

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# Sondrel’s Project Flow

- Planning Phase
- Development Phase
- Execution Phase

- Each phase has a Sign Off Requirement.

# Planning Phase

Defines the strategy for verifying the design under test.

Two documents are  developed during this phase

1. Verification Plan Document
2. Verification Architecture Document

# Planning Phase: Verification Plan Development

- Lists the cover points, checkers and testcases
- This plan links detailed feature lists to cover points, checkers and testcases, which allows to track progress and measure it against the plan
- Milestones / Checkpoints are set for metrics

# Sample of the document

| Verification Requirement ID (VREQ-ID) | Design Feature | Covergroup | Checker |
|---|---|---|---|
| **Interface1** | | | |
| VREQ01 | Design feature 1 for interface1 | cg_if1_f1 | Assertion/Model/Scoreboard/Register Predictor |
| VREQ02 | Design feature 2 for interface1 | cg_if1_f2 | Assertion/Model/Scoreboard/Register Predictor |
| VREQ03 | Design feature 3 for interface1 | cg_if1_f3 | Assertion/Model/Scoreboard/Register Predictor |
| **Interface2** | | | |
| VREQ04 | Design feature 1 for interface2 | cg_if2_f1 | Assertion/Model/Scoreboard/Register Predictor |
| VREQ05 | Design feature 2 for interface2 | cg_if2_f2 | Assertion/Model/Scoreboard/Register Predictor |
| VREQ06 | Design feature 3 for interface2 | cg_if2_f3 | Assertion/Model/Scoreboard/Register Predictor |

# Planning Phase: Verification Architecture Document

This document gives the detailed testbench architecture along with description of testbench components. It mainly should contain:

- Testbench Block Diagram
- Testbench Stimulus and Checking Mechanism
- VIP Details
- It also includes the description of the methodology , EDA tools used

# Planning Phase Sign Off

- Sign off document lists a number of tasks that need to be completed to properly sign-off this phase and it is filled by stake holders
- Project Manager, Verification engineers and Design engineer reviews sign-off document along with Verification Expert and a Design Expert
- First review is called by verification engineer verifying that block
- Can be repeated a number of times to make sure all requirements of the sign-off document have been accomplished

# Sign-Off Requirements

| S. No. | Tasks | Status |
|---|---|---|
| 1. | Check if the verification plan follows the standard verification plan template? | Y/N |
| 2. | Check if the verification strategy for the DUT has been reviewed? | Y/N |
| 3. | Check if all the features of the DUT been captured in the verification plan? | Y/N |
| 4. | Check if all action items, which were identified during review meetings been taken care off? | Y/N |
| 5. | Check if the re-usability of the verification components from other blocks been considered? | Y/N |
| 6. | Check if the possibility of usage of off the shelf VIPs been considered? | Y/N |
| 7. | Check if the verification plan has considered all modes of operation of the DUT? | Y/N |

# Sign-Off Requirements

| S. No. | Tasks | Status |
|---|---|---|
| 8. | Check if all action items, which were identified during review meetings been taken care off? | Y/N |
| 9. | Check if for every feature of the DUT, a cover point has been identified in the verification plan? | Y/N |
| 10. | Check if for every feature of the DUT, a checker has been identified in the verification plan? | Y/N |

# Development Phase

The second phase in the project is the Development phase.

- Testbench code must be readable, well commented and must strictly follow the Customer’s Methodology
- Testcases should be constrained random and should not use complex constraint that require high compute resources
- Checkers/Scoreboards should be re-usable at the top level

# Development Phase: Sign Off Phase

- Verification Development Sign-off document is filled in by the Project Manager, Verification Engineer, Design Engineer, Verification Expert, Design Expert
- These people are also  responsible for reviewing the development phase

# Execution Phase

- Involves execution of the test-cases developed in the development phase
- Verification management tool in use generates functional and code coverage figures

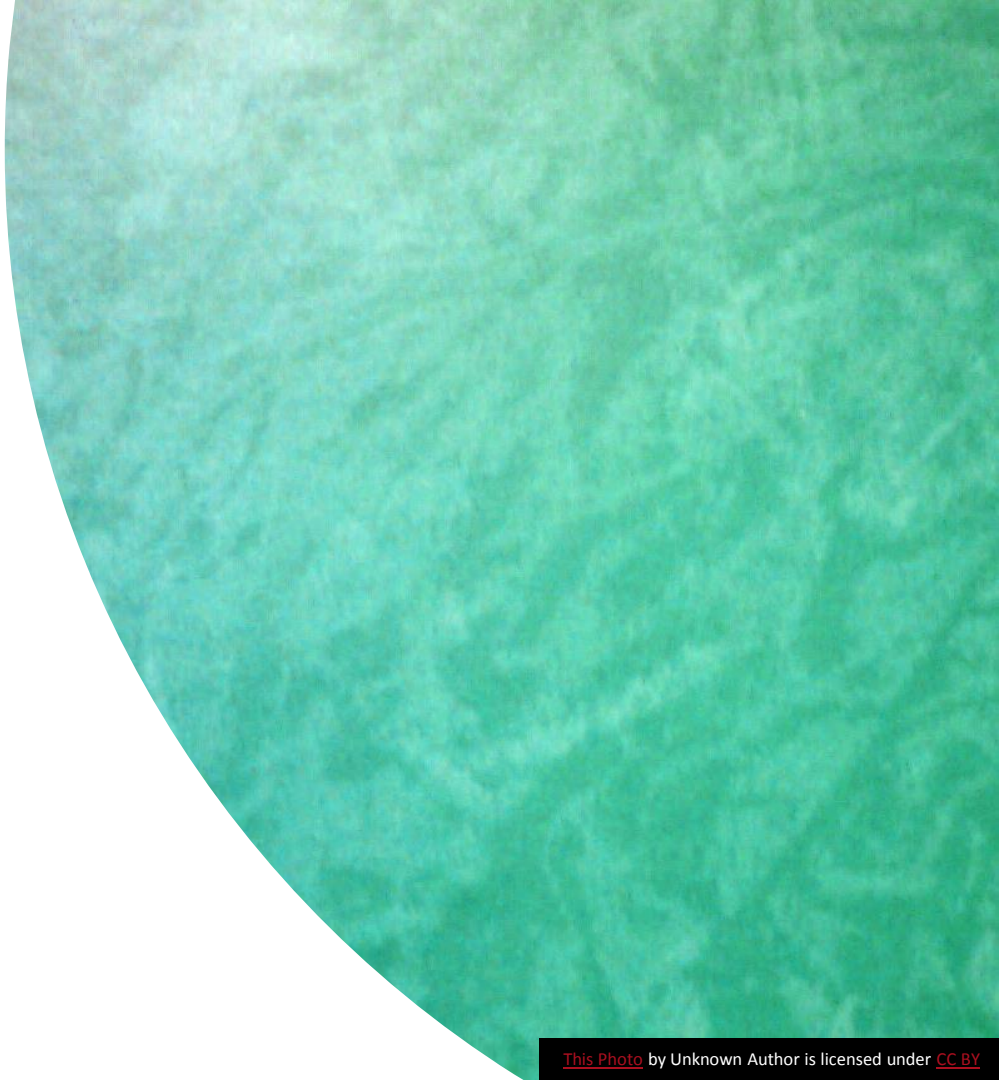
# Execution Phase: Review Process

It is based on verification execution sign-off document which is filled in by the Design Engineer, Verification Engineer.

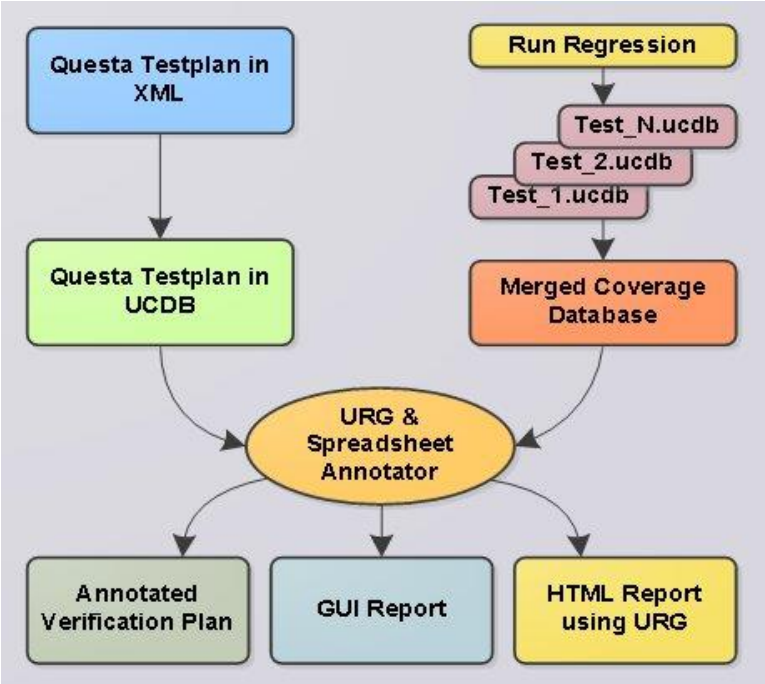
- Review if all coverage goals are met
- Multiple reviews can be conducted to make sure all required tasks are accomplished

# Case Study

- Introduction
- The design was ~400kgate



# Case Study: Typical Flow

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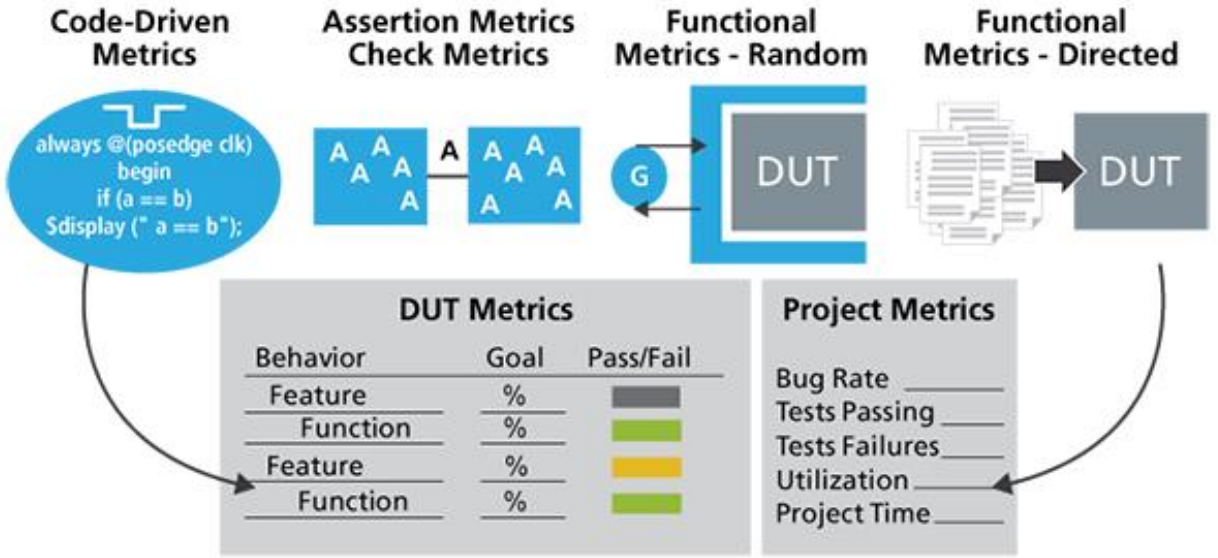
# Different Metrics

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# Case Study: Planning Phase

## TestPlan

- Questa Testplan  was used and  have used the MS Excel to create TestPlan as suggested by Mentor.
- We had to install Questa add-in which is open source and freely available

Sample of the TestPlan

| Section | Title | Description | Link | Type | Weight | Goal |
|---|---|---|---|---|---|---|
| 1 | | | | | | |
| 1.1 | | | | | | |
| 1.2 | | | | | | |

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# Case Study: Development Phase

- In this particular project, the methodology used was UVM.
- Questa VIPs were integrated as monitors for Protocol Check and to collect Functional Coverage.
- Assertions were used for specific interfaces e.g.: QChannels, PChannels
- Metrics like Code, Branch, Toggle, FEC, Functional, Assertions Coverages were collected measured.

# Sample Questa TestPlan in HTML


| Scope | Coverage | % of Goal | Bins | Hits | % Hit | Description | Link Status | Weight | Goal |
|---|---|---|---|---|---|---|---|---|---|
| 1 Coverage Plan | 63.69% | 63.69% | 5354 | 4381 | 81.82% | | Partial | 1 | 100% |
| 1.1 Transmitter | 37.71% | 37.71% | 1413 | 1048 | 74.16% | The transmitter is able to transmit frames in a number of different | Partial | 1 | 100% |
| 1.2 Pre-processor | 81.25% | 81.25% | 10 | 7 | 70.00% | The pre-processor needs to regonise frame patterns from all the | Clean | 1 | 100% |
| 1.3 Post-processor | 48.95% | 48.95% | 26 | 14 | 53.84% | The Post Processor extacts data from the frame store based on the | Clean | 1 | 100% |
| 1.4 Frame_Store_Arbitrator | 100.00% | 100.00% | 8 | 8 | 100.00% | The arbitrator function sits between the BONDING chip and the | Clean | 1 | 100% |
| 1.5 Micro processor_Interface | 75.90% | 75.90% | 510 | 365 | 71.56% | The micro processor interface is used to set-up the chip and read back its | Clean | 1 | 100% |
| 1.6 All_Code_Coverage | 86.53% | 86.53% | 3367 | 2932 | 87.08% | | Clean | 1 | 100% |
| 1.7 All_Assertions | 16.66% | 16.66% | 12 | 2 | 16.66% | | Clean | 1 | 100% |
| 1.8 Functional Coverage Example | 62.50% | 62.50% | 8 | 5 | 62.50% | | Clean | 1 | 100% |

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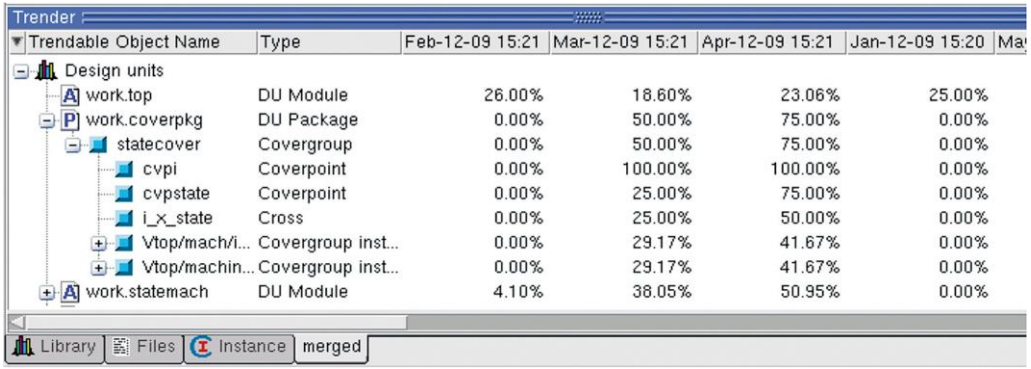
# Case Study: Trend Analysis using Questa

Trend Reporting helped to keep the track on the Coverage trend

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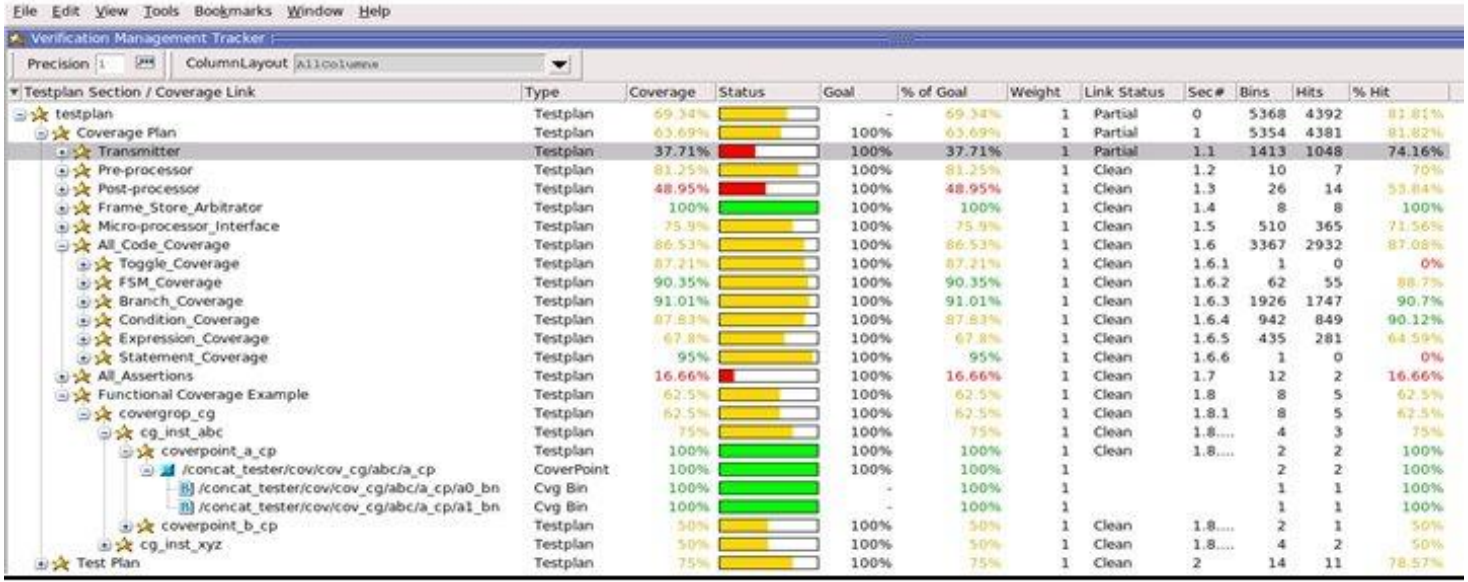
# Example of Metric Tracking




| Testplan Section / Coverage Link | Type | Coverage | Status | Goal | % of Goal | Weight | Link Status | Sec# | Bins | Hits | % Hit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| testplan | Testplan | 69.34% | | - | 69.34% | 1 | Partial | 0 | 5368 | 4392 | 81.81% |
| Coverage Plan | Testplan | 63.69% | | 100% | 63.69% | 1 | Partial | 1 | 5354 | 4381 | 81.82% |
| Transmitter | Testplan | 37.71% | | 100% | 37.71% | 1 | Partial | 1.1 | 1413 | 1048 | 74.16% |
| Pre-processor | Testplan | 81.25% | | 100% | 81.25% | 1 | Clean | 1.2 | 10 | 7 | 70% |
| Post-processor | Testplan | 48.95% | | 100% | 48.95% | 1 | Clean | 1.3 | 26 | 14 | 53.84% |
| Frame_Store_Arbitrator | Testplan | 100% | | 100% | 100% | 1 | Clean | 1.4 | 8 | 8 | 100% |
| Micro-processor_Interface | Testplan | 75.9% | | 100% | 75.9% | 1 | Clean | 1.5 | 510 | 365 | 71.56% |
| All_Code_Coverage | Testplan | 86.53% | | 100% | 86.53% | 1 | Clean | 1.6 | 3367 | 2932 | 87.08% |
| Toggle_Coverage | Testplan | 87.21% | | 100% | 87.21% | 1 | Clean | 1.6.1 | 1 | 0 | 0% |
| FSM_Coverage | Testplan | 90.35% | | 100% | 90.35% | 1 | Clean | 1.6.2 | 62 | 55 | 88.7% |
| Branch_Coverage | Testplan | 91.01% | | 100% | 91.01% | 1 | Clean | 1.6.3 | 1926 | 1747 | 90.7% |
| Condition_Coverage | Testplan | 87.83% | | 100% | 87.83% | 1 | Clean | 1.6.4 | 942 | 849 | 90.12% |
| Expression_Coverage | Testplan | 67.8% | | 100% | 67.8% | 1 | Clean | 1.6.5 | 435 | 281 | 64.59% |
| Statement_Coverage | Testplan | 95% | | 100% | 95% | 1 | Clean | 1.6.6 | 1 | 0 | 0% |
| All_Assertions | Testplan | 16.66% | | 100% | 16.66% | 1 | Clean | 1.7 | 12 | 2 | 16.66% |
| Functional Coverage Example | Testplan | 62.5% | | 100% | 62.5% | 1 | Clean | 1.8 | 8 | 5 | 62.5% |
| covergrop_cg | Testplan | 62.5% | | 100% | 62.5% | 1 | Clean | 1.8.1 | 8 | 5 | 62.5% |
| cg_inst_abc | Testplan | 75% | | 100% | 75% | 1 | Clean | 1.8.... | 4 | 3 | 75% |
| coverpoint_a_cp | Testplan | 100% | | 100% | 100% | 1 | Clean | 1.8.... | 2 | 2 | 100% |
| /concat_tester/cov/cov_cg/abc/a_cp | CoverPoint | 100% | | 100% | 100% | 1 | | | 2 | 2 | 100% |
| /concat_tester/cov/cov_cg/abc/a_cp/a0_bn | Cvg Bin | 100% | | - | 100% | 1 | | | 1 | 1 | 100% |
| /concat_tester/cov/cov_cg/abc/a_cp/a1_bn | Cvg Bin | 100% | | - | 100% | 1 | | | 1 | 1 | 100% |
| coverpoint_b_cp | Testplan | 50% | | 100% | 50% | 1 | Clean | 1.8.... | 2 | 1 | 50% |
| cg_inst_xyz | Testplan | 50% | | 100% | 50% | 1 | Clean | 1.8.... | 4 | 2 | 50% |
| Test Plan | Testplan | 75% | | 100% | 75% | 1 | Clean | 2 | 14 | 11 | 78.57% |

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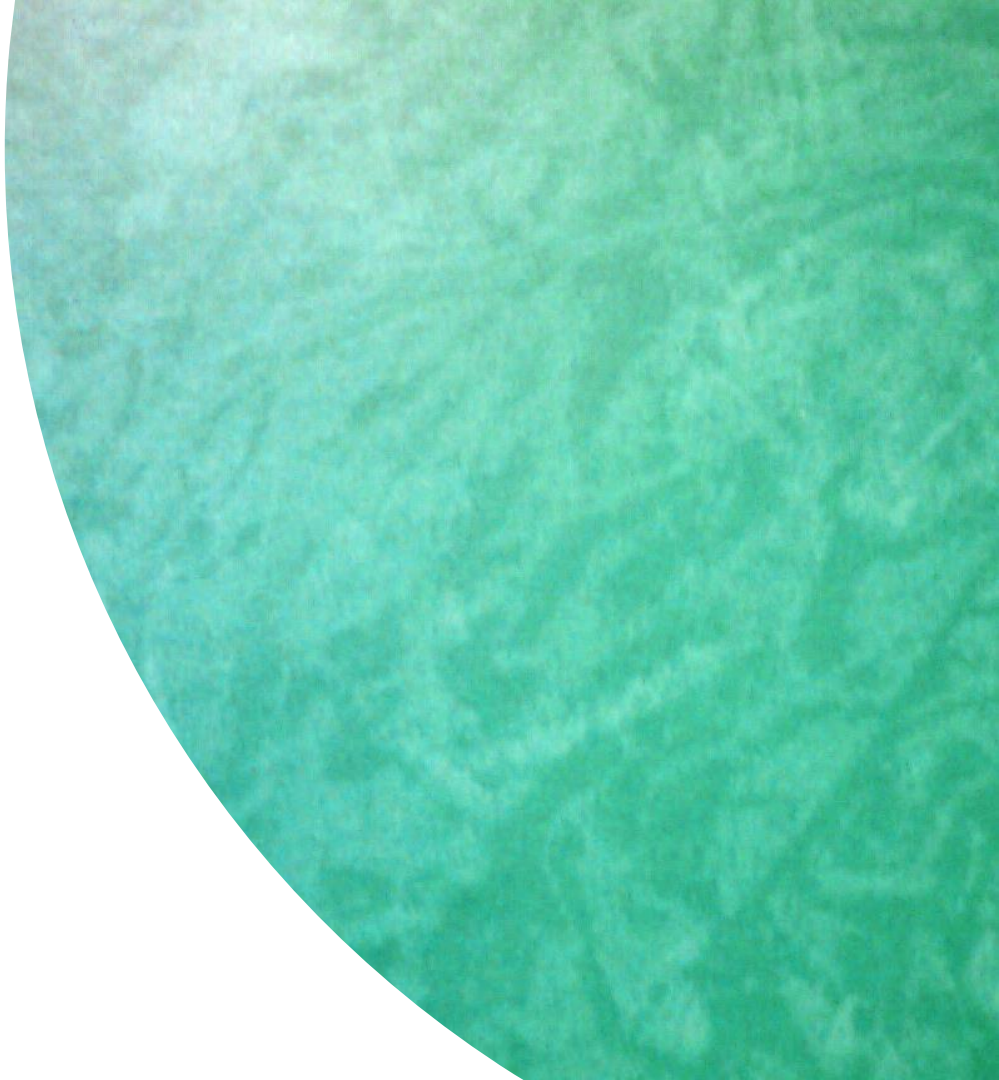
# Case Study: Reviews

- Early reviews were conducted to make sure that there was traceability
- All the signoff documents were signed off after the reviews by relevant stake holders.

# Summary

Following all the best practices, and using a Verification Planner, helped in achieving predictability and helped us keep a tab on Verification Effort .



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