PCIe vs. SDIO Wi-Fi

Choosing the Right Solution for your Freescale i.MX-based Product

The i.MX series of processors unleashes a scalable multicore platform that includes single-, dual- and quad-core families based on the ARM® Cortex™-A9 architecture for next-generation consumer, industrial and automotive applications.

This white paper will provide information on the trade-offs between PCIe and SDIO Wi-Fi Radios to help you select the right Wi-Fi technology for your i.MX-based product.

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Executive Summary

As a device manufacturer, you may be evaluating the new Freescale i.MX6 or i.MX7 processor.

Wi-Fi is becoming ubiquitous, finding its way into all sorts of devices including those in consumer, industrial and automotive applications. But there are several Wi-Fi technology options available from multiple suppliers. Specifically, most i.MX6 and i.MX7 support interface options to add either a SDIO or PCIe radio module.

So, which Wi-Fi radio interface is best for your application?

While this guide was written specifically for device manufacturers who need to integrate Wi-Fi for the Freescale i.MX 6 and i.MX7 platform, the general principles are not specific to Freescale application processors. Based on Silex Technology's decades of experience providing embedded networking solutions, we have written this guide to help you understand the pros and cons of different Wi-Fi radio options.

This white paper will focus on the impact that the radio's host bus has on the system performance. First, the PCIe and SDIO communications busses will be explained in a general overview. Power considerations for both busses will be discussed and analyzed. Finally, actual throughput testing results will be provided as real-world performance examples.

"Wi-Fi connectivity is a key feature for customers designing products based on our i.MX 6 series processors. Silex Technology delivers outstanding technology engineered to help our i.MX 6 customers differentiate and win in competitive markets."
- Rajeev Kumar, i.MX product manager at Freescale Semiconductor

Wi-Fi Radio Interface Options and Freescale i.MX6 and i.MX7 Support

When choosing a radio module, many design considerations must be taken into account. Host processor, available communications busses, driver architecture, power consumption, and data throughput requirements are all key factors that influence the design decision.

Choosing a radio host interface bus may seem like a minor consideration. However, selecting the proper communication bus between the host and the radio can be a driving factor for picking the correct module. Radio modules are inherently a means of data communication, so the way the data is transmitted and processed is critical to the overall function of the module.

There are a number of Wi-Fi radio interface options. Below is a summary of the most common:

PCIe

PCI Express (Peripheral Component Interconnect Express), officially abbreviated as PCIe, is a high-speed serial computer expansion bus standard designed to replace the older PCI, PCI-X, and AGP bus standards. PCIe radios are commonly found in computers and are used in devices like access points that require high throughput.

SDIO

SDIO (Secure Digital Input Output) card is an extension of the SD specification to cover I/O functions. SDIO cards are only fully functional in host devices designed to support their input-output functions. Typical applications include tablets, smart phones and other battery powered devices.

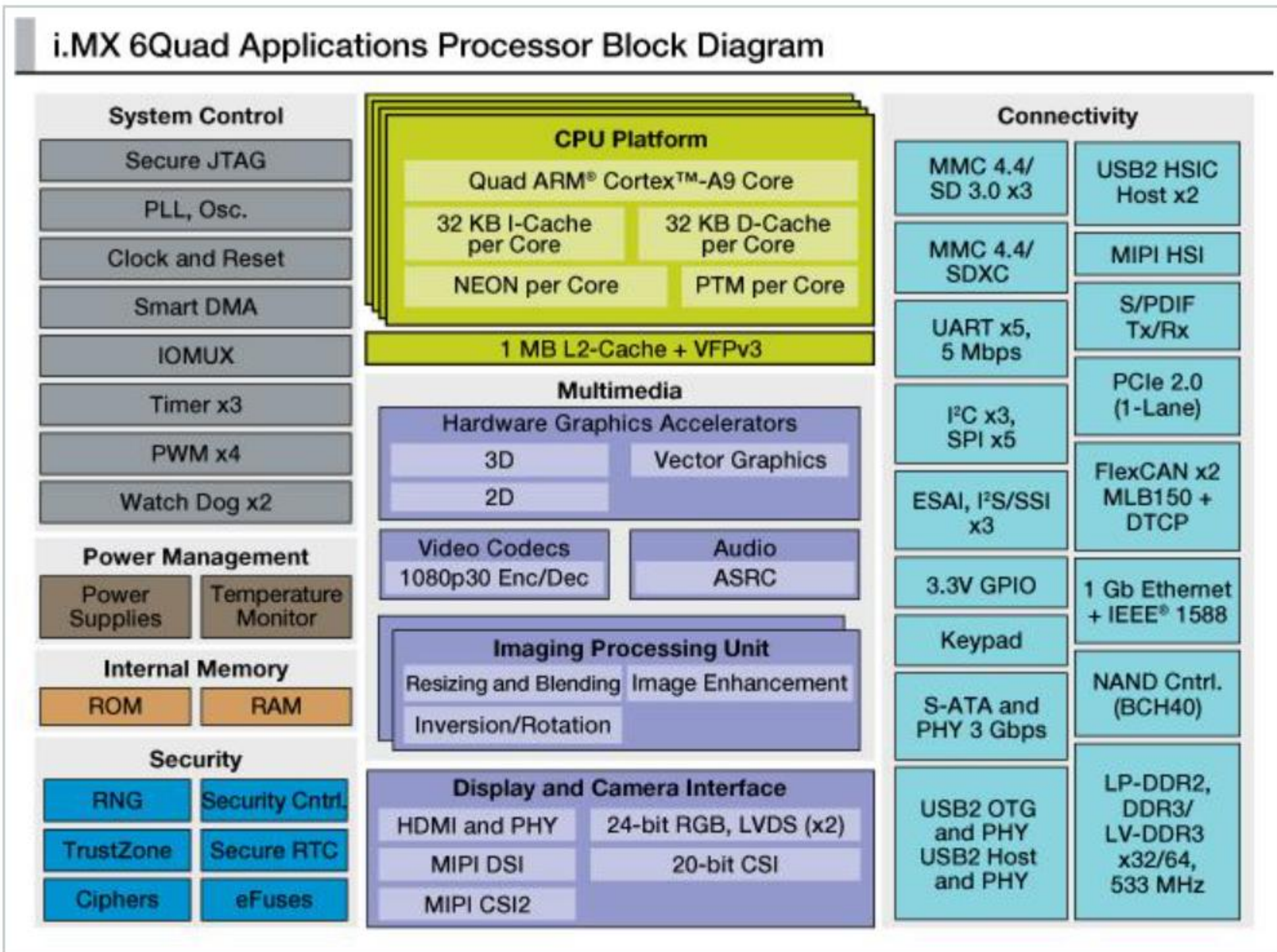
USB

USB, short for Universal Serial Bus, is an industry standard developed in the mid-1990s that defines the cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices. USB Wi-Fi radios are typically external dongles for consumer devices like PC's and TV's.

SPI/UART

The Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. A universal asynchronous receiver/transmitter, abbreviated UART, is a computer hardware device that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as RS-232, RS-422 or RS-485. SPI/UART radios are low performance so they are ideal for MCU based (i.e. Freescale Kinetis) IoT applications.

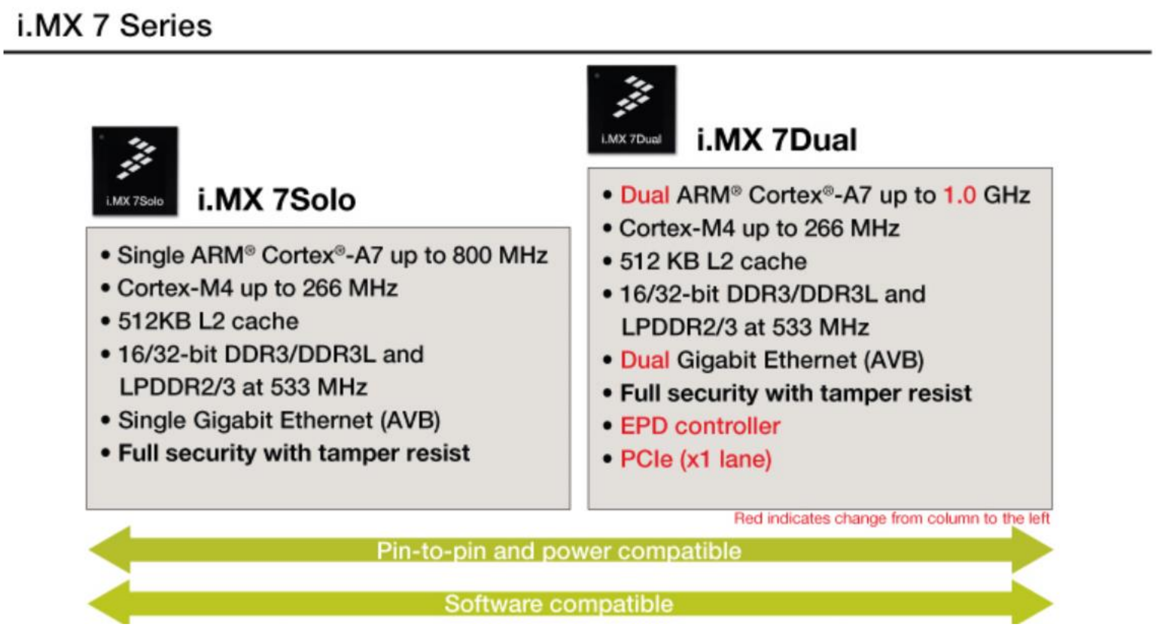
Since USB Wi-Fi radios are targeted for non-embedded consumer applications and SPI/UART Wi-Fi radios have a maximum throughput of 10 Mbps, this white paper will focus on the relative merits of PCIe and SDIO Wi-Fi radios.



The above block diagram for the Freescale i.MX6 Quad application processor shows many connectivity options. Of course, some of the interfaces may be used for other purposes and may not be available for the Wi-Fi radio.

All i.MX6 applications processors support both SDIO and PCIe, with the exception of the low-end options (specifically i.MX6 Solo Lite and Ultra Lite). As you will learn later, this is because the target applications for the entry level i.MX6 processors will typically not require the higher performance of a PCIe radio.

i.MX7 will be similar where the entry level SKU (i.MX7 Solo) supports SDIO but does not support PCIe while the high end SKU (i.MX7 Dual) supports both SDIO and PCIe.



Theoretical Maximum Throughput

This section defines both the PCIe and SDIO bus, as well as provides calculations for the maximum available throughput based on physical bus constraints. These calculations define the high end throughput cap on data transmission over each bus.

Wi-Fi theoretical throughput will also be reviewed to help identify where the performance bottleneck may occur in your application.

PCIe Bus Overview

PCIe, or PCI Express, is a replacement for the older PCI (Peripheral Component Interconnect) bus standard. PCIe has a number of improvements over the older standard, including a higher maximum system bus throughput, lower I/O pin count and smaller physical footprint, and better performance scaling for bus devices.

PCIe devices communicate over a logical connection known as a link. The PCIe link is built around dedicated unidirectional differential wire pairs of serial, point-to-point connections, known as lanes. This is in contrast to the earlier PCI connection, which is a bus-based system where all the devices share the same bidirectional parallel bus.

PCIe Wi-Fi modules operate as endpoints in the PCIe fabric system. Due to the widespread use in high data rate transfer applications, PCIe is ideally suited to Wi-Fi peripherals requiring high throughput.

Silex PCIe radio modules use a single lane PCIe v1.1 bus, providing a theoretical bit transfer speed of up to 2.5 Gbps. Since PCIe v1.1 uses 8B/10B byte conversion, you can see from the below equation that the maximum throughput for a single, bidirectional lane is 500 MB/s: 250MB/s from Master to Slave and 250 MB/s from Slave to Master.

$$PCIe\ Theoretical\ Max\ Bandwidth\ (B/s) = \frac{2.5Gbps \times (bidirectional) \times (\#\ of\ Lanes)}{10\ bits/byte}$$

Embedded processors, such as the Freescale i.MX6 family, use PCIe as an expansion port for added connectivity into the processor. The i.MX6 processor uses a PCIe v2.0 bus with 1 lane of data available. PCIe v2.0 increases the transfer rate to 5 gigabits/s (or 1000 MB/s), and is backwards compatible with modules, like the Silex devices, that use PCIe v1.1.

SDIO Bus Overview

SDIO, or Secure Digital Input Output, is designed as an extension of the SD memory card specification to cover I/O functions. It is used primarily in small embedded devices where either additional memory or I/O functionality can be added to a host controller. While SDIO and SD memory card interfaces are mechanically and electrically identical, SDIO modules can only be used with host devices that support the SDIO driver functionality, like the i.MX6Q from Freescale.

The SDIO standard, maintained by the SD Association (SDA), is currently at version v4.1, as with all previous versions the latest one is backward compatible with the previous releases. The small form factor, low pin count on the interface and availability of SDIO buses on a wide range of embedded CPU devices has made the SDIO interface one of the most popular choices for I/O expansion and memory enhancement.

Silex SDIO radio modules conform to the SDIO 2.0 HS specification, providing transfer of 4 data bits SDR (Single Data Rate). Assuming a 50MHz clock (i.MX6 SDIO controller), we see that the theoretical maximum speed is 200 Mbps for SDIO.

$$Theoretical\ Maximum\ (bits/s) = (\#\ of\ data\ lines)\ \times (clock\ speed)$$

The 200 Mbps transfer speed for SDIO radios is an order of magnitude slower than the 2.5 Gbps transfer speed of PCIe. This speed difference comes with a commensurate increase in power to utilize the bus. This is described in the power considerations section.

For this reason, SDIO radio modules are typically selected when low power embedded connectivity is required over high data throughput. The 200Mbps theoretical limit makes SDIO better suited to client applications with lower bandwidth requirements. The PCIe bandwidth capability makes it the best choice for high band width applications like Wi-Fi Access Points, routers and HD video clients.

Wi-Fi Technology Throughput Limitations

It is important to also have a basic understanding of theoretical Wi-Fi performance. Without going into the details behind the data, 802.11ac provides higher throughput than the older 802.11n standard, primarily because it can transmit data through a wider “pipe” (i.e. 80 Mhz). The other major factor is the number of spatial streams that are supported (1SS in the chart below indicates 1 spatial stream). More commonly a Wi-Fi radio that supports 1 spatial stream will be referred to as 1x1 or single stream.

- **Maximum datarates (in Mbps) for each channel width**

	802.11n 1SS	802.11n 2SS	802.11n 3SS	802.11ac 1SS	802.11ac 2SS	802.11ac 3SS
20 MHz	72.2	144.4	216.7	96.3	192.6	288.9
40 MHz	150	300	450	200	400	600
80 MHz	N/A	N/A	N/A	433.3	866.7	1,300

System Performance Implications

Using the theoretical maximum throughput for the PCIe and SDIO bus interfaces, compared with 802.11n and 802.11ac performance, we get the following chart:

	Wi-Fi Performance	PCIe Bus	SDIO Bus
802.11n (1x1)	150 Mbps	2500 Mbps	200 Mbps
802.11n (2x2)	300 Mbps	2500 Mbps	200 Mbps
802.11n (3x3)	450 Mbps	2500 Mbps	200 Mbps
802.11ac (1x1)	433 Mbps	2500 Mbps	200 Mbps
802.11ac (2x2)	867 Mbps	2500 Mbps	200 Mbps
802.11ac (3x3)	1300 Mbps	2500 Mbps	200 Mbps

PCIe vs. SDIO Performance Summary

- PCIe bus provides sufficient bandwidth to support any of the above radios (including high end 802.11ac implementations). Note that there may be other system bottlenecks.
- SDIO bus bandwidth limits the performance of most Wi-Fi radios. There may be some moderate performance improvement moving from 802.11n 1x1 to a 802.11n 2x2 implementation. Qualcomm Atheros does not even offer 802.11ac 2x2 radio with a SDIO interface for this very reason.
- For this white paper, Silex Technology America benchmarked single stream 802.11n PCIe and SDIO radio to compare real-life performance. While the PCIe radio provided better performance, significant gains with PCIe Wi-Fi radios would be found with 802.11n radios with more streams or with 802.11ac radios. The next revision of this white paper will include additional benchmark results.

Driver Architecture Overview

For a Wi-Fi solution, the driver consists of two major components. The driver that resides on the host and provides the channel for the host software to interact with the hardware and the radio firmware which is the functional code that performs the radio processing of the RF layer interactions and the host communications.

The driver architecture implementation may vary between Wi-Fi silicon providers. The information below describes the differences in which radio firmware is handled between Qualcomm Atheros PCIe and SDIO 802.11n radios.

Figure 1. Split MAC Host based driver block diagram

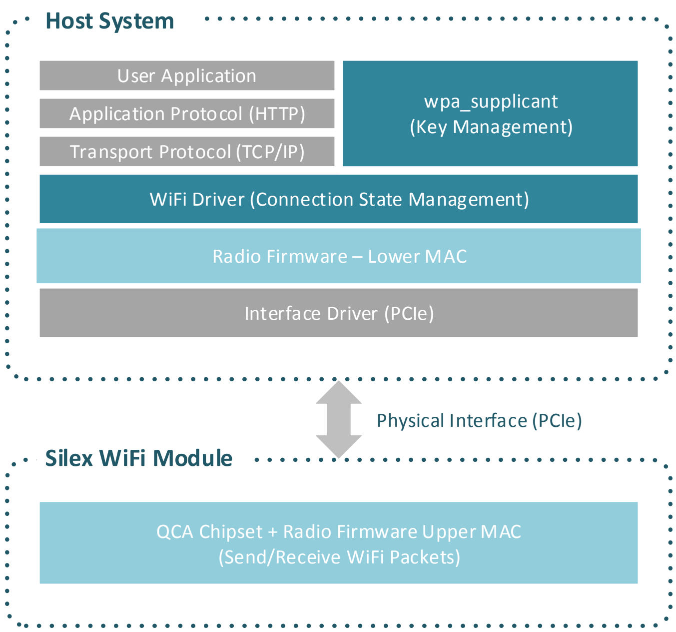


Figure 2. Full MAC Host based driver block diagram

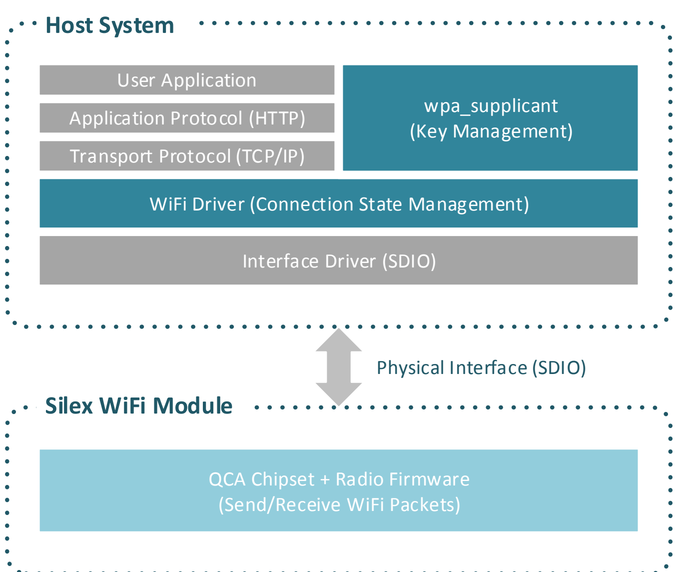


Figure 1 and Figure 2 show the driver block diagram for a host based system. Host based means that all aspects of the network communication and link maintenance are loaded and executed by the host CPU. In contrast, a hostless system would be fully encapsulated in the Wi-Fi module. While outside the scope of this white paper, the Silex Intelligent Module line and SX-ULPAN IoT modules can operate in hostless mode.

PCIe driver architecture differs from SDIO Wi-Fi driver architecture due to the inherent communication speed of the bus and the types of processors that use each peripheral set. PCIe is typically suited to a high powered, high speed processor that takes advantage of the high available throughput, while SDIO is associated with embedded processors requiring flexibility due to a limited peripheral set. As discussed previously, some embedded processors, like the Freescale i.MX6Q, offer both SDIO and PCIe as an available peripheral interface.

PCIe Radio Module Drivers

PCIe radio drivers have a higher utilization of the host processor than the SDIO drivers. They use a split MAC architecture that has the radio firmware split between the host processor and the radio module. In this configuration the radio takes advantage of the host processor to run a large part of the MAC functionality. This is in part because the total available bandwidth of the PCIe bus is so large. The traffic between the radio and host processor contains not only data but significant control and management interaction, even with this additional overhead the large bandwidth of the PCIe bus is more than capable of supporting even the fastest of today's 802.11ac radio modules.

SDIO Radio Module Drivers

Silex Technology SDIO radio modules have specialized baseband processors to ease the communications traffic back to the host processor. These modules still utilize an IP stack on the host CPU, but manage the connection and roaming functionality on the radio module level instead of the host. Radio Firmware is the code that runs on the module baseband processor, and in the case of SDIO modules from Silex Technology, is what controls and maintains the connection between the radio and the access point. The SDIO driver loads this radio firmware at runtime.

It is important to note that because the host processor does not have to manage the connection directly. SDIO bus traffic is mostly data messages instead of management messages. This split in functionality allows the host to efficiently utilize the limited bandwidth and increase overall data throughput.

In either case, the driver abstracts bus communication specifics away from the end user. However, it is important to understand the basic functionality difference because it is the underlying reason why embedded, lightweight processors typically use SDIO modules and heavy weight CPUs use PCIe modules.

Power Considerations

Perhaps the most obvious architecture consideration between PCIe and SDIO is the power required for running the two peripherals. Power is of particular concern in embedded mobile applications.

All radio modules operate with a specified current output per mode and speed. These metrics can be found in radio data sheets downloadable from the Silex website. Radio power consumption can then be calculated using the following basic formula.

$$Power\ (Watts) = Voltage\ (V) * Current\ (A)$$

Wi-Fi Radio Power Differences

Due to lower bus speeds and differences in design, SDIO radio modules consume less power than PCIe radio modules. Because current consumption is dependent on number of channels, it is important to consider the same communications mode between different radio modules. For example, the SX-SDMAN, an SDIO 1x1 module, only has one data transmission stream, and thus one RF transmit chain. The SX-PCEAN2, a PCIe 2x2 radio module has two data streams, and thus two RF transmit chains, equating to more overall power due to the repeated amplifiers.

It is best to choose similar radios (single stream with 2.4GHz) to do a direct comparison. In this case, a comparison can be performed between the SDIO and PCIe modules by looking at the SX-SDMGN, the 1x1 SDIO radio module, and the SX-PCEGN-BT, a 1x1 PCIe radio module. Both of these modules use a single chain RF transceiver, further isolating the power comparison away from the radio module to the underlying bus.

Table 1. Current and Power Consumption for Maximum Data Rate

Radio Description	*Radio Module*	*Operating Voltage (V)*	*Tx Current (mA)*	*Tx Power (mW)*
SDIO 1x1 (2.4 GHz)	SX-SDMGN	3.3	190	**627**
SDIO 1x1 (2.4/5 GHz)	SX-SDMAN	3.3	260	**858**
PCIe 1x1 (2.4 GHz)	SX-PCEGN-BT	3.3	295	**973.5**
PCIe 2x2 (2.4/5 GHz)	SX-PCEAN2	3.3	560	**1,848**

The transmit power for the SX-SDMGN is 627mW while the transmit power for the same settings for the SX-PCEGN-BT is 973.5mW. Because the signal chains of the radio modules are roughly equivalent, the 35% difference in power can be attributed to the difference in bus power consumption.

PCIe vs. SDIO Power Consumption Summary

- There is a significant power reduction (i.e. 35%) when comparing PCIe and SDIO radio modules with like configurations (single stream, 2.4GHz).
- There are potentially additional system performance benefits that can be realized from using a Silex SDIO radio modules. Because SDIO radios utilize a Full MAC architecture, SDIO radios offload the host processor and is one reason why embedded, lightweight processors typically use SDIO modules and heavy weight CPUs use PCIe modules.
- If you start comparing PCIe radio modules with multiple streams (i.e. 2x2 or 3x3) vs. single stream SDIO radio modules, the power requirements increase dramatically. PCIe radio modules that support 802.11ac will require even more power.

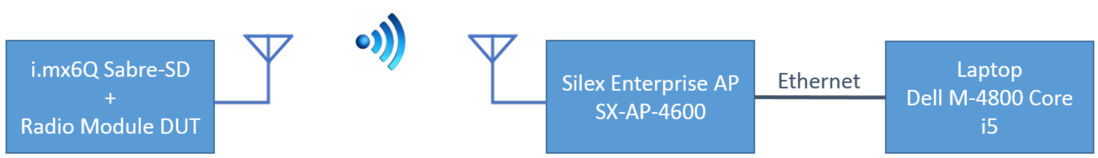
Throughput Testing (PCIe vs. SDIO)

This section presents real-world results from throughput testing performed on both PCIe (SX-PCEGN-BT) and SDIO (SX-SDMAN) radio modules from Silex Technology. The purpose of the real-world testing was to observe the impact the bus interface, host processor, and radio driver would have on actual data throughput performance.

Each test used the Freescale i.MX6Q Sabre-SD Reference Board (MCIMX6Q-SDB) as the host processor for the radios. A Silex SX-AP-4800 enterprise access point was used as the reference network access point to which the radios connected. A Dell Precision M-4800 (i5-4210M CPU) laptop was connected, to the SX-AP-4800 via the wired LAN port. The laptop acted as the network host platform. This setup is shown below.

All tests were run 10 times using the above environment. iperf, a common network measurement tool was used to generate data traffic and measure the throughput. The iperf test was run using the PC as the server and the i.MX6Q Sabre-SD as client. The test was then repeated with the i.MX6Q Sabre-SD being the server and PC as the client.

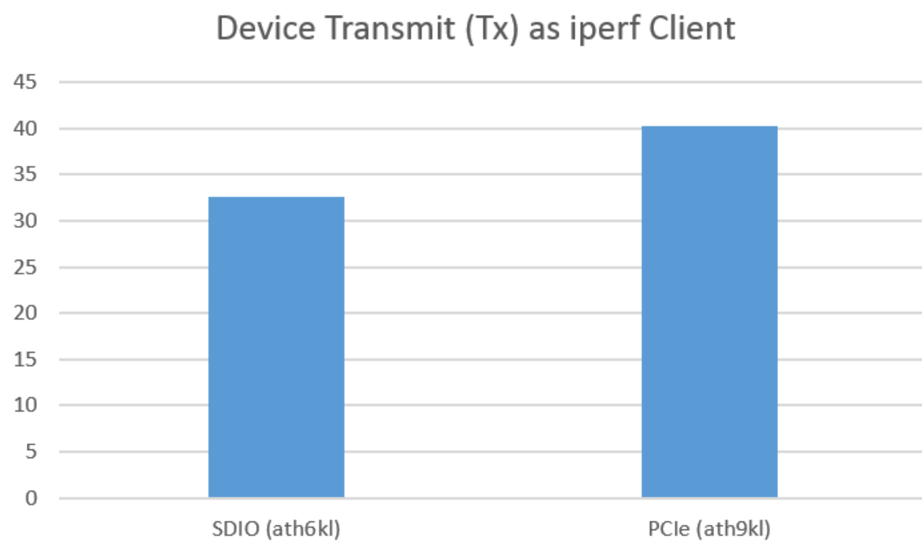
The PCIe (SX-PCEGN-BT) was tested using the Linux open source ath9K driver while the SDIO (SX-SDMAN) was tested using the Linux open source ath6K driver.

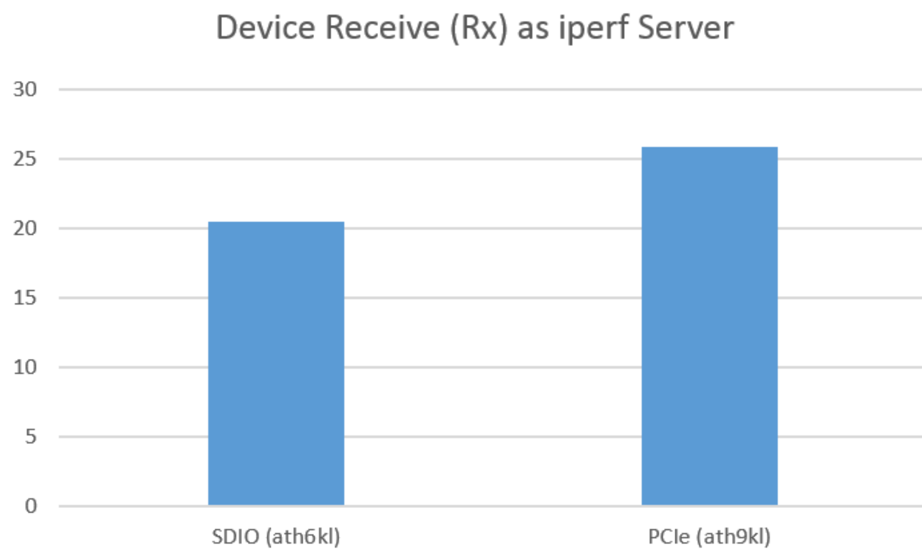


The SX-SDMAN is a dual-band 802.11a/b/g/n 1x1 SDIO module plus Bluetooth v4.0 that is based on the Qualcomm Atheros AR6233 SiP. This radio has a maximum link rate of 135 Mbps and supports SDIO v2.0. The SX-PCEGN-BT is a 1x1 single band 2.4 GHz PCIe module that includes Bluetooth. It uses the AR9485 radio and has a link rate of 150 Mbps.

Performance was measured in the 2.4GHz band only, using the setup shown below:

AP	SX-AP-4800, 2.4 GHz band, HT20
Device Under Test (DUT)	Freescale i.MX6Q Sabre-SD
PC	Dell Precision M-4800 (i5-4210M CPU)
Driver	ath6kl & ath6kl open source





As you would expect the PCIe radio (SX- PCEGN-BT) had the better throughput. This was expected given the advantage the PCIe interface and driver architecture provide. It can be seen above that the SDIO radio (SX-SDMAN) had a throughput of 32.6 Mbps, while the PCIe radio (SX-PCEGN-BT) had a throughput of 40.2 Mbps over the 10 tests performed in in transmit mode. These numbers offer the most direct comparison between the PCIe and SDIO bus as both modules use a 1x1 architecture and were tested on the same platform.

The test results above do not provide conclusive evidence which of the differences between test platform, host interface and driver architecture contributed more significantly to the delta in performance. However it is safe to assume each contributed in some way.

Finally, the link rate of the data frames was monitored during the benchmarks with AirPcap (typically between 58.5 and 65.0 Mbps). The difference between link rate and actual throughput should be understood. Link rate is the negotiated speed in bits per second that data can transfer between the Access Point and Client in an 802.11 network. The link rate states the theoretical maximum bandwidth available for the connection, but is not the same as actual measured throughput for a number of reasons. There is an efficiency limit due to frame header and message overhead in the Wi-Fi data packets, bandwidth absorption in the maintenance of the WLAN MAC, as well as overhead in the TCP protocol. Throughput is further affected by the ability for the firmware code at the MAC layer to process the messages. For these reasons, actual throughput is always markedly lower than link rate.

Conclusion

Reviewing the host bus performance against project needs is critical to overall success. Choosing the wrong component in any of the sections above can result in poor performance in different areas of the overall system, and therefore produce a non-viable end product. Processor type, available peripherals, driver architecture requirements, and power considerations all come together to form the final design decision.

The data clearly shows the difference in performance between the radios. As would be expected the PCIe host interface radio was able to provide higher data throughput against the SDIO radio modules. Additionally, power consumption of the different modules should be taken into account in relation to overall system specifications and design. It was shown that the PCIe module consumed more power than the corresponding SDIO module. It should also be noted that PCIe modules with multiple data streams will significant increase the power consumption.

It is important to understand that the throughput testing above shows the implementation of a specific system with a specific AP in a specific environment. These results will vary per system, but do provide a reasonable baseline.

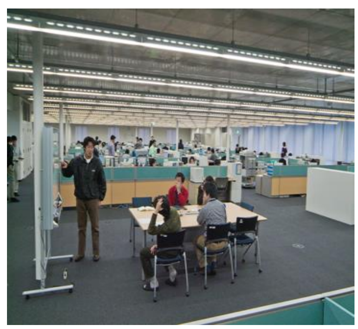
About Silex Technology

Silex Technology, Inc. has built its brand and business with a commitment to technology innovation, reliable products, quality manufacturing and premier customer support. Our core technology is being shipped all over the world today in products and as embedded network solutions for leading manufacturers.

Silex Technology America, Inc. (STA) is a wholly owned subsidiary of Silex Technology Inc. (STI), a $40M dollar and OEM supplier of leading-edge network technology that enables devices to have wired and wireless connectivity. STI was recently acquired by the Muratec family of companies in Japan. Muratec is a $1.75B, private company well known for their driven commitment to innovation and development of products that change the lives of people at home and in the work place.

At Silex Technology, we serve technical decision makers in companies that know reliable wireless connectivity is of paramount concern for product success and customer satisfaction. To get a Wi-Fi solution for your product, device, or machine, you need a trusted partner with proven design expertise in wireless technology to develop and deliver a connectivity solution you can trust.

You make it – from medical device to document imaging product to video or digital display – and Silex Technology will connect it to the network. With our expertise, we transform your products into reliable wireless devices and machines that deliver a completely connected, always-on experience for your customers.



Engineering

Building on more than 40 years of hardware and software connectivity know-how and IP, custom design experience, and manufacturing capabilities, we bring value to customers with a foundation of technical expertise. As an exclusive Qualcomm Atheros Authorized Design Center, we provide leading wireless technology with support that is unmatched anywhere in the world. Our wireless experts create a customized reliable network connectivity solution for your specific requirements and support you from design through deployment.

With relentless attention to quality, exclusive access to Qualcomm Atheros expertise, in-house manufacturing, and strategic partnerships with leading real-time operating system (RTOS) and semiconductor providers, we are the trusted leader in reliable connectivity solutions. We work with companies that need a partner to invest in and understand their business, and create a product with reliable Wi-Fi.

With Silex Technology, you get a single vendor that provides hardware and software support from design through manufacturing for successful product after successful product...One source of Expertise, One source of Trust, and One source of Support.

Operations

Time and again we give you reliable wireless connectivity – we design it, build it, and support it – exactly how you need it.

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