From a Custom 2 Series Core to Hello World in 30 Minutes

Drew Barbier - Sr. Product Marketing Manager
Amy Lindburg - Director Product Management

May, 2019

About This Presentation

This presentation will introduce SiFive Core Designer, our RISC-V Core IP deliverables, and software development methodologies.

At the end of this presentation you will know how to create a custom SiFive 2 Series Core and write software targeting that core.

3-Part Webinar Series

An Introduction to the RISC-V Architecture

SiFive's 2 Series RISC-V Core IP

From a Custom 2 Series Core to Hello World in 30 Minutes

https://info.sifive.com/risc-v-second-webinar-series

SiFive Core Designer

2 Series IP Bundle

SCD-deliverable

- **arty-a7-100t-scd-deliverable**
  - FPGA bitstream
- **docs**
  - **Manual** - functional description of the deliverable
  - **User Guide** - detailed deliverable description including information on the integration, and testbench
  - **Arty FPGA User Guide** - describes how to use the FPGA deliverable
- **info**
  - Metadata about the design including device tree, retiming, and SiFive Insight description
- **tests**
  - Included testbench tests
- **verilog**
  - Design
    - the actual verilog design
  - Memories
    - SRAM behavioural models
  - sifive_insight
    - Sifive Insight modules
  - Testbench
    - simulation testbench
- **Makefile - runs the simulation testbench**

2 Series Clocking

2 Series has 2 clocks

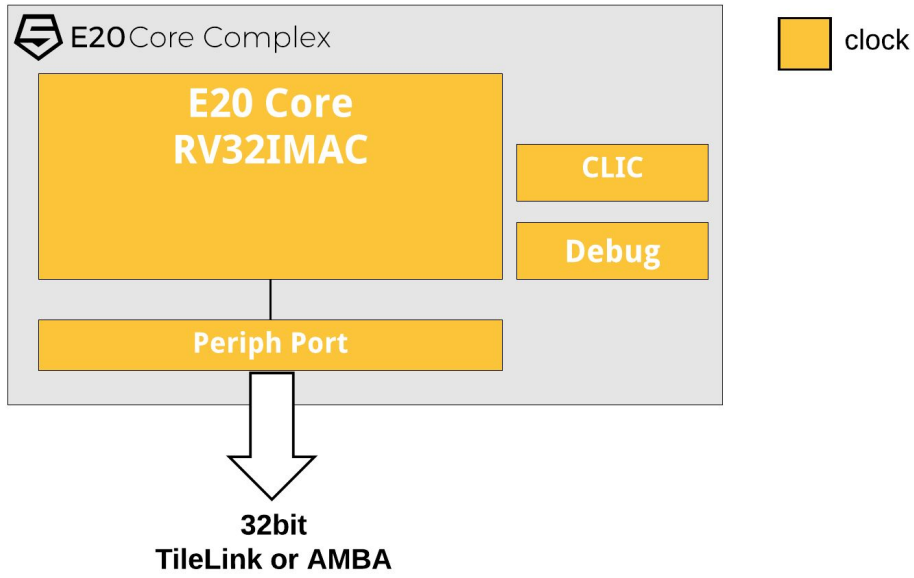
- ***clock***
  - Main CPU and L1 memory clock
- ***rtc_toggle***
  - Real Time Clock input as defined by RISC-V Architecture (mtime)
  - Must run at strictly less than half the rate of *clock*
- **Clocking relationship**
  - clock > (2x rtc_toggle)

Constraints File

- Constraint files, if required, are documented in the User Guide

Retiming

- Module retiming can help improve frequency
- Modules which need to be retimed are documented in the info folder in the retiming_modules.txt file
- 2 Series FPU benefits from retiming



SiFive

Software Development

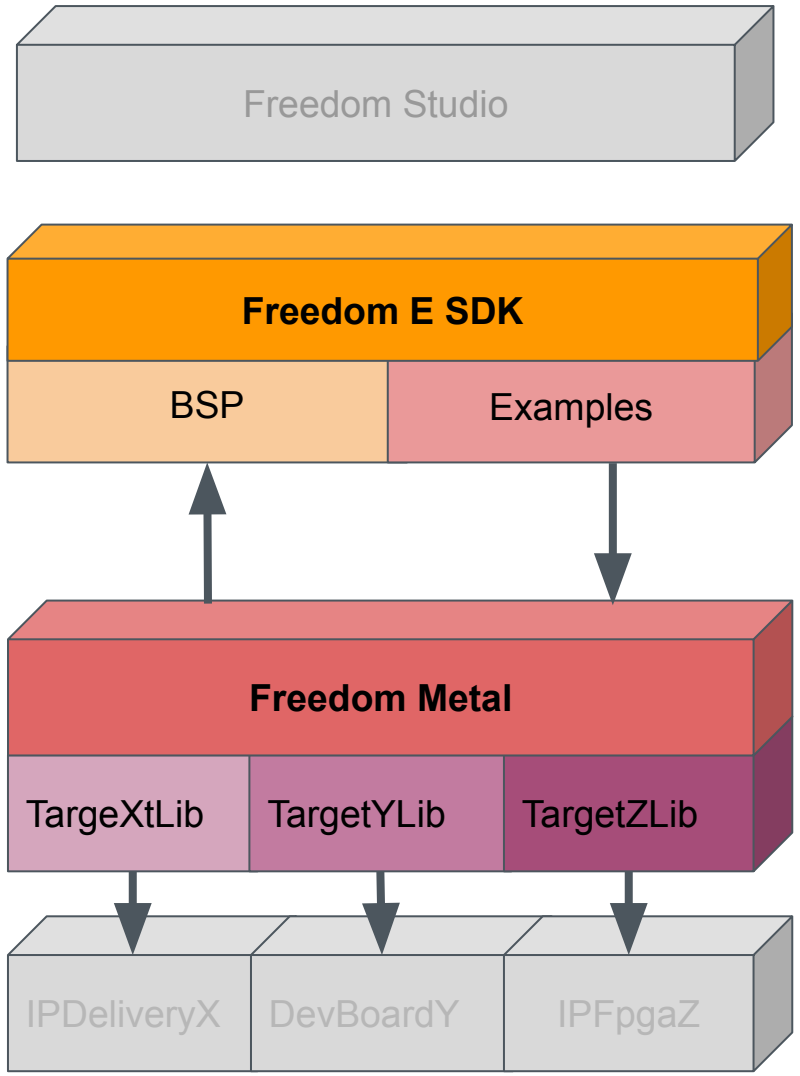
Freedom E SDK & Metal - A Bare Metal SW Stack for SiFive Devices

What is Freedom E SDK

- Embedded development kit providing a command line driven workflow with Examples and Utilities including BSP's for
  - Standard Core IP Deliverables
  - Standard Core FPGA Deliverables
  - SiFive Development Boards
- Examples use Freedom Metal to provide portability
- Open source repository
  - https://github.com/sifive/freedom-e-sdk

What is Freedom Metal

- Library for writing Portable, Bare Metal SW for all SiFive devices
  - A Bare Metal C application environment
  - An API for controlling CPU features and peripherals
  - The ability to retarget to any SiFive RISC-V product
  - A RISC-V hardware abstraction layer (HAL)
- Uses BSP's to provide target adaptation
- Open source repository
  - https://github.com/sifive/freedom-metal

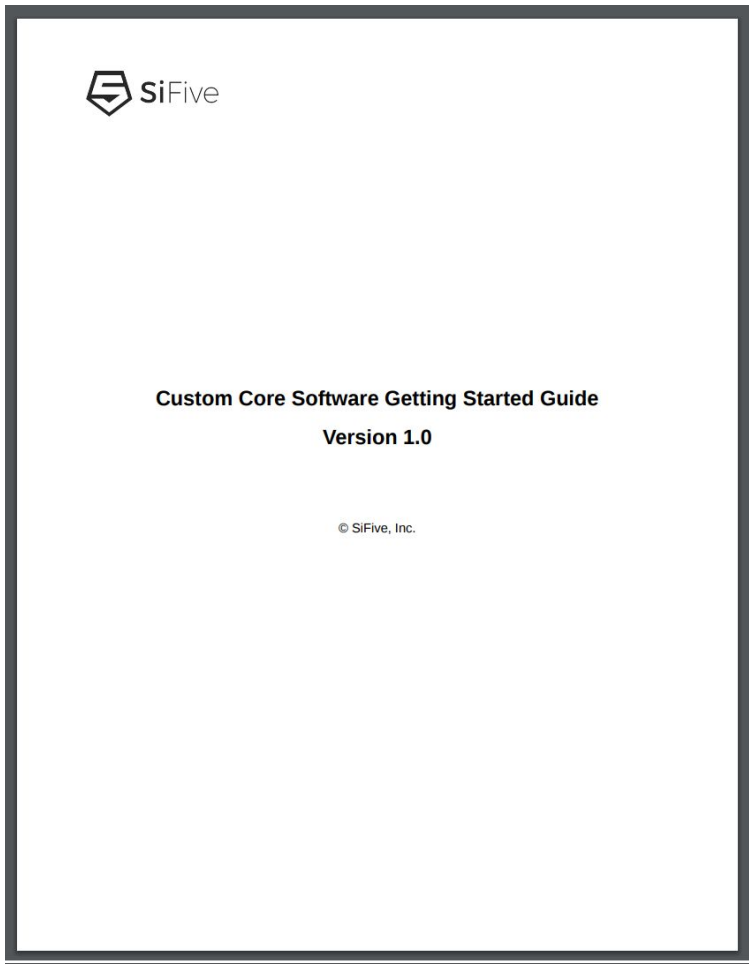


Freedom Metal BSP for Custom Cores

- **The customizability of our RISC-V Core IP also means that our software has to be as easily customizable**

- **SiFive have created tools to quickly and easily create Freedom Metal BSPs using the DTS delivered with our Core IP**
  - https://github.com/sifive/freedom-devicetree-tools
  - Application Note describing how to create custom core BSPs

- Moving forward, Freedom Metal BSPs will be included in the IP delivery bundle



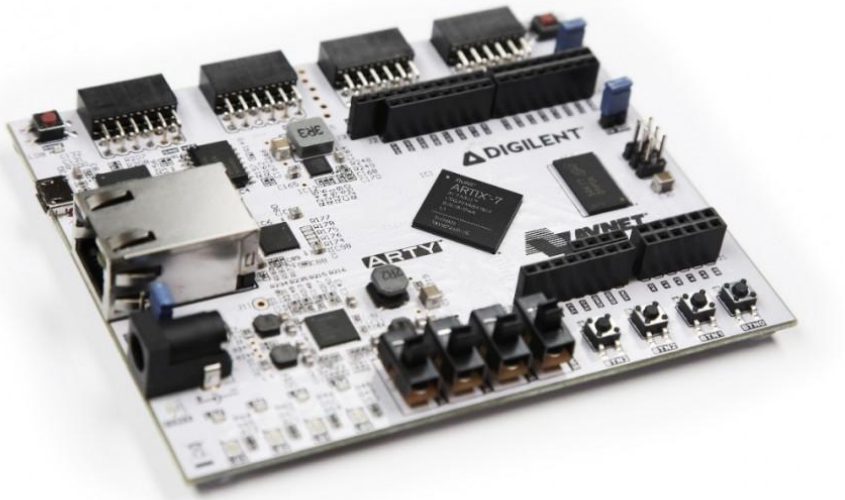
https://www.sifive.com/documentation

SiFive

Using the FPGA Bitstream

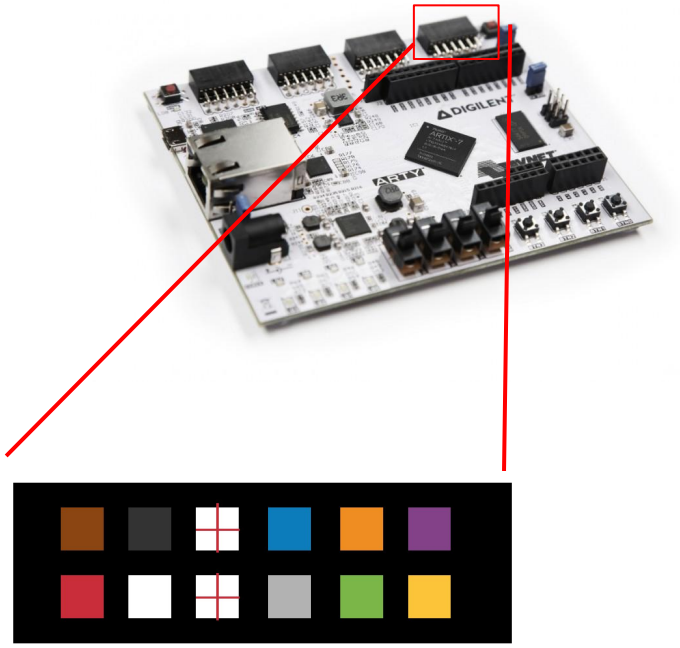
Digilent Arty FPGA Platform

- **Popular, Low cost, FPGA development board**
  - Xilinx Artix-100T FPGA - 101,440 Xilinx logic cells
  - 16MB QSPI serial flash interface, 256MB DDR3
  - USB-UART, buttons, switches, LEDs, etc…
- **2 Series synthesises to 32 MHz for fast program execution**
  - Allows for evaluation of CPU performance running real software on real hardware at speed
- **Purchase directly from Digilent:**
  - http://store.digilentinc.com/arty-a7-artix-7-fpga-development-board-for-makers-and-hobbyists/



Connecting the FPGA to a JTAG Debugger

- Debug signals are connected to the Arty Board's JD PMOD header (closest to the reset button)
- Tested Probes:
  - Olimex ARM-USB-Tiny (OpenOCD)
  - SEGGER JLINK
  - IAR i-jet
  - Lauterbach TRACE32
- JTAG Signal Mapping
  - Purple – TDO Yellow - TDI
  - Orange- nTRST Green – TMS
  - Blue - TCK Grey - nRST
  - Black - GND White - GND
  - Brown – VREF RED - VREF



JD PMOD

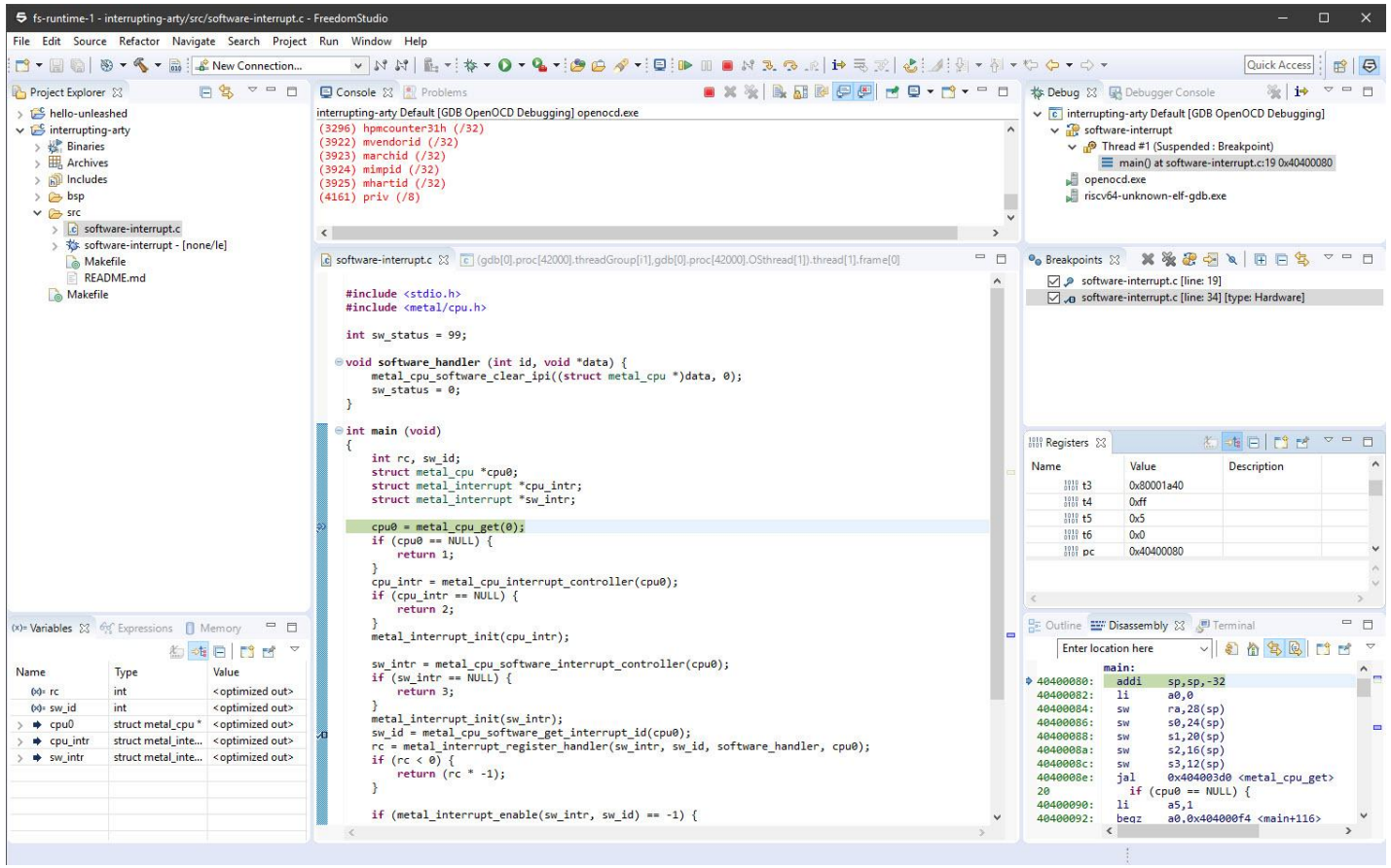
ARM 20 Pin Header

Demo

1. Use Freedom Studio to program the Arty 100T FPGA with the SiFive Core Designer generated bitfile

2. Create a new project targeting this specific FPGA platform

3. Program the application into the FPGA and run/debug it



SiFive

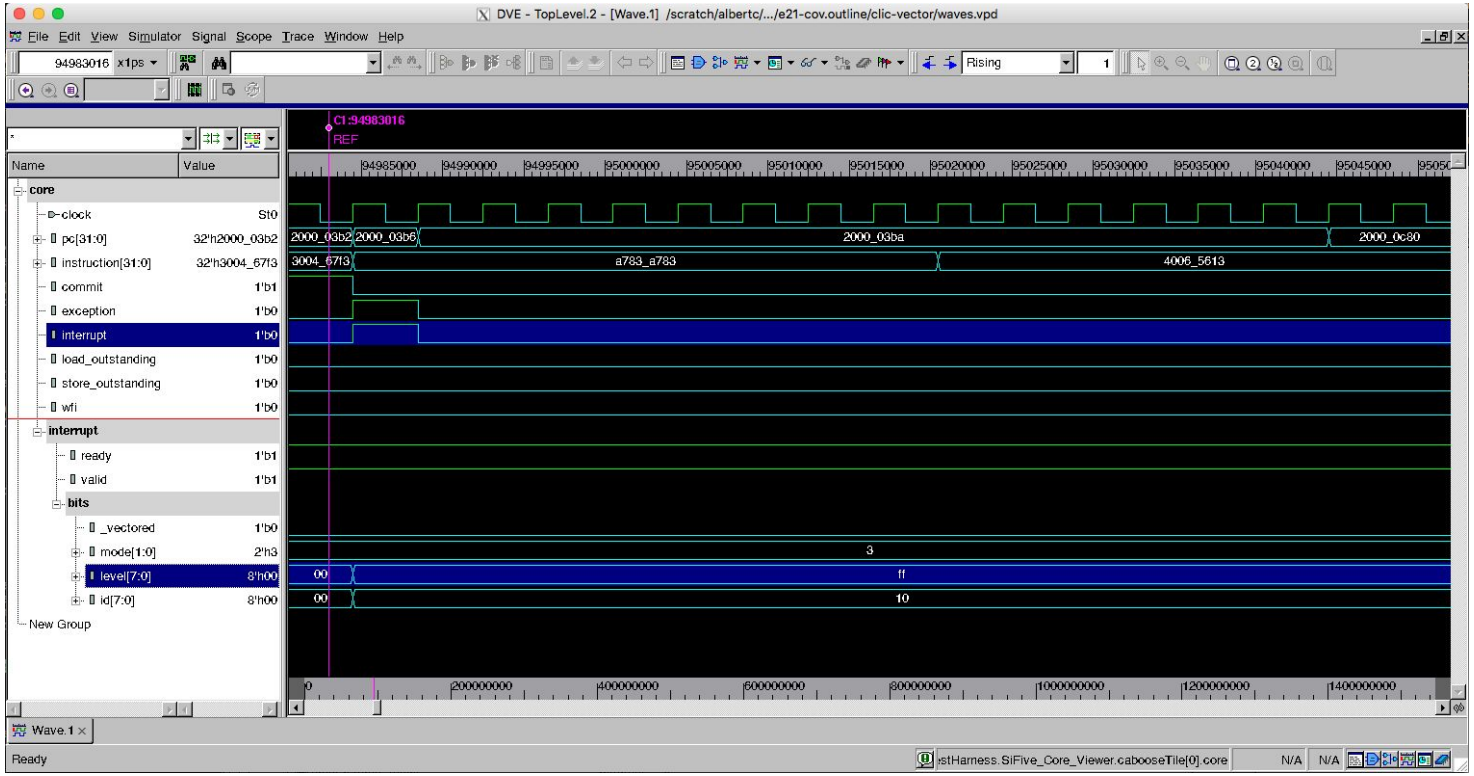
Using the RTL Testbench

Demo

1. Use Freedom Studio to create a new project targeting the RTL testbench

2. Run the test

3. Explore the resulting wave using SiFive Insight



Testbench Logs

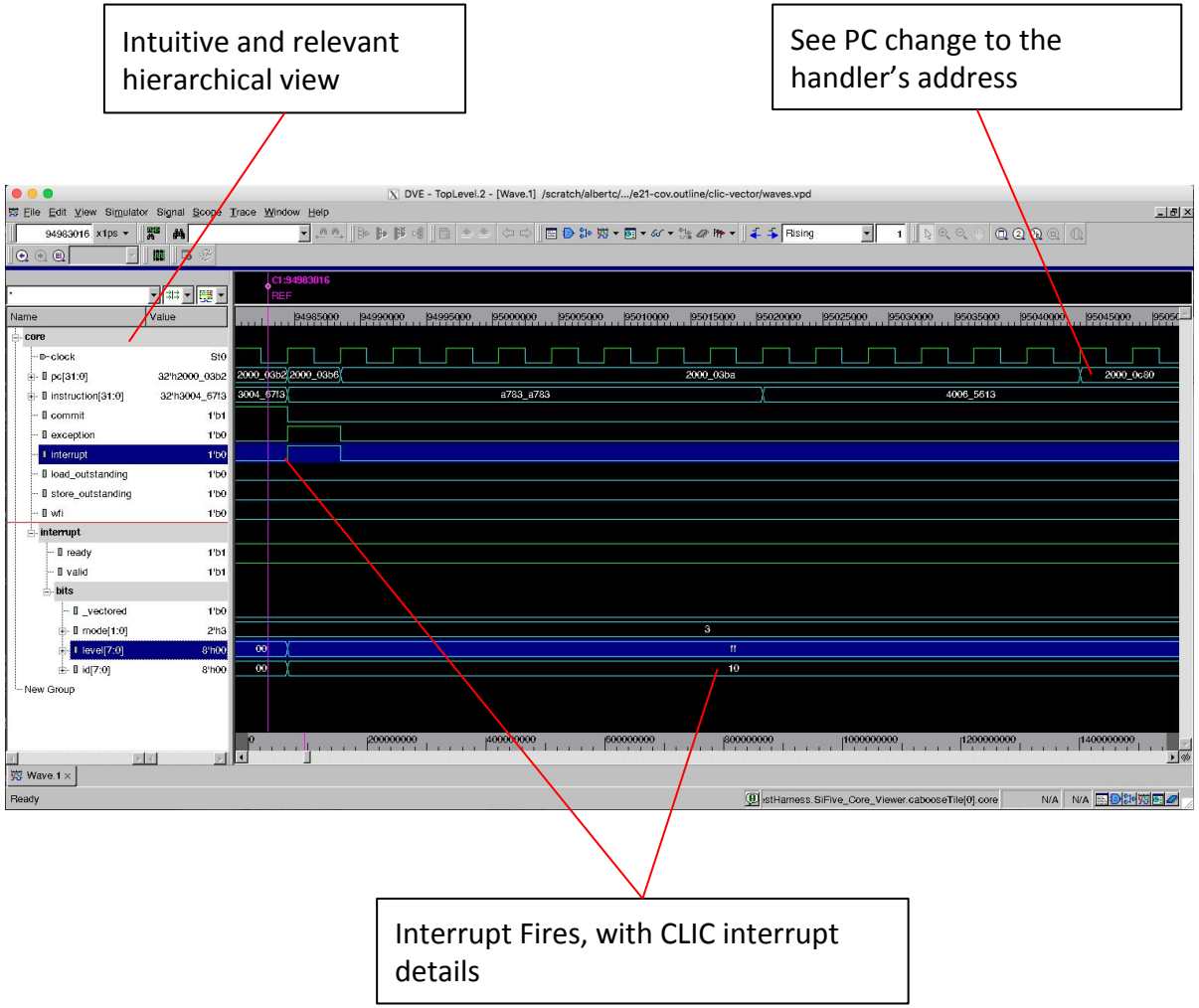
SiFive testbench produces logs for each test providing cycle-by-cycle information

SiFive Insight - The Fast and Easy Way to See Inside SiFive Core IP

- **All important SiFive IP signals exposed in a single Verilog module**
  - Logical hierarchy allows for easily discovering signals of interest
  - Clear and intuitive signal names
  - Signals and hierarchy picked and used by the IP designers

- **All signals have an English language description**
  - Documented in each release
  - A yaml file is also included in the delivery allowing for easy integration with 3rd party tools

- **SiFive Insight is conditionally included in the design**
  - Use for simulation, and by default is removed for synthesis
  - Or… Include in synthesis and connect SCV signals to on chip debug facilities like chipscope or Debug IP



SiFive

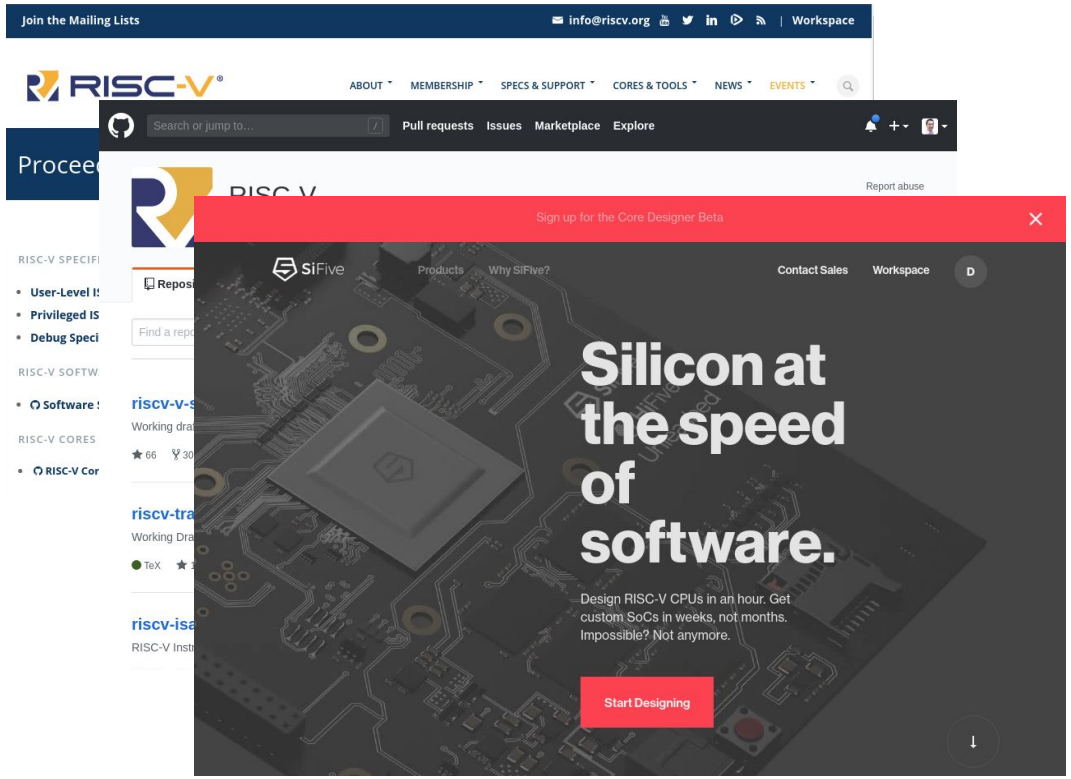
More Information

Resources

- **https://riscv.org/**
  - RISC-V Specifications
  - Links to the RISC-V mailing lists
  - Workshop proceedings

- **GitHub**
  - https://github.com/sifive/
  - https://github.com/riscv

- **https://www.sifive.com/**
  - RISC-V IP and Development Boards
  - RISC-V Tools
  - Forums



3-Part Webinar Series

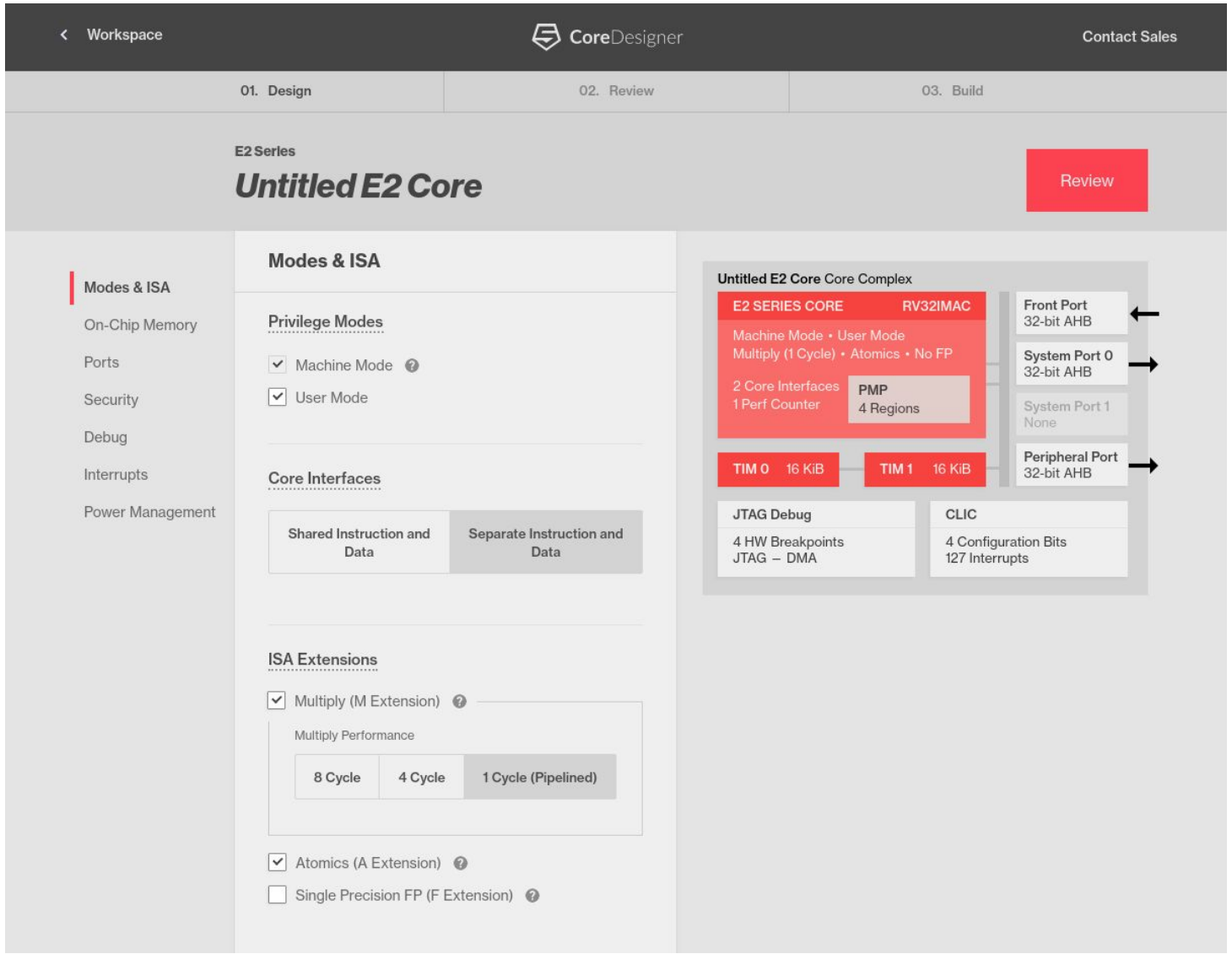
An Introduction to the RISC-V Architecture

SiFive's 2 Series Core IP

From a Custom 2 Series Core to Hello World in 30 Minutes

https://info.sifive.com/risc-v-second-webinar-series

Configure a 2 Series Core Now!!!



https://www.sifive.com/

Thank You