Q:

Is the RISC-V user spec for embedded developers et al, and privileged spec is for those who want to design RISC C based chips?

A:

The best way to understand the specifications is in a traditional UNIX model: in this case the user spec is for applications programmers and the supervisor spec is for kernel programmers. As embedded development tends to blur these boundaries, embedded RISC-V developers will be expected to understand both of the specifications. For example: the supervisor specification defines how to handle interrupts, which is a common task embedded programmers need to know how to do.

Q:

Are the extensions only for instructions and not for things like hardware options (multicore etc)?

A:

ISA extensions on RISC-V determine the set of instructions that is legal for the processor to execute. Some of these extensions are more useful when discussing multicore hardware, for example the "A" extension for atomic instructions is a lot more useful on multicore systems, but the actual specification of the ISA doesn't disallow the A extension on single-core systems (as there's uses there as well). In order to aid software portability, we provide dynamic mechanisms for determining things like core count, the presence of various system devices, and things like the interrupt map. The mechanisms for interrogating the system are defined by the priv spec.

Q:

There are 32 registers for both RV32 and RV64? The only difference is the width of the registers dependent on RV32 or RV64?

A:

Yes, both RV32I and RV64I have 32 registers, varying in their width.
Note that in both, register x0 always holds the value 0, so is not a fully R/W register.

Q:

Are the calling conventions also standardized for RV*F and *D (say, the registers used for `float` and `double` function arguments)?

A:

Yes, and there's a document at http://github.com/riscv/riscv-elf-psabi-doc We accept pull requests :)

Q:

What's the canonical URL for the latest, up-to-date RISC-V Reference Card?

A:

The canonical version can be found in the textbook Computer Organization and Design, by David Patterson and John Hennessy: https://www.amazon.com/Computer-Organization-Design-RISC-V-Architecture/dp/0128122757

Q:

Is there a downloadable/printable RISC-V Reference card?

A:

There is a freely available version online at http://www.cl.cam.ac.uk/teaching/1617/ECAD+Arch/files/docs/RISCVGreenCardv8-20151013.pdf But the canonical version will be found in the Computer Organization and Design, Patterson and Hennessy textbook

Q:

How does RV32C compare to ARMv6-M? or ARMv7-M?

A:

RV32C isn't actually a valid RISC-V ISA string, so there's two things you could mean here:

The C extension is an extension that adds 16-bit encodings of some common RISC-V instructions. It's most similar to Thumb, the biggest difference is that it's not a mode (since RISC-V is extensible it just adds additional instructions). There's a whole thesis chapter on RVC, if you're interested https://people.eecs.berkeley.edu/~krste/papers/EECS-2016-1.pdf.

RV32IMAC, the 32-bit RISC-V instruction set with Multiple, Atomic, and Compressed (but no Float or Double) would be comparable to ARMv7-M (IIRC there's no FPU there, and if there's no atomics you could drop the A extension). The thesis goes into lots of detail about this.

Q:

Regarding performance measurement -- out of curiosity, has there been an effort to specifically architect the available performance counters and related instructions for RISC-V ISA to enable constructing accurate CPI stacks (bottleneck contributions breakdown)?
To clarify, here are some examples of what I have in mind:

- "Performance Monitoring on the POWER5 Microprocessor," A. Mericas, Performance Evaluation and Benchmarking 2006.

- "A Top-Down Approach to Architecting CPI Component Performance Counters," S. Eyerman, L. Eeckhout, T. Karkhanis, and J. Smith. IEEE Micro 27(1), 84–93 (2007)

- "A Top-Down Method for Performance Analysis and Counters Architecture," Ahmad Yasin. ISPASS 2014.

A:

Right now, the only specified performance counters are the simple ones we knew everyone would want (instrution count and real-time). Doing comprehensive performance counters correctly is hard, so this would be part of additional specification work. I don't know of any working group started, if you're interested you can come to the RISC-V workshop or discuss it on the mailing lists.

Q:

Is there any plan for a RISC-V MOOC?

A:

We are not aware of any at this time, but there is a RISC-V mailing list for teaching-related questions, and you may want to ask your question there: riscv-teach@groups.riscv.org https://riscv.org/mailing-lists/

Q:

What Linux OS can the RV gcc tools be installed on? Is there a list somewhere?

A:

We have binary distributions on the SiFive website for Windows, Linux, and macOS. The toolchain source files are available on github.com/riscv/riscv-tools

Q:

Also are there any RISC V based microcontrollers on the market?

A:

The FE310 is available from SiFive. More information can be found here: https://www.sifive.com/products/freedom-e310/

Q:

Where can I get commercial implementations of RISV-V cores?

A:

SiFive offers commercial RISC-V cores, you can find more information on www.sifive.com , including easy access to evaluation RTL and FPGA bitstreams.

Q:

Any plans to support the clang compiler?

A:

There is an LLVM port in active development right now, and a thread on the RISC-V sw-dev mailing list right now about an early release of it.

Q:

How much would these cost?

A:

More information on SiFive's Coreplex can be found here, including pricing: https://www.sifive.com/products/coreplex-risc-v-ip/

Q:

How does the SiFive cores differ from the UCB rocket chip cores?

A:

The SiFive cores come with commercial support, warranty, indemnification, testbenches. integration guides, synthesis scripts, etc.. They are also a fixed implementation with a specific performance level that SiFive stands behind.

The rocket chip cores are an open source project. While SiFive is maintaining those they are open projects that are always changing.

Q:

Is the RISC V Reader book available for purchase in electronic formats?

A:

You can find it here: https://www.amazon.com/RISC-V-Reader-Open-Architecture-Atlas/dp/099924910X/ref=sr_1_1?ie=UTF8&qid=1505240759&sr=8-1&keywords=andrew+waterman