BXT7059 / BXTS7059

7059-xxx

No. 87-007062-000 Revision J

HARDWARE

TECHNICAL REFERENCE

Intel® Xeon® E5-2400 v2 Series
&
Intel® Xeon® E5-2400 Series

10, 8, 6 and 4-Core

PROCESSOR-BASED

SHB

WARRANTY

The following is an abbreviated version of Trenton Systems' warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonSystems.com.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Systems Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Systems' discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Systems Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Systems Inc. Trenton Systems Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Systems Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Systems Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Systems Inc.

RETURN POLICY

A Return Material Authorization (RMA) number, obtained from Trenton Systems prior to return, must accompany products returned for repair. The customer must prepay freight on all returned items, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton Systems via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

TRENTON Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

E-mail: Support@TrentonSystems.com
Web: www.TrentonSystems.com

TRENTON Systems, Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales: (800) 875-6031 • Phone: (770) 287-3100 • Fax: (770) 287-3150

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HANDLING PRECAUTIONS

WARNING: This product has components that may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD HANDLING PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your BXT7059 or BXTS7059 (7059-xxx) SHB. System performance may be affected by incorrect usage of these features.

DDR3 MEMORY

Trenton recommends ECC registered DDR3-1600 Mini-DIMM memory modules for use on the BXT7059 / BXTS7059 SHBs and these ECC registered (72-bit) DDR3 Mini-DIMMs must be PC3-12800 compliant. Unbuffered ECC DDR3 Mini-DIMMs are also supported on the BXT/BXTS boards, however you cannot mix the ECC registered and unbuffered ECC memory types on the same board.

Each processor on a BXT7059 / BXTS7059 SHB supports three direct-connect DDR3 memory interfaces. The maximum possible memory interface speed obtained depends on the specific Intel® Xeon® E5-2400 v2 or Intel® Xeon® E5-2400 series processor(s) used on the board and other board configuration options listed in the notes section below. The table below illustrates the maximum DDR3 **memory speed** supported as a function of each specific Intel® Xeon® processor when using the recommended PC3-12800 compliant Mini-DIMM modules and an SHB with the latest BIOS support.

Max. DDR3 Speed	Processor	Cores / Threads	Cache	Long-Life Availability	Maximum Thermal Design Power (TDP)	Operating Temperature Range*
DDR3-1600	Intel® Xeon® E5-2450 v2	8 / 16	20MB	Yes	95W	0°C to 40°C
DDR3-1600	Intel® Xeon® E5-2430 v2	6 / 12	15MB	Yes	80W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2448L v2	10 / 20	25MB	Yes	70W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2428L v2	8 / 16	20MB	Yes	60W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2418L v2	6 / 12	15MB	Yes	50W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2448L	8 / 16	20MB	Yes	70W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2430	6 / 12	15MB	Yes	95W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2428L	6 / 12	15MB	Yes	60W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2418L	4 / 8	10MB	Yes	50W	0°C to 50°C

*Requires a continuous airflow across the board of 350LFM.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR3-1600 Mini-DIMMs and using an even number of memory modules on the BXT7059 dual-processor board configuration.
- All memory modules must have gold contacts.
- Low-voltage (DDR3L) Mini-DIMMs are not supported.
- The SHB supports the following memory module memory latency timings:
  - 9-9-9 for 1600MHz DDR3 Mini-DIMMs
- Populate the memory sockets starting with the Mini-DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:

Mini-DIMM Population Order	CPU0*	Mini-DIMM Population Order	CPU1*
1	BK00	1a	BK10
2	BK01	2a	BK11
3	BK02	3a	BK12

- *CPU0 and CPU1 are both available on BXT7059 SHBs.
- Using a balanced memory population approach with the BXT7059 configuration; meaning an equal number of Mini-DIMMs per processor, ensures maximum memory interface performance.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board. The BXTS7059 SHB versions feature one processor; however, memory slots BK10, BK11 and BK12 are installed on the SHB but are not active in this single-processor board version.

SAS / SATA RAID Operation

The SHB's Intel® C604 Platform Controller Hub (PCH) features Intel® Rapid Storage Technology, which enables SHB support for RAID 0, 1 and 10 implementations. To configure the SAS / SATA ports as RAID drives, you must install the Intel® RST enterprise driver software. This link takes you to version 3.2 that was tested and validated on the SHB. A later version 3.5 is also available for download, but this version has not been tested on the board. Links to both driver versions are located on Trenton's website by accessing the Downloads tab of either the BXT7059 or the BXTS7059 product detail web pages or the RAID Drivers section of the Technical Support page.

PCI Express 3.0 Links and PICMG® 1.3 Backplanes

The A0 through A3 PCI Express® links on the SHB connect directly to processor CPU0. These links can operate as either PCI Express 3.0, 2.0 or 1.1 links based on the end-point devices on the backplane that are connected to the SHB and the backplane's PCIe link design itself. In addition to automatically configuring themselves for either PCIe 3.0, 2.0 or 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple x4 links from CPU0 (links A0, A1, A2 and A3) can be utilized on a backplane as a single x16 PCIe electrical link, two x8 links, or four x4 links. CPU0's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. PCIe link B0 comes from the board's PCH and is a PCIe 2.0 interface. Link B0 has a x4 default configuration that can automatically bifurcate into four, x1 PCIe links. An optional PEX10 module connects to the second processor (CPU1) on the dual-processor BXT7059 board to extend the PICMG 1.3 base specification by providing four additional x4 PCIe links. These additional links may also operate as either PCI Express 3.0, 2.0 or 1.1 links and can be combined into one x16, or two x8 or four x4 PCIe interfaces on a PEX10-supported PICMG 1.3 backplane. This BXT7059 capability provides additional PCI Express bandwidth and option card support in the system design. Refer to the *PCI Express® Reference* and to *PCI Express Backplane Usage* chapters of the BXT7059 / BXTS7059 Hardware Manual for more information.

A Word About PCI Express 3.0 Interfaces

PCIe 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen 3, Gen 2 and Gen 1.1 I/O cards on the same interface link. Running a PCIe 3.0 target device such as a Gen 3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the BXT7059) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

PICMG 1.3 Backplane I/O

The BXT7059 and BXTS7059 enable the following PICMG 1.3 backplane I/O connectivity via the SBC's edge connector C:

- Four USB 2.0 interfaces
- One 10/100Base-T Ethernet interface
- One SATA/300 interface

PICMG 1.3 Backplane Classification

Virtually all of Trenton's PICMG 1.3 backplanes may be used with the BXT7059 and BXTS7059 system host boards without restrictions. The BXT7059 and BXTS7059 are system host boards that can operate as either a Server or Graphics-Class PICMG 1.3 SHB. The BXT SHBs are essentially combo-class boards because of the capabilities of the PCI Express links built into the SHBs' processors. To take advantage of the extra x16 PCIe link available on CPU1 of the BXT7059 dual-processor SHB configuration; use a Trenton combo-class PICMG 1.3 backplane such as the Trenton BPC7009 or BPC7041. This extra x16 link is not available with the single-processor BXTS7059 board configuration. See *Appendix C, PCI Express Backplane Usage* for more details.

OFF-BOARD VIDEO CARD USAGE

If the system design requires an off-board video card, then the card must be placed in a backplane slot driven with PCI Express links from the BXT7059's first processor. This is an Aptio® 4.x BIOS limitation that may be corrected in future software revisions. Listed below are the acceptable BPC7041 backplane slots for use with an off-board video card:

BPC7041 - Card slot PCIe6, PCIe7, PCIe8, PCIe9 or PCIe10

BIOS

The BXT7059 and BXTS7059 feature the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *BXT7059 / BXTS7059 BIOS Technical Reference* manual.

OPERATING SYSTEMS

Trenton's BXT7059 and BXTS7059 have been tested using a number of popular and readily available operating systems including: Microsoft Windows XP X64, Windows Server 2003, Windows Server 2008 R2, Windows 7 and a number of variations of Linux including Red Hat. This testing process confirms the SHB's PCI Express interface and device I/O functionality. Trenton does not recommend using the Microsoft Windows XP32 SP2 or SP3 operating system due to limited functionality concerns. Contact Trenton Tech Support for additional information.

MOUSE/KEYBOARD "Y" CABLE

If you have an IOB33 I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation.

POWER CONNECTION

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The BXT7059/BXTS7059 supports these signals, controlled by the ACPI and are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to - *Power Connection* section in the BXT manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections *BXT7059 / BXTS7059 Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the BXT7059 or BXTS7059 web pages.

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Chapter 1 Specifications

Introduction

The BXT7059 and BXTS7059 are combo-class, PICMG® 1.3 system host boards that support either the Intel® Xeon® E5-2400 v2 Series or the Intel® Xeon® E5-2400-series processors. The CPUs featured on the board were formally codenamed "Ivy Bridge-EN" and "Sandy Bridge-EN" respectively. The Ivy Bridge-EN processors are built using the 22nm Intel Micro-Architecture while the Sandy-Bridge-EN processors were built using the 32nm Intel Micro-Architecture. The 22nm micro-architecture enabled several performance improvements including additional executing cores, better TDP ratingss and improved power utilization. Both processor families feature PCI Express 3.0 I/O support and a three-channel DDR3 integrated memory controller. The three-channel memory controller in most of the processors support DDR3-1600 memory interface speeds. The three memory channels per processor results in six direct access memory interfaces on the BXT7059 board version and the interfaces connect to six DDR3-1600 Mini-DIMM sockets. With 4GB DDR3 Mini-DIMMs the total system memory capacity for a BXT7059 is 24GB and doubles to 48GB when using 8GB DDR3 Mini-DIMMs. If 16GB DDR3-1600 Mini-DIMMs become a reality, the maximum practical system memory capacity supported on the BXT7059 will grow to 96GB; with 192GB being the maximum theoretical capacity. The system memory capacities are cut in half for the single processor BXTS7059 board version.

Each processor option supports twenty-four (24) PCI Express 3.0 links. In the BXT7059 board design, sixteen of these links from CPU0 plus four additional PCIe 2.0 links from the board's Intel® C604 Platform Controller Hub (PCH) comprise the PICMG 1.3 edge connector A & B backplane interfaces. CPU0 also provides an additional x4 PCIe PCIe 3.0 link for use on a backplane equipped with an I/O expansion slot that supports an optional IOB33 I/O expansion module attached to either a BXT7059 or BTXS7059 SHB. CPU1 on the BXT7059 dual-processor board configuration delivers a x16 PCIe 3.0 interface to the PEX10 expansion module and these PEX10 extra links provide added bandwidth to systems equipped with a backplane such as the Trenton BPC7041. The Intel® Quick Path Interface (Intel® QPI); with a maximum transfer speed for some processor versions of up to 8GT/s, provides the communication path between CPUs on the BXT7059 to enable resource sharing. All of the PCI Express interface links needed for a PICMG 1.3 compliant backplane are provided by the links out of CPU0 and the additional PCIe link out of the Intel® C604 Platform Controller Hub (PCH).

Video and I/O features on the BXT boards include:

- A Graphics Processing Unit (GPU) driven with an internal x1 PCIe link and capable of supporting pixel resolutions up to 1920 x 1200 (WUXGA) with a 64k color depth
- Three Gigabit Ethernet interfaces with two on the I/O plate and one available for use on a PICMG 1.3 compliant backplane or via the P22 alternate backplane cable connection.
- Two SATA/600 ports that can support independent drives or RAID drive arrays
- Four SAS / SATA/300 ports that can support independent drives or RAID drive arrays
- Eight USB 2.0 interfaces, with four routed to edge connector C for use on a backplane
- One SATA/300 interface routed to edge connector C for use on a backplane

The listing below summarizes the available versions of the BXT7059 and BXTS7059 system host boards.

Dual-Processor Models - Intel® Xeon® E5-2400 v2 Series (22nm Intel® Micro-Architecture/Ivy Bridge-EN)

Model #	Model Name	Speed	Intel Product Name
Dual Intel Xeon E5-2430 v2 Processors (Ivy Bridge-EN) – 8-core, 20MB cache, 7.2GT/s QPI, With H-T*:			
392705970400000	BXT/2.5SRV20	2.5GHz	Intel® Xeon® Processor v2 E5-2450 [E]
Dual Intel Xeon E5-2430 v2 Processors (Ivy Bridge-EN) – 6-core, 15MB cache, 7.2GT/s QPI, With H-T*:			
392705971700000	BXT/2.5SRV15	2.5GHz	Intel® Xeon® Processor v2 E5-2430 [E]
Dual Intel Xeon E5-2448L v2 Processors (Ivy Bridge-EN) – LV, 10-core, 25MB cache, 8.0GT/s QPI, With H-T			
392705972200000	BXT/1.8LTRV25	1.8GHz	Intel® Xeon® Processor v2 E5-2448L [E]

* H-T = Intel® Hyper-Threading, [E] = **Embedded/Long-life processor version**

Dual-Processor Models - Intel® Xeon® E5-2400 v2 Series (continued)

Model #	Model Name	Speed	Intel Product Name
Dual Intel Xeon E5-2428L v2 Processors (Ivy Bridge-EN) – LV, 8-core, 20MB cache, 7.2GT/s QPI, With H-T			
392705973200000	BXT/1.8LERV20	1.8GHz	Intel® Xeon® Processor v2 E5-2428L[E]
Dual Intel Xeon E5-2418L v2 Processors (Ivy Bridge-EN) – LV, 6-core, 15MB cache, 6.4GT/s QPI, With H-T*			
392705974300000	BXT/2.0LSRV15	1.8GHz	Intel® Xeon® Processor v2 E5-2418L[E]

* H-T = Intel® Hyper-Threading, [E] = **Embedded/Long-life processor version**

Single-Processor Models - Intel® Xeon® E5-2400 v2 Series (22nm Intel® Micro-Architecture/Ivy Bridge-EN)

Model #	Model Name	Speed	Intel Product Name
Single Intel Xeon E5-2450 v2 Processor (Ivy Bridge-EN) – 8-core, 20MB cache, 7.2GT/s QPI, With H-T*:			
392705980400000	BXTS/2.5SRV20	2.5GHz	Intel® Xeon® Processor v2 E5-2430[E]
Single Intel Xeon E5-2430 v2 Processor (Ivy Bridge-EN) – 6-core, 15MB cache, 7.2GT/s QPI, With H-T*:			
392705981700000	BXTS/2.5SRV15	2.5GHz	Intel® Xeon® Processor v2 E5-2430[E]
Single Intel Xeon E5-2448L v2 Processor (Ivy Bridge-EN) – LV, 10-core, 25MB cache, 8.0GT/s QPI, With H-T			
392705982200000	BXTS/1.8LTRV25	1.8GHz	Intel® Xeon® Processor v2 E5-2448L[E]
Single Intel Xeon E5-2428L v2 Processor (Ivy Bridge-EN) – LV, 8-core, 20MB cache, 7.2GT/s QPI, With H-T			
392705983200000	BXTS/1.8LERV20	1.8GHz	Intel® Xeon® Processor v2 E5-2428L[E]
Single Intel Xeon E5-2418L v2 Processor (Ivy Bridge-EN) – LV, 6-core, 15MB cache, 6.4GT/s QPI, With H-T			
392705984300000	BXTS/2.0LSRV15	1.8GHz	Intel® Xeon® Processor v2 E5-2418L[E]

Dual-Processor Models - Intel® Xeon® E5-2400 Series (32nm Intel® Micro-Architecture/Sandy Bridge-EN)

Dual Intel Xeon E5-2430 Processors (Sandy Bridge-EN) – 6-core, 15MB cache, 7.2GT/s QPI, With H-T*:			
392705901400000	BXT/2.2SRB15	2.0GHz	Intel® Xeon® Processor E5-2430[E]

* H-T = Intel® Hyper-Threading, [E] = **Embedded/Long-life processor version**

Dual Intel Xeon E5-2448L[E] Processors (Sandy Bridge-EN) – LV, 8-core, 20MB cache, 8.0GT/s QPI, With H-T			
392705903200000	BXT/1.8LERB20	1.8GHz	Intel® Xeon® Processor E5-2448L[E]
Dual Intel Xeon E5-2428L[E] Processors (Sandy Bridge-EN) – LV, 6-core, 15MB cache, 7.2GT/s QPI, With H-T:			
392705904100000	BXT/1.8LSRB15	1.8GHz	Intel® Xeon® Processor E5-2448L[E]
Dual Intel Xeon E5-2418L[E] Processors (Sandy Bridge-EN) – LV, 4-core, 10MB cache, 6.4GT/s QPI, With H-T*:			
392705905300000	BXT/2.0LRB10	2.0GHz	Intel® Xeon® Processor E5-2448L[E]
Dual Intel Xeon E5-2407[#] Processors (Sandy Bridge-EN) – LV, 4-core, 10MB cache, 6.4GT/s QPI, No H-T[N]:			
392705902400000	BXT/2.0QB10	2.0GHz	Intel® Xeon® Processor E5-2448L[E]

[#] = **Non-embedded processor**, [N]No H-T = Intel® Hyper-Threading **Not** Supported

Single-Processor Models (32nm Intel® Micro-Architecture/Sandy Bridge-EN)

Model #	Model Name	Speed	Intel Product Name
Single Intel Xeon E5-2430[E] Processor (Sandy Bridge-EN) – 6-core, 15MB cache, 7.2GT/s QPI, With H-T:			
392705911400000	BXTS/2.2SRB15	2.0GHz	Intel® Xeon® Processor E5-2430[E]
Single Intel Xeon E5-2448L[E] Processor (Sandy Bridge-EN) – LV, 8-core, 20MB cache, 8.0GT/s QPI, With H-T			
392705913200000	BXTS/1.8LERB20	1.8GHz	Intel® Xeon® Processor E5-2448L[E]
Single Intel Xeon E5-2428L[E] Processor (Sandy Bridge-EN) – LV, 6-core, 15MB cache, 7.2GT/s QPI, With H-T:			
392705914100000	BXTS/1.8LSRB15	1.8GHz	Intel® Xeon® Processor E5-2448L[E]

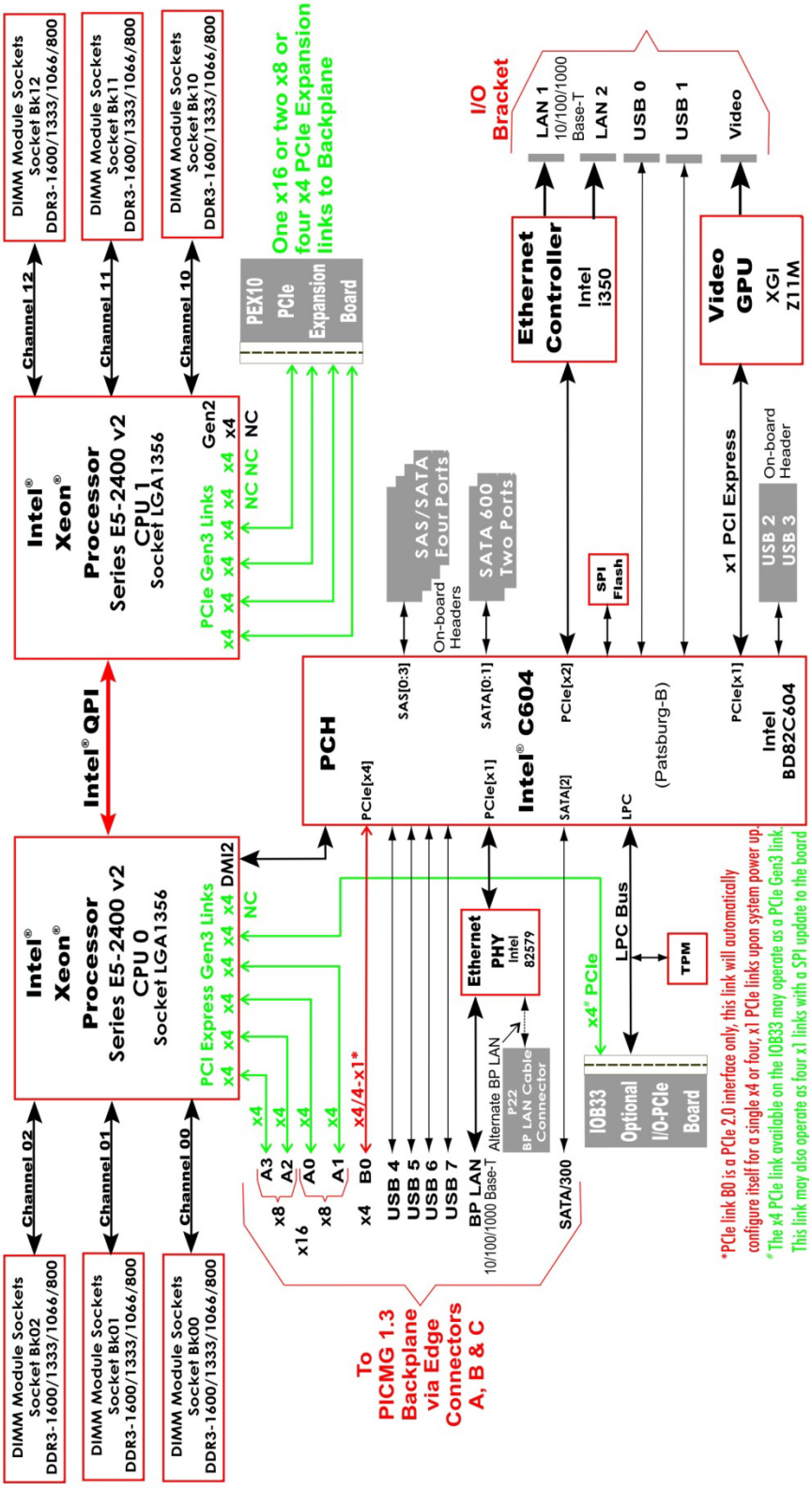
Single-Processor Models (32nm Intel® Micro-Architecture/Sandy Bridge-EN, continued)

Model #	Model Name	Speed	Intel Product Name
Single Intel Xeon E5-2418L[E] Processor (Sandy Bridge-EN) – LV, 4-core, 10MB cache, 6.4GT/s QPI, With H-T*:			
392705915300000	BXTS/2.0LRB10	2.0GHz	Intel® Xeon® Processor E5-2448L[E]
Single Intel Xeon E5-2407[#] Processor (Sandy Bridge-EN) – LV, 4-core, 10MB cache, 6.4GT/s QPI, No H-T[N]:			
392705912400000	BXTS/2.0QB10	2.0GHz	Intel® Xeon® Processor E5-2448L[E]

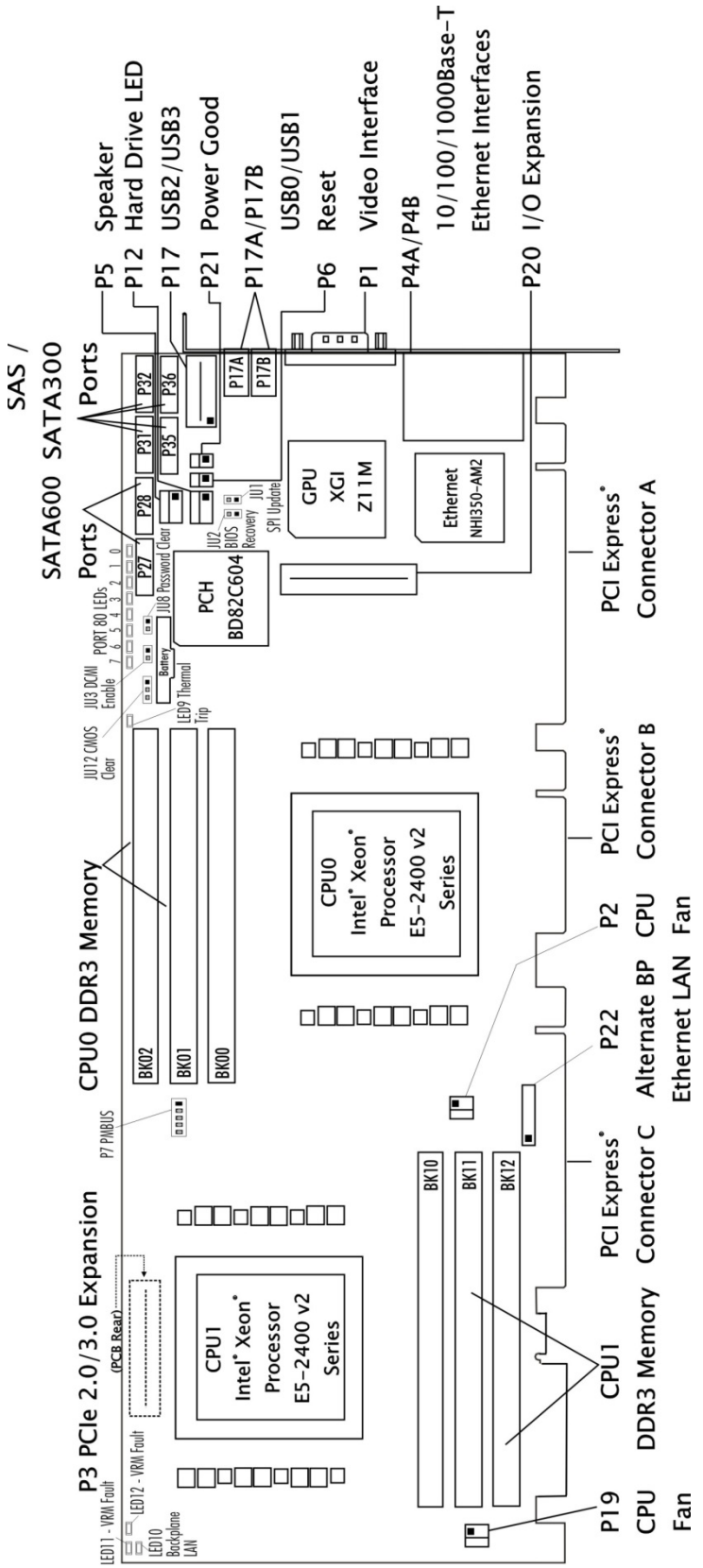
Board Features

- Intel® Xeon® E5-2400 v2 Series Processors (Ivy Bridge-EN)
- Intel® Xeon® E5-2400 Series Processors (Sandy Bridge-EN)
- Intel® C604 Platform Controller Hub (Patsburg-B)
- Direct PCI Express® 3.0 links into the Intel® Xeon® E5-2400 Series Processors
- A Combo-class SHB that is compatible with PCI Industrial Computer Manufacturers Group (PICMG) 1.3 Specification
- BXT7059 provides a total of 40 lanes of PCI Express for off-board system integration
- Direct DDR3-1600 Memory Interfaces into the Intel® Xeon® E5-2400 Series Processors
- Six DDR3 Mini-DIMM sockets capable of supporting up to 192GB of system memory on a dual-processor BXT7059, 24GB maximum capacity with readily available 4GB DDR3 Mini-DIMMs
- Video interface utilizing XGI® Volari™ Z11M Graphics Processing Unit
- Two 10/100/1000Base-T Ethernet interfaces available on the SHB's I/O plate
- Four on-board Serial Attached SCSI (SAS) / SATA/300 ports support independent SATA storage devices or may be configured to support RAID 0, 1 or 10 implementations
- Two on-board SATA/600 ports support independent SATA storage devices or may be configured to support RAID 0, 1 or 10 implementations
- Eight Universal Serial Bus (USB 2.0) interfaces
- Off-board I/O support provided for one, SATA/300 interface, one 10/100Base-T Ethernet interface and four USB 2.0 port connections on a PICMG 1.3 backplane
- Legacy I/O, dual serial port and x4 PCIe link expansion available via Trenton IOB33 expansion board
- An additional x16 PCI Express 3.0 lanes are available when using an optional PEX10 board on a BXT7059 connected to a Trenton BPC7041 PICMG 1.3 backplane
- Full-length stiffener bars and backer plate on the rear of the SHB enhances the rugged nature on the board by maximizing component protection and simplifying mechanical system integration
- Full PC compatibility

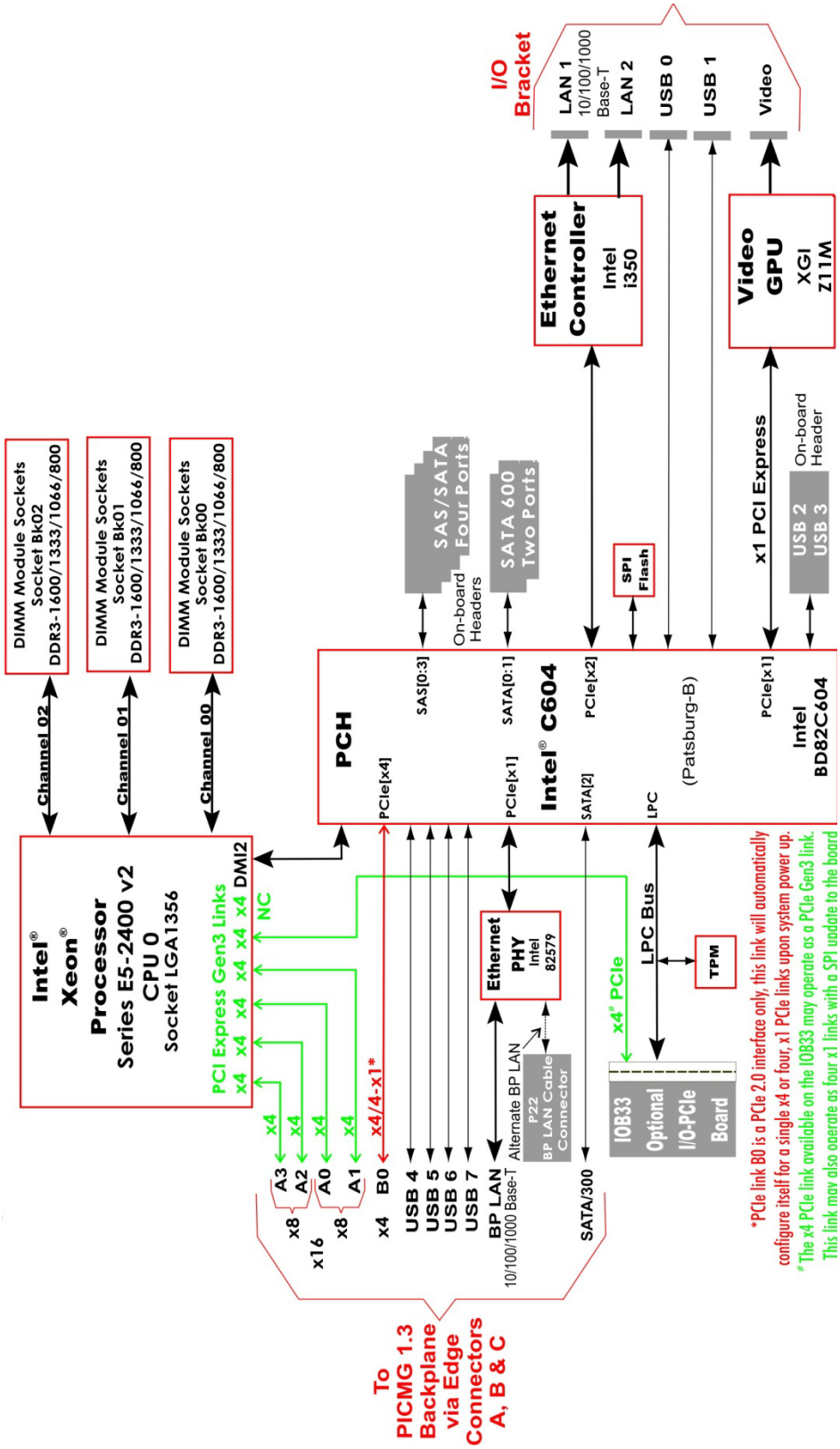
BXT7059 (7059-xxx) – Dual-Processor SHB Block Diagram



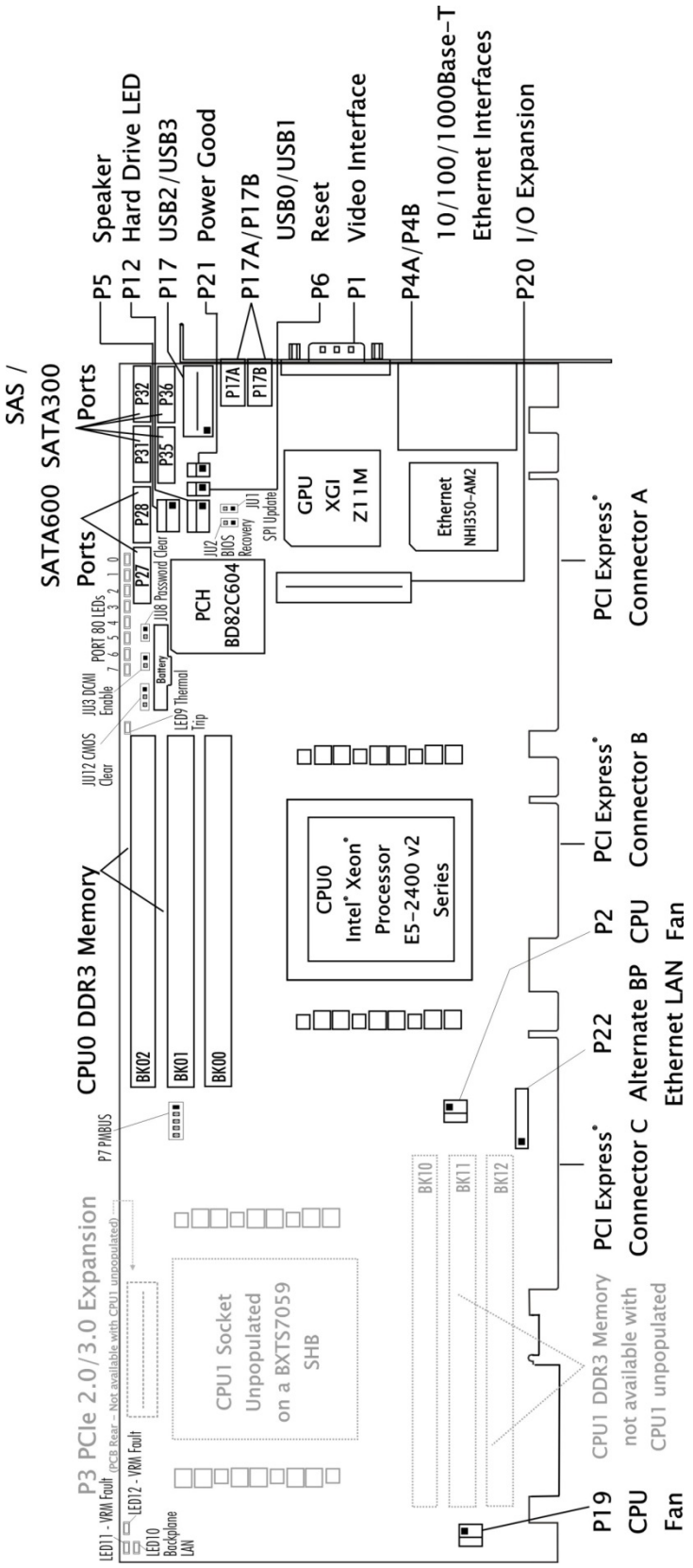
BXT7059 (7059-xxx) – Dual-Processor SHB Layout Diagram



BXTS7059 (7059-xxx) – Single-Processor SHB Block Diagram



BXTS7059 (7059-xxx) – Single-Processor SHB Layout Diagram



Processors

- Intel® Xeon® E5-2400 v2 Series Processors (Ivy Bridge-EN)
- Intel® Xeon® E5-2400 Series Processors (Sandy Bridge-EN)
- Processors plug into LGA1356 sockets

Platform Controller Hub (PCH)
Intel® C604 (Patsburg-B)

Serial Interconnect Interface
PCI Express® 3.0, 2.0 and 1.1 compatible

Data Path (max speed supported*)
DDR3-1600 Memory - 72-bit (per channel)
* Processor dependent

Serial Interconnect Speeds
PCI Express 3.0 – 8.0GHz per lane (with proper PCIe 3.0 root complex to the target card tuning and optimization)
PCI Express 2.0 – 5.0GHz per lane
PCI Express 1.1 - 2.5GHz per lane

Intel® Quick Path Interconnect Between CPUs
The Quick Path Interconnect enables processor-to-processor resource sharing and fast data transfers between CPUs. The Intel® QPI speed between CPUs in a dual-processor BXT7059 configuration is a function of the specific processors used on the board as illustrated in the following table.

Processor	Intel® Quick Path Interconnect (QPI) Speed
Intel® Xeon® E5-2450 v2, Intel® Xeon® E5-2448L v2 and Intel® Xeon® E5-2448L	8.0GT/s
Intel® Xeon® E5-2430 v2, Intel® Xeon® E5-2430, Intel® Xeon® E5-2428L v2 and Intel® Xeon® E5-2428L	7.2GT/s
Intel® Xeon® E5-2418L v2 and Intel® Xeon® E5-2418L	6.4GT/s
Intel® Xeon® E5-2407	6.4GT/s

Intel® Direct Media Interface 2 (DMI2) Between Processor and Intel® C604 PCH
This x4 PCIe 2.0 interface provides the data communication path between the PCH and processor. On a dual-processor, BXT7059 the CPU0 connects directly to the PCH and the CPU1 feeds its information to the PCH via QPI link between processors and the CPU0 DMI link.

Memory Interface
Three DDR3-1600MHz memory channels per processor provide a peak memory interface bandwidth 38.4GB/s when using PC3-12800 Mini-DIMMs *and* the Intel® Xeon® E5-2448L v2 processor(s). Unlike past Trenton single board computers; the BTX7059's peak memory bandwidth is a function of both the Mini-DIMM type and the specific processors used in the SHB configuration.

DMA Channels
The SHB is fully PC compatible and the Intel® C604 PCH used on the SHB provides seven independently programmable DMA channels. Channels 0–3 are hardwired to 8-bit, count-by-byte transfers, and channels 5–7 are hardwired to 16-bit, count-by-word transfers. Any two of the seven DMA channels can be programmed to support fast Type-F transfers.

Interrupts
The Intel® C604 PCH incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts are: system timer, keyboard controller, serial ports, parallel ports, floppy disk, mouse, and the DMA channels. In addition, this interrupt controller can support the PCI based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line.

Bios (Flash)
The Aptio® 4.x BIOS from American Megatrends Inc. (AMI) resides in the BTX board's 128MB SPI flash device U62A. The BIOS features built-in advanced CMOS setup for the SHB's operational parameters plus management menus for configuring peripherals and other system configuration parameters. The BIOS may be upgraded from a USB thumb drive storage device by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the USB device installed in drive A. Contact Trenton Technical Support for more information on the latest BIOS revision for your system board. Custom BIOSs are also available, contact Trenton for more information.

Operating Systems
Trenton's BXT7059 and BXTS7059 have been tested using a number of popular and readily available operating systems including: Microsoft Windows XP X64, Windows Server 2003, Windows Server 2008 R2, Windows 7 and a number of variations of Linux including Red Hat. This testing process confirms the SHB's PCI Express interface and device I/O functionality. Trenton does not recommend using the Microsoft Windows XP32 SP2 or SP3 operating system due to limited functionality concerns. Contact Trenton Tech Support for additional information.

Cache Memory
The Intel® Xeon® E5-2400 series processors offer different cache memory capacities. The table below summarizes the cache memory capacities for selected processors available for use with the BXT7059 and BXTS7059 boards.

Processor	Cache Memory Capacity
Intel® Xeon® E5-2448L v2	25MB
Intel® Xeon® E5-2450 v2, Intel® Xeon® E5-2428L v2 and Intel® Xeon® E5-2448L	20MB
Intel® Xeon® E5-2430 v2, Intel® Xeon® E5-2418L v2, Intel® Xeon® E5-2430 and Intel® Xeon® E5-2428L	15MB
Intel® Xeon® E5-2418L and Intel® Xeon® E5-2407	10MB

DDR3 Memory & SHB Memory Population Rules
Trenton recommends ECC registered DDR3-1600 Mini-DIMM memory modules for use on the BXT7059 / BXTS7059 SHBs and these ECC registered (72-bit) DDR3 Mini-DIMMs must be PC3-12800 compliant. Unbuffered ECC DDR3 Mini-DIMMs are also supported on the BXT/BXTS boards, however you cannot mix the ECC registered and unbuffered ECC memory types on the same board.

Each processor on a BXT7059 / BXTS7059 SHB supports three direct-connect DDR3 memory interfaces. The maximum possible memory interface speed obtained depends on the specific Intel® Xeon® E5-2400 v2 or Intel® Xeon® E5-2400 series processor(s) used on the board and other board configuration options listed in the notes section below. The table on the following page illustrates the maximum DDR3 **memory speed** supported as a function of each specific Intel® Xeon® processor when using the recommended PC3-12800 compliant Mini-DIMM modules and an SHB with the latest BIOS support.

DDR3 Memory (continued)

Max. DDR3 Speed	Processor	Cores / Threads	Cache	Long-Life Availability	Maximum Thermal Design Power (TDP)	Operating Temperature Range*
DDR3-1600	Intel® Xeon® E5-2450 v2	8 / 16	20MB	Yes	95W	0°C to 40°C
DDR3-1600	Intel® Xeon® E5-2430 v2	6 / 12	15MB	Yes	80W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2448L v2	10 / 20	25MB	Yes	70W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2428L v2	8 / 16	20MB	Yes	60W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2418L v2	6 / 12	15MB	Yes	50W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2448L	8 / 16	20MB	Yes	70W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2430	6 / 12	15MB	Yes	95W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2428L	6 / 12	15MB	Yes	60W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2418L	4 / 8	10MB	Yes	50W	0°C to 50°C

*Requires a continuous airflow across the board of 350LFM.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR3-1600 Mini-DIMMs.
  - Using an even number of memory modules; particularly with dual-processor BXT7059 board configurations, is not recommended.
  - Using a balanced memory population approach with the BXT7059 configuration; meaning an equal number of Mini-DIMMs per processor, ensures maximum memory interface performance.
- All memory modules must have gold contacts.
- Low-voltage (DDR3L) Mini-DIMMs are not supported.
- The SHB supports the following memory module memory latency timings:
  - 9-9-9 for 1600MHz DDR3 Mini-DIMMs
- **Populate the memory sockets starting with the Mini-DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:**

Mini-DIMM Population Order	CPU0*	Mini-DIMM Population Order	CPU1*
1	BK00	1a	BK10
2	BK01	2a	BK11
3	BK02	3a	BK12

- *CPU0 and CPU1 are both available on BXT7059 SHBs.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board. The BXTS7059 SHB versions feature one processor; however, memory slots BK10, BK11 and BK12 are installed on the SHB but are not active in this single-processor board version.

Universal Serial Bus (USB)

The SHB supports eight high-speed USB 2.0 ports. Connectors for two of the USB ports (0 and 1) are on the I/O bracket and USB ports 2 and 3 are available via headers on the SHB. USB ports 4, 5, 6 and 7 are routed directly to edge connector C of the SHB for use on a PICMG 1.3 backplane.

Video Interface

The SHB features a Graphics Processing Unit (GPU) with 8MB of video memory, and the GPU is driven by a x1 PCIe link from the SHB's Intel® 604 PCH. This combination of features enables the SHB's video port; located on the board's I/O plate, to support pixel resolutions up to 1920 x 1200 (WUXGA) with a 64k color depth.

PCI Express Interfaces
The A0 through A3 PCI Express® links on the SHB connect directly to processor CPU0. These links can operate as either PCI Express 3.0, 2.0 or 1.1 links based on the end-point devices on the backplane that are connected to the SHB and the backplane's PCIe link design itself. In addition to automatically configuring themselves for either PCIe 3.0, 2.0 or 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple x4 links from CPU0 (links A0, A1, A2 and A3) can be utilized on a backplane as a single x16 PCIe electrical link, two x8 links, or four x4 links. CPU0's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. PCIe link B0 comes from the board's PCH and is a PCIe 2.0 interface. Link B0 has a x4 default configuration that can automatically bifurcate into four, x1 PCIe links. An optional PEX10 module connects to the second processor (CPU1) on the dual-processor BXT7059 board to extend the PICMG 1.3 base specification by providing four additional x4 PCIe links. These additional links may also operate as either PCI Express 3.0, 2.0 or 1.1 links and can be combined into one x16, or two x8 or four x4 PCIe interfaces on a PEX10-supported PICMG 1.3 backplane. This BXT7059 capability provides additional PCI Express bandwidth and option card support in the system design. Refer to the *PCI Express® Reference* and to *PCI Express Backplane Usage* chapters of the BXT7059 / BXTS7059 Hardware Manual for more information.

A Word About PCI Express 3.0 Interfaces
PCIe 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen 3, Gen 2 and Gen 1.1 I/O cards on the same interface link. Running a PCIe 3.0 target device such as a Gen 3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the BXT7059) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

Ethernet Interfaces
The BXT7059/BXTS7059 SHB supports three Ethernet interfaces. The first two interfaces are on-board 10/100/1000Base-T Ethernet interfaces located on the board's I/O bracket and implemented using an Intel® i350-AM2 Ethernet Controller. These I/O bracket interfaces support Gigabit, 100Base-T and 10Base-TX Fast Ethernet modes and are compliant with the IEEE 802.3 Specification.

The main components of the I/O bracket Ethernet interfaces are:

- Intel® i350-AM2 for 10/100/1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCIe interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connectors on the SHB's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

The third LAN is supported by the Intel® C604 and the Intel® 82579 Gigabit Ethernet PHY. This 10/100/1000Base-T Ethernet interface is routed to the PICMG 1.3 backplane via edge connector C of the SHB. An alternate backplane LAN cable option is supported via board connector P22. You may elect to create your own backplane LAN cable using the P22 pin-out and mating Molex connector information found in the connectors section of this chapter. However, Trenton Systems does offer a pre-made alternate backplane LAN cable with the mating Molex connector on one end and an RJ45 connector mounted into an I/O bracket on the other end. The Trenton part number for the alternate backplane LAN cable is: **193500001150-00**.

Software drivers are supplied for most popular operating systems.

SATA/600, Serial Attached SCSI (SAS) and SATA/300 Ports

There are seven Serial ATA (SATA) interfaces available on the BXT7059 board. Six SATA ports are on the SHB and four of these ports are capable of supporting either SAS or SATA devices. A seventh SATA/300 interface is routed to edge connector C of the SHB for use on a SATA-equipped PICMG 1.3 backplane. All of the SATA interfaces are driven with a built-in SAS/SATA controller from the Intel® C604 Platform Controller Hub (PCH). The board's SATA ports can support seven independent SATA storage devices such as hard disks and CD-RW devices at data transfer rates up to 300MB per second on each port. The board's PCH features the Intel® Rapid Storage Systems functionality, which allows a third BIOS-selectable SAS/SATA controller configuration that enables either two or four-drive RAID array configurations capable of supporting RAID 0, 1 and 10 implementations.

The board's P31, P32, P35 and P36 ports are the SAS/ SATA/300 interfaces that comply with the Serial Attached SCSI and the SATA 1.0 specifications. These ports can support four independent SAS\SATA storage devices such as hard disks and CD-RW devices at data transfer rates up to 300MB per second on each port.

Ports P27 and P28 are SATA/600 interfaces compatible with the SATA 2.0 specification and capable of supporting data transfer rates up to 600MB per second on each port.

The SAS/SATA controller has three BIOS selectable modes of operation located under the Advanced/SATA Configuration menu with a legacy (i.e. IDE) mode using I/O space, an AHCI mode using memory space and a RAID mode. Software drivers that uses legacy mode will not have AHCI capabilities. The board's Intel® C604 supports the Intel® Rapid Storage Systems feature that enables RAID configurations on the SATA or SAS ports.

Watchdog Timer (WDT)
The BXT7059 provides a programmable Watchdog Timer with 7 programmable timeout periods ranging from 32msec to 32 seconds. When enabled the WDT will generate a system reset. WDT control is supplied via the C604's (PCH) General Purpose IO pins. The C604's GPIO_LVL3 register control the states of GPIO signals that select the timeout period. The C604's GPIO_LVL2 register provides the WDT's enable\disable function. Both of these 32-bit registers are located within GPIO IO spaces. The GPIO_BASE IO address is determined by the values programmed into the C604's LPC Bridge PCI configuration at offset 48-4B(h).

GPIO Bit Definitions:

Watchdog Timer Enable (WDT_EN#)
Watchdog timer enable\disable functionality is controlled by GPIO46. Clearing bit 15 of the GP_LVL2 register enables the WDT. The GP_LVL2 register is located at IO address GPIO_BASE + offset 38(h). The power-on default for this bit is a "1" which disables WDT functionality. Setting this bit to a "0" enables the WDT at the pre-selected interval.

Watchdog Select 0 (WDT_S0)
The state of this bit in conjunction with WatchDog Select 1 will select the WDT time out period. This function is controlled by GPIO64 and the state of this bit is determined by bit 0 of the GP_LVL3 register at IO address GPIO_BASE + offset 48(h). After POST the inverted state of this bit is reflected on Port80, LED0. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on. See Table 1 for WDT interval selection.

Watchdog Select 1 (WDT_S1)
The state of this bit in conjunction with WatchDog Select 0 will select the WDT time out period. This function is controlled by GPIO65 and the state of this bit is determined by bit 1 of the GP_LVL3 register at IO address GPIO_BASE + offset 48(h). After POST the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on. See Table 1 for WDT interval selection.

WatchDOG Select 2 (WDT_S2)
The state of this bit in conjunction with WatchDog Select 2 will select the WDT time out period. This function is controlled by GPIO66 and the state of this bit is determined by bit 2 of the GP_LVL3 register at IO address GPIO_BASE + offset 48(h). After POST the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on. See Table 1 for WDT interval selection.

Watchdog_ Input (WDT_IN)
When the WDT is enabled this bit must be toggled (0 -> 1 or 1->0) within the selected watchdog timeout period, failure to do so will result in a system reset. This function is supported by the GPIO71 bit and its state is controller by bit 7 the GP_LVL3 register which is at IO address GPIO_BASE + offset 48(h). The inverted state of this bit is reflected on Port80, LED7. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on.

Watchdog Timeout Period Selections:

WDT_EN# (GPIO46)	WD_S2 (GPIO66)	WD_S1 (GPIO65)	WD_S0 (GPIO64)	Watchdog Timeout Period
1	X	X	X	Disabled
0	0	0	0	32 msec
0	0	0	1	128 msec
0	0	1	0	512 msec
0	0	1	1	1 sec
0	1	0	0	4 sec
0	1	0	1	8 sec
0	1	1	0	32 sec
0	1	1	1	Disabled

Watchdog Timer (WDT - continued)
The Watchdog Timer may require initialization prior to usage. GPIOs 46, 64, 65, 66, 71 are required to be configured as outputs. While these GPIOs do default to outputs at power-on, care should be taken to insure they have not been altered prior to WDT usage. These GPIOs are configured to outputs by clearing bits 0, 1, 2 and 7 of the GP_IO_SEL3 register at GPIO_BASE + offset 44(h) to a "0", as well a clearing bit 15 of GP_IO_SEL2 register at GPIO_BASE + offset 34(h) to a "0".

After initialization is completed (if required) the Watchdog timer period is selected by the WDT_S2, WD_SELS1 and WDT_S0 bits. Once the timeout period has been programmed the WDT is then "enabled" by clearing the WDT_EN# bit. To avoid the WDT from generating a system reset the WDT_IN bit must be toggled within the timeout period.

Programming Example: Enable WDT with 1-second timeout period

Note: *When writing to any of the WDT controlling GPIO bits the remaining bits of the selected GP_LVL2 and GP_LVL3 register should remain unchanged.*

Write bit 15 of GP_LVL2 to 1	pre condition GPIO32 for WDT disable
Write bits 2,1,0 of GP_LVL3 to 0,1,1,	set Watchdog timeout period to 1 sec
Write bit 15 of GP_LVL2 to 0	enable Watchdog timer

At this point the bit 7 of GP_LVL7 (GPIO71) must be toggled within a 1 second time period or the WDT will expire resulting in a system reset.

Power Fail Detection
A hardware reset may be issued when monitored voltages on the SHB drop below a specified nominal low voltage limit. In addition, the BXT/BXTS board is capable of generating an SMI# on the de-assertion of the Power Good signal from the backplane. This allows a processor to sense an impending power failure with the system power supply being responsible for maintaining the +12V, +5V and 3.3V rails in tolerance for the period of time necessary to service the SMI# interrupt. The monitored voltages and their nominal low limits are listed below.

Monitored Voltage	Power Source	Usage	Nominal Low Limit		Comment
12V	System Power Supply		10.2V	+/- 2%	Fixed
5V	System Power Supply		4.63V	+/-2.5%	Fixed
3.3V	System Power Supply		2.88V	+/- 2.5%	Fixed
1.5V	On-board Regulator	Chipset	1.5V	+/- 4.5%	Fixed
1.1V	On-board Regulator	Chipset	0.89V	+/- 3.5%	Fixed
1.05V	On-board Regulator	Processor	0.88V	+/- 3.5%	Fixed
CPUx_PLL	On-board Regulator	Processor	(V_{PLL} * 0.88)	+/- 3.5%	V_{PLL}: 1.8V Sandy Bridge / 1.7V Ivy Bridge
CPUx_VTT	On-board Regulator	Processor	(V_{VTT} * 0.88)	+/- 3.5%	V_{VTT}: 1.05V Sandy Bridge / 1.0V Ivy Bridge

Battery
A built-in lithium battery is provided, for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Power Requirements – Dual-Processor BXT7059

Typical values* - 100% stress state with 24GB of DDR3 system memory installed:

Processor Type	Processor Speed	+5V	+12V	+3.3V
Intel® Xeon® E5-2450 v2	2.5GHz	1.93A	19.57A	3.55A
Intel® Xeon® E5-2430 v2	2.5GHz	1.72A	12.32A	3.21A
Intel® Xeon® E5-2448L v2	1.8GHz	1.68A	12.60A	3.11A
Intel® Xeon® E5-2428L v2	1.8GHz	1.72A	10.07A	3.23A
Intel® Xeon® E5-2418L v2	2.0GHz	1.62A	8.31A	3.19A
Intel® Xeon® E5-2430	2.2GHz	1.34A	15.11A	4.55A
Intel® Xeon®E5-2407	2.2GHz	1.31A	8.86A	4.21A
Intel® Xeon® E5-2448L	1.8GHz	1.37A	11.60A	4.49A
Intel® Xeon® E5-2428L	1.8GHz	1.34A	10.27A	4.55A

Typical values* - Static desktop (system idle) state with 24GB of DDR3 system memory installed:

Processor Type	Processor Speed	+5V	+12V	+3.3V
Intel® Xeon® E5-2450 v2	2.5GHz	1.65A	6.66A	3.11A
Intel® Xeon® E5-2430 v2	2.5GHz	1.56A	5.22A	3.21A
Intel® Xeon® E5-2448L v2	1.8GHz	1.66A	5.58A	3.03A
Intel® Xeon® E5-2428L v2	1.8GHz	1.58A	4.96A	3.05A
Intel® Xeon® E5-2418L v2	2.0GHz	1.48A	4.13A	2.98A
Intel® Xeon® E5-2430	2.2GHz	1.30A	3.73A	4.15A
Intel® Xeon®E5-2407	2.2GHz	1.22A	3.08A	3.89A
Intel® Xeon® E5-2448L	1.8GHz	1.34A	4.06A	4.11A
Intel® Xeon® E5-2428L	1.8GHz	1.30A	3.89A	4.18A

Power Requirements – Single-Processor BXTS7059

Typical values* - 100% stress state with 12GB of DDR3 system memory installed:

Processor Type	Processor Speed	+5V	+12V	+3.3V
Intel® Xeon® E5-2450 v2	2.5GHz	1.53A	9.15A	3.07A
Intel® Xeon® E5-2430 v2	2.5GHz	1.81A	6.96A	3.35A
Intel® Xeon® E5-2448L v2	1.8GHz	1.75A	7.45A	3.45A
Intel® Xeon® E5-2428L v2	1.8GHz	1.74A	5.96A	3.41A
Intel® Xeon® E5-2418L v2	2.0GHz	1.71A	4.61A	3.27A
Intel® Xeon® E5-2430	2.2GHz	1.26A	7.77A	3.57A
Intel® Xeon®E5-2407	2.2GHz	1.24A	4.49A	3.44A
Intel® Xeon® E5-2448L	1.8GHz	1.23A	5.79A	3.52A
Intel® Xeon® E5-2428L	1.8GHz	1.25A	5.17A	3.60A

Typical values* - Static desktop (system idle) state with 12GB of DDR3 system memory installed:

Processor Type	Processor Speed	+5V	+12V	+3.3V
Intel® Xeon® E5-2450 v2	2.5GHz	1.33A	4.07A	2.83A
Intel® Xeon® E5-2430 v2	2.5GHz	1.63A	2.79A	3.21A
Intel® Xeon® E5-2448L v2	1.8GHz	1.69A	3.13A	3.31A
Intel® Xeon® E5-2428L v2	1.8GHz	1.68A	2.87A	3.33A
Intel® Xeon® E5-2418L v2	2.0GHz	1.63A	2.74A	3.22A
Intel® Xeon® E5-2430	2.2GHz	1.19A	1.70A	3.60A
Intel® Xeon®E5-2407	2.2GHz	1.18A	1.52A	3.48A

Processor Type	Processor Speed	+5V	+12V	+3.3V
Intel® Xeon® E5-2448L	1.8GHz	1.17A	1.67A	3.57A
Intel® Xeon® E5-2428L	1.8GHz	1.21A	1.75A	3.63A

Ten-core CPU – E5-2448L v2
Eight-core CPU - E5-2450 v2, E5-2428L v2 and E5-2448L
Six-core CPUs - E5-2430 v2, E5-2418L v2, E5-2430 and E5-2428L
Four-core CPU - E5-2407

Note 1: All CPUs support Intel® Turbo Boost Technology except the Intel® Xeon® E5-2418L v2 and the Intel® Xeon® E5-2407 processors
Note 2: All CPUs have Intel® Hyper-Threading except the Intel® Xeon® E5-2407 processor

* Typical power numbers; actual power numbers will vary as a function of the specific BXT7059 system configuration design. Tolerance for all voltages is +/- 5%

CAUTION: Trenton recommends an EPS type of power supply for systems using high-performance processors. The power needs of backplane option cards, high-performance processors and other system components may result in drawing 20A of current from the +12V power supply line. If this occurs, hazardous energy (240VA) could exist inside the system chassis. Final system/equipment suppliers must provide protection to service personnel from these potentially hazardous energy levels.

Stand-by voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

Temperature/Environment

Operating Temperature: 0-50° C. with the standard cooling solution and 350LFM of continuous airflow
0-40° C. when using two Intel® Xeon® E5-2450 v2 processors in a BXT7059 SHB configuration with the standard cooling solution and 350LFM of continuous airflow

Air Flow Requirement: 350LFM continuous airflow

Storage Temperature: - 40º C. to 70º C.

Humidity: 5% to 90% non-condensing

Mechanical

The standard cooling solution used on the BXT7059 and BXTS7059 SHBs enables placement of option cards approximately 2.15" (54.61mm) away from the top component side of the SHB. Contact Trenton for a system engineering consultation if your application needs a lower profile cooling solution. The SHB's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

Board Stiffener Bars & Backer Plate

The two stiffener bars and backer plate on the bottom side of the SHB maximize system integrity by ensuring proper SHB alignment within the card guides of a computer chassis. The stiffeners and backer plate provide reliable SHB operation by protecting sensitive board components from mechanical damage and assist in the safe insertion and removal of the SHB from the system.

Configuration Jumpers
The setup of the configuration jumpers on the SHB is described below. * indicates the default value of each jumper.

NOTE: For the three-position JU12 jumper, "RIGHT" is toward the I/O bracket side of the board; "LEFT" is toward the CPU1 DDR3 Memory sockets.

Jumper	Description
JU1	**SPI Update** (two position jumper) Install for one power-up cycle to enable the board to unprotect the SHB's SPI storage device. Remove for normal operation. * **CAUTION:** Installing this jumper is only done for special board operations such as changing the PCI Express link bifurcation operation. Contact Trenton tech support ***before*** installing this jumper to prevent any unintended system operation.
JU2	**BIOS Recovery** (two position jumper) Install for one power-up cycle to recover factory default BIOS settings. Remove for normal operation. *
JU3	**DCMI Enable** (two position jumper) Install to enable Intel® Data Center Manageability Interface (Intel® DCMI) operation. Remove for Intel® Advanced Management Technology (Intel® AMT 7.0) operation. * NOTE: Intel® DCMI is an optional operating condition supported on the BXT7059. This mode of operation requires an updated SPI image since DCMI requires changes to the board's BIOS and management engine firmware. Contact Trenton for additional information.
JU8	**Password Clear** (two position jumper) Install for one power-up cycle to reset the password to the default (null password). Remove for normal operation. *
JU12	**CMOS Clear** (three position jumper) Install on the LEFT to clear. Install on the RIGHT to operate. * **NOTE:** To clear the CMOS, power down the system and install the JU12 jumper on the LEFT. Wait for at least two seconds, move the jumper back to the RIGHT and turn the power on. Clearing CMOS on the BXT7059 will not result in a checksum error on the following boot. If you want to change a BIOS setting, you must press DEL or the F2 key during POST to enter BIOS setup after clearing CMOS.

P4A/P4B Ethernet LEDs and Connectors

The I/O bracket houses the two RJ-45 network connectors for Ethernet LAN1 and LAN2. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

LED/Connector	Description
Activity LED	Yellow LED indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).
Off	No current network transmit or receive activity
On (solid)	Indicates a valid link established, but no network activity.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Green/Orange bi-color LED identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).
Off	Indicates a valid link at 10-Mb/s.
On (orange)	Indicates a valid link at 100-Mb/s.
On (green)	Indicates a valid link at 1000-Mb/s or 1-Gb/s.

Status LEDs

The following status LEDs are located on the topside on the SHB. Refer to the board layout drawings for each LED's location.

LED9 ERROR LED

The error LED indicates several different error conditions noted below. The LED is located just above the BK02 DIMM socket

LED Status	Description
Off	Indicates the normal board operation.
On (solid)	Indicates a CPU is throttling down to a lower operating speed due to rising CPU temperature. Indicates the CPU has reached the thermal shutdown threshold limit. The SHB may or may not be operating, but a board shutdown condition will soon occur
On (fast blink rate)	Indicates a catastrophic error condition has occurred. The SHB suspends system operation until the error condition is corrected. Contact Trenton tech support.
On (slow blink rate)	A potential error condition has been detected. The SHB continues to operate, but the system should be checked for errors.

NOTE: When a thermal shutdown occurs, the LED will stay on in systems using non- ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the SHB. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all SHB LEDs will turn off; however, stand-by power will still be present.

LED10 Backplane LAN LED

The backplane LAN LED is located below LED11 in the upper left corner of the board. This LED indicated the status of the Ethernet communications link between the SHB and the backplane as show below:

LED Status	Description
Off	Indicates LAN is inactive and link communications have not been established.
On (flashing)	Indicates data is being transferred between the SHB and the backplane.
On (solid)	Indicates the LAN has a valid link and is ready for data transfers.

Status LEDs (continued)

LED11 and LED12 **VRM LEDs**

These LEDs monitor the status on the power circuits associated with the SHBs processors.

LED Status	Description
Off	All power circuits are operating within acceptable limits and driving the CPUs correctly.
On	The CPUs have shut down most likely due to a VRM fault. Contact Trenton for assistance.

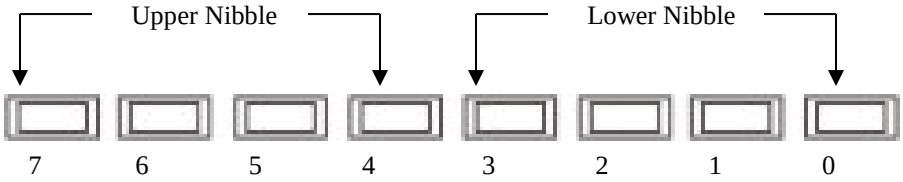
Post Code LEDs - LED0 through LED7

As the POST, (Power On Self Test) routines are performed during boot-up; test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7). Refer to the board layout diagram for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. After a normal POST sequence the LEDs are off (00h) indicating that the SHB's BIOS has passed control over to the operating system loader typically at interrupt INT19h. Specific test codes and their meaning along with the following chart are listed in Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



BXT7059 & BXTS7059 POST Code LEDs

System BIOS Setup Utility

The BXT7059 and BXTS7059 feature the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. The TSE setup utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details of the Aptio TSE are provided in the separate *BXT7059 / BXTS7059 BIOS Technical Reference* manual. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the BXT7059 or BXTS7059 web pages.

Connectors

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - **Video Interface Connector**
15 pin connector, Amp 1-1734530-3

Pin	Signal	Pin	Signal	Pin	Signal
		6	Gnd		
1	Red			11	NC
		7	Gnd		
2	Green			12	EEDI
		8	Gnd		
3	Blue			13	HSYNC
		9	+5		
4	NC			14	VSYNC
		10	Gnd		
5	Gnd			15	EECS

Note:
1 – Connector supports standard DB15 video cables

P2, P19 - **CPU Fan Power Connectors**
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

Notes:
1 – P2 is the fan connector of CPU2 and P19 is for CPU1

P4A, P4B - **10/100/1000Base-T Ethernet Connectors - LAN1/LAN2**
Dual RJ-45 connector, Pulse #JG0-0024NL
Each individual RJ-45 connector is defined as follows:

Pin	Signal	Pin	Signal
1A	L2_MDI0n	1B	L1_MDI0n
2A	L2_MDI0p	2B	L1_MDI0p
3A	L2_MDI1n	3B	L1_MDI1n
4A	L2_MDI1p	4B	L1_MDI1p
5A	L2_MDI2n	5B	L1_MDI2n
6A	L2_MDI2p	6B	L1_MDI2p
7A	L2_MDI3n	7B	L1_MDI3n
8A	L2_MDI3p	8B	L1_MDI3p
9A	VCC_1.8V	9B	VCC_1.8V
10A	GND_A	10B	GND_b

Notes:
1 - LAN ports support standard CAT5 Ethernet cables
2 – P4A is LAN2 and P4B is LAN1

P5 - **Speaker Port Connector**
4 pin single row header, Amp #640456-4

Pin	Signal
1	Speaker Data
2	Key
3	Gnd
4	+5V

Connectors (Continued)

P6 - **Reset Connector**
2 pin single row header, Amp #640456-2

Pin	Signal	Pin	Signal
1	Gnd	2	Reset In

P7 - **PMBUS Connector**
5 pin single row Mini MI2 header, Molex # 554470570
(For use in optional DCMI applications only)

Pin	Signal
1	SMCLK_Link1
2	SMDATA_Link1
3	PMBUS_Alert#
4	GND
5	+3.3V

P12 - **Hard Drive LED Connector**
4 pin single row header, Amp #640456-4

Pin	Signal
1	LED+
2	LED-
3	LED-
4	LED+

P17 - **Dual Universal Serial Bus (USB) Connector**
10 pin dual row header, Molex #702-46-1001
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3
9	NC	10	NC

P17A - **Universal Serial Bus (USB) Connector**
USB vertical connector, Molex #6739-8001
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB0
2	USB0-
3	USB0+
4	Gnd-USB0

P17B - Universal Serial Bus (USB) Connector

USB vertical connector, Molex #6739-8001
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB1
2	USB1-
3	USB1+
4	Gnd-USB1

P21 - Power Good LED Connector

2 pin single row header, Amp #640456-2

Pin	Signal	Pin	Signal
1	LED-	2	LED+

P22 - 10/100/1000Base-T Ethernet Connector – Alternate Backplane LAN Over Cable

8 pin single row connector, Molex #0554500859

Pin	Signal
1	A_MDI2N
2	A_MDI2P
3	A_MDI3N
4	A_MDI3P
5	A_MDI1N
6	A_MDI1P
7	A_MDI0N
8	A_MDI0P

BP LAN Cable Option

You may elect to create your own backplane LAN cable using the P22 pin-out data and the mating Molex connector information below. However, Trenton Systems does offer a pre-made alternate backplane LAN cable with the mating Molex connector on one end and an RJ45 connector mounted into an I/O bracket on the other end. The Trenton part number for the alternate backplane LAN cable is: **193500001150-00**.

Note: Using the alternate backplane LAN cable effectively disconnects the LAN routing down to SHB edge connector C.

Note: The mating Molex connector to use when making this alternative backplane LAN cable has a Molex part number of 0513360810.

P27, P28 - SATA/600 Ports

7 pin vertical connector with latch, Molex #67800-8005

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

Notes:
1 – P27 = SATA0 interface, P28 = SATA1 interface
2 – Connectors support standard SATA II interface cables

P31, P32, P35, P36 - SAS/SATA/300 Ports

7 pin vertical connector with latch, Molex #67800-8005

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

Notes:
1 – P31 = SATA2 interface, P32 = SATA3 interface, P35 = SATA4 interface, P36 = SATA5 interface
2 – Connectors support standard SATA II interface cables

Connectors (Continued)

P20 - I/O Expansion Mezzanine Card Connector

76 pin controlled impedance connector, Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12	2	+5V_STANDBY
3	HDA_SDIN2	4	+5V_STANDBY
5	HDA_SDIN1	6	+5V_DUAL
7	HDA_SDIN0	8	+5V_DUAL
9	HDA_SYNC	10	HDA_BITCLK
11	HDA_SDOUT	12	HDA_ACRST
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SBMCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP5	48	C_PE_RXP5
49	C_PE_TXN5	50	C_PE_RXN5
51	Gnd	52	Gnd
53	NC	54	NC
55	NC	56	NC
57	Gnd	58	Gnd
59	NC	60	NC
61	NC	62	NC
63	Gnd	64	Gnd
65	NC	66	NC
67	NC	68	NC
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5V

Connectors (Continued)

P3 - PCI Express Gen 3.0 Expansion Connector

(For PEX10 option module)

80 pin (40 differential pairs) high-speed socket strip, Samtec #QSH-040-01-F-D-DP

(Note: Connector P3 is not active on the BTXS7059 board configuration.)

Pin	Signal	Pin	Signal
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	P1_PE_RXN15	10	P1_PE_TXN15
11	P1_PE_RXP15	12	P1_PE_TXP15
13	P1_PE_RXN14	14	P1_PE_TXN14
15	P1_PE_RXP14	16	P1_PE_TXP14
17	P1_PE_RXN13	18	P1_PE_TXN13
19	P1_PE_RXP13	20	P1_PE_TXP13
21	P1_PE_RXN12	22	P1_PE_TXN12
23	P1_PE_RXP12	24	P1_PE_TXP12
25	P1_PE_RXN11	26	P1_PE_TXN11
27	P1_PE_RXP11	28	P1_PE_TXP11
29	P1_PE_RXN10	30	P1_PE_TXN10
31	P1_PE_RXP10	32	P1_PE_TXP10
33	P1_PE_RXN9	34	P1_PE_TXN9
35	P1_PE_RXP9	36	P1_PE_TXP9
37	P1_PE_RXN8	38	P1_PE_TXN8
39	P1_PE_RXP8	40	P1_PE_TXP8
41	NC	42	NC
43	NC	44	NC
45	P1_PE_CFG3	46	P1_PE_CGF1
47	P1_GEN2_DSBL#	48	P1_PE_CFG0
49	P1_PE_RXN7	50	P1_PE_TXN7
51	P1_PE_RXP7	52	P1_PE_TXP7
53	P1_PE_RXN6	54	P1_PE_TXN6
55	P1_PE_RXP6	56	P1_PE_TXP6
57	P1_PE_RXN5	58	P1_PE_TXN5
59	P1_PE_RXP5	60	P1_PE_TXP5
61	P1_PE_RXN4	62	P1_PE_TXN4
63	P1_PE_RXP4	64	P1_PE_TXP4
65	P1_PE_RXN3	66	P1_PE_TXN3
67	P1_PE_RXP3	68	P1_PE_TXP3
69	P1_PE_RXN2	70	P1_PE_TXN2
71	P1_PE_RXP2	72	P1_PE_TXP2
73	P1_PE_RXN1	74	P1_PE_TXN1
75	P1_PE_RXP1	76	P1_PE_TXP1
77	P1_PE_RXN0	78	P1_PE_TXN0
79	P1_PE_RXP0	80	P1_PE_TXP0

Note:

1 – Need CPU2 installed for PCIe GEN 2.0 link expansion via the Trenton PEX10 option module.

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Chapter 2 PCI Express® Reference

Introduction

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

PCI Express Links

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion. A link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. In PCI Express Gen 1 the bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	250MB/s	500MB/s
x4	1GB/s	2GB/s
x8	2GB/s	4GB/s
x16	4GB/s	8GB/s

In PCI Express Gen 2 the bandwidths for the PCIe links are doubled as compared to PCIe Gen 1.1 as shown below:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	500MB/s	1GB/s
x4	2GB/s	4GB/s
x8	4GB/s	8GB/s
x16	8GB/s	16GB/s

PCI Express Links (continued)

PCI Express 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen 3, Gen 2 and Gen 1.1 I/O cards on the same interface link. In PCI Express Gen 3 the bandwidths for the PCIe links are doubled as compared to PCIe Gen 2.0 as shown below:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	1GB/s	2GB/s
x4	4GB/s	8GB/s
x8	8GB/s	16GB/s
x16	16GB/s	32GB/s

Running a PCIe 3.0 target device such as a Gen 3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the BXT7059) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

Scalability is a core feature of PCI Express. Some chipsets allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. In addition, although a board with a higher number of lanes will not function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) because the connectors are mechanically and electrically incompatible, the reverse configuration will function. A board with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot). The link auto-negotiates between the PCI Express devices to establish communication. The mechanical option card slots on a PICMG 1.3 backplane must have PCI Express configuration straps that alert the SHB to the PCI Express electrical configuration expected. The SHB can then reconfigure the PCIe links for optimum system performance.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express® System Host Board PCI Express Specification, PICMG® 1.3*.

SHB Configurations

The BXT7059 and BXTS7059 are combo class SHBs that support either PCI Express server-class or graphics-class backplane configurations. Server applications require multiple, high-bandwidth PCIe links, and therefore the server-class SHB/backplane configuration is identified by multiple x8 and x4 links to the SHB edge connectors.

SHBs, which require high-end video or graphics cards generally, use a x16 PCI Express link. The graphics-class SHB/backplane configuration is identified by one x16 PCIe link and one x4 or four x1 links to the edge connectors. As PCI Express chipsets continue to evolve, it is possible that more x4 and/or x1 links could be supported in graphics-class SHBs. Currently, most video or graphics cards communicate to the SHB at an effective x1, x4 or x8 PCI Express data rate and do not actually make use of all of the signal lanes in a x16 connector.

NOTE: The BXT7059 / BXTS7059 eliminates the PICMG 1.3 requirement that server-class SHBs should always be used with server-class PICMG 1.3 backplanes and graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes. This is because the PCIe links integrated BXT processors and SHB architecture itself can sense the backplane end-point devices and configure the SHB links for either server or graphics-class operations. For this reason the Trenton BXT7059 and BXTS7059 are called combo-class SHBs.

PCI Express Edge Connector Pin Assignments

Trenton's BXT7059/BXTS7059 SHB uses edge connectors A, B and C. Optional I/O signals are defined in the PICMG 1.3 specification and if implemented must be located on edge connector C of the SHB. The SHB makes the Intelligent Platform Management Bus (IPMB) signals available to the user. The SHB supports four USB ports (USB 4, 5, 6 and 7) and one 10/100/1000Base-T Ethernet interface on PICMG 1.3 compatible backplanes via the SHB's edge connector C. The following table shows pin assignments for the PCI Express edge connectors on the BXT7059 / BXTS7059 SHB.

* Pins 3 and 4 of Side B of Connector A (TDI and TDO) are jumpered together.

Connector A			Connector B			Connector C			Connector D (Not Available)		
	Side B	Side A		Side B	Side A		Side B	Side A		Side B	Side A
1	SMCLK	SMBDAT	1	+5VSBY	+5VSBY	1	USBP0+	GND	1	INTB#	INTA#
2	GND	GND	2	GND	NC	2	USBP0-	GND	2	INTD#	INTC#
3	TDI TDO*	NC	3	A_PE_TXP8	GND	3	GND	USBP1+	3	GND	NC
4	TDI TDO*	NC	4	A_PE_TXN8	GND	4	GND	USBP1-	4	REQ3#	GNT3#
5	NC	ICH WAKE#	5	GND	A_PE_RXP8	5	USBP2+	GND	5	REQ2#	GNT2#
6	PWRBTN#	ICH PCIPME#	6	GND	A_PE_RXN8	6	USBP2-	GND	6	PCIRST#	GNT1#
7	PWROK	PSON#	7	A_PE_TXP9	GND	7	GND	USBP3+	7	REQ1#	GNT0#
8	SHBRST#	EXP RESET#	8	A_PE_TXN9	GND	8	GND	USBP3-	8	REQ0#	SERR#
9	CFG0	CFG1	9	GND	A_PE_RXP9	9	USBOC0	GND	9	NC	3.3V
10	CFG2	CFG3	10	GND	A_PE_RXN9	10	GND	USBOC1	10	GND	CLKFI
11		GND	11	RSVD	GND	11	USBOC2	GND	11	CLKFO	GND
Mechanical Connector			Mechanical Connector			Mechanical Connector			Mechanical Connector		
12	GND	RSVD	12	GND	RSVD	12	GND	USBOC3	12	CLKC	CLKD
13	B_PE_TXP0	GND	13	A_PE_TXP10	GND	13	S5_TXP	GND	13	GND	3.3V
14	B_PE_TXN0	GND	14	A_PE_TXN10	GND	14	S5_TXN	GND	14	CLKA	CLKB
15	GND	B_PE_RXP0	15	GND	A_PE_RXP10	15	GND	S5_RXP	15	3.3V	GND
16	GND	B_PE_RXN0	16	GND	A_PE_RXN10	16	GND	S5_RXN	16	AD31	PME#
17	B_PE_TXP1	GND	17	A_PE_TXP11	GND	17	S4_TXP	GND	17	AD29	3.3V
18	B_PE_TXN1	GND	18	A_PE_TXN11	GND	18	S4_TXN	GND	18	M6_6_EN	AD30
19	GND	B_PE_RXP1	19	GND	A_PE_RXP11	19	GND	S4_RXP	19	AD27	AD28
20	GND	B_PE_RXN1	20	GND	A_PE_RXN11	20	GND	S4_RXN	20	AD25	GND
21	B_PE_TXP2	GND	21	A_PE_TXP12	GND	21	A_MDI0P	GND	21	GND	AD26
22	B_PE_TXN2	GND	22	A_PE_TXN12	GND	22	A_MDI0N	GND	22	CBE3#	AD24
23	GND	B_PE_RXP2	23	GND	A_PE_RXP12	23	GND	A_MDI1P	23	AD23	3.3V
24	GND	B_PE_RXN2	24	GND	A_PE_RXN12	24	GND	A_MDI1N	24	GND	AD22
25	B_PE_TXP3	GND	25	A_PE_TXP13	GND	25	A_MDI2P	GND	25	AD21	AD20
26	B_PE_TXN3	GND	26	A_PE_TXN13	GND	26	A_MDI2N	GND	26	AD19	PCIXCAP
27	GND	B_PE_RXP3	27	GND	A_PE_RXP13	27	GND	A_MDI3P	27	+5V	AD18
28	GND	B_PE_RXN3	28	GND	A_PE_RXN13	28	NC	A_MDI3N	28	AD17	AD16
29	REFCLK0	GND	29	A_PE_TXP14	GND	29	IPMB_CLK	GND	29	CBE2#	GND
30	REFCLK0#	GND	30	A_PE_TXN14	GND	30	IPMB_DAT	GND	30	GND	FRAME#
31	GND	REFCLK1#	31	GND	A_PE_RXP14	31	NC	NC	31	IRDY#	TRDY#
32	RSVD-G	REFCLK1	32	GND	A_PE_RXN14	32	NC	NC	32	DEVSEL#	+5V

Connector A		
	Side B	Side A
33	REFCLK2#	GND
34	REFCLK2	GND
35	GND	REFCLK3#
36	RSVD-G	REFCLK3
37	REFCLK4#	GND
38	REFCLK4	GND
39	GND	REFCLK5# PU
40	RSVD-G	REFCLK PU
41	REFCLK6# PU	GND
42	REFCLK6 PU	GND
43	GND	REFCLK7# PU
44	GND	REFCLK7 PU
45	A_PE_TXP0	GND
46	A_PE_TXN0	GND
47	GND	A_PE_RXP0
48	GND	A_PE_RXN0
49	A_PE_TXP1	GND
50	A_PE_TXN1	GND
51	GND	A_PE_RXP1
52	GND	A_PE_RXN1
53	A_PE_TXP2	GND
54	A_PE_TXN2	GND
55	GND	A_PE_RXP2
56	GND	A_PE_RXN2
57	A_PE_TXP3	GND
58	A_PE_TXN3	GND
59	GND	A_PE_RXP3
60	GND	A_PE_RXN3
61	A_PE_TXP4	GND
62	A_PE_TXN4	GND
63	GND	A_PE_RXP4
64	GND	A_PE_RXN4
65	A_PE_TXP5	GND
66	A_PE_TXN5	GND
67	GND	A_PE_RXP5
68	GND	A_PE_RXN5
69	A_PE_TXP6	GND
70	A_PE_TXN6	GND
71	GND	A_PE_RXP6
72	GND	A_PE_RXN6
73	A_PE_TXP7	GND
74	A_PE_TXN7	GND
75	GND	A_PE_RXP7
76	GND	A_PE_RXN7
77	SERIRQ	GND
78	3.3V	3.3V
79	3.3V	3.3V
80	3.3V	3.3V
81	3.3V	3.3V
82	NC	NC

Connector B		
	Side B	Side A
33	A_PE_TXP15	GND
34	A_PE_TXN15	GND
35	GND	A_PE_RXP15
36	GND	A_PE_RXN15
37	NC	GND
38	NC	NC
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND
44	+12V	+12V
45	+12V	+12V
46	+12V	+12V
47	+12V	+12V
48	+12V	+12V
49	+12V	+12V

Connector C		
	Side B	Side A
33	NC	NC
34	NC	GND
35	NC	GND
36	GND	NC
37	GND	NC
38	NC	GND
39	NC	GND
40	GND	NC
41	GND	NC
42	3.3V	3.3V
43	3.3V	3.3V
44	3.3V	3.3V
45	3.3V	3.3V
46	3.3V	3.3V
47	3.3V	3.3V
48	3.3V	3.3V
49	3.3V	3.3V
50	3.3V	3.3V
51	GND	GND
52	GND	GND
53	GND	GND
54	GND	GND
55	GND	GND
56	GND	GND
57	GND	GND
58	GND	GND
59	+5V	+5V
60	+5V	+5V
61	+5V	+5V
62	+5V	+5V
63	GND	GND
64	GND	GND
65	GND	GND
66	GND	GND
67	GND	GND
68	GND	GND
69	GND	GND
70	GND	GND
71	GND	GND
72	GND	GND
73	+12V_VRM	+12V_VRM
74	+12V_VRM	+12V_VRM
75	+12V_VRM	+12V_VRM
76	+12V_VRM	+12V_VRM
77	+12V_VRM	+12V_VRM
78	+12V_VRM	+12V_VRM
79	+12V_VRM	+12V_VRM
80	+12V_VRM	+12V_VRM
81	+12V_VRM	+12V_VRM
82	+12V_VRM	+12V_VRM

Connector D (Not Available)		
	Side B	Side A
33	PLOCK#	STOP#
34	PERR#	GND
35	GND	CBE1#
36	PAR	AD14
37	NC	GND
38	GND	AD12
39	AD15	AD10
40	AD13	GND
41	GND	AD9
42	AD11	CBE0#
43	AD8	GND
44	GND	AD6
45	AD7	AD5
46	AD4	GND
47	GND	AD2
48	AD3	AD1
49	AD0	GND

PCI Express Signals Overview

The following table provides a description of the SHB slot signal groups on the PCI Express connectors.

Type	Signals	Description	Connector	Source
Global	GND, +5V, +3.3V, +12V	Power		Backplane
	PSON#	Optional ATX support	A	SHB
	PWRGD, PWRBT#, 5Vaux	Optional ATX support	A and B	Backplane
	TDI	Optional JTAG support	A	Backplane
	TDO	Optional JTAG support	A	SHB
	SMCLK, SMDAT	Optional SMBus support	A	SHB & Backplane
	IPMB_CL, IPMB_DA	Optional IPMB support	C	SHB & Backplane
	CFG[0:3]	PCIe configuration straps	A	Backplane
	SHB_RST#	Optional reset line	A	SHB
	RSVD	Reserved	A and B	
	RSVD-G	Reserved ground	A	Backplane
	WAKE#	Signal for link reactivation	A	Backplane
PCIe	a_PETp[0:15] a_PETn[0:15] a_PERp[0:15] a_PERn[0:15]	Point-to-point from SHB slot through the x16 PCIe connector (A) to the target device(s)	A and B	SHB & Backplane
	b_PETp[0:3] b_PETn[0:3] b_PERp[0:3] b_PERn[0:3]	Point-to-point from SHB slot through the x8 PCIe connector (B) to the target device(s)	A	SHB & Backplane
	REFCLK[0:7]+, REFCLK[0:7]-	Clock synchronization of PCIe expansion slots	A	SHB
	PERST#	PCIe fundamental reset	A	SHB & Backplane
PCI(-X) (Not Available)	AD[0:31], FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, C/BE[0:3], SDONE, SBO#, PAR	Bussed on SHB slot and expansion slots	D	SHB & Backplane
	GNT[0:3], REQ[0:3], CLKA, CLKB, CLKC, CLKD, CLKFO, CLKFI	Point-to-point from SHB slot to each expansion slot	D	SHB & Backplane
	INTA#, INTB#, INTC#, INTD#	Bussed (rotating) on SHB slot and expansion slots	D	Backplane
	M66EN, PCIXCAP	Bussed on SHB slot and expansion slots	D	Backplane
	PCI_PRST#	PCI(-X) present on backplane detect	D	Backplane
	PME#	Optional PCI wake-up event bussed on SHB and backplane expansion slots	A	Backplane
Misc. I/O	USB[0:3]P, USB[0:3]N, USBOC[0:3]#	Optional point-to-point from SHB Connector C to a destination USB device	C	SHB & Backplane
SATA	ESATATX(4:5)P, ESATATX(4:5)N, ESATARX(4:5)P, ESATARX(4:5)N,	Optional point-to-point from SHB Connector C to a destination SATA device	C	SHB & Backplane
Ethernet	a_MDI(0:1)p, a_MDI(0:1)n	Optional point-to-point from SHB Connector C to a destination Ethernet device	C	SHB & Backplane

Optional PCI Express Link Expansion

An optional Trenton PEX10 module may be used with the BXT7059 SHB to provide additional PCIe links to a backplane equipped with a PEX10 expansion slot. The Trenton BPC7041 backplane feature this PEX10 option slot. A PEX10 routes the additional PCIe links available from the BXT7059's second processor down to a backplane for use in PCI Express link and/or bandwidth expansion. These additional links may operate as either PCIe 1.1, 2.0 or 3.0 links depending on the backplane and end-point configuration.

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Chapter 3 BXT7059 / BXTS7059 System Power Connections

Introduction

The combination of new power supply technologies and the system capabilities defined in the SHB Express® (PICMG® 1.3) specification requires a different approach to connecting system power to a PICMG 1.3 backplane and/or SHB hardware.

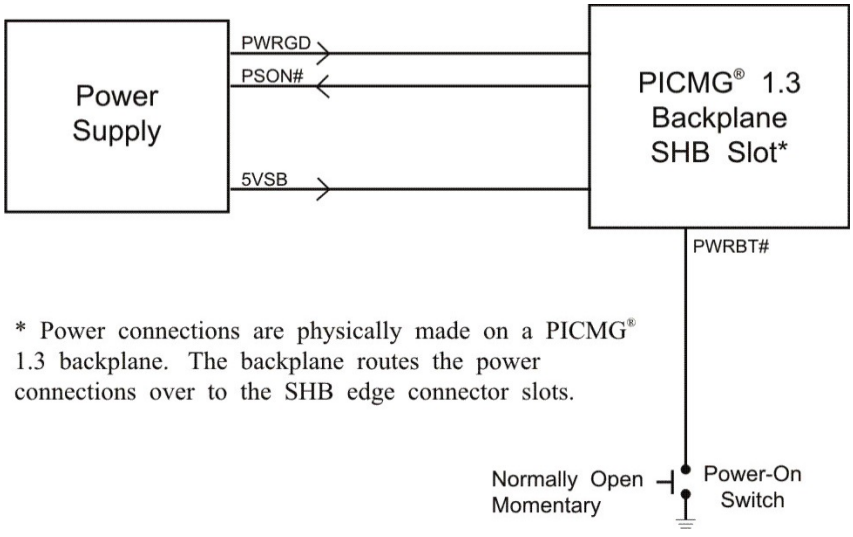
To improve system MTTR (Mean Time To Repair), the PICMG 1.3 specification defines enough power connections to the SHB's edge connectors to eliminate the need to connect auxiliary power to the SHB. All power connections in a PICMG 1.3 system can be made to the PICMG 1.3 backplane. This is true for SHBs that use high-performance processors. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive these high-performance SHBs. Trenton's PICMG 1.3 backplanes define ATX/EPS and +12V connectors that are compatible with ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in this manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

Power Supply and SHB Interaction

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.



Power Supply and SHB Interaction

PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

Electrical Connection Configurations

There are a number of different connector types, such as EPS, ATX or terminal blocks, which can be utilized in wiring power supply and control functions to a PICMG 1.3 backplane. However, there are only two basic electrical connection configurations: **ACPI Connection** and **Legacy Non-ACPI Connection.**

ACPI Connection

The diagram on the previous page shows how to connect an ACPI compliant power supply to an ACPI enabled PICMG 1.3 system. The following table shows the required connections that must be made for soft power control to work.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up.	Power Supply
PWRGD	Power Good. This signal indicates that the power supply's voltages are stable and within tolerance.	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply.	SHB/Backplane
PWRBT#	Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state. If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs.	Power Button

Legacy Non-ACPI Connection

For system integrators that either do not have or do not require an ACPI compliant power supply as described in the section above, an alternative electrical configuration is described in the table on the following page.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	Not Required	Power Supply
PWRGD	Not Required	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply. If an ATX or EPS power supply is used in this legacy configuration, a shunt must be installed on the backplane from PSON# to signal Ground. This forces the power supply DC outputs on whenever AC to the power supply is active.	Backplane
PWRBT#	Not Used	

In addition to these connections, there is usually a switch controlling AC power input to the power supply.

When using the legacy electrical configuration, the SHB BIOS **Power Supply Shutoff** setting should be set to **Manual shutdown**. Refer to the *General ACPI Configuration* section of the *Advanced Setup* chapter in this manual for details.

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Chapter 4 PCI Express Backplane Usage

Introduction

PCI Express® is a scalable, full-duplex serial interface which consists of multiple communication lanes grouped into links. PCI Express scalability is achieved by grouping these links into multiple configurations. A x1 ("by 1") PCI Express link is made up of one full-duplex link that consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. A x4 configuration is made up of four PCI Express links. The most commonly used PCIe link sizes are x1, x4, x8 and x16.

PCI Express devices with different PCI Express link configurations establish communication with each other using a process called auto-negotiation or link training. For example, a PCI Express device or option card that has a x16 PCI Express interface and is placed into a x16 mechanical/x8 electrical slot on a backplane establishes communication with a PICMG® 1.3 SHB using auto-negotiation. The option card's PCI Express interface will "train down" to establish communication with the SHB via the x8 PCI Express link between the SHB and the backplane option card slot.

SHB Edge Connectors

The PICMG 1.3 specification enables SHB vendors to provide multiple PCI Express configuration options for edge connectors A and B of a particular SHB. These edge connectors carry the PCI Express links and reference clocks down to the SHB slot on the PICMG 1.3 backplane. The potential PCI Express link configurations of an SHB fall into three main classifications: server-class, graphics-class and combo-class. The specific class and PCI Express link configuration of an SHB is determined by the chipset components used on the SHB.

In a server-class configuration, the main goal of the SHB is to route as many high-bandwidth PCI Express links as possible down to the backplane. Typically, these links are a combination of x4 and x8 PCI Express links.

A graphics-class configuration should provide a x16 PCI Express link down to the backplane in order to support high-end PCI Express graphics and video cards. Graphics-class SHB configurations also provide as many lower bandwidth (x1 or x4) links as possible.

A combo-class configuration is provided by SHBs like the BXT7059 or BXTS7059. These system host board types have PCI Express hardware and software implementations that are capable of combining links to support either server or graphics-class PICMG 1.3 backplane configurations.

The A0 through A3 PCI Express® links on the BXT7059 connect directly to the processors. These links can operate as either PCI Express 3.0, 2.0 or 1.1 links based on the end-point devices on the backplane that are connected to the SHB and the backplane's PCIe link design. In addition to automatically configuring themselves for either PCIe 3.0, 2.0 or PCIe 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple x4 links from the processors (links A0, A1, A2 and A3) can be combined into a single x16 PCIe electrical link or two x8 or four x4 links on a backplane. The CPU's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. The PCIe link (B0) from the board's PCH is a PCIe 2.0 interface and has a x4 default configuration that can automatically bifurcate into four, x1 PCIe links. An optional PEX10 module connected to a dual-processor BXT7059 expends the PICMG 1.3 base specification by providing four x4 links. These links may also operate as either PCI Express 3.0, 2.0 or PCI Express 1.1 links and can be combined into one x16, or two x8 or four x4 PCIe interfaces on a PEX10-supported backplane. This BXT7059 capability provides additional PCI Express bandwidth and option card support in the system design. Refer to the *PCI Express® Reference* chapter and to *Appendix C - PCI Express Backplane Usage* of the BXT7059 / BXTS7059 Hardware Manual for more information.

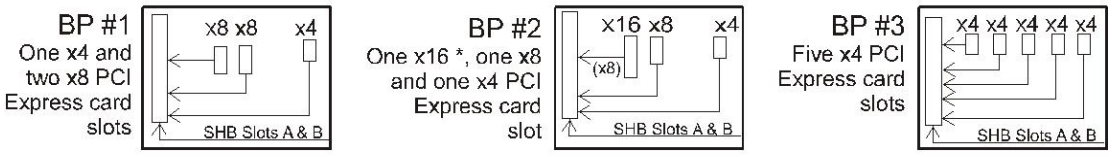
In addition to the standard PICMG 1.3 edge connector PCIe interfaces and the PEX10 expansion links, the BXT boards also have an additional x4 PCIe 3.0 link available for use on a backplane. This extra x4 link is routed to the SHB's controlled impedance connector for use with the Trenton IOB33 plug-in option card.

The IOB33 routes this x4 PCI Express link down to a physical x4 PCIe edge connector on the board. The IOB33 edge connector mates with a backplane's PCIe Expansion slot. This extra link is useful in supporting an additional system card slot. Refer to the *IOB Expansion Board - Appendix D* for more information the IOB33 and the *PCI Express Reference* chapter for more information on the PCI Express signal routings to the SHB edge connectors.

The figures below show some typical SHB and backplane combinations that would result in all of the PCI Express slots successfully establishing communication with the SHB host device. The first figure shows a server-class SHB; the second shows a graphics-class SHB.

Server-Class SHB:

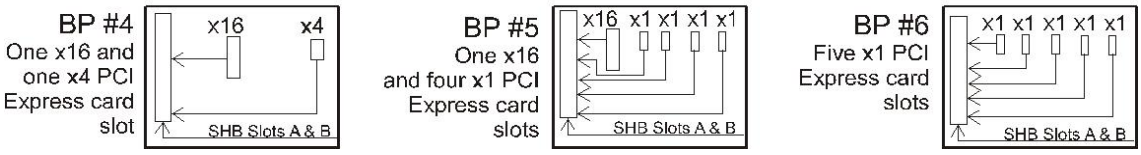
PCI Express™ Edge Connectors A & B: One x4 and two x8 PCI Express™ Links with five reference clocks



* x16 slot is x16 mech./x8 elec.

Graphics-Class SHB:

PCI Express™ Edge Connectors A & B: One x16 and one x4 PCI Express™ Link with five reference clocks



PCI Express link configuration straps for each PCI Express option card slot on a PICMG 1.3 backplane are required as part of the PICMG 1.3 SHB Express® specification. These configuration straps alert the SHB as to the specific link configuration expected on each PCI Express option card slot. PCI Express communication between the SHB and option card slots is successful only when there are enough available PCI Express links established between the PICMG 1.3 SHB and each PCI Express slot or device on the backplane.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express® System Host Board PCI Express Specification, PICMG® 1.3*.

Off-Board Video Card Usage

If the system design requires an off-board video card, then the card must be placed in a backplane slot driven with PCI Express links from the BXT7059's first processor. This is an Aptio® 4.x BIOS limitation that may be corrected in future software revisions. Listed below are the acceptable BPC7041 backplane slots for use with an off-board video card:

BPC7041 - Card slot PCIe6, PCIe7, PCIe8, PCIe9 or PCIe10

BXT7059 & BXTS7059 and Compatible Trenton Backplanes

The BXT7059 and BXTS7059 will function with a wide variety of industry standard PICMG 1.3 backplanes. However, some non-Trenton backplanes may not utilize the full capabilities of the Trenton BXT7059 and BXTS7059 boards. The table below illustrates the BXT/BXTS electrical compatibility with the current listing of Trenton PICMG 1.3 backplanes. A "Yes" in the compatible column below means that all slots on the backplane will function with a BXT7059 board. The clarification column explains any specific backplane limitations; such as mechanical option card slot interferences. Trenton continuously adds backplanes to our product line. Contact us or visit our website for the latest backplane availability.

PICMG 1.3 Backplane	**Compatible with BXT7059 / BXTS7059** (i.e. all backplane slots are functional)	**Why not or clarification**
2U Butterfly Backplanes		
BPC8219	Yes	
BPG6741	Yes, option card slot restrictions	PCIe4 slot accommodates single width cards only
BPX6736	Yes, option card slot restrictions	PCIe2 slot obstructed*, PCIe4 slot accommodates single width cards only
Multi-Segment Backplanes		
BP6FS6605	No	SHB segment spacing
BP4FS6890	Yes, option card slot restrictions	The first and second PCIe slots in each segment are obstructed* and the third slot in any segment accommodates single-width cards only
BP2S6929	Yes, option card slot restrictions	SLTA1 and SLTC1 slots are obstructed*, SLTA2 and SLTC2 accommodate single-width cards only
Combo Backplanes		
BPC7041	Yes for the BXT7059 with a PEX10	CPU2 needed to provide the links for BP slots PCIe 1 through PCIe4
BPC7009	No	Link compatibility issue
Server-Class Backplanes		
BPX8093#	Yes	Requires BXT7059 with PEX10 for PCIe1 and PCIe3 slot functionality
BPX6806#	Yes, option card slot restrictions	PCIe1 slot obstructed*, PCIe2 slot accommodates single-width cards only
BPX6620#	Yes, option card slot restrictions	PCIe1 slot obstructed*, PCIe2 slot accommodates single-width cards only
BPX6610	Yes, option card slot restrictions	PCIe1 slot obstructed*, PCIe2 slot accommodates single-width cards only
BPX6571	Yes, option card slot restrictions	PCIe1 slot obstructed*, PCIe2 slot accommodates single-width cards only
BPX3/14#	Yes, need IOB33 for PCIe2 slot	BXT7059 provides x4 via IOB33
BPX3/8	Yes, option card slot restrictions	SLTD1 card slot obstructed*, SLTD2 slot accommodates single-width cards only
BPX6719#	Yes, need IOB33 for PCIe1 slot	PCIe1 slot obstructed*, PCIe2 slot accommodates single width cards only
BPX3/2	Yes, option card slot restrictions	PCIe1 & PCIe2 slots obstructed*, SLTA1 slot accommodates single-width cards only
BPX5#	Yes, option card slot restrictions	PCIe1 slot obstructed*, PCIe2 slot accommodates single-width cards only
Graphics-Class Backplanes		
BPG8150	Yes	Requires BXT7059 with PEX10 for PCIe1 and PCIe2 slot functionality
BPG8032	Yes, option card slot restrictions	PCIe1 & PCIe2 slots obstructed*, PCIe3 slot accommodates single-width cards only
BPG7087#	Yes, need IOB33 for PCIe1 slot	BXT7059 provides x4 via IOB33
BPG6615	Yes, option card slot restrictions	PCIe2 slot accommodates single-width cards only
BPG6600	No	32b/33MHz slots C1, C2, C3 & C4 are inoperative when using a BXT7059 SHB
BPG6544	No	32b/33MHz slots C1, C2, & ISA slots D1 & D2 are inoperative when using a BXT7059 SHB
BPG6714#	Yes, option card slot restrictions	PCIe1 slot obstructed*
BPG2/2	Yes, option card slot restrictions	PCIe2 slot obstructed*, SLTA1 slot accommodates single-width cards only
BPG4#	Yes, option card slot restrictions	PCIe1 slot obstructed*, PCIe2 slot accommodates single-width cards only

*The slot obstruction on this backplane generally only applies to I/O cards longer than 4.3" (109.2mm). Contact Trenton for additional information.
#An optional IOB33 plug-in card is needed on the BXT/BXTS to provide a x4 PCIe link for the PCIe1 or PCIe2 option card slot on these select backplanes.

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Chapter 5 I/O Expansion Boards – IOB33 & PEX10

IOB33 Overview

The IOB33 is optional I/O expansion board designed for use with the BXT7059 and BXTS7059 SHBs. Additional board versions are available for use with other Trenton SHBs. The IOB33 provides legacy I/O support and features a x4 PCIe edge connector along the bottom edge of the card. This x4 card edge connector routes a x4 PCIe Gen 3.0 electrical link from the boards CPU0 down to the PCIe expansion slot on a PICMG 1.3 backplane. This extra link is useful in supporting an additional system card slot.

The optional IOB33 also expands the I/O capabilities of the system. The IOB33 has the following interfaces available for use by the system designer:

- Two - RS232 communication ports
- One - Floppy drive interface
- One - Parallel printer interface
- One – PS/2 Mini-DIN connector for PS/2 keyboard and mouse connections
  - Also includes separate, on-board PS/2 keyboard and mouse headers for systems that require separate PS/2 connections

There are three versions of the Trenton IOB33 I/O expansion board. This optional board is designed for the BXT7059 and BXTS7059 SHBs, but the additional versions may be used on other Trenton SHBs. The chart below identifies the IOB33 version that is compatible with specific Trenton SHBs.

IOB Module	T4L (6483)	TML (6490)	TQ9 (6731)	MCG-Series (6680, 6690, 6675, 6695)	NLI / NLT (6313, 6396)	SLT / SLI (6515, 6521)	MCX-Series (6633, 6685, 6638, 6700)	BXT / BXTS JXT / JXTS (7059, 6966)
IOB33JX (7015-004)								X
IOB33MC (7015-002)			X	X			X	
IOB33 (7015-000)	X	X			X	X		

IOB33 Models

Model #	Model Name	Description
7015-004	IOB33JX	Includes the I/O Plate for use with the BXT7059 / BXTS7059 or JXT6966 / JXTS6966 system host boards
7015-002	IOB33MC	Includes the I/O Plate for use with MCX, MCG and TQ9 system host boards
7015-000	IOB330	Includes the I/O Plate for use with TML, SLT, SLI, NLT, NLI and T4L system host boards

IOB33 Features

IOB33 (7015-004, 7015-002, 7015-001)

- I/O plate versions for a variety of Trenton system host boards
- Two serial ports and PS/2 mouse/keyboard mini DIN on the I/O bracket
- PS/2 mouse, keyboard, parallel port and floppy drive connectors
- PCI Express expansion capability for use with PCI Express backplanes
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG®) PCI Express Specification

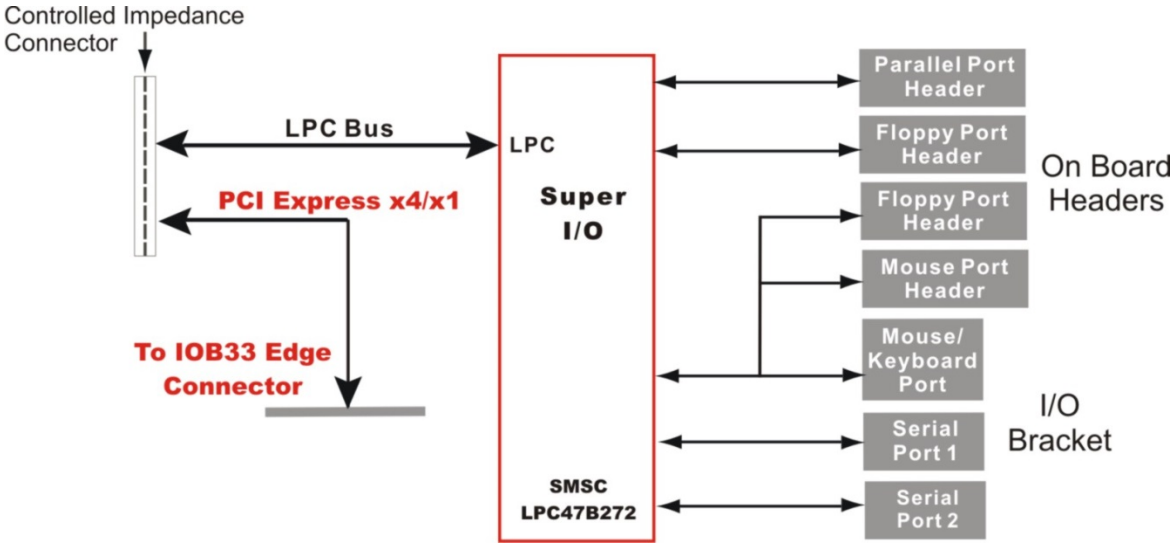
IOB33 Temperature/Environment

Operating Temperature: 0º C. to 60º C.

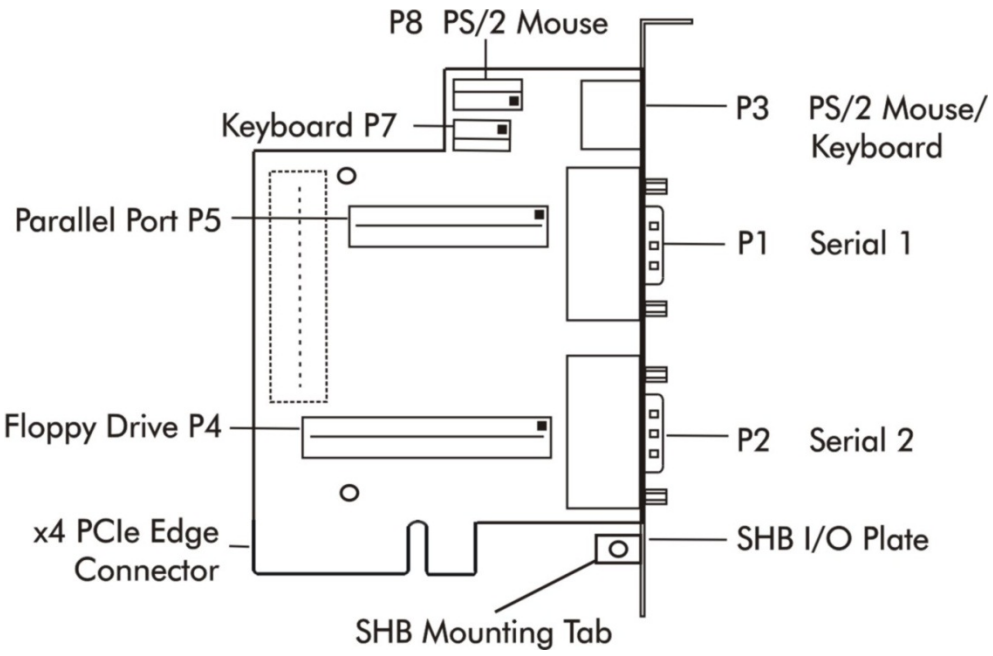
Storage Temperature: -20º C. to 70º C.

Humidity: 5% to 90% non-condensing

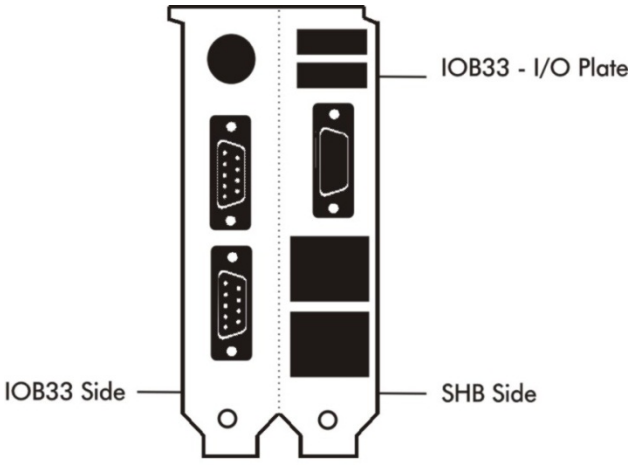
IOB33 (7015-xxx) Block Diagram



IOB33 (7015-xxx) Layout Diagram



IOB33 (7015-xxx) I/O Plate Diagram



IOB33 Connectors

NOTE: the square pad on the PCB indicates Pin 1 on the connectors.

P1 - Serial Port Connector

9 position "D" right angle, Spectrum #56-402-001

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-O	8	Clear to Send-
4	Data Terminal Ready-O	9	Ring Indicator-I
5	Signal Gnd		

P2 - Serial Port Connector

9 position "D" right angle, Spectrum #56-402-001

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-O	8	Clear to Send-
4	Data Terminal Ready-O	9	Ring Indicator-I
5	Signal Gnd		

P3 - PS/2 Mouse and Keyboard Connector

6 pin mini DIN, Kycon #KMDG-6S-B4T

Pin	Signal
1	Ms Data
2	Kbd Data
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P4 - Floppy Drive Connector

34 pin dual row header, Amp #103308-7

Pin	Signal	Pin	Signal
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Change

IOB33 Connectors (continued)

P5 - Parallel Port Connector
26 pin dual row header, Amp #103308-6

Pin	Signal	Pin	Signal
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

P7 - Keyboard Header
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self resetting fuse

P8 - PS/2 Mouse Header
6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	Reserved
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

IOB33 Connectors (continued)

P6 - Impedance Connector
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12	2	+5V_STANDBY
3	NC	4	+5V_STANDBY
5	NC	6	+5V_DUAL
7	NC	8	+5V_DUAL
9	NC	10	NC
11	NC	12	NC
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SBMCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP4	48	C_PE_RXP4
49	C_PE_TXN4	50	C_PE_RXN4
51	Gnd	52	Gnd
53	C_PE_TXP3	54	C_PE_RXP3
55	C_PE_TXN3	56	C_PE_RXN3
57	Gnd	58	Gnd
59	C_PE_TXP2	60	C_PE_RXP2
61	C_PE_TXN2	62	C_PE_RXN2
63	Gnd	64	Gnd
65	C_PE_TXP1	66	C_PE_RXP1
67	C_PE_TXN1	68	C_PE_RXN1
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5v

PEX10 Overview

The PEX10 is an optional PCI Express link expansion board that takes advantage of the additional PCI Express 3.0 interfaces available in the Intel® Xeon® E5-2400-series (i.e. Sandy Bridge-EN) processors.

Direct PCI Express 3.0 interfaces from the Sandy Bridge-EN processors are a compelling feature of Trenton's BXT7059 and BXTS7059 system host boards. The BXT7059 is a dual-processor SHB with more available PCIe links than the 20 PCIe links currently defined in the PICMG® 1.3 SHB Express® industry specification. Many system designs can utilize the additional x16 PCIe link offered by the second processor on a Trenton BXT7059 SHB to increase a system's data bandwidth and information throughput. The PEX10 is an optional PCI Express expansion board that makes these additional links available to the system designer. These addition links may operate as a single x16 or 4 – x4 links on a backplane equipped to handle this additional interface.

The PEX10 is a passive board that mounts to the back of a Trenton BXT7059. This PEX10 passive interface card routes the four additional PCIe 3.0 x4 electrical links from second processor on a BXT7059 down to a mechanical x16 PCIe link expansion slot on the backplane.

The Trenton BPC7009 and BPC7041 backplanes support the PEX10 plug-in card via an additional x16 PCI Express link expansion slot. The design architecture of these two backplanes will likely result in PCIe 2.0 data rate operation for any I/O cards connected to this PCIe 3.0 expansion link.

NOTE: Currently, the PEX10 is compatible with the Trenton BXT7059 when the SHB is used with the BPC7041 backplane. Trenton's JXT6966 SHB is compatible with either the BPC7009 or BPC7041 backplanes. Trenton is constantly expanding its PCI Express backplane product offerings. See the Trenton website or contact us for latest backplane availability information.

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Appendix A BIOS Messages

Introduction
A status code is a data value used to indicate progress during the boot phase. These codes are outputted to I/O port 80h on the SHB. Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

Aptio Boot Flow
While performing the functions of the traditional BIOS, Aptio 4.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

[1] Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality in legacy BIOS

BIOS Beep Codes
The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

BIOS Status Codes

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the BXT7059 and BXTS7059 SHBs. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

The HEX to LED chart in the POST Code LEDs section will serve as a guide to interpreting specific BIOS status codes.

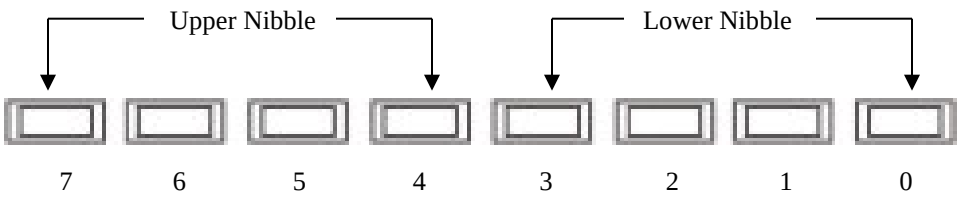
BIOS Status POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the BXT7059 and BXTS7059 SHBs. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



BXT7059 & BXTS7059 POST Code LEDs

Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

There are no SEC Beep codes associated with this phase of the Aptio BIOS boot process.

PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization

0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes