Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your HEP8225 (8225-xxx) SHB. System performance may be affected by incorrect usage of these features.

DDR4 MEMORY

There are four active DDR4 standard DIMM sockets on the board for each processor. Each standard DIMM socket can support a 32GB DIMM for a total possible DDR4 system memory capacity of 256GB. When 64GB DDR4 DIMMs become readily available, the maximum supported SHB memory capacity will increase to 512GB.

In most applications, 8GB or 16 GB DIMM sizes are sufficient providing a maximum memory capacity of 64GB and 128GB respectively. The required DIMM size will depend on the needs of the application. For many workloads, 8GB or 16GB DIMMs should be fine. For applications or benchmarks that benefit from memory capacity more than memory performance, such as TPC-C and TPC-E, there are two options. Option 1 is likely best for TPC-C since it allows a greater memory capacity.

Option 1) Use the largest DIMMs available, currently expected to be 32GB or 64GB quad rank DDR4 LRDIMMs.

Option 2) Use the largest dual rank registered DIMMs available these currently include 16GB or 32GB dual rank DIMMs.

The processor's four individual direct-connect memory channel interfaces terminate with a single in-line standard DIMM memory module socket BK0 through BK7. The System BIOS automatically detects memory type, size and speed.

Trenton recommends ECC registered DDR4-2400 standard DIMM memory modules for use on the HEP8225, and these ECC registered (72-bit) DDR4 standard DIMMs must be PC4-19200 compliant.

The SHB uses industry standard gold finger standard DIMM memory modules, which must be PC4-19200 compliant and have the following features: 288-pin, gold-plated contacts and ECC registered (72-bit) DDR4-2133 memory.

Populate all even numbers of channels per processor socket. Sub-optimal memory channel utilization may occur if only1 or 3 memory channels per processor are populated.

*Requires a continuous airflow across the board of 350LFM.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR4-2400 DIMMs on the HEP8225 dual-processor board.
- All memory modules must have gold contacts.
- Low-voltage (DDR4L) DIMMs are supported, but are costly and supply may be limited. Contact Trenton for more details.

Populate the memory sockets starting with the DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:

DIMM Population Order	CPU0	CPU1
1	BK1	BK5
2	BK3	BK7
3	BK0	BK4
4	BK2	BK6

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

PROCESSOR OPTIONS

Max. DDR4 Speed	Processor	Base Clock Speed	Cores / Threads	Cache	Long-Life Availability (5 to 7 years)	Maximum Thermal Design Power (TDP)	Operating Temperature Range*
DDR4-2400	Intel® Xeon® E5-2680 v4	2.4GHz	14 / 28	35MB	Yes	120W	0°C to 45°C
DDR4-2133	Intel® Xeon® E5-2680 v3	2.5GHz	12 / 24	30MB	Yes	120W	0°C to 45°C
DDR4-2400	Intel® Xeon® E5-2658 v4	2.3GHz	14 / 28	35MB	Yes	105W	0°C to 50°C
DDR4-2133	Intel® Xeon® E5-2658 v3	2.2GHz	12 / 24	30MB	Yes	105W	0°C to 50°C
DDR4-2400	Intel® Xeon® E5-2648L v4	1.8GHz	14 / 28	35MB	Yes	75W	0°C to 50°C
DDR4-1866	Intel® Xeon® E5-2648L v3	1.8GHz	12 / 24	30MB	Yes	75W	0°C to 50°C
DDR4-2133	Intel® Xeon® E5-2628L v4	1.9GHz	12 / 24	30MB	Yes	75W	0°C to 50°C
DDR4-1866	Intel® Xeon® E5-2628L v3	2.0GHz	10 / 20	25MB	Yes	75W	0°C to 50°C
DDR4-2133	Intel® Xeon® E5-2618L v4	2.2GHz	10 / 20	25MB	Yes	75W	0°C to 50°C
DDR4-1866	Intel® Xeon® E5-2618L v3	2.3GHz	8 / 16	20MB	Yes	75W	0°C to 50°C
DDR4-1600	Intel® Xeon® E5-2608L v3	2.0GHz	6 / 12	15MB	Yes	50W	0°C to 50°C

SAS / SATA RAID Operation

The SHB's Intel® C612 Platform Controller Hub (PCH) features Intel® Rapid Storage Technology, which enables SHB support for RAID 0, 1 and 10 implementations. To configure the SAS / SATA ports as RAID drives, you must install the Intel® RST enterprise driver software. This link takes you to version 3.2 that was tested and validated on the SHB. A later version 3.5 is also available for download, but this version has not been tested on the board. Links to both driver versions are located on Trenton's website by accessing the Downloads tab of the HEP8225 product detail web pages or the RAID Drivers section of the Technical Support page.

A Word About RAID

The Intel® C612 Platform Controller Hub supports eight SATA/600 channels on two separate controllers notated as SATA and sSATA. The Trenton HEP8225 SHB supports these channels with two ports on the SHB itself and up to six passed down to a backplane (dependent on configuration, refer to the Trenton Systems HDEC® Backplane Technical Reference for more information). The Intel® C612 Platform Controller Hub RAID arrays are limited to four drives total and arrays cannot span controllers. This results in a capability of up to two (2) RAID arrays of up to four (4) drives total.

The ports on the SHB are controlled by the SATA controller, designated P10 and P11.

A Word About PCI Express 3.0 Interfaces

PCIe 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen 3, Gen 2 and Gen 1.1 I/O cards on the same interface link. Running a PCIe 3.0 target device such as a Gen 3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the HEP8225) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specific of your particular PCIe 3.0 implementation.

High Density Embedded Computing Backplane I/O

The HEP8225 enables the following backplane I/O connectivity via the HDEC dual-density edge connector:

- 80 lanes of PCIe 3.0
- Six SATA 3.0/600 Interfaces
- 2- 10Gigabit Ethernet, 2- Gigabit Ethernet
- Six USB Interfaces, 4- USB 2.0 2- USB 3.0, 2- PS/2
- 1- RS232
- Status I/O, 2- SMBus, 1- IPMB, 8- GPIO, Intruder Alert, CMOS Clear input, 4- SHB Present Detect Pins
- Power and Reset Switches and LEDs, Power Supply ON LED, 10- Additional LED output, 1- Power Good LED, HDD LED out
- System Speaker and Audio In/Out
- 8- Fan PWM and Tach interfaces

HDEC-series Backplane Classification

Virtually all of Trenton's HDEC® series backplane solutions can be utilized with the HEP8225. These include, but are not limited to: HDB8236, HDB8237, HDB8228, HDB8227 and HDB8229. Each of these backplane designs have different form factors and target operators. Contact Trenton for more information on each backplane and which would perform optimally for your application, or, a custom solution tailored exactly to your needs.

BIOS

The HEP8225 feature the Aptio® 5.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *HEP8225 BIOS Technical Reference* manual.

Operating Systems

Trenton's HEP8225 has been tested using a number of popular and readily available operating systems including: Microsoft Windows Server 2008 R2, Windows Server 2012 x64, Windows 7.1 x64, Windows 8.1 x64 and a number of variations of Linux including Red Hat Enterprise Linux 7.1 x64, CentOS 7.x x64 and OpenSUSE 13.1 x64. This testing process confirms the SHB's PCI Express interface and device I/O functionality. Trenton does not recommend using the Microsoft Windows XP32 SP2 or SP3 operating system due to limited functionality concerns. Contact Trenton Tech Support for additional information.

Power Connection

The HEP8225 supports soft power signals along the Advanced Configuration and Power Interface (ACPI). They are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to the *Power Connection* section in the BXT manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

For More Information

For more information on any of these features, refer to the appropriate sections *HEP8225 Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the HEP8225 web page.