Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your JXT6966 or JXTS6966 (6966-xxx) SHB. Overall system performance may be affected by incorrect usage of these features.

MOUSE/KEYBOARD "Y" CABLE

If you have an IOB33 I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation.

DDR3-1333 MEMORY

Trenton recommends ECC registered DDR3 memory modules for use on the JXT6966/JXTS6966 SHBs and these ECC registered (72-bit) DDR3 Mini-DIMMs must be PC3-10600 or PC3-8500 compliant. Unbuffered ECC DDR3 Mini-DIMMs are also supported on the JXT boards, but you cannot mix the two different memory types on the same SHB.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR3 Mini-DIMMs with the same interface speed.
- All memory modules must have gold contacts.
- Low voltage (DDR3L) Mini-DIMMs are not supported.
- The SHB supports the following memory module memory latency timings:
  - 6-6-6 for 800MHz DDR3 Mini-DIMMs
  - 7-7-7 and 8-8-8 for 1066MHz DDR3 Mini-DIMMs
  - 9-9-9 for 1333MHz DDR3 Mini-DIMMs
- Populating the memory sockets with Mini-DIMMs having different speeds is supported on the SHB; however, the overall memory interface speed will run at the speed of the slowest Mini-DIMM.
- Populate the memory sockets starting with the Mini-DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:

Population order	CPU1	CPU2*
1	BK00	BK10
2	BK01	BK11
3	BK02	BK12

*CPU2 is available on the JXT6966 dual-processor board version only

*Using a balanced memory population approach ensures maximum memory interface performance. A "balance approach" means using an equal number of Mini-DMMs for each processor on a dual-processor JXT6966 SHB whenever possible.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board. The JXTS6966 SHB versions feature one processor; however, memory slots BK10, BK11 and BK12 are installed on the SHB but are not active in this single-processor board version.

SATA RAID OPERATION

The Intel® 3420 Platform Controller Hub (PCH) used on the SHB features Intel® Rapid Storage Technology (Intel® RST), which allows the PCH's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. To configure the SATA ports as RAID drives or to use advanced features of the PCH, you must install the Intel® RST driver software. A link to the software is also located on Trenton's website by accessing the Downloads tab of the JXT6966 product detail page or the RAID Drivers section of the Technical Support page.

POWER CONNECTION

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The JXT6966/JXTS6966 supports these signals, controlled by the ACPI and are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to - *Power Connection* section in the JXT manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

PCI EXPRESS 2.0 LINKS AND PICMG® 1.3 BACKPLANES

The A0 through A3 PCI Express® links on the JXT6966 connect directly to the processors. These links can operate as either PCI Express 2.0 or PCI Express 1.1 links based on the end-point devices on the backplane that are connected to the SHB. In addition to automatically configuring themselves for either PCIe 2.0 or PCIe 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple x4 links from the processors (links A0, A1, A2 and A3) can be combined into a single x16 PCIe electrical link or multiple x8 links on a backplane. The CPU's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. The PCIe link (B0) from the board's PCH is a PCIe 1.1 interface only and has a x4 default configuration and can be made to bifurcate into four, x1 PCIe links with a factory modification to the JXT board. Contact Trenton if you require this B0 link configuration change. An optional PEX10 module connected to a dual-processor JXT6966 provides more backplane links than are currently supported in the PICMG 1.3 specification. This JXT6966 capability provides additional PCI Express bandwidth and option card support in the system design. Refer to the *PCI Express® Reference* and *PCI Express Backplane Usage* chapters of the *JXT6966 / JXTS6966 Hardware Technical Reference* manual for more information.

PICMG 1.3 BACKPLANE I/O

The JXT6966 and JXTS6966 enable the following PICMG 1.3 backplane I/O connectivity via the SBC's edge connector C:

- Four USB 2.0 interfaces
- One 10/100Base-T Ethernet interface

PICMG 1.3 BACKPLANE CLASSIFICATION

The JXT6966 and JXTS6966 are system host boards that can operate as either a Server or Graphics-Class PICMG 1.3 SHB. The JXT SHBs are essentially combo-class boards because of the capabilities of the PCI Express links built into the SHB's processors. Trenton recommends using a combo-class PICMG 1.3 backplane such as the Trenton BPC7009 or BPC7041 with the SHBs in order to ensure the use of all available backplane option card slots. See *Appendix C, PCI Express Backplane Usage* for more details.

OFF-BOARD VIDEO CARD USAGE

If the system design requires an off-board video card, then the card must be placed in a backplane slot driven with PCI Express links from the JXT6966's first processor. This is an Aptio® 4.x BIOS limitation that may be corrected in future software revisions. Listed below are the acceptable BPC7009 and BPC7041 backplane slots for use with an off-board video card:

BPC7009 - Card slot PCIe1, PCIe2 or PCIe3
BPC7041 - Card slot PCIe6, PCIe7, PCIe8, PCIe9 or PCIe10

BIOS

The JXT6966 and JXTS6966 feature the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *JXT6966 / JXTS6966 BIOS Technical Reference* manual.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections *JXT6966 / JXTS6966 Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the JXT6966 or JXTS6966 web pages.