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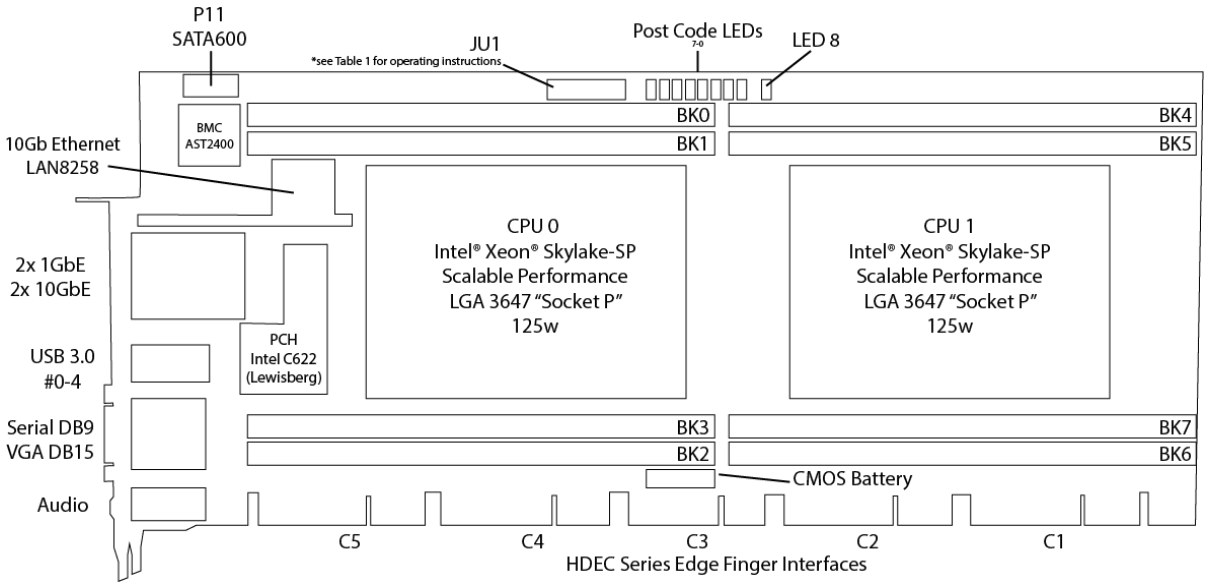
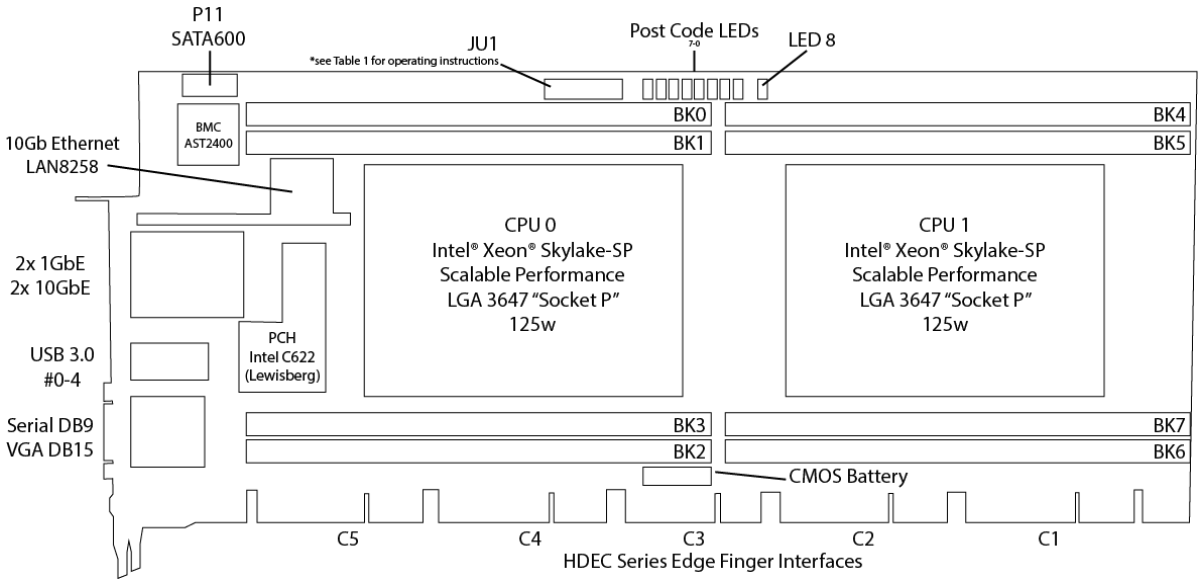
Technical Information – Support Details for the SEP8253 Dual-Processor, HDEC Series System Host Board

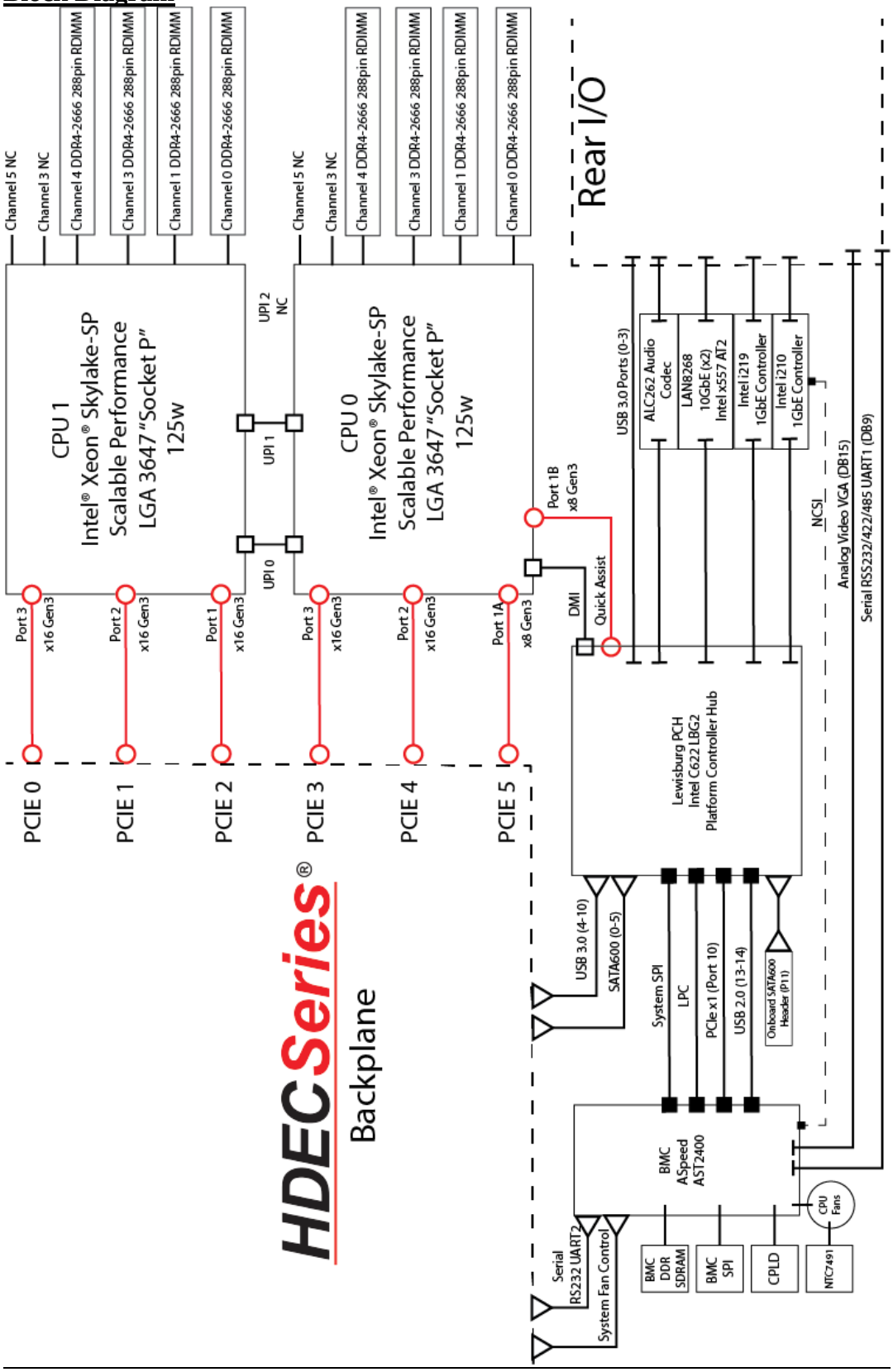
Layout Diagram – Audio Ports Populated



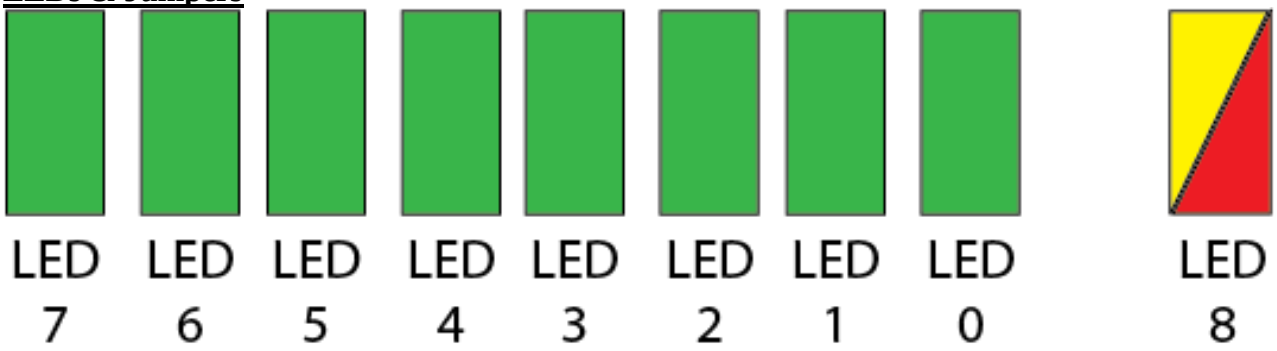
Layout Diagram – Audio Ports Not Populated



Block Diagram



LEDs & Jumpers



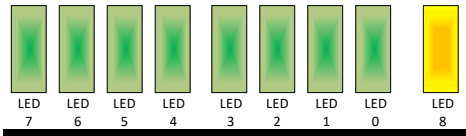
POST Code LEDs 0 - 7

As the POST (Power On Self-Test) routines are performed during boot-up, test codes are displayed on Port 80 POST Code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7). Refer to the board layout diagram for the exact location of the POST code LEDs.

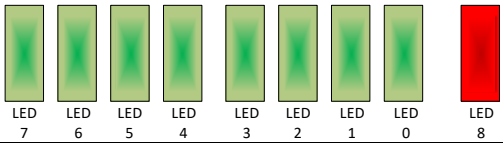
These POST codes may be helpful as a diagnostic tool. Specific test codes are listed in Appendix A - BIOS Messages section of this document. After a normal POST sequence, the LEDs are off (00h) indicating that the SHB's BIOS has passed control over to the operating system loader typically at interrupt INT19h. The chart is from Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



	LED	Before System Power OK	After System Power OK
LED 8 AMBER	**LED 7**	CPU 1 VCCORE/VSA PwrOK	CPU ERROR[1:0]
	LED 6	CPU 1 VCCIO PwrOK	CPU1 PROCHOT
	LED 5	CPU1 DDR PwrOK	CPU0 PROCHOT
	LED 4	CPU 0 VCCORE/VSA PwrOK	DDR_DIMM_EVENT
	LED 3	CPU 0 VCCIO PwrOK	CPU0 DDR345_MEMHOT
	LED 2	CPU0 DDR PwrOK	CPU1 DDR012_MEMHOT
	LED 1	PCH VR PwrOK	CPU0 DDR345_MEMHOT
	LED 0	BMC VR PwrOK	CPU0 DDR012_MEMHOT



LED 8 RED Flashing	**LED 7**	CPU_CATERR
	LED 6	CPU_ERROR2
	LED 5	CPU1 THERMTRIP
	LED 4	CPU1 FIVRFTL
	LED 3	CPU0 THERMTRIP
	LED 2	CPU0 FIVRFTL
	LED 1	*not used*
	LED 0	VR13 FLT

Jumpers

NOTE: Jumper JU1 is a dual-row, 14-pin jumper. Each position controls the operation of a specific SHB implementation.

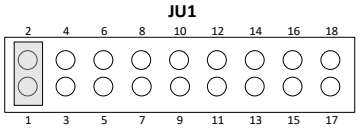


Table 1		
JU1 Pins	Description	Comment
1 – 2	Normal Operation	Shunted for normal operation
3 – 4	Clear CMOS	See Clear CMOS section
5 – 6	ME Recovery	Install jumper for one power-up cycle to force a ME update
7 – 8	Clear Password	Install jumper for one power-up cycle to reset the password
9 – 10	BIOS Recovery	Install jumper to force a Top Swap BIOS recovery
11 – 12	SPI Security Override	Install jumper for one power-up cycle to disable SPI security
13 – 14	Reserved	Factory use only
15 – 16	Reserved	Factory use only
17 – 18	BMC Disable	Disabled CPU execution of firmware

P6

1Gb Ethernet LEDs

The I/O bracket houses the two RJ-45 network connectors for Ethernet LAN3 and LAN4. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

LED/Connector Description

Activity LED	Yellow LED indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).
Off	No current network transmit or receive activity
On (solid)	Indicates a valid link established, but no network activity.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Green/Orange bi-color LED identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).
Off	Indicates a valid link at 10-Mb/s.
On (orange)	Indicates a valid link at 100-Mb/s.
On (green)	Indicates a valid link at 1000-Mb/s or 1-Gb/s.

P7

10Gb Ethernet LEDs

The I/O bracket also contains to two upper RJ-45 network connectors for the 10Gb Ethernet connections LAN1 and LAN2.

Note: Some SHB configurations may not provide these two 10GbE LAN connections.

LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

LED/Connector Description

Activity LED	Yellow LED indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).
Off	No current network transmit or receive activity
On (solid)	Indicates a valid link established, but no network activity.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Green/Orange bi-color LED identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).
Off	Indicates a valid link at 100-Mb/s.
On (orange)	Indicates a valid link at 1000-Mb/s or 1-Gb/s.
On (green)	Indicates a valid link at 10000-Mb/s of 10-Gb/s.

Connectors

NOTE:
A connectors' square solder pad located on the bottom side of the PCB indicates pin 1.

P6 – Dual 10/100/1000Base-T Ethernet Connector – LAN3 and LAN4

RJ-45/Dual connector, Pulse #JG0-101NL
Each individual RJ-45 connector is defined as:

PIN	SIGNAL	PIN	SIGNAL
1A	L3_MDI0n	1B	L4_MDI0n
2A	L3_MDI0p	2B	L4_MDI0p
3A	L3_MDI1n	3B	L4_MDI1n
4A	L3_MDI1p	4B	L4_MDI1p
5A	L3_MDI2n	5B	L4_MDI2n
6A	L3_MDI2p	6B	L4_MDI2p
7A	L3_MDI3n	7B	L4_MDI3n
8A	L3_MDI3p	8B	L4_MDI3p
9A	VCC_1.8V	9B	VCC_1.8V
10A	GND_A	10B	GND_b

P1A – Right Angle Stacked Connector - Video

DB15 HD video, Kycon # K42X-E9P/E15S-A4N

PIN	SIGNAL	PIN	SIGNAL
1	Red	9	+5V
2	Green	10	Gnd
3	Blue	11	NC
4	NC	12	EEDI
5	Gnd	13	HSYNC
6	Gnd	14	VSYNC
7	Gnd	15	EECS
8	Gnd		

P1B – Right Angle Stacked Connector - Serial

DB9 serial, Kycon # K42X-E9P/E15S-A4N

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	6	Clear To Send
2	Data Set Ready	7	Data Terminal Ready
3	Receive Data	8	Ring Indicator
4	Request To send	9	Signal Gnd
5	Transmit Data		

DB15 video connector is to the left and has female sockets
DB9 serial connector is to the right and has male pins

P9 – Quad USB 3.0 Stacked Connector, Type A

Four USB connectors, Foxconn #UEA1112C-QHD6-4F

PIN	P9A USB0 SIGNAL	PIN	P9B USB1 SIGNAL
A1	+5V-USB0	B1	+5V-USB1
A2	USB P0-	B2	USB P1-
A3	USB P0+	B3	USB P1+
A4	Gnd-USB0	B4	Gnd-USB1
A5	USB RXN0	B5	USB RXN1
A6	USB RXP0	B6	USB RXP1
A7	Gnd-USB0	B7	Gnd-USB1
A8	USB TXN0	B8	USB TXN1
A9	USB TXP0	B9	USB TXP1

PIN	P9C USB2 SIGNAL	PIN	P9D USB3 SIGNAL
C1	+5V-USB2	D1	+5V-USB3
C2	USB P2-	D2	USB P3-
C3	USB P2+	D3	USBP3+
C4	Gnd-USB2	D4	Gnd-USB3
C5	USB RXN2	D5	USB RXN3
C6	USB RXP2	D6	USB RXP3
C7	Gnd-USB2	D7	Gnd-USB3
C8	USB TXN2	D8	USB TXN3
C9	USB TXP2	D9	USB TXP3

Note:
1 – P9A is USB0 and located on the left side of the I/O plate directly above the VGA video port. P9B is USB1, P9C is USB2 and P9D is USB3 located on the right side of the I/O bracket farthest from the board and above the serial port.

P10, P11 – SATA III 600 / SATA II 300 Ports

7 pin vertical connector with latch, Molex #67800-8005

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	5	RX-
2	TX+	6	RX+
3	TX-	7	Gnd
4	Gnd		

Notes:
1 – P10 = SATA0 interface, P11 = SATA1 interface

Connectors (continued)

P5 and P12 – CPU Fan Power Connectors

4 pin single row header, Molex # 47053-1000

PIN	SIGNAL
1	Gnd
2	+12V
3	Fan Tach
4	PWM Control Signal

Note:
1 – P5 is the fan connector for CPU0 and P11 is for CPU1

P8 - Audio Port*

3 position audio, Foxconn #JA13331-N20B-4F

SOCKET COLOR	SIGNAL
Light Blue	Line In
Lime	Line Out
Pink	Mic

*Audio port P8 is not populated for board versions that are integrated into 2U rackmount computer chassis

P7 – Dual 10GbBase-T Ethernet Connector – LAN1 and LAN2 - (Optional)

RJ-45/Dual 10GbE connector, MagJack #JG0-101NL
Each individual RJ-45 connector is defined as follows:

Upper/Right PIN	SIGNAL	Lower/Left PIN	SIGNAL
1	L1_MDI_DP0	1	L2_MDI_DP0
2	L1_MDI_DN0	2	L2_MDI_DN0
3	2.5V_X540	3	2.5V_X540
4	L1_MDI_DP1	4	L2_MDI_DP1
5	L1_MDI_DN1	5	L2_MDI_DN1
6	2.5V_X540	6	2.5V_X540
7	L1_MDI_DP2	7	L2_MDI_DP2
8	L1_MDI_DN2	8	L2_MDI_DN2
9	2.5V_X540	9	2.5V_X540
10	L1_MDI_DP3	10	L2_MDI_DP3
11	L1_MDI_DN3	11	L2_MDI_DN3
12	2.5V_X540	12	2.5V_X540
13	L1_MDI_DP4	13	L2_MDI_DP4
14	L1_MDI_DP4	14	L2_MDI_DP4

Note1: The 10GbE LAN ports are the upper two connectors on the board's I/O bracket.
Note2: Some configurations of the HEP8225 system host board may not include the P7, dual LAN 10GbE connector.

Appendix A: Status Codes

Status Code Range	Description
0x01 - 0x0B	SEC execution
0x0C - 0x0F	SEC errors
0x10 - 0x2F	PEI execution up to and including memory detection
0x30 - 0x4F	PEI execution after memory detection
0x50 - 0x5F	PEI errors
0x60 - 0x8F	DXE execution up to BDS
0x90 - 0xCF	BDS execution
0xD0 - 0xDF	DXE errors
0xE0 - 0xE8	S3 Resume (PEI)
0xE9 - 0xEF	S3 Resume Errors (PEI)
0xF0 - 0xF8	Recovery (PEI)
0xF9 - 0XFF	Recovery Errors (PEI)

Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not Used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading.
0x03	North Bridge initialization before microcode loading.
0x04	South Bridge initialization before microcode loading.
0x05	OEM initialization before microcode loading.
0x06	Microcode loading.
0x07	AP initialization after microcode loading.
0x08	North Bridge initialization after microcode loading.
0x09	South Bridge initialization after microcode loading.
0x0A	OEM initialization after microcode loading.
0x0B	Cache initialization.
SEC Error Codes	
0x0C - 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found.
0x0F	Microcode not loaded.

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started.
0x11	Pre-memory CPU initialization is started.
0x12	Pre-memory CPU initialization (CPU module specific).
0x13	Pre-memory CPU initialization (CPU module specific).
0x14	Pre-memory CPU initialization (CPU module specific).
0x15	Pre-memory North Bridge initialization is started.
0x16	Pre-memory North Bridge initialization (North Bridge module specific.)
0x17	Pre-memory North Bridge initialization (North Bridge module specific.)
0x18	Pre-memory North Bridge initialization (North Bridge module specific.)
0x19	Pre-memory South Bridge initialization is started.
0x1A	Pre-memory South Bridge initialization (South Bridge module specific.)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific.)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific.)
0x1D - 0x2A	OEM pre-memory initialization codes.
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading.
0x2C	Memory initialization. Memory presence detection.
0x2D	Memory initialization. Programming memory timing information.
0x2E	Memory initialization. Configuring memory.
0x2F	Memory initialization. (other)
0x30	Reserved for ASL (see ASL status Codes section below)
0x31	Memory installed.
0x32	CPU post-memory initialization is started.
0x33	CPU post-memory initialization. Cache initialization.
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization.
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection.
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization.
0x37	Post-Memory North Bridge initialization is started.
0x38	Post-Memory North Bridge initialization (North Bridge Module Specific).
0x39	Post-Memory North Bridge initialization (North Bridge Module Specific).
0x3A	Post-Memory North Bridge initialization (North Bridge Module Specific).
0x3B	Post-Memory South Bridge initialization is started.
0x3C	Post-Memory South Bridge initialization (South Bridge Module Specific).
0x3D	Post-Memory South Bridge initialization (South Bridge Module Specific).
0x3E	Post-Memory South Bridge initialization (South Bridge Module Specific).
0x3F - 0x4E	OEM post memory initialization codes.
0x4F	DXE IPL is started.

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed.
0x51	Memory initialization error. SPD reading has failed.
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected.
0x54	Unspecified memory initialization error.
0x55	Memory not installed.
0x56	Invalid CPU type or speed.
0x57	CPU mismatch.
0x58	CPU self-test failed or possible CPU cache error.
0x59	CPU micro-code is not found or micro-code update is failed.
0x5A	Internal CPU error.
0x5B	Reset PPI is not available
0x5C - 0x5F	Reserved for Future AMI error codes.
S3 Resume Progress Codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by the DXE IPL)>
0xE1	S3 Boot Script execution.
0xE2	Video repost.
0xE3	OS S3 wake vector call
0xE4 - 0xE7	Reserved for Future AMI error codes.
S3 Resume Error Codes	
0xE8	S3 Resume failed.
0xE9	S3 Resume PPI not found.
0x3A	S3 Resume Boot script error.
0xEB	S3 OS wake error.
0xEC - 0xEF	Reserved for Future AMI error codes.
Recovery Progress Codes	
0xF0	Recovery condition trigged by firmware (Auto recovery).
0xF1	Recovery condition triggered by user (Forced recovery).
0xF2	Recovery process started.
0xF3	Recovery firmware image is found.
0xF4	Recovery firmware image is loaded.
0xF5 - 0xF7	Reserved for Future AMI progress codes.
Recovery Error Codes	
0xF8	Recovery PPI is not available.
0xF9	Recovery capsule is not found.
0xFA	Invalid recovery capsule.
0xFB - 0xFF	Reserved for Future AMI error codes.

PEI Beep Codes

# of Beeps	Description
1	Memory not installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice).
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume Failed
7	Reset PPI is not available

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started.
0x64	CPU DXE initialization is started. (CPU module specific).
0x65	CPU DXE initialization is started. (CPU module specific).
0x66	CPU DXE initialization is started. (CPU module specific).
0x67	CPU DXE initialization is started. (CPU module specific).
0x68	PCI host bridge initialization.
0x69	North Bridge DXE initialization is started.
0x6A	North Bridge DXE SMM initialization is started.
0x6B	North Bridge DXE initialization (North Bridge module specific.)
0x6C	North Bridge DXE initialization (North Bridge module specific.)
0x6D	North Bridge DXE initialization (North Bridge module specific.)
0x6E	North Bridge DXE initialization (North Bridge module specific.)
0x6F	North Bridge DXE initialization (North Bridge module specific.)
0x70	South Bridge DXE initialization is started.
0x71	South Bridge DXE SMM initialization is started.
0x72	South Bridge devices initialization.
0x73	South Bridge DXE initialization (South Bridge module specific.)
0x74	South Bridge DXE initialization (South Bridge module specific.)
0x75	South Bridge DXE initialization (South Bridge module specific.)
0x76	South Bridge DXE initialization (South Bridge module specific.)
0x77	South Bridge DXE initialization (South Bridge module specific.)
0x78	ACPI module initialization.
0x79	CSM initialization.
0x7A - 0x7F	Reserved for future AMI DXE codes
0x80 - 0x8F	OEM DXE initialization codes

0x90	Boot Device Selection (BDS) phase is started.
0x91	Driver connecting is started.
0x92	PCI Bus initialization is started.
0x93	PCI Bus Hot Plug Controller Initialization.
0x94	PCI Bus Enumeration.
0x95	PCI Bus Request Resources.
0x96	PCI Bus Assign Resources.
0x97	Console Output devices connect.
0x98	Console input devices connect.
0x99	Super IO initialization.
0x9A	USB initialization is started.
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E - 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready to Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP begin
0xB1	Runtime Set Virtual Address MAP end
0xB2	Legacy Option Rom Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM setting)
0xB8 - 0xBF	Reserved for future AMI codes
0xC0 - 0xCF	OEM BDS initialization codes

DXE Error Codes

0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources.
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset Protocol is not available

DXE Beep Codes

# of Beeps	**Description**
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Checkpoints

Status Code	**Description**
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D - 0x2A	OEM pre-memory initialization codes
0x3F - 0x4E	OEM PEI post memory initialization codes
0x80 - 0x8F	OEM DXE initialization codes
0xC0 - 0xCF	OEM BDS initialization codes

Appendix B: HDEC Series Interface

Note: The HDEC Series interface is Trenton Systems proprietary. Contact Trenton for more information about integrating the SEP8253 into your program.