TKL8255

8255-xxx

No. 87-008255-000 Revision D

HARDWARE

TECHNICAL REFERENCE

Intel® Xeon® E3-1200 v5 series
Intel® Core™ i7-6700
Intel® Core™ i5-6500
Intel® Core™ i3-6100TE
(Skylake-S)

Dual and Quad Core

PROCESSOR-BASED

SHB

Warranty

The following is an abbreviated version of Trenton Systems' warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at: www.trentonsystems.com/about-us/company-policies/.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Systems, Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Systems' discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Systems, Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Systems, Inc. Trenton Systems, Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Systems, Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Systems, Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Systems, Inc.

Return Policy

A Return Material Authorization (RMA) number, obtained from Trenton Systems prior to return, must accompany products returned for repair. The customer must prepay freight on all returned items, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton via Ground, unless prior arrangements are made by the customer for an alternative shipping method.

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Lawrenceville, Georgia

Trenton Systems, Inc.
1725 MacLeod Drive
Lawrenceville, Georgia 30043
Attn: Repair Department

Contact Trenton Systems for our complete service and repair policy.

TRADEMARKS

IBM, PC/AT, VGA, EGA, OS/2 and PS/2 are trademarks or registered trademarks of International Business Machines Corp.
AMI and APTIO are trademarks of American Megatrends Inc.
Intel, Xeon, Intel Core, Intel AMT, Intel TXT, Intel Hyper-Threading Technology and Intel Virtualization Technology are trademarks or registered trademarks of Intel Corporation.
MS-DOS and Microsoft are registered tradema`rks of Microsoft Corp.
PICMG, SHB Express and the PICMG logo are trademarks or registered trademarks of the PCI Industrial Computer Manufacturers Group.
PCI Express is a trademark of the PCI-SIG
All other brand and product names may be trademarks or registered trademarks of their respective companies.

LIABILITY DISCLAIMER

This manual is as complete and factual as possible at the time of printing; however, the information in this manual may have been updated since that time. Trenton Systems, Inc. reserves the right to change the functions, features or specifications of their products at any time, without notice.

E-mail: Support@TrentonSystems.com
Web: www.TrentonSystems.com

TRENTON Systems, Inc.
1725 MacLeod Drive, Lawrenceville, Georgia 30043
Sales: (800) 875-6031 • Phone: (770) 287-3100 • Fax: (770) 287-3150

This page intentionally left blank

Contents

HANDLING PRECAUTIONS

WARNING: This product has components that may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD STORAGE PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

Before You Begin

Introduction

It is important to be aware of the system considerations listed below before installing your TKL8255 (8255-xxx) SHB. Overall system performance may be affected by incorrect usage of these features.

DDR4-2133 Memory

Trenton recommends unbuffered ECC PC4-17000 memory modules for use on the TKL8255. These unbuffered ECC (64-bit) DDR4 DIMMs must be DDR4-2133 (PC4-17000) compliant. The TKL8255 supports DDR4-1866 (PC4-14900) but optimal performance will not be achieved when these modules are utilized. The TKL8255 supports a maximum of 64GB of memory.

NOTES:

- To maximize memory interface speed, populate each memory channel with DDR4 DIMMs having the same interface speed. The SHB will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- All memory modules must have a 288-pin edge connector
- The SHB supports the following memory module memory latency timings:
  - 16-16-16 for 2133MHz DDR4 DIMMs
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the TKL8255 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

Population order[#]	CPU1
1	BK0A
2	BK1A
3	BK0B
4	BK1B

[#]Using a balanced memory population approach ensures maximum memory interface performance. A "balanced approach" means using an even number of DIMMs on the TKL8255 SHB whenever possible.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

PCI Express 3.0 Links and PICMG® 1.3 Backplanes

The A0, A2 and A3 PCI Express® links on the SHB connect directly to the processor onboard the TKL8255. These links can operate as either PCI Express 3.0, 2.0 or 1.1 links based on the end-point devices on the backplane that are connected to the SHB and the backplane's PCIe link design itself. In addition to automatically configuring themselves for either PCIe 3.0, 2.0 or 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple links from the CPU (links A0, A2 and A3) can be utilized on a backplane as a single x16 PCIe electrical link, two x8 links, or one x8 and two x4 links. The CPU's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. PCIe link B0 comes from the board's PCH and is a x4 PCIe 3.0 interface. **NOTE**: PCIe 3.0 support is dependent on several variables, including target card type and tolerances. Contact Trenton Systems for more information on PCIe 3.0 support.

PICMG 1.3 Backplane Usage with the TKL8255

The TKL8255 combo-class, PICMG 1.3 system host board supports the standard's optional SHB-to-backplane USB (4) and Gigabit Ethernet (1) interfaces. Both 3rd party industry standard PICMG 1.3 backplanes as well as a variety of Trenton backplanes are compatible with the TKL8255 including the Trenton BPG8194, BPG8155 and the BPG8032. There are several backplanes Trenton does not recommend for use on the TKL8255. See Tech Info – Trenton PICMG 1.3 Backplanes Compatible with the TKL8255 on-line document.

Power Connection

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The TKL8255 supports these signals, controlled by the ACPI and are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to the *Power Connection* section in the TKL8255 manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

SATA RAID Operation (Windows O/S Setup)
The Intel® C236 Platform Controller Hub (PCH) used on the SHB features Intel® Rapid Storage Technology (Intel® RST) and requires unique drivers. A .zip file is available on the Trenton Systems website to help you configure the SATA ports as RAID drives connected to the TKL8255 while taking advantage of the PCH's drive array management.

If you would like your system to provide you with an immediate notification of a failed drive in the RAID array then the "Hot Plug" setting on the Advanced/SATA TKL8255 BIOS screen needs to be ENABLED for each drive in the array. If this BIOS setting is DISABLED a drive failure, notification alert may take several minutes or even longer if there is no hard drive activity on the RAID array.

DisplayPort and DVI-D
The TKL8255 offers both a Display Port and two, DVI-D video interfaces. The DisplayPort is a vertical port mounted directly on the SHB at the I/O bracket. The DVI-D ports are located on the board. These ports are useful in system designs that incorporate a flat panel LCD display directly into the system enclosure. Contact Trenton Systems for information on routing the internal DVI-D connections outside of a chassis. The ports may run simultaneously; however, the specific dual monitor implementation is a function of the system's operating system and video driver parameters. Like the SATA RAID, file a TKL8255 video driver file is available under the DOWNLOADS tab of the TKL8255 product detail webpage.

Realtek AL262 HD Audio Codec
Onboard audio capability on the TKL8255 is provided by the Realtek AL262 HD Audio Codec. An onboard header (P38) is provided to connect to the audio codec. Use Trenton part # 92-00677700 to provide 1/8" audio jacks to a standard I/O bracket. This board provides Line In, Line Out and Microphone connections. The driver can be downloaded from this link.

Intel® vPro™
The TKL8255 is Intel® vPro™ technology enabled for select processors. vPro™ provides administrators with additional management capabilities that aid in threat management, encryption and remote administration. The Intel Management Engine drivers must be installed for these features to function. Contact Trenton Systems Support for specific application requirements for vPro™.

BIOS
The TKL8255 features the Aptio® BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE.

Operating Systems
Trenton Systems has successfully tested the TKL8255 system host board with a wide variety of contemporary operating systems including Linux (Red Hat RHEL, Centos and SUSE), Windows® 8.1, Windows® 10, Windows® 2012 Server, and Windows® 2016 Server. Legacy 32-bit operating systems are not supported on the TKL8255.
See this application note for specific operating system compatibility.
Note: Trenton Systems does not recommend Windows® 7 or Windows® Server 2008 for use with the TKL8255 as Intel® "Greenlow" architecture limitations prevent full hardware functionality.

For More Information
Refer to the appropriate sections *TKL8255 Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the Downloads tab on the TKL8255 web page.

This page intentionally left blank

Specifications

Introduction

The TKL8255 is a combo-class, PICMG® 1.3 system host board featuring the choice of a long-life / embedded, Intel® Xeon® E3-1200 v5 Series, Intel® Core™ i7-6700, Intel® Core™ i5-6500 or Intel® Core™ i3-6100(TE) processor formally known as Skylake-S. These processors utilize a 14nm micro-architecture, and have a DDR4-1866/2133 integrated memory controller that supports two, dual-channel DDR4-1866/2133 memory interfaces. The TKL8255 supports four DDR4 DIMM sockets. With 4GB, DDR4 DIMMs the total system memory capacity for a TKL8255 is 16GB and doubles to 32GB using 8GB DDR4 DIMMs and again to 64GB using 16GB DIMMs. 64GB is the maximum memory capacity of the TKL8255.

PCI Express 3.0 links form the off-board interfaces on the TKL8255 edge connectors including the B0 link from the board's Intel® C236 Platform Controller Hub or PCH. The TKL8255 supplies the twenty PCI Express 3.0 interface links needed for a PICMG 1.3 compliant server or graphics-class backplane. All TKL8255 links support auto-negotiation with automatic link training and may also operate as PCI Express 2.0 or 1.1 electrical interfaces. This SHB design also supports the PICMG 1.3 optional PCI 32-bit/33MHz serial interface on edge connector D.

Video and I/O features on the TKL8255 boards include:

- Three video interfaces (one DisplayPort and two DVI-D) that are driven with the Intel HD Graphics 530 onboard the processor
- x4 PCIe 3.0 M.2 Slot supports NVMe storage solutions
- Three Gigabit Ethernet interfaces with two on the I/O plate and one available for use on a PICMG 1.3 compliant backplane or over a cable
- Six SATA/600 ports that can support independent drives or RAID drive arrays
- Ten USB interfaces (4, USB3.0 and 6, USB 2.0)
- An RS232 high-speed serial port and a configurable RS232/422/485 serial interface port
- PS/2 Mouse and Keyboard Header
- HD Audio Support
- Integrated TPM 2.0 for Trusted Computing applications

The listing below summarizes the targeted embedded processors supported on the TKL8255 board.

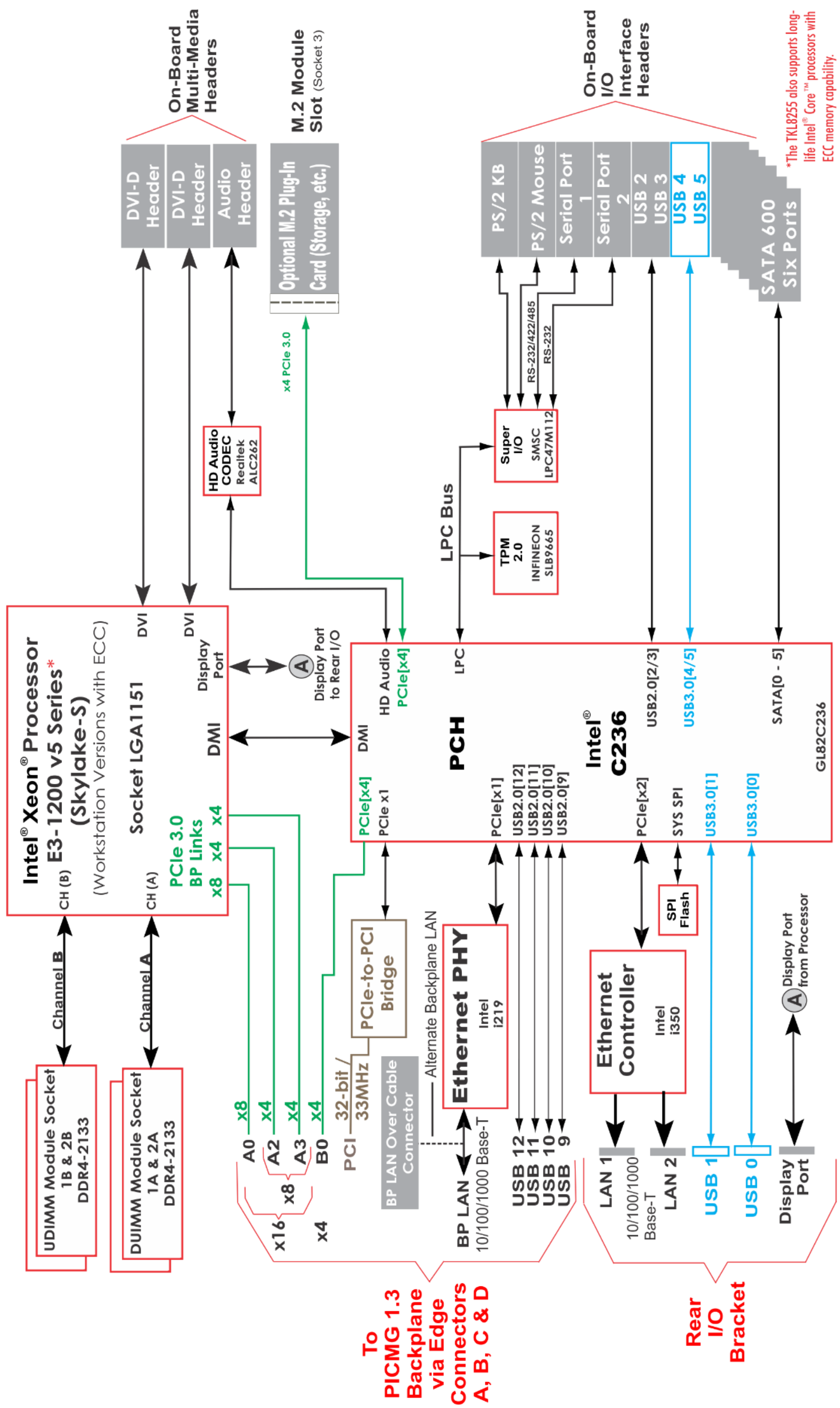
Model #	Model Name	Speed	Intel CPU Number
Intel Xeon Processor (Skylake-S) - Quad Core, 8MB cache, H-T, VT, TXT, ECC*:			
8255-006	TKL/3.6SR8	3.6GHz	E3-1275 v5
* H-T = Intel Hyper-Threading, VT = Intel Virtualization Technology, TXT= Intel Trusted Execution Technology, ECC Memory Support, L=Low Power			
Intel Xeon Processor (Skylake-S – Quad Core, 8MB Cache, H-T, VT, TXT, ECC			
8255-022	TKL/2.4SRL8	2.3GHz	E3-1268L v5
Intel Xeon Processor (Skylake-S) - Quad Core, 8MB cache, VT, TXT, ECC:			
8255-013	TKL/3.3/S8	3.3GHz	E3-1225 v5
Intel Core i7 Processor (Skylake-S) – Quad Core, 8MB cache, H-T, VT, TXT			
8255-035	TKL/3.4SRN8	3.4GHz	Core i7-6700
Intel Core i5 Processor (Skylake-S) – Quad Core, 6MB cache, VT, TXT			
8255-045	TKL/3.2SN6	3.2GHz	Core i5-6500
Intel Core i3 Processor (Skylake-S) - Dual Core, 4MB cache, H-T, VT, ECC:			
8255-063	TKL/2.7DSR4	2.7GHz	Core i3-6100TE

Additional embedded and non-embedded processor options are available for use on the TKL8255 system host board.

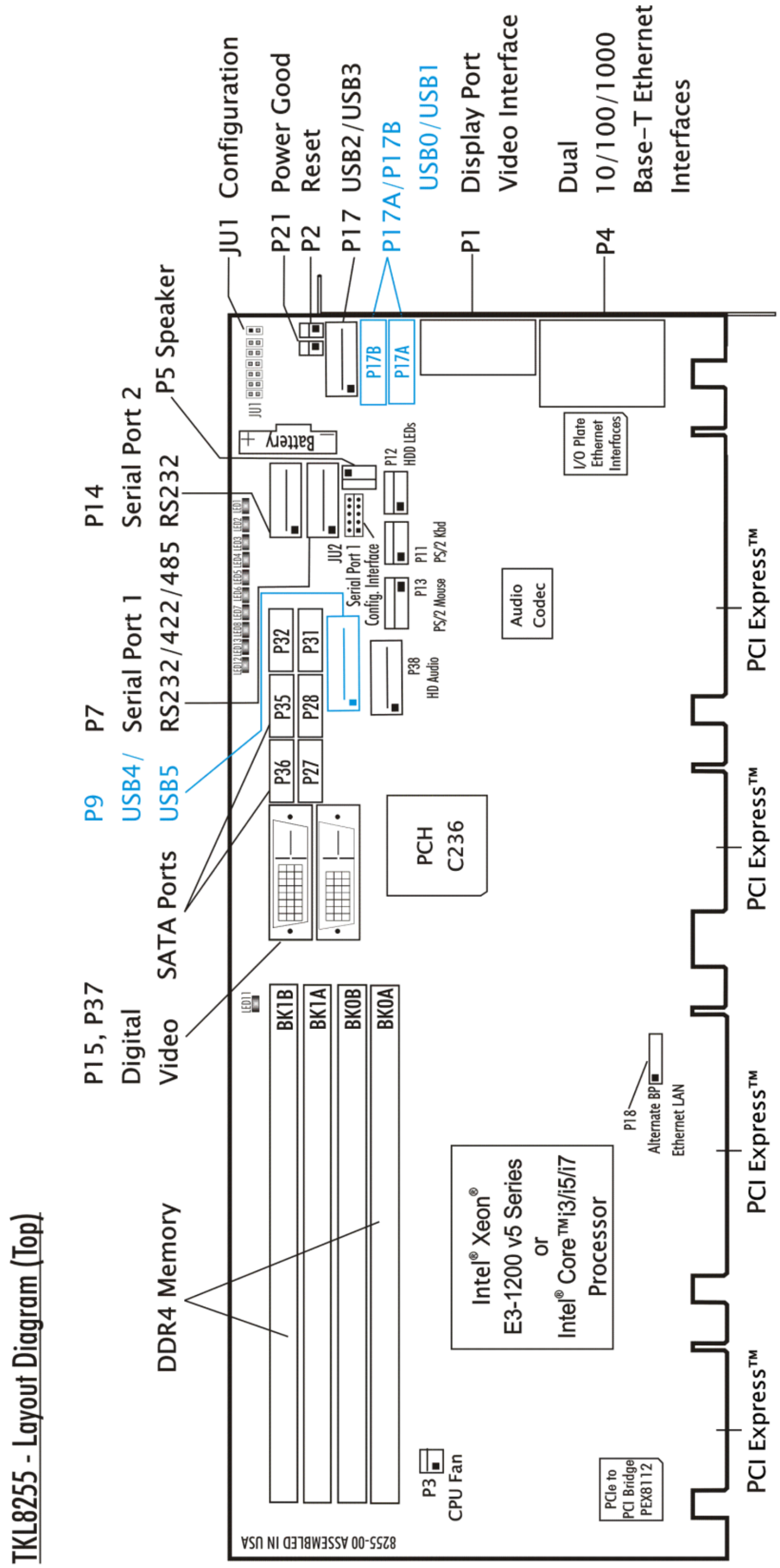
Features

- Intel® Xeon® E3-1200 v5 Series and select Intel® Core™ i7, i5 and i3 Processors (Skylake-S)
- Intel® C236 Platform Controller Hub (Greenlow)
- Direct PCI Express® 3.0 links from the processor to the board's edge connectors
- A Combo-class SHB that is compatible with PCI Industrial Computer Manufacturers Group (PICMG) 1.3 Specification
- TKL8255 provides a total of 21 lanes of PCI Express for off-board system integration
- Direct DDR4-1866/2133 Memory Interfaces into the Skylake-S Processor
- Four DDR4 DIMM sockets capable of supporting up to 64GB of system memory with 16GB DDR4 DIMMs and 32GB maximum capacity with readily available 8GB DDR4 DIMMs
- Three digital video interfaces with one DisplayPort on the rear I/O bracket and 2 DVI-D ports onboard
- M.2 Slot provides x4 PCIe 3.0 lanes for new NVMe SSD storage solutions
- Two 10/100/1000Base-T Ethernet interfaces available on the SHB's I/O plate
- Six Serial on-board ATA/600 ports support six independent SATA storage devices
    - SATA/600 ports may be configured to support RAID 0, 1, 5 or 10 implementations
- Six Universal Serial Bus (USB 2.0) interfaces
- Four Universal Serial Bus (USB 3.0) interfaces
- Off-board I/O support provided for one 10/100/1000Base-T Ethernet interface and four USB 2.0 port connections on a PICMG 1.3 backplane
- PS/2 mouse and keyboard headers, high-speed RS232 and RS232/422/RS485 serial ports
- A full-length backer plate on the rear of the SHB enhances the rugged nature of the board by maximizing component protection and simplifying mechanical system integration
- Full PC compatibility
- Revision controlled Aptio 5.x BIOS for American Megatrends, Inc. (AMI) resides in the SHB's SPI flash device to simplify field upgrades and BIOS customization
    - See the *BIOS Setup Manual* for TKL8255 System Host Board for more information

TKL8255 (8255-xxx) – Single-Processor SHB Block Diagram

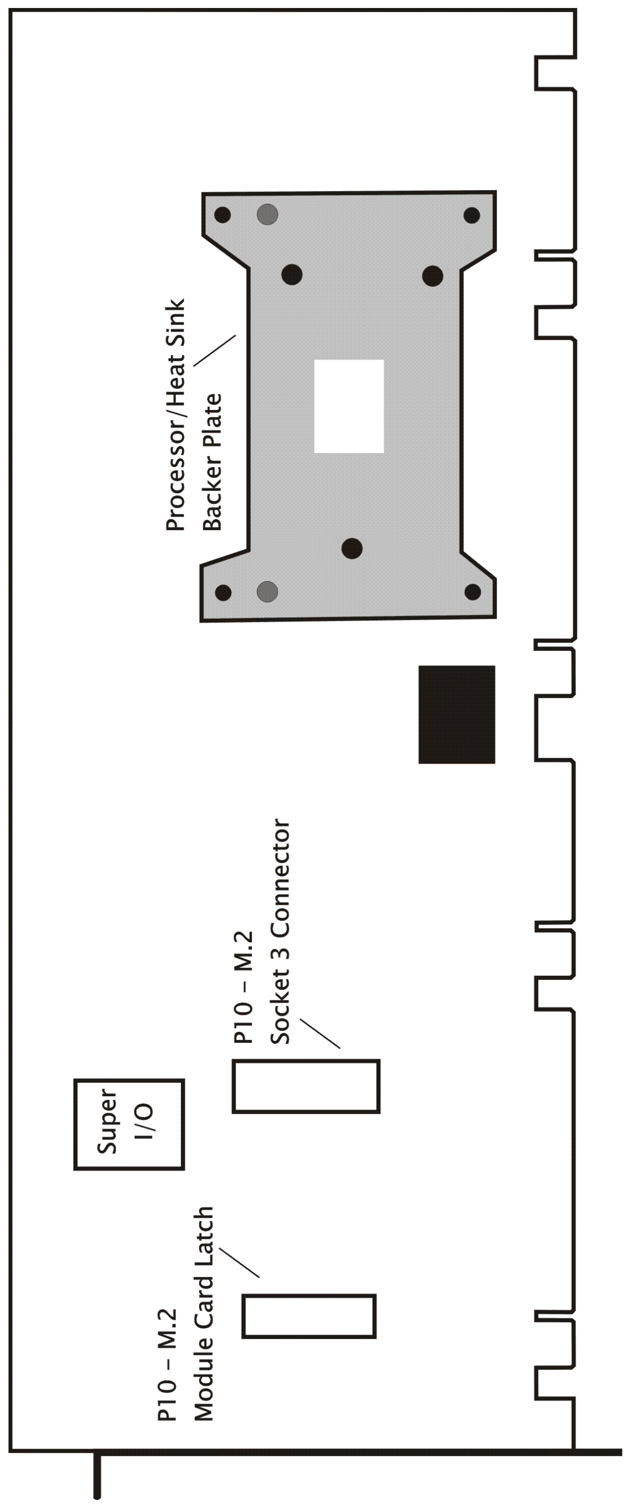


TKL8255 (8255-xxx) – Single-Processor SHB Layout Diagram – Top



TKL8255 (8255-xxx) – Single-Processor SHB Layout Diagram – Bottom

Note: The backer plate has been removed in the view below. Access holes are provided in the plate in order to allow access to the M.2 Connector (P10).



Processor

- Intel® Xeon® E3-1200 v5 Series Processor – Long-life 14nm/Skylake-S processor or the long-life desktop versions including the Intel® Core™ i7-6700, Intel® Core™ i5-6500 and Intel® Core™ i3-6100TE processor
- Processor plugs into an LGA1151 socket

Supported Intel® Processor Technologies

The Intel® technologies supported on the TKL8255 system host board include:

- Intel® vPro – Intel vPro is a combination of processor technologies, silicon hardware enhancements and features that enable system designers to implement more stringent security protocols and remote management functions.

- Intel® Hyper-Threading (Intel® HT) – This processor technology allows simultaneous multithreading of CPU tasks to enable parallel system operations. An operating system that is hyper-threading aware can address each core as a logical processor in order to spread out execution tasks to improve application software efficiency and overall system speed.

- Intel Virtualization Technology (Intel® VT-x) - Enabled in the SHB's BIOS, this technology enables multiple operating systems to run in specific processor cores thereby creating virtual machines (VMs) on a single SHB.

- Intel Virtualization Technology for Directed I/O (Intel® VT-d) – This is a sub-set of Intel VT-x and enables I/O device assignments to specific processor cores or VMs. Intel VT-d also supports DMA remapping, interrupt remapping and software DMA and interrupt status reporting. Intel VT-d is an optional extension to the Intel VT-x technology.

- Intel® VT-x with Extended Page Tables (EPT) – This feature is enabled in the Skylake-S micro-architecture to supports the processor's "real mode" or unrestricted guest feature.

- Intel Trusted Execution Technology (Intel® TXT) – This processor feature works in conjunction with the SHB's on-board Trusted Platform Module or TPM to allow the system designer to create multiple and separated execution environments or partitions with multiple levels of protection and security. The TPM provides for a way to generate and store an encrypted access key for authenticated access to sensitive applications and data. This private key never leaves the TPM, is generally available only to authorized system administrators, and enables remote assurance of a system's security state.

- Intel Turbo Boost Technology 2.0 – The higher performance Skylake-S processors may run above the processors stated clock speed via a new dynamic processor speed control technology called Intel Turbo Boost 2.0. The processor enters the boost mode when the operating system requests the highest possible performance state as defined by the Advanced Configuration and Power Interface or ACPI.

- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI) – Seven new instructions available in the Skylake-S micro-architecture makes pervasive encryption in an IT environment possible while enabling implementation that is faster and more affordable by providing advanced data protection and greater hardware platform security.

Note: The Intel® Core™ i3 processor options do not support many of these advanced Intel processor technologies.

The following chart defines which Intel technology is supported on which particular embedded Skylake-S processor featured on the TKL8255 system host board.

Intel Technology	Intel Xeon E3-1275 v5	Intel Xeon E3-1225 v3	Intel Xeon E3-1268L v3	Intel Core i7-6700	Intel Core i5-6500	Intel Core i3-6100 TE
Intel vPro	Yes	Yes	Yes	Yes	Yes	No
Intel HT	Yes	No	Yes	Yes	No	Yes
Intel Turbo Boost 2.0	Yes	Yes	Yes	Yes	Yes	No
Intel VT-x	Yes	Yes	Yes	Yes	Yes	Yes
Intel VT-d	Yes	Yes	Yes	Yes	Yes	Yes
Intel VT-x with EPT	Yes	Yes	Yes	Yes	Yes	Yes
Intel TXT	Yes	Yes	Yes	Yes	Yes	No
Intel Turbo Boost 2.0	Yes	Yes	Yes	Yes	Yes	No
Intel AES-NI	Yes	Yes	Yes	Yes	Yes	Yes

Serial Interconnect Interface
PCI Express® 3.0, 2.0, and 1.1 compatible

Data Path
DDR4-2133 Memory - 64-bit (per channel)

Serial Interconnect Speeds
PCI Express 3.0 – 8.0GHz per lane
PCI Express 2.0 – 5.0GHz per lane
PCI Express 1.1 - 2.5GHz per lane

Platform Controller Hub (PCH)
- Intel® C236 Platform Controller Hub (Greenlow)

Intel® Direct Media Interface (DMI)
The Skylake-S processors support the latest interface version called DMI. DMI supports communications between the board's processor and Intel® C236 PCH up to 20Gb/s each direction, full duplex and is transparent to software.

Memory Interface
The TKL8255 features two memory channels of unbuffered DDR4 with two DIMMs per channel. These DDR4-2133 memory interface channels support up to four, unbuffered, ECC PC4-17000 standard memory DIMMs. Non-ECC DDR4 DIMMs are also supported, but the two memory types cannot be used together on the SHB. The peak memory interface transfer rate per channel is 2133MT/s when using PC4-17000 DIMMs. The TKL8255 supports DDR4-1866 (PC4-14900) but optimal performance will not be achieved when these modules are utilized; peak memory interface transfer rate per channel is 1866MT/s when utilizing these DIMMs.

The System BIOS automatically detects memory type, size and speed. Trenton recommends unbuffered ECC PC4-17000 or PC4-14900 DDR4 memory modules for use on the TKL8255. These unbuffered ECC (64-bit) DDR4 DIMMs must be PC4-17000 or PC4-14900 compliant.

DMA Channels
The SHB is fully PC compatible with seven DMA channels, each supporting type F transfers.

Interrupts
The SHB is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Bios (Flash)

The TKL8255 board uses an Aptio® 5.x BIOS from American Megatrends Inc. (AMI). The BIOS features built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. The BIOS resides in a 128Mb Macronix MX25L12835FM2I-10G SPI Serial EEPROM (SPI Flash). The BIOS may be upgraded from a USB thumb drive storage device by pressing <Ctrl> + <Home> immediately after reset or power-up with the USB device installed. Custom BIOSs are available.

Cache Memory

The processors include either a 4MB, 6MB or 8MB Intel® Smart Cache memory capacity that is equally shared between all of the processor cores on the die.

Ethernet Interfaces

The TKL8255 supports three Ethernet interfaces. The first two interfaces are on-board 10/100/1000Base-T Ethernet interfaces located on the board's I/O bracket and implemented using an Intel® i350-AM2 Dual Gigabit Ethernet Controller. These I/O bracket interfaces support Gigabit, 100Base-T and 10Base-TX Fast Ethernet modes and are compliant with the IEEE 802.3 Specification.

The main components of the I/O bracket Ethernet interfaces are:

- Intel® i350-AM2 for 10/100/1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCIe interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connectors on the SHB's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

The third LAN is supported by the Intel® C236 and the Intel® i217-LM Gigabit Ethernet PHY. This 10/100/1000Base-T Ethernet interface is routed to the PICMG 1.3 backplane via SHB edge connector C. The SHB includes an Ethernet connector (P18) that can be utilized to route this interface over an Ethernet cable rather than to the PICMG 1.3 backplane.

Software drivers are supplied for most popular operating systems.

Trusted Platform Module

The TKL8255 provides support for Trusted Platform Module 2.0 operations via an Infineon SLB9665 controller. This feature aids in assuring platform integrity by providing a system designer the capability to form a root of trust in conjunction with the BIOS that ensures a computer is of a specified hardware and software configuration.

Watchdog Timer (WDT)

The TKL8255 provides a programmable watchdog timer with programmable timeout periods of 100 msec to 3 minutes via board component U11. When enabled the WDT (i.e. U11) will generate a system reset. WDT control is supplied via the General Purpose IO pins from the Intel® C236 Platform Controller Hub (PCH). The PCH’s GPIO_LVL2 register controls the state of each GPIO signal. This 32-bit register is located within GPIO IO spaces. The GPIO_BASE IO address is determined by the values programmed into the PCH’s LPC Bridge PCI configuration at offset 48-4B(h).

Watchdog Timer (WDT) (Continued)

GPIO Bit Definitions:

Watchdog Timer Enable (WDT_EN#)
Watchdog timer enable\disable functionality is controlled by GPIO32. Clearing bit 0 of the GP_LVL register enables the WDT. The GP_LVL2 register is located at IO address GPIO_BASE + offset 38(h). The power-on default for this bit is a “1” which disables WDT functionality. Setting this bit to a “0” enables the WDT at the pre-selected interval.

Watchdog Select 0 (WDT_S0)
The state of this bit in conjunction with Watchdog Select 0 will select the WDT time out period. This function is controlled by GPIO33 and the state of this bit is determined by bit 1 of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST, the inverted state of this bit is reflected on Port80, LED0. If this bit is set to a “1” the LED is off, if set to a “0” the LED is on. The state of the GPIO pin is inverted at the Select 0 input of U11. See the Watchdog Timeout Period Selection table below for WDT interval selection information.

Watchdog Select 1 (WDT_S1)
The state of this bit in conjunction with Watchdog Select 1 will select the WDT time out period. This function is controlled by GPIO34 and the state of this bit is determined by bit three of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST, the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a “1” the LED in off, if set to a “0” the LED is on. The state of the GPIO pin is inverted at the Select 0 input of U11. See the Watchdog Timeout Period Selection table below for WDT interval selection information.

Watchdog_ Input (WDT_IN)
When the WDT is enabled this bit must be toggled (0 -> 1 or 1->0) within the selected watchdog timeout period, failure to do so will result in a system reset. This function is supported by the GPIO71 bit and its state is controlled by bit 23 of the GP_LVL3 register which is at IO address GPIO_BASE + offset 48(h). The inverted state of this bit is reflected on Port80, LED7. If this bit is set to a “1” the LED in off, if set to a “0” the LED is on.

Watchdog Timeout Period Selections:

WDT_EN# (GPIO32)	WD_S1 (GPIO34)	WD_S0 (GPIO33)	Watchdog Timeout Period
1	X	X	Disabled
0	1	1	100msec
0	1	0	1 sec
0	0	1	10 sec
0	0	0	1 min

The Watchdog Timer may require initialization prior to usage. GPIO 32, 33, 34 and 71 must be configured as outputs. While these GPIOs do default to outputs at power-on, care should be taken to insure they have not been altered prior to WDT usage. These GPIO are configured to outputs by clearing bits 0, 1 and 2 of the GP_IO_SEL2 register at GPIO_BASE + offset 34(h) to a “0”, as well as clearing bit 7 of the GP_IO_SEL3 register at GPIO_BASE + offset 44(h) to a “0”.

After initialization is completed (if required) the Watchdog timer period is selected by via the WDT_S1 and WDT_S0 bits. Once the timeout period has been programmed the WDT is “enabled” by clearing the WDT_EN# bit. To avoid the WDT from generating a system reset the WDT_IN bit must be toggled within the timeout period.

Watchdog Timer (WDT) (Continued)

Programming Example: Enable WDT with 10-second timeout period

Note: When writing to any of the WDT controlling GPIO bit the remaining bits of the selected GP_LVL2 and GP_LVL3 registers should remain unchanged.

Write bit 0 of GP_LVL2 to 1	pre condition GPIO32 for WDT disable
Write bits 2,1 of GP_LVL2 to 0,1	set Watchdog timeout period to 10 sec
Write bit 0 of GP_LVL2 to 0	enable Watchdog timer

At this point, the bit 7 of GP_LVL3 (GPIO71) must be toggled within a 10 sec period or the WDT will expire resulting in a system reset.

Power Requirements

The following power requirements table reflects nominal lab test values that were produced when 16GB of system memory were installed in the board installed.

Processor Type	SHB Type	Processor Speed	+5V	+12V	+3.3V
CPU Idle State:					
Intel Xeon E3-1275 v5	TKL8255	3.6GHz	0.41A	1.28A	1.38A
Intel Xeon E3-1225 v5	TKL8255	3.3GHz	0.48A	1.25A	1.39A
Intel Xeon E3-1268L v5	TKL8255	2.4GHz	0.47A	1.15A	0.00A
Intel Core i7-6700	TKL8255	3.4GHz	0.4A	1.46A	1.40A
Intel Core i5-6500	TKL8255	3.2GHz	0.38A	0.96A	1.36A
Intel Core i3-6100TE[D]	TKL8255	2.7GHz	0.38A	0.95A	1.28A
100% CPU Stress State:					
Intel Xeon E3-1275 v5	TKL8255	3.6GHz	0.56A	6.69A	2.04A
Intel Xeon E3-1225 5	TKL8255	3.3GHz	0.55A	5.79A	1.40A
Intel Xeon E3-1268L v5	TKL8255	2.4GHz	0.56A	5.51A	1.37A
Intel Core i7-6700	TKL8255	3.4GHz	0.59A	7.13A	1.49A
Intel Core i5-6500	TKL8255	3.2GHz	0.56A	5.04A	2.06A
Intel Core i3-6100TE[D]	TKL8255	2.7GHz	0.53A	3.80A	1.49A

Tolerance for all voltages is +/- 5%
[D]Dual-core processor, all other processors are quad-core CPUs
Actual power number will vary as a function of system application.

CAUTION: Trenton recommends an EPS type of power supply for systems using high-performance processors. The power needs of backplane option cards, high-performance processors and other system components may result in drawing 20A of current from the +12V power supply line. If this occurs, hazardous energy (240VA) could exist inside the system chassis. Final system/equipment suppliers must provide protection to service personnel from these potentially hazardous energy levels.

Stand-by voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

Power Fail Detection

A hardware reset is issued when any of the voltages being monitored drops below its specified nominal low voltage limit. The monitored voltages and their nominal low limits are listed below.

Monitored Voltage	Nominal Low Limit	Voltage Source
+5V	4.75 volts	System Power Supply
+3.3V	2.97 volts	System Power Supply
Vcc_DDR(+1.5V)	1.15 volts	On-Board Regulator
VCCIO_CPU(1.05V)	0.70 volt	On-Board Regulator
+1.05V(Chipset)	0.924 volt	On-Board Regulator
+1.05V(Chipset-ME)	0.924 volt	On-Board Regulator

Battery

A built-in lithium battery is provided for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the battery manufacturer. Dispose of used batteries according to the battery manufacturer's instructions.

Temperature/Environment

Operating Temperature: 0º C. to 50º C. for all CPU options except the E3-1275 v3 processor. Maximum TKL8255 operating temperature when using the Intel® Xeon® E3-1275 v3 processor is 45° C.

Air Flow Requirement: 350LFM continuous airflow

Storage Temperature: - 40º C. to 70º C.

Humidity: 5% to 90% non-condensing

Mechanical

The standard cooling solution used on the TKL8255 enables placement of option cards approximately 2.15" (54.61mm) away from the top component side of the SHB. Contact Trenton for a system engineering consultation if your application needs a lower profile cooling solution. The SHB's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

Board Stiffener Bars / Full-Length Backer Plate

The TKL8255 board's full-length backer plate ensures the safe insertion and removal of the SHB from any system by ensuring proper SHB alignment within the card guides of a computer chassis. This rugged backer plate design maximizes system reliability by shielding the SHB's rear-mounted components from mechanical damage.

Mean Time Between Failures (MTBF)

Trenton Engineers are currently working to determine a Mean Time Between Failures figure. Contact Trenton for the most up-to-date-information.

Industry Certifications

This SHB is designed to meet a variety of internationally recognized industry standards including UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN6100-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996 and EN61000-4-11:1994.

Configuration Jumpers

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

NOTE: Jumper JU1 is a dual-row, 14-pin jumper. Each position controls the operation of a specific SHB implementation

NOTE: For the three-position JU12 jumper, "RIGHT" is toward the I/O bracket side of the board; "LEFT" is toward the header connector P14.

JU1 Pins 1-2 and 3-4

CMOS Clear
Install on pins 1 and 2 to operate *
Install on pins 3 and 4 to clear.

Note: To clear the CMOS, power down the system and install the JU1 jumper on pins 3 and 4. Wait for at least two seconds, move the jumper back to pins 1 and 2 and turn the power on. Clearing CMOS on the TKL8255 will not result in a checksum error on the following boot. If you want to change a BIOS setting, you must press *DEL* or the *F2* key during POST to enter BIOS setup after clearing CMOS.

JU1 Pins 5-6

Management Engine (ME Recovery)
No jumper installed on pins 5 and 6 is the normal SHB operating mode.*
Install a jumper on pins 5 and 6 for one power-up cycle to force a management engine update.

JU1 Pins 7-8

Clear Password
No jumper installed on pins 7 and 8 is the normal SHB operating mode.*
Install jumper on pins 7 and 8 for one power-up cycle to reset the password to the default (null password).

JU1 Pins 9-10

BIOS Recovery
No jumper installed on pins 9 and 10 is the normal SHB operating mode.*
Install jumper on pins 9 and 10 to force a Top Block Swap (Alternate Boot Block).

JU1 Pins 11-12

Flash Descriptor Security
No jumper installed on pins 11-12 enables the Flash Descriptor Security.*
Install jumper on pins 11 and 12 to disable Flash Descriptor Security.

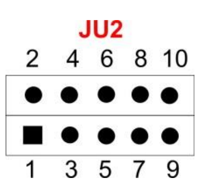
JU1 Pins 13-14

SPI Voltage Enable (Factory Use Only)
No jumper installed on pins 13 and 14 is the normal SHB operating mode.*
Installing a jumper on pins 13 and 14 allows SPI factory programming via a clip-on programmer.

CAUTION: Installing this jumper is required for certain factory operations. Field installation of a jumper in JU1 position 13-14 may result in unintended system operation.

JU2

Serial Port 1 Interface Configuration
JU2 uses five jumpers to allow serial port one to be configured as either a RS232 or a RS422/RS485 electrical interface. The jumper tables below illustrate the possible interface configurations for serial port one.



RS232 operation* – Jumper 1 to 2 **and** 3 to 4 **and** 9 to 10
RS485 Full Duplex, No Termination – Jumper 1 to 2 **and** 9 to 10[1]
RS485 Half Duplex, No Termination – Jumper 9 to 10
RS485 Full Duplex, With Termination – Jumper 1 to 2 **and** 5 to 6[2]
RS485 Half Duplex, With Termination – Jumper 5 to 6 **and** 9 to 10

Notes:
1 – Shut between pins 9 and 10 can optionally be removed to unconditionally enable the Tx driver
2 – Shut between pins 9 and 10 can optionally be installed to unconditionally enable the Tx driver

Status LEDs

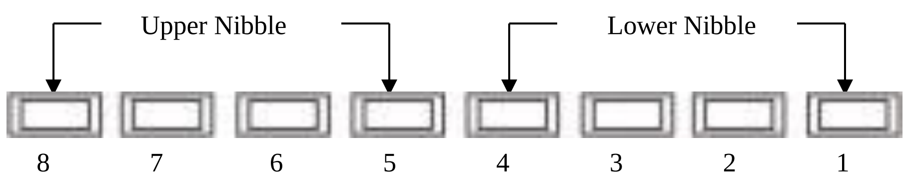
POST Code LEDs 1 - 8

As the POST (Power On Self-Test) routines are performed during boot-up, test codes are displayed on Port 80 POST Code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LEDs are located on the top of the SHB, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED1) to left (position 8 – LED8). Refer to the board layout diagram for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. Specific test codes are listed in Appendix A - BIOS Messages section of the TKL8255 Technical Reference Manual. After a normal POST sequence, the LEDs are off (00h) indicating that the SHB's BIOS has passed control over to the operating system loader typically at interrupt INT19h. The chart is from Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

Upper Nibble (UN)				
Hex. Value	LED8	LED7	LED6	LED5
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED4	LED3	LED2	LED1
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



TKL8255 POST Code LEDs

P4A/P4B Ethernet LEDs

The I/O bracket houses the two RJ-45 network connectors for Ethernet LAN1 and LAN2. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

LED/Connector	Description
Activity LED	This LED identifies the validity of a link on the specific interface. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).
Off	No valid link exists on this interface.
On (flashing)	Indicates network transmit or receive activity.
On (solid)	Indicates a valid link with no transmit or receive activity.
Speed LED	This multi-color LED identifies the connection speed of the SHB's P4A (LAN2) and P4B (LAN1) Ethernet interfaces. These are the lower LEDs on the dual LAN connector (i.e., toward the edge connectors).
Green	Indicates a valid link at 1000-Mb/s or 1Gb/s
Orange	Indicates a valid link at 100-Mb/s.
Off	Indicates a valid link at 10-Mb/s
RJ-45 Network Connectors	The RJ-45 network connector requires a Connector category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection.

LED11 - Backplane LAN LED

LED11 is located just above the right side of memory DIMM connector BK1B. A flashing LED11 indicates that network transmit and receive activity is occurring on the Ethernet LAN routed to the board's edge connector C / cable connector P18. This LAN provides a network interface for use on a compatible PICMG 1.3 backplane or over a cable.

LED13 – M.2 Activity LED

LED13 is located on the rear of the SHB, near the M.2 slot. A flashing LED13 indicates that I/O activity is occurring on the M.2 bus.

System BIOS Setup Utility

The TKL8255 features the Aptio® BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. The TSE setup utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details of the Aptio TSE are provided in the separate *TKL8255BIOS Technical Reference* manual. The BIOS and hardware technical reference manuals are available under the Downloads tab on the TKL8255 web page.

Connectors

NOTE:
A connector's square solder pad located on the bottom side of the PCB indicates pin 1.

P1 –DisplayPort Connector

20-pin digital A/V interface,
Molex #105020-001

PIN	SIGNAL	PIN	SIGNAL
1	TXP0	13	GND
2	GND	14	GND
3	TXN0	15	AUX_P
4	TXP1	16	GND
5	GND	17	AUX_N
6	TXN1	18	HPDET
7	TXP2	19	GND
8	GND	20	VCC3 DP
9	TXN2	21	SGGND1
10	TXP3	22	SGGND2
11	GND	23	SGGND3
12	TXN3	24	SGGND4

P2 - Reset Connector

2 pin single row header, Amp #640456-2

PIN	SIGNAL
1	Gnd
2	Reset In

P3 – CPU Fan Power Connector

4 pin single row MTA, Molex #47053-1000

PIN	SIGNAL
1	Gnd
2	+12V
3	Fan Tach
4	PWM Control Signal

P4A/P4B – Dual 10/100/1000Base-T Ethernet Connector - LAN1 and LAN2

RJ-45/Dual connector, Pulse #JG0-0024NL
Each individual RJ-45 connector is defined as follows:

PIN	SIGNAL	PIN	SIGNAL
1A	L2_MDI0n	1B	L1_MDI0n
2A	L2_MDI0p	2B	L1_MDI0p
3A	L2_MDI1n	3B	L1_MDI1n
4A	L2_MDI1p	4B	L1_MDI1p
5A	L2_MDI2n	5B	L1_MDI2n
6A	L2_MDI2p	6B	L1_MDI2p
7A	L2_MDI3n	7B	L1_MDI3n
8A	L2_MDI3p	8B	L1_MDI3p
9A	VCC_1.8V	9B	VCC_1.8V
10A	GND_A	10B	GND_b

Notes:
1 – LAN ports support standard CAT5 Ethernet cables
2 – P4A is LAN2 and P4B is LAN1

P5 - Speaker Port Connector

4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	Speaker Data
2	NC
3	Gnd
4	+5V

Connectors (continued)

P7 – Serial Port 1 Connector – RS422/RS485 Full Duplex Connections
10 pin dual row header, Amp #5103308-1

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Gnd	10	NC

Note: See JU2 pin-puts listed in the Jumpers & LEDs section on this document to enable serial port 1 signal connections.

P9 – Dual Universal Serial Bus (USB) 3.0 Connector
19 pin dual row header, Lotes ABA-USB-152-K04
(+5V fused with self-resetting fuse)

PIN	USB4 SIGNAL	PIN	USB5 SIGNAL
1	+5V-USB4	11	USBP5P
2	USB3_RX5AN	12	USBP5N
3	USB3_RX5AP	13	GND
4	GND	14	USB3_TX6BP
5	USB3_TX5BN	15	USB3_TX6BN
6	USB3_TX5BP	16	GND
7	GND	17	USB3_RX6AP
8	USBP4N	18	USB_RX6AN
9	USBP4P	19	+5V-USB5
10	ID		

P10 – M.2 M-Key Slot (SHB bottom side)
74 pin, JAE Electronic SM3ZS067U410AMR1000

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	3.3V
3	GND	4	3.3V
5	M2_PE_RXN3	6	NC
7	M2_PE_RXP3	8	NC
9	GND	10	SSD LED#
11	M2_PE_TXN3	12	GND
13	M2_PE_TXP3	14	GND
15	GND	16	GND
17	M2_PE_RXN2	18	GND
19	M2_PE_RXP2	20	NC
21	GND	22	NC
23	M2_PE_TXN2	24	NC
25	M2_PE_TXP2	26	NC
27	GND	28	NC
29	M2_PE_RXN1	30	NC
31	M2_PE_RXP1	32	NC
33	GND	34	NC
35	M2_PE_TXN1	36	NC
37	M2_PE_TXP1	38	M2_DEVSLP
39	GND	40	NC
41	M2_PE_RXP0	42	NC
43	M2_PE_RXN0	44	NC
45	GND	46	NC
47	M2_PE_TXN0	48	NC
49	M2_PE_TXP0	50	IO_RESET#
51	GND	52	M2SSD_CLKREQ
53	M2_CLK100N	54	PCH WAKE#
55	M2_CLK100P	56	NC
57	GND	58	NC
67	NC	68	PCH_SUSCLK
69	M2_PEDET	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

Connectors (continued)

P11 – PS/2 Keyboard Header
5 pin single row header, Amp #640456-5

PIN	SIGNAL
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused) with self resetting fuse

P12 – Hard Drive LED Connector
4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	LED +
2	LED -
3	LED -
4	LED +

P13 – PS/2 Mouse Header
6 pin single row header, Amp #640456-6

PIN	SIGNAL
1	Ms Data
2	NC
3	Gnd
4	Ms Power (+5V fused) with self resetting fuse
5	Ms Clock
6	NC

P14 – Serial Port 2 Connector – RS232 Connections
10 pin dual row header, Amp #5103308-1

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Gnd	10	NC

Contact Trenton Systems support for specific application information on Serial Port 2 (P14).

P15, P37 – Digital Video Connector (DVI-D)
24-socket digital video connector, Molex #0743205004

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DVI_TX2N	9	DVI_TX1N	17	DVI_TX0N
2	DVI_TX2P	10	DVI_TX1P	18	DVI_TX0P
3	Gnd	11	Gnd	19	Gnd
4	NC	12	NC	20	NC
5	NC	13	NC	21	NC
6	DVI_SCLK	14	5V	22	Gnd
7	DVI_SDAT	15	Gnd	23	DVI_TXCP
8	NC	16	DVI_HPD	24	DVI_TXCN

Note: Video connector supports standard DVI-D digital video cables

P17A, P17B – Universal Serial Bus (USB) 3.0 Connectors (I/O Bracket)
USB vertical connectors, Molex #48404-0003
(+5V fused with self-resetting fuse)

PIN	P17A SIGNAL	PIN	P17B SIGNAL
1	+5V-USB0	1	+5V-USB1
2	USB0-	2	USB1-
3	USB0+	3	USB1+
4	GND	4	GND
5	USB3_RX1AN	5	USB3_RX2AN
6	USB3_RX1AP	6	USB3_RX2AP
7	GND	7	GND
8	USB3_TX1BN	8	USB3_TX2BN
9	USB3_TX1BP	9	USB3_TX2BP

Note: P17A is USB0 and P17B is USB1

Connectors (continued)

P18 - 10/100/1000Base-T Ethernet Connector – Alternate Backplane LAN Over Cable

8 pin single row connector, Molex #0554500859

PIN	SIGNAL
1	A_MDI2N
2	A_MDI2P
3	A_MDI3N
4	A_MDI3P
5	A_MDI1N
6	A_MDI1P
7	A_MDI0N
8	A_MDI0P

BP LAN Cable Option
You may elect to create your own backplane LAN cable using the mating Molex connector information below. However, Trenton does offer a pre-made alternate backplane LAN cable with the mating Molex connector on one end and an RJ45 connector mounted into an I/O bracket on the other end. The Trenton part number for the alternate backplane LAN cable is:193500001150-00.

Note: Using the alternate backplane LAN cable effectively disconnects the LAN routing down to SHB edge connector C.

Note:
The mating Molex connector to use when making this alternative Ethernet cable has a Molex part number of 0513360810.

P21 – Power Good LED

2 pin single row header, Amp #640456-2

PIN	SIGNAL
1	LED -
2	LED +

Connectors (continued)

P27, P28, P31, P32, P35, P36 – SATA III 600 Ports

7 pin vertical locking connector, Molex #67800-8005

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	5	RX-
2	TX+	6	RX+
3	TX-	7	Gnd
4	Gnd		

Notes:
1 – P27 = SATA0 interface, P28 = SATA1 interface,
P31 = SATA2 interface, P32 = SATA3 interface,
P35 = SATA4 interface, P36 = SATA5 interface,
2 – SATA connectors support standard SATA interface cables
3 – All SATA ports support SATA 3.0, SATA 2.0 and SATA 1.0 devices
4 – SATA 3.0 = 600MB/s data transfers, SATA 2.0 = 300MB/s data transfers and SATA 1.0 = 150MB/s data transfers

P38 –HD Audio Connector – Audio Connections

10 pin dual row header, Amp #5103308-1

PIN	SIGNAL	PIN	SIGNAL
1	Line In L	2	Line In R
3	GND	4	GND
5	Mic L	6	Mic R
7	GND	8	Sense_A
9	Line Out L	10	Line Out R

Notes:
1 – For applications requiring external 1/8" audio jacks, use Trenton part # 92-00677700. This board provides Line In, Line Out and Microphone connections from the onboard audio codec to an I/O plate.

This page intentionally left blank

PCI Express® Reference

Introduction

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

PCI Express Links

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion. A link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth for each version of PCI Express listed below ranges from 500MB/s up to 2GB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. In PCI Express Gen1.1 the bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	250MB/s	500MB/s
x4	1GB/s	2GB/s
x8	2GB/s	4GB/s
x16	4GB/s	8GB/s

In PCIe Gen2 the bandwidths for the PCIe links are doubled as compared to PCIe Gen1.1 as shown below:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	500MB/s	1GB/s
x4	2GB/s	4GB/s
x8	4GB/s	8GB/s
x16	8GB/s	16GB/s

Link protocol changes and speed increases double PCIe Gen3 bandwidths compared to PCIe Gen2 speeds:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	1GB/s	2GB/s
x4	4GB/s	8GB/s
x8	8GB/s	16GB/s
x16	16GB/s	32GB/s

Scalability is a core feature of PCI Express. Some chipsets allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. In addition, although a board with a higher number of lanes will not function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) because the connectors are mechanically and electrically incompatible, the reverse configuration will function. A board with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot). The link auto-negotiates between the PCI Express devices to establish communication. The mechanical option card slots on a PICMG 1.3 backplane must have PCI Express configuration straps that alert the SHB to the PCI Express electrical configuration expected. The SHB can then reconfigure the PCIe links for optimum system performance.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express® System Host Board PCI Express Specification, PICMG® 1.3*.

SHB Configuration

The TKL8255 is a combo class SHB designed to support either PCI Express server-class or graphics-class backplane configurations. Server applications require multiple, high-bandwidth PCIe links, and therefore the server-class SHB/backplane configuration is identified by multiple x8 and x4 links to the SHB edge connectors.

SHBs which require high-end video or graphics cards generally use a x16 PCI Express link. The graphics-class SHB/backplane configuration is identified by one x16 PCIe link and one x4 link to the edge connectors. Previous generation PCIe video or graphics cards communicated to the SHB at an effective x1, x4 or x8 PCI Express data rate over the card's x16 PCIe mechanical connector and did not actually make use of all of the signal lanes in a x16 connector. The latest video and graphics cards make full use of the available x16 bandwidth by communicating to the SHB at the x16 PCIe data rate. An example of such a high-end x16 card is the Matrox Mura™ MPX video controller board.

NOTE: The TKL8255 eliminates the PICMG 1.3 requirement that server-class SHBs should always be used with server-class PICMG 1.3 backplanes and graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes. This is because of the PCIe links integrated into the TKL8255 processor, and the SHB architecture itself that can sense the backplane end-point devices and configure the SHB links for either server or graphics-class operations. For this reason, the Trenton TKL8255 is referred to as a combo-class SHB.

PCI Express Edge Connector Pin Assignments

Trenton's TKL8255 SHB uses edge connectors A, B, C and D. Optional I/O signals are defined in the PICMG 1.3 specification and if implemented must be located on edge connector C of the SHB. The SHB makes the Intelligent Platform Management Bus (IPMB) signals available to the user. The SHB supports four USB ports (USB 4, 5, 6 and 7) and one 10/100/1000Base-T Ethernet interface on PICMG 1.3 compatible backplanes via the SHB's edge connector C. Connector D offers a 32-bit/33MHz parallel interface for backplanes that provide the PICMG 1.3 optional D connector.

The following table shows pin assignments for the PCI Express edge connectors on the TKL8255 SHB.

* Pins 3 and 4 of Side B of Connector A (TDI and TDO) are jumpered together.

Connector A			Connector B			Connector C			Connector D		
	Side B	Side A		Side B	Side A		Side B	Side A		Side B	Side A
1	SMCLK	SMBDAT	1	+5VSBY	+5VSBY	1	USBP0+	GND	1	INTB#	INTA#
2	GND	GND	2	GND	NC	2	USBP0-	GND	2	INTD#	INTC#
3	TDI TDO*	NC	3	A_PE_TXP8	GND	3	GND	USBP1+	3	GND	NC
4	TDI TDO*	NC	4	A_PE_TXN8	GND	4	GND	USBP1-	4	REQ3#	GNT3#
5	NC	ICH WAKE#	5	GND	A_PE_RXP8	5	USBP2+	GND	5	REQ2#	GNT2#
6	PWRBTN#	ICH PCIPME#	6	GND	A_PE_RXN8	6	USBP2-	GND	6	PCIRST#	GNT1#
7	PWROK	PSON#	7	A_PE_TXP9	GND	7	GND	USBP3+	7	REQ1#	GNT0#
8	SHBRST#	EXP RESET#	8	A_PE_TXN9	GND	8	GND	USBP3-	8	REQ0#	SERR#
9	CFG0	CFG1	9	GND	A_PE_RXP9	9	USBOC0	GND	9	NC	3.3V
10	CFG2	CFG3	10	GND	A_PE_RXN9	10	GND	USBOC1	10	GND	CLKFI
11	NC	GND	11	RSVD	GND	11	USBOC2	GND	11	CLKFO	GND
Mechanical Connector			Mechanical Connector			Mechanical Connector			Mechanical Connector		
12	GND	RSVD	12	GND	RSVD	12	GND	USBOC3	12	CLKC	CLKD
13	B_PE_TXP0	GND	13	A_PE_TXP10	GND	13	NC	GND	13	GND	3.3V
14	B_PE_TXN0	GND	14	A_PE_TXN10	GND	14	NC	GND	14	CLKA	CLKB
15	GND	B_PE_RXP0	15	GND	A_PE_RXP10	15	GND	NC	15	3.3V	GND
16	GND	B_PE_RXN0	16	GND	A_PE_RXN10	16	GND	NC	16	AD31	PME#
17	B_PE_TXP1	GND	17	A_PE_TXP11	GND	17	NC	GND	17	AD29	3.3V
18	B_PE_TXN1	GND	18	A_PE_TXN11	GND	18	NC	GND	18	M6_6_EN	AD30
19	GND	B_PE_RXP1	19	GND	A_PE_RXP11	19	GND	NC	19	AD27	AD28
20	GND	B_PE_RXN1	20	GND	A_PE_RXN11	20	GND	NC	20	AD25	GND
21	B_PE_TXP2	GND	21	A_PE_TXP12	GND	21	A_MDI0P	GND	21	GND	AD26
22	B_PE_TXN2	GND	22	A_PE_TXN12	GND	22	A_MDI0N	GND	22	CBE3#	AD24
23	GND	B_PE_RXP2	23	GND	A_PE_RXP12	23	GND	A_MDI1P	23	AD23	3.3V
24	GND	B_PE_RXN2	24	GND	A_PE_RXN12	24	GND	A_MDI1N	24	GND	AD22
25	B_PE_TXP3	GND	25	A_PE_TXP13	GND	25	A_MDI2P	GND	25	AD21	AD20
26	B_PE_TXN3	GND	26	A_PE_TXN13	GND	26	A_MDI2N	GND	26	AD19	PCIXCAP
27	GND	B_PE_RXP3	27	GND	A_PE_RXP13	27	GND	A_MDI3P	27	+5V	AD18
28	GND	B_PE_RXN3	28	GND	A_PE_RXN13	28	NC	A_MDI3P	28	AD17	AD16
29	REFCLK0	GND	29	A_PE_TXP14	GND	29	IPMB_CLK	GND	29	CBE2#	GND
30	REFCLK0#	GND	30	A_PE_TXN14	GND	30	IPMB_DAT	GND	30	GND	FRAME#
31	GND	REFCLK1#	31	GND	A_PE_RXP14	31	NC	NC	31	IRDY#	TRDY#
32	RSVD-G	REFCLK1	32	GND	A_PE_RXN14	32	NC	NC	32	DEVSEL#	+5V

Connector A			Connector B			Connector C			Connector D		
	Side B	Side A		Side B	Side A		Side B	Side A		Side B	Side A
33	REFCLK2#	GND	33	A_PE_TXP15	GND	33	NC	NC	33	PLOCK#	STOP#
34	REFCLK2	GND	34	A_PE_TXN15	GND	34	NC	GND	34	PERR#	GND
35	GND	REFCLK3#	35	GND	A_PE_RXP15	35	NC	GND	35	GND	CBE1#
36	RSVD-G	REFCLK3	36	GND	A_PE_RXN15	36	GND	NC	36	PAR	AD14
37	REFCLK4#	GND	37	NC	GND	37	GND	NC	37	NC	GND
38	REFCLK4	GND	38	NC	NC	38	NC	GND	38	GND	AD12
39	GND	REFCLK5# PU	39	GND	GND	39	NC	GND	39	AD15	AD10
40	RSVD-G	REFCLK 5 PU	40	GND	GND	40	GND	NC	40	AD13	GND
41	REFCLK6# PU	GND	41	GND	GND	41	GND	NC	41	GND	AD9
42	REFCLK6 PU	GND	42	GND	GND	42	3.3V	3.3V	42	AD11	CBE0#
43	GND	REFCLK7# PU	43	GND	GND	43	3.3V	3.3V	43	AD8	GND
44	GND	REFCLK7 PU	44	+12V	+12V	44	3.3V	3.3V	44	GND	AD6
45	A_PE_TXP0	GND	45	+12V	+12V	45	3.3V	3.3V	45	AD7	AD5
46	A_PE_TXN0	GND	46	+12V	+12V	46	3.3V	3.3V	46	AD4	GND
47	GND	A_PE_RXP0	47	+12V	+12V	47	3.3V	3.3V	47	GND	AD2
48	GND	A_PE_RXN0	48	+12V	+12V	48	3.3V	3.3V	48	AD3	AD1
49	A_PE_TXP1	GND	49	+12V	+12V	49	3.3V	3.3V	49	AD0	GND
50	A_PE_TXN1	GND				50	3.3V	3.3V			
51	GND	A_PE_RXP1				51	GND	GND			
52	GND	A_PE_RXN1				52	GND	GND			
53	A_PE_TXP2	GND				53	GND	GND			
54	A_PE_TXN2	GND				54	GND	GND			
55	GND	A_PE_RXP2				55	GND	GND			
56	GND	A_PE_RXN2				56	GND	GND			
57	A_PE_TXP3	GND				57	GND	GND			
58	A_PE_TXN3	GND				58	GND	GND			
59	GND	A_PE_RXP3				59	+5V	+5V			
60	GND	A_PE_RXN3				60	+5V	+5V			
61	A_PE_TXP4	GND				61	+5V	+5V			
62	A_PE_TXN4	GND				62	+5V	+5V			
63	GND	A_PE_RXP4				63	GND	GND			
64	GND	A_PE_RXN4				64	GND	GND			
65	A_PE_TXP5	GND				65	GND	GND			
66	A_PE_TXN5	GND				66	GND	GND			
67	GND	A_PE_RXP5				67	GND	GND			
68	GND	A_PE_RXN5				68	GND	GND			
69	A_PE_TXP6	GND				69	GND	GND			
70	A_PE_TXN6	GND				70	GND	GND			
71	GND	A_PE_RXP6				71	GND	GND			
72	GND	A_PE_RXN6				72	GND	GND			
73	A_PE_TXP7	GND				73	+12V_VRM	+12V_VRM			
74	A_PE_TXN7	GND				74	+12V_VRM	+12V_VRM			
75	GND	A_PE_RXP7				75	+12V_VRM	+12V_VRM			
76	GND	A_PE_RXN7				76	+12V_VRM	+12V_VRM			
77	NC	GND				77	+12V_VRM	+12V_VRM			
78	3.3V	3.3V				78	+12V_VRM	+12V_VRM			
79	3.3V	3.3V				79	+12V_VRM	+12V_VRM			
80	3.3V	3.3V				80	+12V_VRM	+12V_VRM			
81	3.3V	3.3V				81	+12V_VRM	+12V_VRM			
82	NC	NC				82	+12V_VRM	+12V_VRM			

PCI Express Signals Overview

The following table provides a description of the SHB slot signal groups on the PCI Express connectors.

Type	Signals	Description	Connector	Source
Global	GND, +5V, +3.3V, +12V	Power		Backplane
	PSON#	Optional ATX support	A	SHB
	PWRGD, PWRBT#, 5Vaux	Optional ATX support	A and B	Backplane
	TDI	Optional JTAG support	A	Backplane
	TDO	Optional JTAG support	A	SHB
	SMCLK, SMDAT	Optional SMBus support	A	SHB & Backplane
	IPMB_CL, IPMB_DA	Optional IPMB support	C	SHB & Backplane
	CFG[0:3]	PCIe configuration straps	A	Backplane
	SHB_RST#	Optional reset line	A	SHB
	RSVD	Reserved	A and B	
	RSVD-G	Reserved ground	A	Backplane
	WAKE#	Signal for link reactivation	A	Backplane
PCIe	a_PETp[0:15] a_PETn[0:15] a_PERp[0:15] a_PERn[0:15]	Point-to-point from SHB slot through the x16 PCIe connector (A) to the target device(s)	A and B	SHB & Backplane
	b_PETp[0:3] b_PETn[0:3] b_PERp[0:3] b_PERn[0:3]	Point-to-point from SHB slot through the x8 PCIe connector (B) to the target device(s)	A	SHB & Backplane
	REFCLK[0:7]+, REFCLK[0:7]-	Clock synchronization of PCIe expansion slots	A	SHB
	PERST#	PCIe fundamental reset	A	SHB & Backplane
PCI(-X)	AD[0:31], FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, C/BE[0:3], SDONE, SBO#, PAR	Bussed on SHB slot and expansion slots	D	SHB & Backplane
	GNT[0:3], REQ[0:3], CLKA, CLKB, CLKC, CLKD, CLKFO, CLKFI	Point-to-point from SHB slot to each expansion slot	D	SHB & Backplane
	INTA#, INTB#, INTC#, INTD#	Bussed (rotating) on SHB slot and expansion slots	D	Backplane
	M66EN, PCIXCAP	Bussed on SHB slot and expansion slots	D	Backplane
	PCI_PRST#	PCI(-X) present on backplane detect	D	Backplane
	PME#	Optional PCI wake-up event bussed on SHB and backplane expansion slots	A	Backplane
Misc. I/O	USB[0:3]P, USB[0:3]N, USBOC[0:3]#	Optional point-to-point from SHB Connector C to a destination USB device	C	SHB & Backplane
SATA	ESATATX(4:5)P, ESATATX(4:5)N, ESATARX(4:5)P, ESATARX(4:5)N,	Optional point-to-point from SHB Connector C to a destination SATA device Note: These optional SATA connections to the backplane are not available with the TKL8255.	C	SHB & Backplane
Ethernet	a_MDI(0:1)p, a_MDI(0:1)n	Optional point-to-point from SHB Connector C to a destination Ethernet device	C	SHB & Backplane

This page intentionally left blank

TKL8255 System Power Connections

Introduction

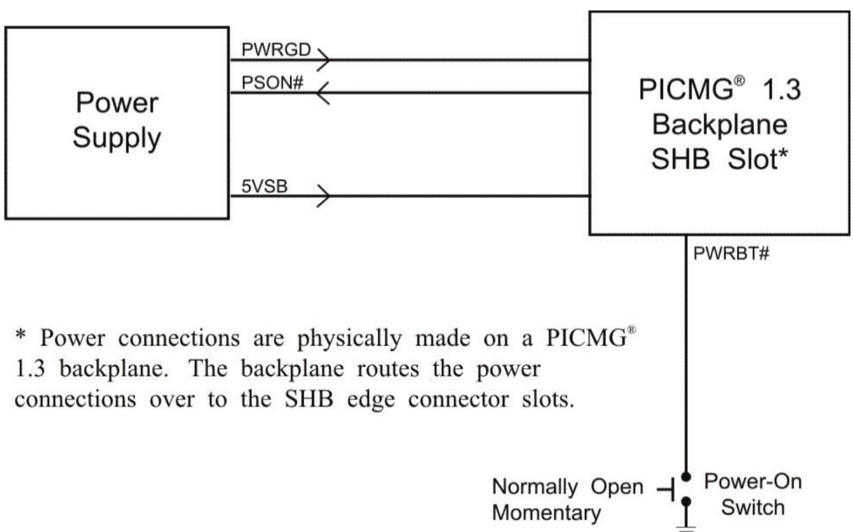
To improve system MTTR (Mean Time To Repair), the PICMG 1.3 specification defines enough power connections to the SHB's edge connectors to eliminate the need to connect auxiliary power to the SHB. All power connections in a PICMG 1.3 system can be made to the PICMG 1.3 backplane. This is true for SHBs that use high-performance processors. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive these high-performance SHBs. Trenton's PICMG 1.3 backplanes define ATX/EPS and +12V connectors that are compatible with ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in this manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

Power Supply and SHB Interaction

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.



PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

Electrical Connection Configurations

There are a number of different connector types, such as EPS, ATX or terminal blocks, which can be utilized in wiring power supply and control functions to a PICMG 1.3 backplane. However, there are only two basic electrical connection configurations: ACPI Connection and Legacy Non-ACPI Connection.

ACPI Connection

The diagram on the previous page shows how to connect an ACPI compliant power supply to an ACPI enabled PICMG 1.3 system. The following table shows the required connections that must be made for soft power control to work.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up.	Power Supply
PWRGD	Power Good. This signal indicates that the power supply's voltages are stable and within tolerance.	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply.	SHB/Backplane
PWRBT#	Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state. If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs.	Power Button

Legacy Non-ACPI Connection

For system integrators that either do not have or do not require an ACPI compliant power supply as described in the section above, an alternative electrical configuration is described in the table on the following page.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	Not Required	Power Supply
PWRGD	Not Required	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply. If an ATX or EPS power supply is used in this legacy configuration, a shunt must be installed on the backplane from PSON# to signal Ground. This forces the power supply DC outputs on whenever AC to the power supply is active.	Backplane
PWRBT#	Not Used	

In addition to these connections, there is usually a switch controlling AC power input to the power supply.

When using the legacy electrical configuration, the SHB BIOS Power Supply Shutoff setting should be set to Manual shutdown. Refer to the *General ACPI Configuration* section of the *Advanced Setup* chapter in this manual for details.

Windows Wake-On LAN Compatibility

The standard state that occurs when a system is “shutdown” from within Windows 8.1 or later is a, “hybrid shutdown state S4” which does not support Wake-On LAN (WOL) by default. WOL can be enabled on the TKL8255 running these operating systems by disabling this S4 state. To enable WOL:

1. In the Windows Control Panel, open the Power Options
2. Click “Choose what the power buttons do”
3. Clear the check box for “Turn on fast startup (recommended)”
4. Click ‘Save’ Settings
5. Select the i219 Ethernet Controller in the Windows Device Manager (Windows Key → “Device Manager” Enter →Double Click on the Controller)
    a. In the window that pops up, select the “Properties” tab.
    b. Ensure “Wake from Magic Packet in S5” is selected under Power Management & apply changes
6. Ensure WOL is enabled in the BIOS.

This page intentionally left blank

PCI Express Backplane Usage

SHB Edge Connectors and the Backplane SHB Slot

The PICMG® 1.3 specification enables SHB vendors to provide multiple PCI Express configuration options for edge connectors A and B of a particular SHB to support up to twenty (20) PCIe links. These edge connectors carry the twenty PCI Express links and reference clocks down to the SHB slot on the PICMG 1.3 backplane. The potential PCI Express link configurations of an SHB fall into three main classifications: server-class, graphics-class and combo-class. The specific class and PCI Express link configuration of an SHB is determined by the chipset components or Platform Controller Hub (PCH), and the processor(s) used on the board.

Server-class SHB configurations route as many high-bandwidth x8 and x4 PCI Express links as possible down to the backplane. Graphics-class configurations provide a x16 PCI Express link down to the backplane in order to support high-end PCI Express graphics and video cards plus one x4 PCIe link.

A combo-class configuration is provided by SHBs like the TKL8255. These system host board types have PCI Express hardware and software implementations that are capable of combining links to support either server or graphics-class PICMG 1.3 backplane configurations.

The A0, A2 and A3 PCI Express links on the TKL8255 connect from the processor to the backplane. The A0, A2 and A3 links out of the TKL8255 operate as either PCI Express 3.0, 2.0 or 1.1 links based on the end-point devices on the backplane. In addition to automatically configuring themselves for either PCIe 3.0, 2.0 or 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the two x4 links and the one x8 link from processor links A0, A2 and A3 can be combined into a single x16 PCIe electrical link or two x8 links on a backplane. The CPU’s A2 and A3 x4 links can operate as x4 links of the backplane or train down to x1 links; however, these links cannot bifurcate into multiple x1 links.

Note: The TKL8255’s processor only supports a x8, x4 and x4 PCIe Gen3 root link configuration. This means that A0 cannot bifurcate into two x4 links. An SHB-to-backplane link configuration of A0=x4, A1=x4, A3=x4 and A3=x4 is <u>not possible</u> in the single Skylake-S board architecture of the TKL8255.

The B0 PCIe link is from the board’s Platform Controller Hub (PCH) and this link operates as either a x4 PCIe 3.0, 2.0 or PCIe 1.1 interface.

PCI Express link configuration straps for each PCI Express option card slot on a PICMG 1.3 backplane are required as part of the PICMG 1.3 specification. These configuration straps alert the SHB as to the specific link configuration expected on each PCI Express option card slot. PCI Express communication between the SHB and option card slots is successful only when there are enough available PCI Express links established between the PICMG 1.3 SHB and each PCI Express slot or device on the backplane.

TKL8255 and Compatible Trenton Backplanes

Trenton Systems recommends the PICMG 1.3 backplanes noted in green in the table below for use with the TKL8255 PICMG 1.3 system host board. The SHB will also function with a wide variety of non-Trenton, industry standard PICMG 1.3 backplanes. However, some non-Trenton backplanes may not utilize the full capabilities of the Trenton TKL8255 SHB. The table below illustrates the TKL8255 compatibility with the current listing of Trenton PICMG 1.3 backplanes. A "Yes" in the compatible column below means that all slots on the backplane will function with a TKL8255 board. The clarification column explains any limitations of using a TKL8255 single processor SHB with a particular backplane. Visit our website to learn about the latest Trenton PICMG 1.3 backplane availability listings.

PICMG 1.3 Backplane	Compatible with TKL8255 (i.e. all backplane slots are functional)	Why not or clarification
2U Butterfly Backplanes		
BPC8219	Yes	All card slots operate at PCIe Gen2 speed
BPX8087	No	Multiple slots inactive due to no A1 link
Server-Class Backplanes		
BPX8093	No, the TKL8255 does not support the PEX10 for PCIe link expansion	PEX10 needed to provide the links for BP slots PCIe1 and PCIe3*
BPX6806+	Yes	The B0 links do not pass the Intel Gen3 margining test*
Graphics-Class Backplanes		
BPG8194	Yes	All slots operate at PCIe Gen3 speeds
BPG8155	Yes	All slots operate at PCIe Gen3 speeds*
BPG8150	No, the TKL8255 does not support the PEX10 for PCIe link expansion	PEX10 needed to provide the links for BP slots PCIe 1 and PCIe2
BPG8032	Yes	All slots operate at PCIe Gen2 speeds
BPG7087	Yes	

+Backplane does not have an SHB edge connector D slot. The backplane will function normally, but the system designer should ensure the exposed SHB edge connector D pins are protected from potential damage

*These backplanes successfully establish PCIe 3.0 links from the processor to the slots, however, the links are not fully within the Intel Margining Test Tolerances. These links may work at PCIe Gen3 or may train down to PCIe Gen2 in order to preserve link integrity, depending on the target card. Contact Trenton Systems for detailed PCIe link information or to discuss your particular application.

NOTE: Trenton SHBs that support the optional Ethernet routing to the card edge connectors support one backplane LAN interface. Some backplanes provide two optional LAN connectors as defined in the PICMG 1.3 specification, but *the second backplane LAN connector is not functional* with Trenton PICMG 1.3 system host boards.

This page intentionally left blank

This page intentionally left blank

BIOS Messages

Introduction

A status code is a data value used to indicate progress during the boot phase. These codes are outputted to I/O port 80h on the SHB. Aptio core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio core follows the firmware model dscribed by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers to the following "boot phases," which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization [1]
- Driver Execution Environment (DXE) – main hardware initialization [2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, etc.)

[1] Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality of legacy BIOS

BIOS Beep Codes

The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

BIOS Status Codes

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the TKL8255 SHB. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

The HEX to LED chart in the POST Code LEDs section will serve as a guide to interpreting specific BIOS status codes.

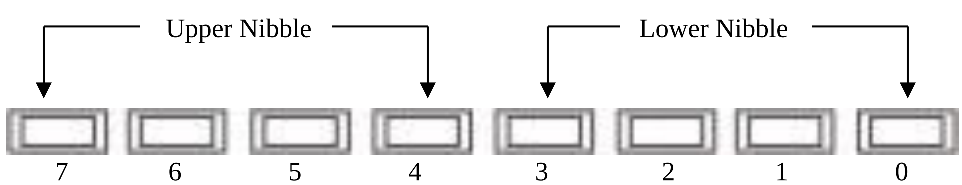
BIOS Status POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the TKL8255 SHB. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



TKL8255 POST Code LEDs
(Labeled 1 through 8 on Rev0 boards)

Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

There are no SEC Beep codes associated with this phase of the Aptio BIOS boot process.

PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization

0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes