Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your TSB7053 (7053-xxx) SHB. Overall system performance may be affected by incorrect usage of these features.

DDR3-1600 MEMORY*

Trenton recommends unbuffered ECC PC3-12800*, PC3-10600 or PC3-8500 DDR3 memory modules for use on the TSB7053. These unbuffered ECC registered (64-bit) DDR3 DIMMs must be PC3-12800, PC3-10600 or PC3-8500 compliant. Unbuffered non-ECC DDR3 DIMMs are also supported on the TSB7053 SHB, but you cannot mix the two different memory types on the same board.

NOTES:

- To maximize memory interface speed, populate each memory channel with DDR3 DIMMs having the same interface speed. The SHB will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- The SHB supports the following memory module memory latency timings:
  - 7-7-7 and 8-8-8 for 1066MHz DDR3 DIMMs
  - 9-9-9 for 1333MHz DDR3 DIMMs
  - 11-11-11 for 1600MHz DDR3 DIMMs*
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the TSB7053 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

Population order*	CPU1
1	BK0A
2	BK1A
3	BK0B
4	BK1B

*Using a balanced memory population approach ensures maximum memory interface performance. A "balance approach" means using an equal number of DIMMs on the TSB7053 SHB whenever possible.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

SATA RAID OPERATION (WINDOWS O/S SETUP)

The Intel® C206 Platform Controller Hub (PCH) used on the SHB features Intel® Rapid Storage Technology (Intel® RST) and requires a driver called: Intel® RST F6. Intel® RST allows the PCH's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. To configure the SATA ports as RAID drives while taking advantage of the PCH's drive array management features you must first install the Intel® RST driver software if you are using a Windows XP 64 or the Windows 2003 Server family of operating systems. A link to the software is also located on Trenton's website by accessing the Downloads tab of the TSB7053 product detail page or the RAID Drivers section of the Technical Support page. Later operating systems such as Windows 7 or Windows Server 2008 R2 do not require Intel® RST F6 driver installation.

The Microsoft Windows .NET FrameWork 3.0 software framework includes libraries and other useful tools that allow the RST Rapid Storage Manager to install and function properly in reporting drive failure alerts correctly. Windows .NET Framework 3.0 or later may be required to support the latest revisions of the RST Rapid Storage Manager. Windows .NET Framework is already included with Windows 7 or Windows 2008 O/S installations but it does need to be enabled.

If you would like your system to immediately inform you of a failed drive in the RAID array then the "Hot Plug" setting on the Advanced/SATA TSB7053 BIOS screen needs to be ENABLED for each drive in the array. If this BIOS setting is DISABLED a drive failure notification alert may take several minutes or even longer if there is no hard drive activity on the RAID array.

MOUSE/KEYBOARD "Y" CABLE

Many of the legacy I/O connections that previously required an optional IOB33 board have been incorporated into the TSB7053 design. Unless you need the additional PCIe expansion link down to your backplane or a parallel printer or floppy port, you should not need an IOB33 in your TSB7053-based system. However, if you have an IOB33 I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation.

POWER CONNECTION

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The TSB7053 supports these signals, controlled by the ACPI and are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to - *Power Connection* section in the TSB manual to determine the method that will work with your specific system design.

PCI EXPRESS 2.0 LINKS AND PICMG® 1.3 BACKPLANES

The PCI Express® links A0 through A3 on the TSB7053 connect to PCI Express 2.0 repeaters and the repeaters connect directly to the processor. PCIe 2.0 repeaters are used to maximize signal integrity regardless of where an end-point device is located on a PICMG 1.3 backplane. The PCIe links can operate as either PCI Express 2.0 or PCI Express 1.1 links based on the end-point devices on the backplane that are connected to the SHB. In addition to automatically configuring themselves for either PCIe 2.0 or PCIe 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple PCIe links from the processor (links A0, A2 and A3) can be combined into a single x16 PCIe electrical link or a combination of one x8 and two x4 links on a backplane. The CPU's PCIe links may train down to x1 links, but cannot bifurcate into multiple x1 links. The PCIe link (B0) is also a PCIe 2.0 interface and comes from the board's PCH. Link B0 has a x4 default configuration and can automatically bifurcate into four, x1 PCIe links. Refer to the *PCI Express® Reference* and the *PCI Express Backplane Usage* chapters of the *TSB7053 Hardware Technical Reference* manual for more information.

PICMG 1.3 BACKPLANE CLASSIFICATION

The TSB7053 is a combo-class PICMG 1.3 system host board meaning that it can operate as either a Server or Graphics-Class SHB. The TSB7053 also supports the PICMG 1.3 optional SHB-to-backplane USB (4) and Gigabit Ethernet (1) interfaces. Both 3rd party industry standard PICMG 1.3 backplanes as well as a wide variety of Trenton backplanes are compatible with the TSB7053 including the Trenton BPG7087, BPC7009, BPX6610 and the BPG8032. Refer to the *PCI Express® Reference* and the *PCI Express Backplane Usage* chapters of the *TSB7053 Hardware Technical Reference* manual for more information.

DVI-D AND ANALOG VIDEO PORTS

The TSB7053 offers both a DVI-D and an analog video port. The digital DVI-D port is a vertical port mounted directly on the SHB. This port is useful in system designs that incorporate a flat panel LCD display directly into the system enclosure. The ports may run simultaneously; however, the specific dual monitor implementation is a function of the system's operating system and video driver parameters. If using a Windows O/S the Windows .Net Framework 3.5 or higher driver needs to be installed for the Intel HD Graphics Control Panel to function. Right clicking on the Desktop and choosing Graphics Properties allows access to the Intel HD Graphics Control Panel. This control panel enables a simplified set-up of dual video monitor applications.

INTEL® AMT 7.0 / INTEL® AMT 8.0*

Intel® AMT 7.0 / Intel® AMT 8.0 is supported on the TSB7053 and includes useful features for managing clients remotely. Windows .Net Framework 3.5 or higher must be installed to avoid AMT x.x "unknown device" errors.

BIOS

The TSB7053 features the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *TSB705 BIOS Technical Reference* manual.

FOR MORE INFORMATION

For more information, refer to the appropriate sections *TSB7053Hardware Technical Reference Manual*. The BIOS and hardware manuals are available under the **Downloads** tab on the TSB7053 web page.

**DDR3-1600 memory and Intel AMT 8.0 support require a 22nm Intel® Micro-architecture processor (i.e. Ivy Bridge)*