TSB7053

7053-xxx

No. 87-007056-000 Revision J

HARDWARE

TECHNICAL REFERENCE

Intel® Xeon® E3-1200 v2-series
Intel® Core™ i7-3770
Intel® Core™ i5-3550S
Intel® Core™ i3-3220
(Ivy Bridge)

Intel® Xeon® E3-1200-series
Intel® Core™ i7-2600
Intel® Core™ i5-2400
Intel® Core™ i3-2120
(Sandy Bridge)

Dual and Quad Core

PROCESSOR-BASED

SHB

WARRANTY

The following is an abbreviated version of Trenton Systems' warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at: www.trentonsystems.com/about-us/company-policies/.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Systems, Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Systems' discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Systems, Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Systems, Inc. Trenton Systems, Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Systems, Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Systems, Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Systems, Inc.

RETURN POLICY

A Return Material Authorization (RMA) number, obtained from Trenton Systems prior to return, must accompany products returned for repair. The customer must prepay freight on all returned items, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

Trenton Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton Systems for our complete service and repair policy.

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HANDLING PRECAUTIONS

WARNING: This product has components that may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD HANDLING PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your TSB7053 (7053-xxx) SHB. Overall system performance may be affected by incorrect usage of these features.

DDR3-1600 MEMORY*

Trenton recommends unbuffered ECC PC3-12800*, PC3-10600 or PC3-8500 DDR3 memory modules for use on the TSB7053. These unbuffered ECC registered (64-bit) DDR3 DIMMs must be PC3-12800, PC3-10600 or PC3-8500 compliant. Unbuffered non-ECC DDR3 DIMMs are also supported on the TSB7053 SHB, but you cannot mix the two different memory types on the same board.

NOTES:

- To maximize memory interface speed, populate each memory channel with DDR3 DIMMs having the same interface speed. The SHB will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- The SHB supports the following memory module memory latency timings:
  - 7-7-7 and 8-8-8 for 1066MHz DDR3 DIMMs
  - 9-9-9 for 1333MHz DDR3 DIMMs
  - 11-11-11 for 1600MHz DDR3 DIMMs*
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the TSB7053 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

Population order[#]	CPU1
1	BK0A
2	BK1A
3	BK0B
4	BK1B

[#]Using a balanced memory population approach ensures maximum memory interface performance. A "balance approach" means using an equal number of DIMMs on the TSB7053 SHB whenever possible.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

**DDR3-1600 memory support requires a 22nm Intel® Micro-architecture processor (i.e. Ivy Bridge)*

PCI EXPRESS 2.0 LINKS AND PICMG® 1.3 BACKPLANES

The PCI Express® links A0 through A3 on the TSB7053 connect to PCI Express 2.0 repeaters and the repeaters connect directly to the Sandy Bridge processor. PCIe 2.0 repeaters are used to maximize signal integrity regardless of where an end-point device is located on a PICMG 1.3 backplane. The PCIe links can operate as either PCI Express 2.0 or PCI Express 1.1 links based on the end-point devices on the backplane that are connected to the SHB. In addition to automatically configuring themselves for either PCIe 2.0 or PCIe 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple PCIe links from the processor (links A0, A2 and A3) can be combined into a single x16 PCIe electrical link or a combination of one x8 and two x4 links on a backplane. The CPU's PCIe links may train down to x1 links, but cannot bifurcate into multiple x1 links. The PCIe link (B0) is also a PCIe 2.0 interface and comes from the board's PCH. Link B0 has a x4 default configuration and can automatically bifurcate into four, x1 PCIe links. Refer to the *PCI Express® Reference* chapter and to *Chapter 4 - PCI Express Backplane Usage* of this manual for more information.

PICMG 1.3 Backplane Classification

The TSB7053 is a combo-class PICMG 1.3 system host board meaning that it can operate as either a Server or Graphics-Class SHB. The TSB7053 also supports the PICMG 1.3 optional SHB-to-backplane USB (4) and Gigabit Ethernet (1) interfaces. Both 3rd party industry standard PICMG 1.3 backplanes as well as a wide variety of Trenton backplanes are compatible with the TSB7053 including the Trenton BPG7087, BPC7009, BPX6610 and the BPG8032. See *Chapter 4, PCI Express Backplane Usage* for more details.

Power Connection

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The TSB7053 supports these signals, controlled by the ACPI and are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to - *Power Connection* section in the TSB manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

Mouse/Keyboard "Y" Cable

Many of the legacy I/O connections that previously required an optional IOB33 board have been incorporated into the TSB7053 design. Unless you need the additional PCIe expansion link down to your backplane or a parallel printer or floppy port, you should not need an IOB33 in your TSB7053-based system. However, if you have an IOB33 I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation.

SATA RAID Operation (Windows O/S Setup)

The Intel® C206 Platform Controller Hub (PCH) used on the SHB features Intel® Rapid Storage Technology (Intel® RST) and requires a driver called: Intel® RST F6. Intel® RST allows the PCH's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. To configure the SATA ports as RAID drives while taking advantage of the PCH's drive array management features you must first install the Intel® RST driver software if you are using a Windows XP or the Windows 2003 Server family of operating systems. A link to the software is also located on Trenton's website by accessing the Downloads tab of the TSB7053 product detail page or the RAID Drivers section of the Technical Support page. Later operating systems such as Windows 7 or Windows Server 2008 R2 do not require Intel® RST F6 driver installation.

The Microsoft Windows .NET FrameWork 3.0 software framework includes libraries and other useful tools that allow the RST Rapid Storage Manager to install and function properly in reporting drive failure alerts correctly. Windows .NET Framework 3.0 or later may be required to support the latest revisions of the RST Rapid Storage Manager. Windows .NET Framework is already included with Windows 7 or Windows 2008 O/S installations but it does need to be enabled.

If you would like your system to immediately inform you of a failed drive in the RAID array then the "Hot Plug" setting on the Advanced/SATA TSB7053 BIOS screen needs to be ENABLED for each drive in the array. If this BIOS setting is DISABLED a drive failure notification alert may take several minutes or even longer if there is no hard drive activity on the RAID array.

DVI-D and Analog Video Ports

The TSB7053 offers both a DVI-D and an analog video port. The digital DVI-D port is a vertical port mounted directly on the SHB. This port is useful in system designs that incorporate a flat panel LCD display directly into the system enclosure. The ports may run simultaneously; however, the specific dual monitor implementation is a function of the system's operating system and video driver parameters. If using a Windows O/S the Windows dotNetFrameWork 3.5 or higher driver needs to be installed for the Intel HD Graphics Control Panel to function. Right clicking on the Desktop and choosing Graphics Properties allows access to the Intel HD Graphics Control Panel. This control panel enables a simplified set-up of dual video monitor applications.

INTEL® AMT 7.0 / INTEL® AMT 8.0*

Intel® AMT 7.0 / Intel® AMT 8.0 is supported on the TSB7053 and includes useful features for managing clients remotely. Windows .Net Framework 3.5 or higher must be installed to avoid AMT x.x "unknown device" errors.

**Intel AMT 8.0 support requires a 22nm Intel® Micro-architecture processor (i.e. Ivy Bridge)*

BIOS

The TSB7053 features the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *TSB705 BIOS Technical Reference* manual.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections *TSB7053Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the TSB7053 web page.

Chapter 1 Specifications

Introduction

The TSB7053 is a combo-class, PICMG® 1.3 system host board featuring the choice of a long-life / embedded, 22nm (i.e. Ivy Bridge) Intel® Xeon® E3-1200 v2 Series, Intel® Core™ i7-3770, Intel® Core™ i5-3550S or Intel® Core™ i3-3220 processor. Sandy Bridge processors; or those processors with a 32nm micro-architecture are also supported and these long-life processor options include the Intel® Core™ i3-3220, Intel® Xeon® E3-1200 Series, Intel® Core™ i7-2700, Intel® Core™ i5-2400 or Intel® Core™ i3-2120. The processors with the 22nm micro-architecture have a DDR3-1600 integrated memory controller that supports two, dual-channel DDR3-1600 memory interfaces while the 32nm processors support two, dual-channel DDR3-1333 memory interfaces. The TSB7053 supports four DDR3 DIMM sockets. With 4GB, DDR3 DIMMs the total system memory capacity for a TSB7053 is 16GB and doubles to 32GB using 8GB DDR3 DIMMs.

PCI Express 2.0 links form the off-board interfaces on the TSB7053's edge connectors with the exception of the PCIe 1.1 B0 link from the board's Intel® C206 Platform Controller Hub or PCH. PCIe 2.0 link repeaters are utilized in the SHB design for the PCI Express links routed from the board's processor. Even though the 22nm processor options feature PCIe 3.0 links, these links are designed to be secure PCIe 2.0 links on the board's edge connectors by virtue of these particular PCIe Gen2 link repeaters. The TSB7053 supplies the twenty PCI Express interface links needed for a PICMG 1.3 compliant server or graphics-class backplane plus an additional x4 PCI Express 2.0 interface for use on selected PICMG 1.3 backplanes via an optional plug-in card called the Trenton IOB33 module. All TSB7053 links support auto-negotiation with automatic link training and may also operate as PCI Express 1.1 electrical interfaces. This SHB design also supports the PICMG 1.3 optional PCI 32-bit/33MHz serial interface on edge connector D.

Video and I/O features on the TSB boards include:

- Dual video ports (one DVI-D and one VGA analog) that are driven with the internal Graphics Processing Unit inside the PCH
- PCIe Mini-Connector supports industry standard PCI Express Mini Cards
- Three Gigabit Ethernet interfaces with two on the I/O plate and one available for use on a PICMG 1.3 compliant backplane or over a cable for Intel® AMT 7.0 or 8.0 support
- Six SATA/300 ports that can support independent drives or RAID drive arrays
- Eight USB 2.0 interfaces
- An RS232 high-speed serial port and a configurable RS232/422/485 serial interface port
- PS/2 Mouse and Keyboard Header
- Integrated TPM 1.2 for Trusted Computing applications

The listing below summarizes the available versions of the TSB7053 system host board.

22nm, Long-Life Embedded Processor Models (Ivy Bridge)

Model #	Model Name	Speed	Intel CPU Number
Intel Xeon Processor (Ivy Bridge - AS) - Quad Core, 8MB cache, H-T, VT, TXT*:			
7053-135	TSB/3.5HQY8	3.5GHz	E3-1275 v2
	* H-T = Intel Hyper-Threading, VT = Intel Virtualization Technology, TXT = Intel Trusted Execution Technology		
Intel Xeon Processor (Ivy Bridge - AS) - Quad Core, 8MB cache, VT, TXT:			
7053-143	TSB/3.2HQY8	3.2GHz	E3-1225 v2
Intel Core i7 Processor (Ivy Bridge - DT) - Quad Core, 8MB cache, H-T, VT, TXT:			
7053-104	TSB/3.4QYR8	3.4GHz	Core i7-3770
Intel Core i5 Processor (Ivy Bridge - DT) - Quad Core, 6MB cache, VT, TXT:			
7053-112	TSB/3.0QY6	3.0GHz	Core i5-3550S
Intel Core i3 Processor (Ivy Bridge - DT) - Dual Core, 3MB cache, H-T, VT:			
7053-122	TSB/3.3DYR3	3.3GHz	Core i3-3220

32nm, Long-Life Embedded Processor Models (Sandy Bridge)

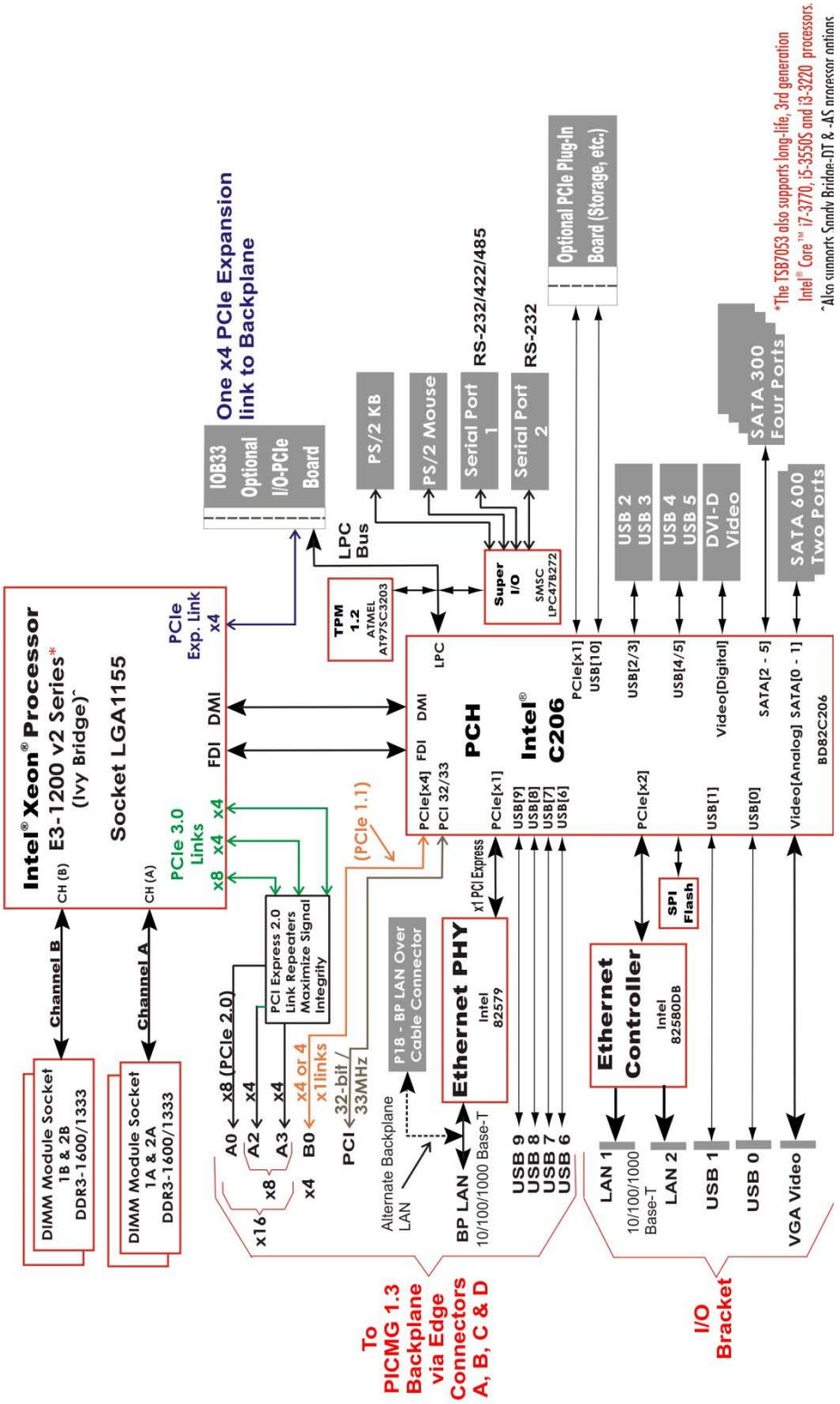
Model #	Model Name	Speed	Intel CPU Number
Intel Xeon Processor (Sandy Bridge - AS) - Quad Core, 8MB cache, H-T, VT, TXT*:			
7053-034	TSB/3.4HRVT8	3.4GHz	E3-1275
	* H-T = Intel Hyper-Threading, VT = Intel Virtualization Technology, TXT = Intel Trusted Execution Technology		
Intel Xeon Processor (Sandy Bridge - AS) - Quad Core, 6MB cache, VT, TXT:			
7053-042	TSB/3.1HRVT6	3.1GHz	E3-1225
Intel Core i7 Processor (Sandy Bridge - DT) - Quad Core, 8MB cache, H-T, VT, TXT:			
7053-004	TSB/3.4QRVT8	3.4GHz	Core i7-2600
Intel Core i5 Processor (Sandy Bridge - DT) - Quad Core, 6MB cache, VT, TXT:			
7053-012	TSB/3.1QVT6	3.1GHz	Core i5-2400
Intel Core i3 Processor (Sandy Bridge - DT) - Dual Core, 3MB cache, H-T, VT:			
7053-022	TSB/3.3DRV3	3.3GHz	Core i3-2120

Other non-embedded 22nm and 32nm processors options are available for use on the TSB7053 system host board.

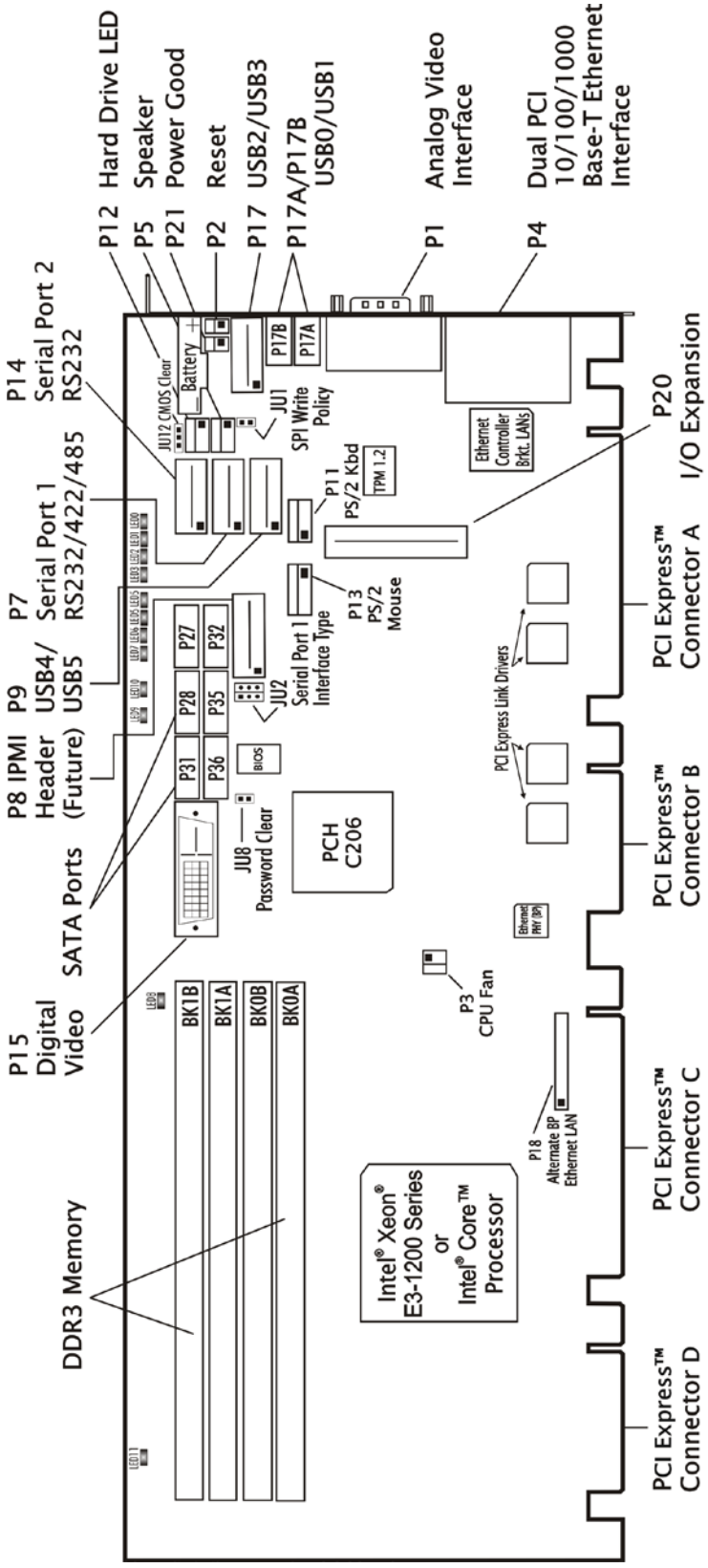
Features

- Intel® Xeon® E3-1200 v2 Series Processors (Ivy Bridge – Advanced Server [AS])
- Intel® Core™ i7-3770, Intel® Core™ i5-3550S & Intel® Core™ i3-3220 Processors (Ivy Bridge – Desktop [DT])
- Intel® C206 Platform Controller Hub (Cougar Point)
- Direct PCI Express® links from the processor to the board's edge connectors
- A Combo-class SHB that is compatible with PCI Industrial Computer Manufacturers Group (PICMG) 1.3 Specification
- TSB7053 provides a total of 24 lanes of PCI Express for off-board system integration
- Direct DDR3-1600 Memory Interfaces into the Ivy Bridge Processor
- Four DDR3 DIMM sockets capable of supporting up to 32GB of system memory with 8GB DDR3 DIMMs and 16GB maximum capacity with readily available 4GB DDR3 DIMMs
- Dual Digital and Analog video interfaces utilizing Intel® HD Graphics P3000 or Intel® HD Graphics 2000 (Xeon E3-1275 or 1225 uses Intel® HD Graphics P3000 all other CPU options is Intel® HD Graphics 2000)
- WiFi, SSD on-board storage and other additional video and I/O on-board capabilities are supported with a PCIe mini-connector supporting industry standard PCI Express Mini Cards
- Two 10/100/1000Base-T Ethernet interfaces available on the SHB's I/O plate
- Six Serial on-board ATA/300 ports support four independent SATA storage devices
    - SATA/300 ports may be configured to support RAID 0, 1, 5 or 10 implementations
- Eight Universal Serial Bus (USB 2.0) interfaces
- Off-board I/O support provided for one 10/100/1000Base-T Ethernet interface and four USB 2.0 port connections on a PICMG 1.3 backplane
- PS/2 mouse and keyboard headers, high-speed RS232 and RS232/422/RS485 serial ports
- An additional x4 PCI Express 2.0 lanes are available when using an Trenton IOB33 expansion board on the TSB7053 connected to a Trenton PICMG 1.3 backplane with an PCIe Expansion Slot
- Full-length stiffner bars on the rear of the SHB enhances the rugged nature on the board by maximizing component protection and simplifying mechanical system integration
- Full PC compatibility
- Revision controlled Aptio 4.x BIOS for American Megatrends, Inc. (AMI) resides in the SHB's SPI flash device to simplify field upgrades and BIOS customization
    - See the ***BIOS Setup Manual*** for TSB7053 System Host Board for more information

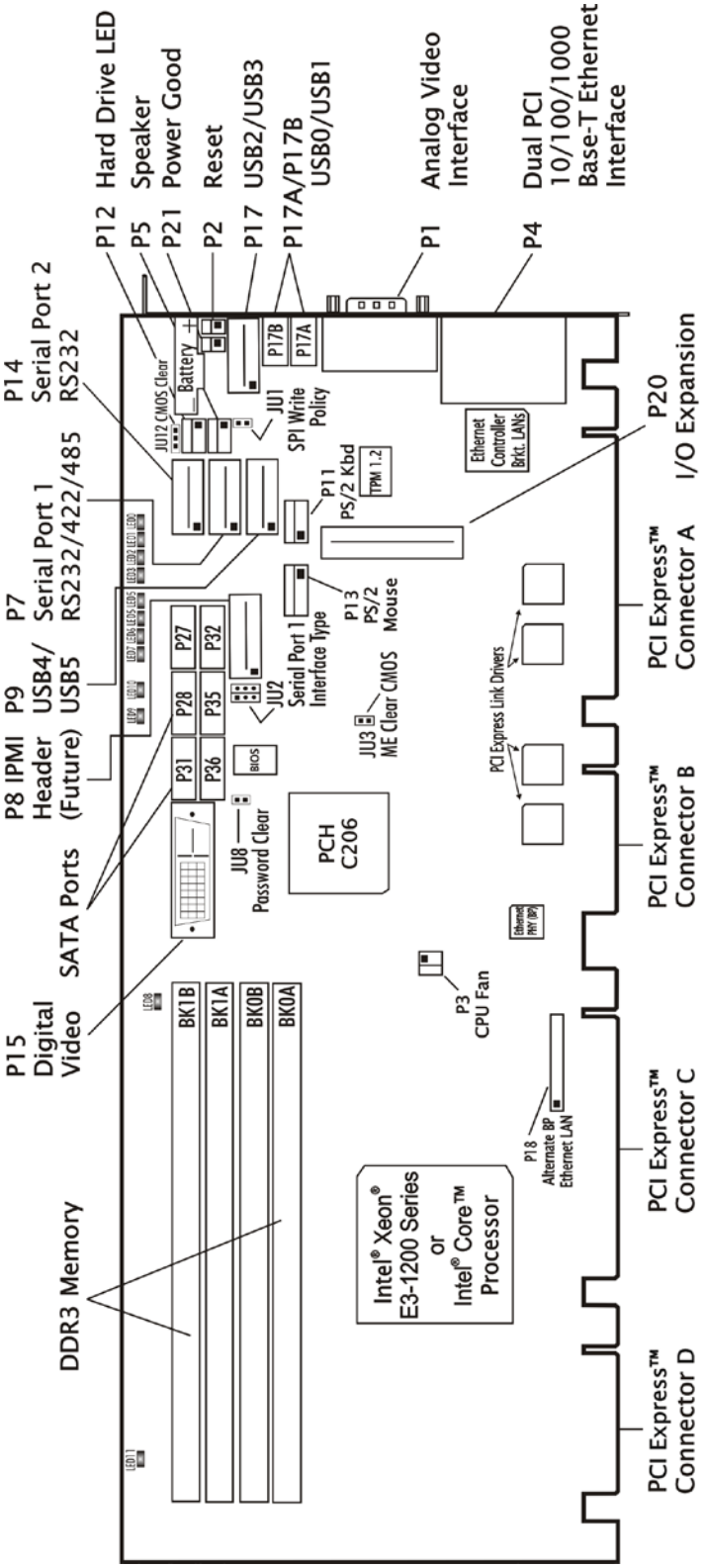
TSB7053 (7053-xxx) – Single-Processor SHB Block Diagram



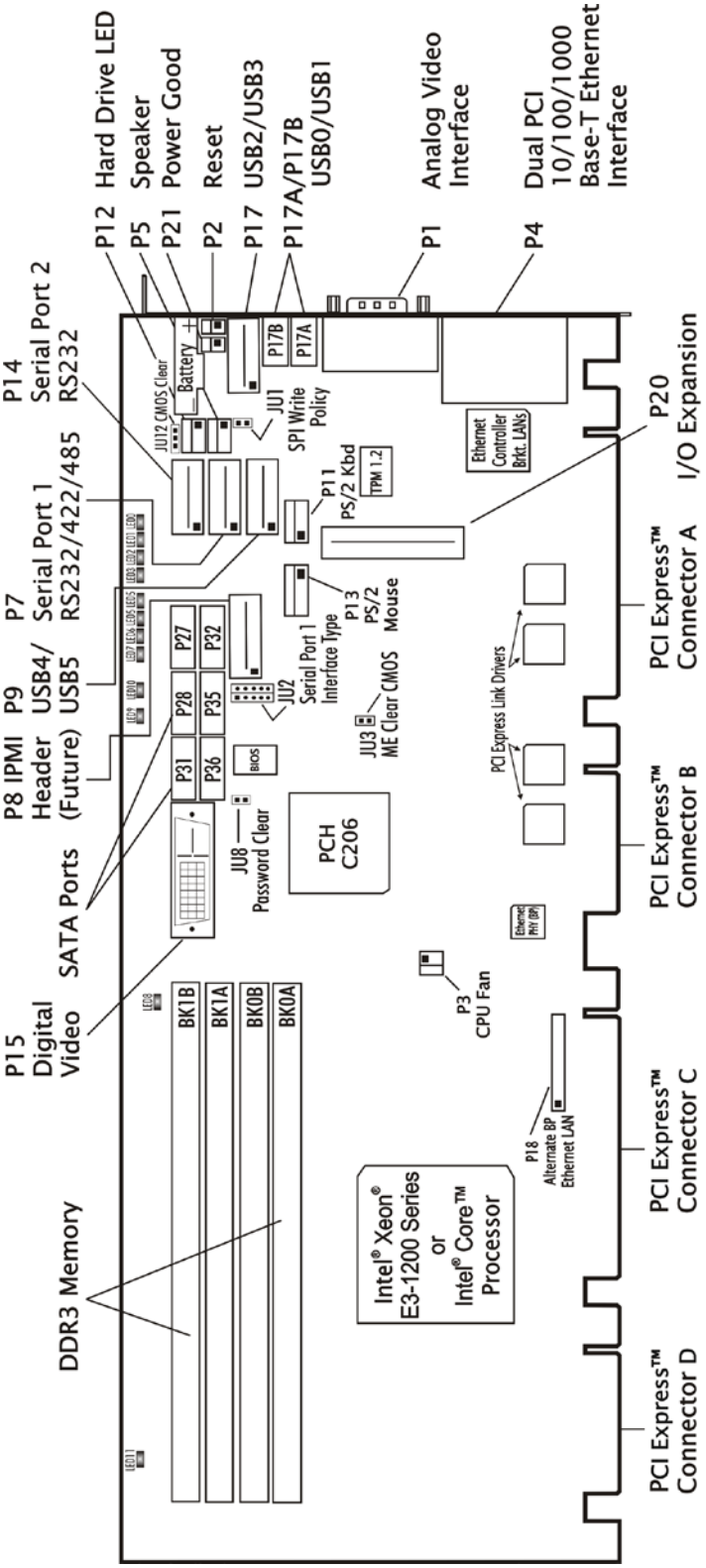
TSB7053 (7053-xxx) – Single-Processor SHB Layout Diagram – Revision –01 (Top)



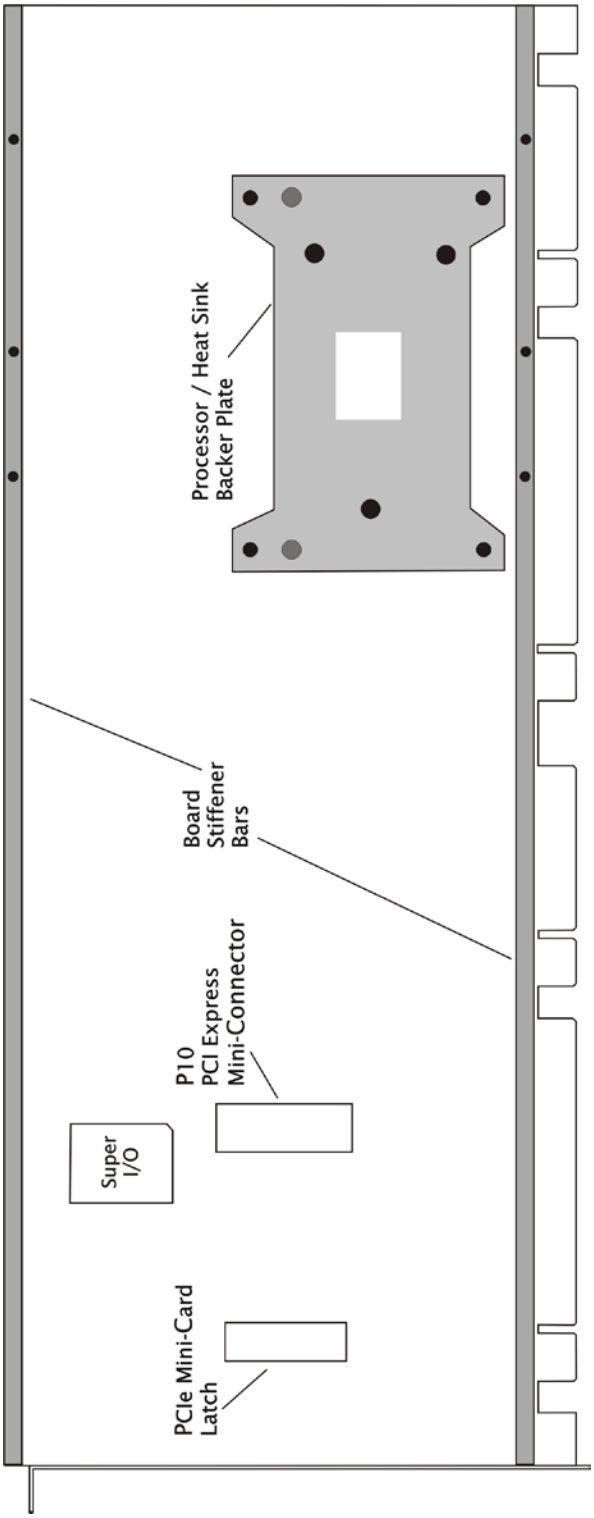
TSB7053 (7053-xxx) – Single-Processor SHB Layout Diagram – Revision –02 (Top)



TSB7053 (7053-xxx) – Single-Processor SHB Layout Diagram – Revision -03 and later (Top)



TSB7053 (7053-xxx) – Single-Processor SHB Layout Diagram (Bottom)



Processor

- Intel® Xeon® E3-1200 v2 Series Processor – Long-life 22nm/Ivy Bridge Advanced Server processor or the long-life 22nm / Ivy Bridge Desktop versions including the Intel® Core™ i7-3770, Intel® Core™ i5-3550S and Intel® Core™ i3-3220 processor
- Intel® Xeon® E3-1200 Series Processor – Long-life 32nm/Sandy Bridge Advanced Server processor or the long-life 32nm/Sandy Bridge Desktop versions including the Intel® Core™ i7-2600, Intel® Core™ i5-2400 and Intel® Core™ i3-2120 processor
- Processor plugs into an LGA1155 socket

Supported Intel® Processor Technologies

There are a wide variety of Intel® technologies supported on the TSB7053 system host board:

- **Intel® Advanced Management Technology 7.0 or 8.0 (Intel® AMT)** – Provides the ability to monitor, maintain, update, upgrade, and repair a system remotely using one of the SHB's available Ethernet interfaces. Intel AMT is part of the processor's Intel Management Engine and the processor must support Intel vPro technology in order to take full advantage of Intel AMT and a 22nm processor option is needed to support Intel AMT 8.0.
- **Intel® vPro** – Intel vPro is a combination of processor technologies, silicon hardware enhancements and management features that enable technologies like Intel AMT 7.0 to function.
- **Intel® Hyper-Threading (Intel® HT)** – This processor technology allows simultaneous multithreading of CPU tasks to enable parallel system operations. An operating system that is hyper-threading aware can address each core as a logical processor in order to spread out execution tasks to improve application software effeciency and overall system speed.
- **Intel Virtualization Technology (Intel® VT-x)** - Enabled in the SHB's BIOS, this technology enables multiple operating systems to run in specific Sandy Bridge processor cores thereby creating virtual machines (VMs) on a single SHB.
- **Intel Virtualization Technology for Directed I/O (Intel® VT-d)** – This is a sub-set of Intel VT-x and enables I/O device assignments to specific processor cores or VMs. Intel VT-d also supports DMA remapping, interrupt remapping and software DMA and interrupt status reporting. Intel VT-d is an optional extension to the Intel VT-x technology
- **Intel Trusted Execution Technology (Intel® TXT)** – This processor feature works in conjunction with the SHB's on-board Trusted Platform Module or TPM to allow the system designer to create multiple and separated execution environments or partitions with multiple levels of protection and security. The TPM provides for a way to generate and store an encrypted access key for authenticated access to sensitive applications and data. This private key never leaves the TPM, is generally available only to authorized system administrators, and enables remote assurance of a system's security state.
- **Intel Turbo Boost Technology 2.0** – The higher performance Sandy Bridge processors may run above the processors stated clock speed via a new dynamic processor speed control technology called Intel Turbo Boost 2.0. The processor enters the boost mode when the operating system requests the highest possible performance state as defined by the Advanced Configuration and Power Interface or ACPI.
- **Intel Advanced Vector Extensions (Intel® AVX)** – Several new Sandy Bridge micro-architecture instruction extensions that features a new CPU coding scheme that results in faster integer operations.

The following chart defines which Intel technology is supported on which particular embedded Sandy Bridge processor featured on the TSB7053 system host board.

Intel Technology	Intel Xeon E3-1275 v2	Intel Xeon E3-1225 v2	Intel Core i7-3770	Intel Core i5-3550S	Intel Core i3-3220	Intel Xeon E3-1275	Intel Xeon E3-1225	Intel Core i7-2600	Intel Core i5-2400	Intel Core i3-2120
Intel AMT 8.0	Yes	Yes	Yes	Yes	No	n/a	n/a	n/a	n/a	n/a
Intel AMT 7.0	n/a	n/a	n/a	n/a	n/a	Yes	Yes	Yes	Yes	No
Intel vPro	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No
Intel HT	Yes	No	Yes	No	Yes	Yes	No	Yes	No	Yes
Intel VT-x	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel VT-d	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No
Intel TXT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Intel Turbo Boost 2.0	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No
Intel AVX	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No
See the Intel ARK website for additional processor specification information.										

Serial Interconnect Interface

PCI Express® 2.0 and 1.1 compatible

Data Path

DDR3-1333 Memory - 64-bit (per channel), [22nm/Ivy Bridge processor options]
DDR3-1333 Memory - 64-bit (per channel), [32nm/Sandy Bridge processor options]

Serial Interconnect Speeds

PCI Express 2.0 – 5.0GHz per lane
PCI Express 1.1 - 2.5GHz per lane

Platform Controller Hub (PCH)

- Intel® C206 Platform Controller Hub (Cougar Point)

Intel® Direct Media Interface (DMI)

The Sandy Bridge processors support the latest interface version called DMI12. DMI12 uses a x4 PCI Express link to connect the processor to the Intel® C206 PCH

Intel® Flexible Display Interface (FDI) Between CPU and PCH

The FDI is a dedicated, two channel interconnect between the processor's display engine and the analog and digital video monitor interfaces connected to the Intel® C206 PCH. Each of the two FDI channels feature differential signaling supporting 2.7Gb/s video data transfers for both single and dual monitor applications.

Memory Interface*

The TSB7053 features two memory channels of unbuffered DDR3 with two DIMMs per channel. These DDR3-1600 memory interface channels support up to four, unbuffered, ECC PC3-12800 standard memory DIMMs. Non-ECC DDR3 DIMMs are also supported, but the two memory types cannot be used together on the SHB. The peak memory interface transfer rate per channel is 1600MT/s when using PC3-12800 DIMMs.

**Assumes a 22nm/Ivy Bridge processor option.*

DMA Channels

The SHB is fully PC compatible with seven DMA channels, each supporting type F transfers.

Interrupts

The SHB is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Bios (Flash)

The TSB7053 board uses an Aptio® 4.x BIOS from American Megatrends Inc. (AMI). The BIOS features built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. The BIOS resides in a 32Mb Atmel® AT25DF321SU SPI Serial EEPROM (SPI Flash). The BIOS may be upgraded from a USB thumb drive storage device by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the USB device installed in drive A:. Custom BIOSs are available.

Cache Memory

The processors include either a 3MB, 6MB or 8MB last-level cache (LLC) memory capacity that is equally shared between all of the processor cores on the die.

DDR3-1600 Memory*

The SHB supports two DDR3-1600 memory interface channels that can support two DIMMs each. The four active DIMM sockets on the TSB7053 models can support up to 8GB DIMMs for a total possible DDR3 system memory capacity of 32GB. However, the most common DDR3 DIMM memory capacities are 1GB, 2GB and 4GB. The system memory capacity limit when using 4GB DIMMS is 16GB. The peak memory interface transfer rate per channel is 1600MT/s when using PC3-12800 (i.e. DDR3-1600) DIMMs.

The System BIOS automatically detects memory type, size and speed. Trenton recommends unbuffered ECC PC3-12800*, PC3-10600 or PC3-8500 DDR3 memory modules for use on the TSB7053. These unbuffered ECC registered (64-bit) DDR3 DIMMs must be PC3-12800, PC3-10600 or PC3-8500 compliant. Unbuffered non-ECC DDR3 DIMMs are also supported on the TSB7053 SHB, but you cannot mix the two different memory types on the same board.

NOTES:

- To maximize memory interface speed, populate each memory channel with DDR3 DIMMs having the same interface speed. The SHB will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- All memory modules must have a 240-pin edge connector
- The SHB supports the following memory module memory latency timings:
  - 7-7-7 and 8-8-8 for 1066MHz DDR3 DIMMs
  - 9-9-9 for 1333MHz DDR3 DIMMs
  - 11-11-11 for 1600MHz DDR3 DIMMs*
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the TSB7053 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

Population order[#]	CPU1
1	BK0A
2	BK1A
3	BK0B
4	BK1B

[#]Using a balanced memory population approach ensures maximum memory interface performance. A “balance approach” means using an equal number of DIMMs on the TSB7053 SHB whenever possible.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board. The TSB7053 SHB versions feature one processor; however, memory slots BK10, BK11 and BK12 are installed on the SHB but are not active in this single-processor board version.

**DDR3-1600 memory support requires a 22nm Intel® Micro-architecture processor (i.e. Ivy Bridge*

Universal Serial Bus (USB)

The SHB supports eight high-speed USB 2.0 ports. Connectors for two of the USB ports (0 and 1) are on the I/O bracket and USB ports 2, 3, 4 and 5 are available via headers on the SHB. USB ports 6, 7, 8 and 9 are routed directly to edge connector C of the SHB for use on a PICMG 1.3 backplane.

Analog Video Interface

The Intel® Xeon® E3-1275 v2, Intel® Xeon® E3--1225 v2 and Intel® Core™ i7-3770 processors feature the Intel® HD Graphics P4000 core while the Intel® Core™ i5-3550S and Intel® Core™ i3-3220 support the Intel® HD Graphics 2500 graphics core.

The Intel® Xeon® E3-1275 and -1225 processors feature the Intel® HD Graphics P3000 core while the Core™ i7-2600, Core™ i5-2400 and Core™ i3-2120 processor options supported on the SHB feature the Intel® HD Graphics 2000 graphics core. A VGA monitor port connects to the SHB's Intel® C206 PCH and video data is routed to the processor via the first Intel® Flexible Display Interface.

Digital Video Interface

A DVI-D monitor port connects to the SHB's Intel® C206 PCH and is routed to the processor via the second Intel® Flexible Display Interface. Both display ports may be used simultaneously.

PCI Express Interfaces

PCI Express® links A0 through A3 on the TSB7053 connect to PCI Express 2.0 repeaters and the repeaters connect directly to the Sandy Bridge processor. PCIe 2.0 repeaters are used to maximize signal integrity regardless of where an end-point device is located on a PICMG 1.3 backplane. The PCIe links can operate as either PCI Express 2.0 or PCI Express 1.1 links based on the end-point devices on the backplane that are connected to the SHB. In addition to automatically configuring themselves for either PCIe 2.0 or PCIe 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple PCIe links from the processor (links A0, A2 and A3) can be combined into a single x16 PCIe electrical link or a combination of one x8 and two x4 links on a backplane. The CPU's PCIe links may train down to x1 links, but cannot bifurcate into multiple x1 links. The PCIe link (B0) is also a PCIe 2.0 interface and comes from the board's PCH. Link B0 has a x4 default configuration and can automatically bifurcate into four, x1 PCIe links. Refer to the *PCI Express® Reference* chapter and to *Appendix C - PCI Express Backplane Usage* of this manual for more information.

Serial ATA (SATA) Ports

The six Serial ATA (SATA) ports on the SHB are driven with a built-in SATA controller from the Intel® C206 Platform Controller Hub (PCH). All of the board's SATA interfaces comply with the SATA 1.0 and SATA 2.0 specifications that define support for data transfer rates of 150MB/s and 300 MB/s respectively. SATA port 0 (header connector P27) and SATA port 1 (P28) have the added capability of supporting data transfer rates up to 600MB/s from SATA 3.0 devices.

The SHB's SATA controller may support up to six independent SATA storage devices such as hard disks and CD-RW devices. The SATA controller has two BIOS selectable modes of operation with a legacy (i.e. IDE) mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

The board's PCH features support for Intel® Rapid Storage Technology (Intel® RST). This feature allows a third BIOS-selectable SATA controller configuration that enables a six drive RAID configuration capable of supporting RAID 0, 1, 5 and 10 storage array implementations.

SATA RAID Operation (Windows O/S Setup)

The Intel® C206 Platform Controller Hub (PCH) used on the SHB features Intel® Rapid Storage Technology (Intel® RST) and requires a driver called: Intel® RST F6. Intel® RST allows the PCH's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. To configure the SATA ports as RAID drives; while taking advantage of the PCH's drive array management features, you must first install the Intel® RST driver software if you are using a Windows XP 64 or the Windows 2003 Server family of operating systems. A link to the software is also located on Trenton's website by accessing the Downloads tab of the TSB7053 product detail page or the RAID Drivers section of the Technical Support page. Later operating systems such as Windows 7 or Windows Server 2008 R2 do not require Intel® RST F6 driver installation.

The Microsoft Windows .NET FrameWork 3.0 software framework includes libraries and other useful tools that allow the RST Rapid Storage Manager to install and function properly in reporting drive failure alerts correctly. Windows .NET Framework 3.0 or later may be required to support the latest revisions of the RST Rapid Storage Manager. Windows .NET Framework is already included with Windows 7 or Windows 2008 O/S installations but it does need to be enabled.

If you would like your system to immediately inform you of a failed drive in the RAID array then the "Hot Plug" setting on the Advanced/SATA TSB7053 BIOS screen needs to be ENABLED for each drive in the array. If this BIOS setting is DISABLED a drive failure notification alert may take several minutes or even longer if there is no hard drive activity on the RAID array.

Ethernet Interfaces

The TSB7053 supports three Ethernet interfaces. The first two interfaces are on-board 10/100/1000Base-T Ethernet interfaces located on the board's I/O bracket and implemented using an Intel® 82580DB Dual Gigabit Ethernet Controller. These I/O bracket interfaces support Gigabit, 10Base-T and 100Base-TX Fast Ethernet modes and are compliant with the IEEE 802.3 Specification.

The main components of the I/O bracket Ethernet interfaces are:

- Intel® 82580DB for 10/100/1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCIe interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connectors on the SHB's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

The third LAN is supported by the Intel® C206 and the Intel® 82579 Gigabit Ethernet PHY. This 10/100/1000Base-T Ethernet interface is routed to the PICMG 1.3 backplane via SHB edge connector C. The SHB includes an Ethernet connector (P18) that can be utilized to route this interface over an Ethernet cable rather than to the PICMG 1.3 backplane. This interface may be useful in Intel® AMT 7.0 system implementations.

Software drivers are supplied for most popular operating systems.

Watchdog Timer (WDT)

The TSB7053 provides a programmable watchdog timer with programmable timeout periods of 100 msec, 1 second, 10 seconds or 1 minute via board component U11. When enabled the WDT (i.e. U11) will generate a system reset. WDT control is supplied via the General Purpose IO pins from the Intel® C206 Platform Controller Hub (PCH). The PCH's GPIO_LVL2 register controls the state of each GPIO signal. This 32-bit register is located within GPIO IO spaces. The GPIO_BASE IO address is determined by the values programmed into the PCH's LPC Bridge PCI configuration at offset 48-4B(h).

GPIO Bit Definitions:

Watchdog Timer Enable (WDT_EN#)
Watchdog timer enable\disable functionality is controlled by GPIO32. Clearing bit 0 of the GP_LVL register enables the WDT. The GP_LVL2 register is located at IO address GPIO_BASE + offset 38(h). The power-on default for this bit is a "1" which disables WDT functionality. Setting this bit to a "0" enables the WDT at the pre-selected interval.

Watchdog Select 0 (WDT_S0)
The state of this bit in conjunction with Watchdog Select 0 will select the WDT time out period. This function is controlled by GPIO33 and the state of this bit is determined by bit 1 of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST, the inverted state of this bit is reflected on Port80, LED0. If this bit is set to a "1" the LED is off, if set to a "0" the LED is on. The state of the GPIO pin is inverted at the Select 0 input of U11. See the Watchdog Timeout Period Selection table below for WDT interval selection information.

Watchdog Select 1 (WDT_S1)
The state of this bit in conjunction with Watchdog Select 1 will select the WDT time out period. This function is controlled by GPIO34 and the state of this bit is determined by bit three of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST, the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on. The state of the GPIO pin is inverted at the Select 0 input of U11. See the Watchdog Timeout Period Selection table below for WDT interval selection information.

Watchdog_ Input (WDT_IN)
When the WDT is enabled this bit must be toggled (0 -> 1 or 1->0) within the selected watchdog timeout period, failure to do so will result in a system reset. This function is supported by the GPIO71 bit and its state is controlled by bit 23 of the GP_LVL3 register which is at IO address GPIO_BASE + offset 48(h). The inverted state of this bit is reflected on Port80, LED7. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on.

Watchdog Timeout Period Selections:

WDT_EN# (GPIO32)	WD_S1 (GPIO34)	WD_S0 (GPIO33)	Watchdog Timeout Period
1	X	X	Disabled
0	1	1	100msec
0	1	0	1 sec
0	0	1	10 sec
0	0	0	1 min

The Watchdog Timer may require initialization prior to usage. GPIO 32, 33, 34 and 71 must be configured as outputs. While these GPIOs do default to outputs at power-on, care should be taken to insure they have not been altered prior to WDT usage. These GPIO are configured to outputs by clearing bits 0, 1 and 2 of the GP_IO_SEL2 register at GPIO_BASE + offset 34(h) to a "0", as well as clearing bit 7 of the GP_IO_SEL3 register at GPIO_BASE + offset 44(h) to a "0".

After initialization is completed (if required) the Watchdog timer period is selected by via the WDT_S1 and WDT_S0 bits. Once the timeout period has been programmed the WDT is "enabled" by clearing the WDT_EN# bit. To avoid the WDT from generating a system reset the WDT_IN bit must be toggled within the timeout period.

Programming Example: Enable WDT with 10-second timeout period

Note: *When writing to any of the WDT controlling GPIO bit the remaining bits of the selected GP_LVL2 and GP_LVL3 registers should remain unchanged.*

Write bit 0 of GP_LVL2 to 1	pre condition GPIO32 for WDT disable
Write bits 2,1 of GP_LVL2 to 0,1	set Watchdog timeout period to 10 sec
Write bit 0 of GP_LVL2 to 0	enable Watchdog timer

At this point, the bit 7 of GP_LVL3 (GPIO71) must be toggled within a 10 sec period or the WDT will expire resulting in a system reset.

Power Requirements

The following power requirements table reflects nominal lab test values that were produced when 16GB of system memory were installed in the board installed.

Processor Type	SHB Type	Processor Speed	+5V	+12V	+3.3V
CPU Idle State:					
Intel Xeon E3-1275 v2	TSB7053	3.5GHz	0.70A	2.75A	3.64A
Intel Xeon E3-1275	TSB7053	3.4GHz	0.7A	1.54A	2.79A
Intel Xeon E3-1225 v2	TSB7053	3.2GHz	0.73A	2.42A	3.65A
Intel Xeon E3-1225	TSB7053	3.1GHz	0.67A	1.54A	2.77A
Intel Xeon E3-1260L	TSB7053	2.4GHz	0.67A	1.51A	2.78A
Intel Core i7-3770	TSB7053	3.4GHz	0.71A	2.34A	3.63A
Intel Core i7-2600	TSB7053	3.4GHz	0.72A	1.56A	2.81A
Intel Core i5-3550S	TSB7053	3.0GHz	0.76A	2.00A	3.55A
Intel Core i5-2400	TSB7053	3.1GHz	0.73A	1.56A	2.81A
Intel Core i3-3220	TSB7053	3.3GHz	0.78A	1.64A	3.51A
Intel Xeon i3-2120 [D]	TSB7053	3.3GHz	0.71A	1.36A	2.68A
100% CPU Stress State:					
Intel Xeon E3-1275 v2	TSB7053	3.5GHz	0.91A	6.95A	3.75A
Intel Xeon E3-1275	TSB7053	3.4GHz	0.78A	5.68A	2.92A
Intel Xeon E3-1225 v2	TSB7053	3.2GHz	0.83A	5.58A	3.73A
Intel Xeon E3-1225	TSB7053	3.1GHz	0.75A	5.24A	2.89A
Intel Xeon E3-1260L	TSB7053	2.4GHz	0.75A	3.93A	2.89A
Intel Core i7-3770	TSB7053	3.4GHz	0.93A	6.39A	3.75A
Intel Core i7-2600	TSB7053	3.4GHz	0.81A	5.85A	2.94A
Intel Core i5-3550S	TSB7053	3.0GHz	0.90A	4.90A	3.75A
Intel Core i5-2400	TSB7053	3.1GHz	0.81A	5.08A	2.91A
Intel Core i3-3220	TSB7053	3.3GHz	0.93A	3.82A	3.67A
Intel Xeon i3-2120[D]	TSB7053	3.3GHz	0.79A	3.44A	2.77A

Shaded boxes are 22nm/Ivy Bridge processor options
Non-shaded boxes are 32nm/Sandy Bridge processor options
Tolerance for all voltages is +/- 5%
[D]Dual-core processor, all other processors are quad-core CPUs

CAUTION: Trenton recommends an EPS type of power supply for systems using high-performance processors. The power needs of backplane option cards, high-performance processors and other system components may result in drawing 20A of current from the +12V power supply line. If this occurs, hazardous energy (240VA) could exist inside the system chassis. Final system/equipment suppliers must provide protection to service personnel from these potentially hazardous energy levels.

Stand-by voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

Power Fail Detection

A hardware reset is issued when any of the voltages being monitored drops below its specified nominal low voltage limit. The monitored voltages and their nominal low limits are listed below.

Monitored Voltage	Nominal Low Limit	Voltage Source
+5V	4.75 volts	System Power Supply
+3.3V	2.97 volts	System Power Supply
Vcc_DDR(+1.5V)	1.15 volts	On-Board Regulator
VCCIO_CPU(1.05V)	0.70 volt	On-Board Regulator
+1.05V(Chipset)	0.924 volt	On-Board Regulator
+1.05V(Chipset-ME)	0.924 volt	On-Board Regulator

Battery

A built-in lithium battery is provided for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the battery manufacturer. Dispose of used batteries according to the battery manufacturer's instructions.

Temperature/Environment

Operating Temperature: 0º C. to 50º C.

Air Flow Requirement: 350LFM continuous airflow

Storage Temperature: - 40º C. to 70º C.

Humidity: 5% to 90% non-condensing

Mechanical

The standard cooling solution used on the TSB7053 enables placement of option cards approximately 2.15" (54.61mm) away from the top component side of the SHB. Contact Trenton for a system engineering consultation if your application needs a lower profile cooling solution. The SHB's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

Board Stiffener Bars / Full-Length Backer Plate

The two stiffener bars located on the back of the most SHBs. Some TSB7053 boards utilize a full-length backer plate on the back of the board. These two mechanical features help to maximize system integrity by ensuring proper SHB alignment within the card guides of a computer chassis. These two product features provide reliable SHB operation by protecting sensitive board components from mechanical damage and assist in the safe insertion and removal of the SHB from the system.

Industry Certifications

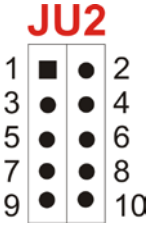
This SHB is designed to meet a variety of internationally recognized industry standards including UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996 and EN61000-4-11:1994.

See Appendix B for certificates of compliance documentation.

Configuration Jumpers

The setup of the configuration jumpers on the SHB is described below. * indicates the default value of each jumper.

NOTE: For the three-position JU12 jumper, "RIGHT" is toward the I/O bracket side of the board; "LEFT" is toward the header connector P14.

Jumper	Description
JU1	**SPI Update** (two position jumper) Install for one power-up cycle to enable the board to unprotect the SHB's SPI storage device. Remove for normal operation. * **CAUTION:** Installing this jumper is only done for special board operations such as changing the PCI Express link bifurcation operation. Contact Trenton tech support ***before*** installing this jumper to prevent any unintended system operation.
JU2 – rev. –01 & -02	**Serial Port 1 Interface Configuration, Board Revisions -01 and -02** JU2 uses three jumpers to allow serial port one to be configured as either a RS232 or a RS422/RS485 electrical interface. The jumper table below illustrates the possible interface configurations for serial port one.  RS232 operation* – Jumper 1 to 2 **and** 3 to 4 RS485 Full Duplex, No Termination – Jumper 1 to 2 RS485 Half Duplex, No Termination – No jumpers installed RS485 Full Duplex, With Termination – Jumper 1 to 2 **and** 5 to 6 RS485 Half Duplex, With Termination – Jumper 5 to 6
JU2 – rev. -03	**Serial Port 1 Interface Configuration, Board Revision –03 or later** JU2 uses five jumpers to allow serial port one to be configured as either a RS232 or a RS422/RS485 electrical interface. The jumper table below illustrates the possible interface configurations for serial port one.  RS232 operation* – Jumper 1 to 2 **and** 3 to 4 **and** 9 to 10 RS485 Full Duplex, No Termination – Jumper 1 to 2 **and** 9 to 10[1] RS485 Half Duplex, No Termination – Jumper 9 to 10 RS485 Full Duplex, With Termination – Jumper 1 to 2 **and** 5 to 6[2] RS485 Half Duplex, With Termination – Jumper 5 to 6 **and** 9 to 10 Notes: 1 – Shut between pins 9 and 10 can optionally be removed to unconditionally enable the Tx driver 2 – Shut between pins 9 and 10 can optionally be installed to unconditionally enable the Tx driver
JU3 – rev. -02 boards or later	**Clear Management Engine (ME) Operational Parameters** (two position jumper)**, Board Rev –02 or later** The board's management engine has its own CMOS Non-Volatile Memory (NVM) that stores operational parameters for Intel AMT 7.0 implementations. Install for one power-up cycle to clear management engine CMOS settings. Remove for normal operation. *

Configuration Jumpers (continued)

JU8 **Password Clear** (two position jumper)
Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

JU12 **CMOS Clear** (three position jumper)
Install on the LEFT to clear.
Install on the RIGHT to operate. *

NOTE: To clear the CMOS, power down the system and install the JU12 jumper on the LEFT. Wait for at least two seconds, move the jumper back to the RIGHT and turn the power on. Clearing CMOS on the TSB7053 will not result in a checksum error on the following boot. If you want to change a BIOS setting, you must press DEL or the F2 key during POST to enter BIOS setup after clearing CMOS.

P4A/P4B Ethernet LEDs and Connectors

The I/O bracket houses the two RJ-45 network connectors for Ethernet LAN1and LAN2. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

LED/Connector	Description
Activity LED	Green LED that indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets).
Off	Indicates there is no current network transmit or receive activity.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	This multi-color LED identifies the connection speed of the SHB's P4A (LAN2) and P4B (LAN1) Ethernet interfaces. These are the lower LEDs on the dual LAN connector (i.e., toward the edge connectors).
Green	Indicates a valid link at 1000-Mb/s or 1Gb/s.
Orange	Indicates a valid link at 100-Mb/s.
Off	Indicates a valid link at 10-Mb/s.
RJ-45 Network Connector	The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection

Status LEDs

Backplane LAN LED – LED8

LED8 is located just above the right side of memory DIMM connector BK1B. A flashing LED8 indicates that network transmit and receive activity is occurring on the Ethernet LAN routed to the board's edge connector C / cable connector P18. This LAN provides a network interface for use on a compatible PICMG 1.3 backplane or over an Ethernet cable connecter to P18.

Thermal Trip LED – LED9
The thermal trip LED indicates when a processor reaches a shut down state. The LED is located just above the BK02 DIMM socket. LED9 indicates the processor shutdown status and thermal conditions as illustrated below:

LED Status	Description
Off	Indicates the processor or processors are operating within acceptable thermal levels
On (flashing)	Indicates the CPU is throttling down to a lower operating speed due to rising CPU temperature
On (solid)	Indicates the CPU has reached the thermal shutdown threshold limit. The SHB may or may not be operating, but a thermal shutdown may soon occur.

NOTE: When a thermal shutdown occurs, the LED will stay on in systems using non- ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the SHB. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all SHB LEDs will turn off; however, stand-by power will still be present.

PCIe Mini Card WLAN LED – LED10
When LED10, located just to the right of LED9, is flashing this indicates that network transmit and receive activity is occurring on an Ethernet LAN that is located on an optional PCIe Mini Card connected to the TSB7053's Mini PCIe Expansion connector P10. P10 is located on the bottom side of the SHB.

VRM LED – LED11
LED11 is a red LED located just above the left side of memory DIMM connector BK1B. If LED11 were to turn on and remain on, this would indicate that the voltage levels of the SHB's VRM circuits are not within the acceptable operating range. In all likelihood the SHB will fail to function if LED11 is on and the source of the voltage error could reside in the system power supply, the power supply wiring or on the board itself. Contact your system integrator or Trenton Tech Support for trouble shooting assistance.

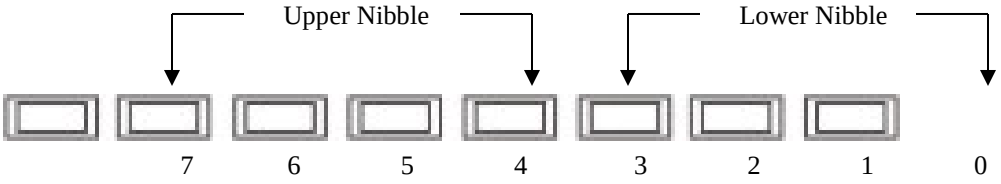
Post Code LEDs 0 – 7

As the POST, (Power On Self Test) routines are performed during boot-up; test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7). Refer to the board layout diagram for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. After a normal POST sequence the LEDs are off (00h) indicating that the SHB's BIOS has passed control over to the operating system loader typically at interrupt INT19h. Specific test codes and their meaning along with the following chart are listed in Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



TSB7053 POST Code LEDs

System BIOS Setup Utility

The TSB7053 features the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. The TSE setup utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details of the Aptio TSE are provided in the separate *TSB7053BIOS Technical Reference* manual. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the TSB7053 web page.

Connectors

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - **Analog Video Interface Connector**
15 position socket connector, Amp/TYCO 1-1734530-3

Pin	Signal	Pin	Signal	Pin	Signal
1	Red	6	Gnd	11	NC
2	Green	7	Gnd	12	EEDI
3	Blue	8	Gnd	13	HSYNC
4	NC	9	+5	14	VSYNC
5	Gnd	10	Gnd	15	EECS

Note: Connector supports standard DB15 analog video cables

P2 - **Reset Connector**
2 pin single row header, Amp #640456-2

Pin	Signal	Pin	Signal
1	Gnd	2	Reset In

P3 - **CPU Fan Power Connector**
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

Note: P2 is the fan connector of CPU2 and P19 is for CPU1

P4A, P4B - **10/100/1000Base-T Ethernet Connectors - LAN1/LAN2**
Dual RJ-45 connector, Pulse #JG0-0024NL
Each individual RJ-45 connector is defined as follows:

Pin	Signal	Pin	Signal
1A	L2_MDI0n	1B	L1_MDI0n
2A	L2_MDI0p	2B	L1_MDI0p
3A	L2_MDI1n	3B	L1_MDI1n
4A	L2_MDI1p	4B	L1_MDI1p
5A	L2_MDI2n	5B	L1_MDI2n
6A	L2_MDI2p	6B	L1_MDI2p
7A	L2_MDI3n	7B	L1_MDI3n
8A	L2_MDI3p	8B	L1_MDI3p
9A	VCC_1.8V	9B	VCC_1.8V
10A	GND_A	10B	GND_b

Notes:
1 - LAN ports support standard CAT5 Ethernet cables
2 – P4A is LAN2 and P4B is LAN1

Connectors (Continued)

P5 - Speaker Port Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	Speaker Data
2	Key
3	Gnd
4	+5V

P7 - Serial Port 1 Connector – RS232 Signal Connections*
10 pin dual row header, Amp #5103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Gnd	10	NC

* See JU2 pin-outs listed in the Configuration Jumper section of this manual to enable serial port 1 signal connections.

P7 - Serial Port 1 Connector – RS422/485 Full Duplex Signal Connections*
10 pin dual row header, Amp #5103308-1

Pin	Signal	Pin	Signal
1	Not applicable	2	Not applicable
3	RX+	4	TX+
5	TX-	6	RX-
7	Not applicable	8	Not applicable
9	Gnd	10	NC

* See JU2 pin-outs listed in the Configuration Jumper section of this manual to enable serial port 1 signal connections.

P7 - Serial Port 1 Connector – RS422/485 Half Duplex Signal Connections*
10 pin dual row header, Amp #5103308-1

Pin	Signal	Pin	Signal
1	Not applicable	2	Not applicable
3	Not applicable	4	DATA+
5	DATA-	6	Not applicable
7	Not applicable	8	Not applicable
9	Gnd	10	NC

* See JU2 pin-outs listed in the Configuration Jumper section of this manual to enable serial port 1 signal connections.

Connectors (Continued)

P9 - Dual Universal Serial Bus (USB) Connector

10 pin dual row header, Amp #1761610-3
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB4	2	+5V-USB5
3	USB4-	4	USB5-
5	USB4+	6	USB5+
7	Gnd-USB4	8	Gnd-USB5
9	NC	10	NC

P10 - PCI Express Mini Card Connector (SHB bottom side)

Standard 52-pin PCIe mini-card edge connector

Pin	Signal	Pin	Signal
1	PCH_WAKE#	2	VCC3_MINIPCIE
3	NC	4	GND
5	NC	6	VCC1_5_MINIPE
7	VCC_MINIPCIE	8	NC
9	GND	10	NC
11	MINIPCIE_CLK100N	12	NC
13	MINIPCIE_CLK100P	14	NC
15	GND	16	NC
17	NC	18	GND
19	NC	20	NC
21	GND	22	EXP_RESET#
23	MINI_PE_RXN0	24	3.3V AUX
25	MINI_PE_RXP0	26	GND
27	GND	28	VCC1_5_MINIPE
29	GND	30	SMBCLK_RESUME
31	MINI_PE_TXN0	32	SMBDAT_RESUME
33	MINI_PE_TXP0	34	GND
35	GND	36	USBP6-
37	NC	38	USBP6+
39	NC	40	GND
41	NC	42	NC
43	NC	44	WLAN_LED10
45	CLINK_CLK	46	NC
47	CLINK_DAT	48	VCC1_5_MINIPE
49	CLINK_RST#	50	GND
51	NC	52	VCC3_MINIPCIE

P11 - PS/2 Keyboard Header

5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	NC
4	Kbd Gnd
5	Kbd Power (+5V fused) with self resetting fuse

Connectors (Continued)

P12 - Hard Drive LED Connector

4 pin single row header, Amp #640456-4

Pin	Signal
1	LED+
2	LED-
3	LED-
4	LED+

P13 - PS/2 Mouse Header

6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	NC
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	NC

P14 - Serial Port 2 Connector – RS232 Signal Connections

10 pin dual row header, Amp #5103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Gnd	10	NC

P15 - Digital Video Interface Connector (DVI-D)

24 position socket digital video connector, Molex #74320-5006

Pin	Signal	Pin	Signal	Pin	Signal
1	DVI_TX2N	9	DVI_TX1N	17	DVI_TX0N
2	DVI_TX2P	10	DVI_TX1P	18	DVI_TX0P
3	Gnd	11	Gnd	19	Gnd
4	NC	12	NC	20	NC
5	NC	13	NC	21	NC
6	DVI_SCLK	14	5V	22	Gnd
7	DVI_SDAT	15	Gnd	23	DVI_TXCP
8	NC	16	DVI_HPD	24	DVI_TXCN

Note: Connector supports standard DVI-D digital video cables

Connectors (Continued)

P17 - Dual Universal Serial Bus (USB) Connector
10 pin dual row header, Amp #1761610-3
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3
9	NC	10	NC

P17A - Universal Serial Bus (USB) Connector
USB vertical connector, Molex #67329-8001
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB0
2	USB0-
3	USB0+
4	Gnd-USB0

P17B - Universal Serial Bus (USB) Connector
USB vertical connector, Molex #67329-8001
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB1
2	USB1-
3	USB1+
4	Gnd-USB1

P18 - 10/100/1000Base-T Ethernet Connector – Alternate Backplane LAN Over Cable
8 pin single row connector, Molex #0554500859

Pin	Signal
1	A_MDI2N
2	A_MDI2P
3	A_MDI3N
4	A_MDI3P
5	A_MDI1N
6	A_MDI1P
7	A_MDI0N
8	A_MDI0P

The mating Molex connector to use when making this alternative Ethernet cable has a Molex part number of 0513360810.

P21 - Power Good LED Connector
2 pin single row header, Amp #640456-2

Pin	Signal	Pin	Signal
1	LED-	2	LED+

Connectors (Continued)

P27, - **SATA Ports**
P28, 7 pin vertical locking connector, Molex #67800-8005
P31,
P32,
P35,
P36

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

Notes:
1 – P27 = SATA0 interface, P28 = SATA1 interface,
P31 = SATA2 interface, P32 = SATA3 interface,
P35 = SATA4 interface, P36 = SATA5 interface
2 – SATA connectors support standard SATA II interface cables
3 – P27 & P28 (SATA0 and SATA1 ports) support SATA 3.0, SATA 2.0 and SATA 1.0 devices while all other SATA ports support SATA 2.0 and 1.0 devices
4 – SATA 3.0 = 600MB/s data transfers, SATA 2.0 = 300MB/s data transfers and SATA 1.0 = 150MB/s data transfers

Connectors (Continued)

P20 - I/O Expansion Mezzanine Card Connector

76 pin controlled impedance connector, Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12	2	+5V_STANDBY
3	HDA_SDIN2	4	+5V_STANDBY
5	HDA_SDIN1	6	+5V_DUAL
7	HDA_SDIN0	8	+5V_DUAL
9	HDA_SYNC	10	HDA_BITCLK
11	HDA_SDOUT	12	HDA_ACRST
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SBMCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP5	48	C_PE_RXP5
49	C_PE_TXN5	50	C_PE_RXN5
51	Gnd	52	Gnd
53	NC	54	NC
55	NC	56	NC
57	Gnd	58	Gnd
59	NC	60	NC
61	NC	62	NC
63	Gnd	64	Gnd
65	NC	66	NC
67	NC	68	NC
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5V

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Chapter 2 PCI Express® Reference

Introduction

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

PCI Express Links

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion. A link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. In PCI Express Gen 1 the bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	250MB/s	500MB/s
x4	1GB/s	2GB/s
x8	2GB/s	4GB/s
x16	4GB/s	8GB/s

In PCI Express Gen 2 the bandwidths for the PCIe links are doubled as compared to PCIe Gen 1.1 as shown below:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	500MB/s	1GB/s
x4	2GB/s	4GB/s
x8	4GB/s	8GB/s
x16	8GB/s	16GB/s

Scalability is a core feature of PCI Express. Some chipsets allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. In addition, although a board with a higher number of lanes will not function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) because the connectors are mechanically and electrically incompatible, the reverse configuration will function. A board with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot). The link auto-negotiates between the PCI Express devices to establish communication. The mechanical option card slots on a PICMG 1.3 backplane must have PCI Express configuration straps that alert the SHB to the PCI Express electrical configuration expected. The SHB can then reconfigure the PCIe links for optimum system performance.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express® System Host Board PCI Express Specification, PICMG® 1.3*.

SHB Configuration

The TSB7053 is a combo class SHB designed to support either PCI Express server-class or graphics-class backplane configurations. Server applications require multiple, high-bandwidth PCIe links, and therefore the server-class SHB/backplane configuration is identified by multiple x8 and x4 links to the SHB edge connectors.

SHBs, which require high-end video or graphics cards generally, use a x16 PCI Express link. The graphics-class SHB/backplane configuration is identified by one x16 PCIe link and one x4 or four x1 links to the edge connectors. Previous generation PCIe video or graphics cards communicated to the SHB at an effective x1, x4 or x8 PCI Express data rate over the card's x16 PCIe mechanical connector and did not actually make use of all of the signal lanes in a x16 connector. The latest video and graphics cards make full use of the available x16 bandwidth by communicating to the SHB at the x16 PCIe data rate. An example of such a high-end x16 card is the Matrox Mura™ MPX video controller board

NOTE: The TSB7053 eliminates the PICMG 1.3 requirement that server-class SHBs should always be used with server-class PICMG 1.3 backplanes and graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes. This is because of the PCIe links integrated into the TSB processor, and the SHB architecture itself that can sense the backplane end-point devices and configure the SHB links for either server or graphics-class operations. For this reason, the Trenton TSB7053 is referred to as a combo-class SHB.

PCI Express Edge Connector Pin Assignments

Trenton's TSB7053 SHB uses edge connectors A, B, C and D. Optional I/O signals are defined in the PICMG 1.3 specification and if implemented must be located on edge connector C of the SHB. The SHB makes the Intelligent Platform Management Bus (IPMB) signals available to the user. The SHB supports four USB ports (USB 4, 5, 6 and 7) and one 10/100/1000Base-T Ethernet interface on PICMG 1.3 compatible backplanes via the SHB's edge connector C. Connector D offers a 32-bit/33MHz parallel interface for backplanes that provide the PICMG 1.3 optional D connector.

The following table shows pin assignments for the PCI Express edge connectors on the TSB7053 SHB.

* Pins 3 and 4 of Side B of Connector A (TDI and TDO) are jumpered together.

Connector A			Connector B			Connector C			Connector D		
	Side B	Side A		Side B	Side A		Side B	Side A		Side B	Side A
1	SMCLK	SMBDAT	1	+5VSBY	+5VSBY	1	USBP0+	GND	1	INTB#	INTA#
2	GND	GND	2	GND	NC	2	USBP0-	GND	2	INTD#	INTC#
3	TDI TDO*	NC	3	A_PE_TXP8	GND	3	GND	USBP1+	3	GND	NC
4	TDI TDO*	NC	4	A_PE_TXN8	GND	4	GND	USBP1-	4	REQ3#	GNT3#
5	NC	ICH WAKE#	5	GND	A_PE_RXP8	5	USBP2+	GND	5	REQ2#	GNT2#
6	PWRBTN#	ICH PCIPME#	6	GND	A_PE_RXN8	6	USBP2-	GND	6	PCIRST#	GNT1#
7	PWROK	PSON#	7	A_PE_TXP9	GND	7	GND	USBP3+	7	REQ1#	GNT0#
8	SHBRST#	EXP RESET#	8	A_PE_TXN9	GND	8	GND	USBP3-	8	REQ0#	SERR#
9	CFG0	CFG1	9	GND	A_PE_RXP9	9	USBOC0	GND	9	NC	3.3V
10	CFG2	CFG3	10	GND	A_PE_RXN9	10	GND	USBOC1	10	GND	CLKFI
11	NC	GND	11	RSVD	GND	11	USBOC2	GND	11	CLKFO	GND
Mechanical Connector			Mechanical Connector			Mechanical Connector			Mechanical Connector		
12	GND	RSVD	12	GND	RSVD	12	GND	USBOC3	12	CLKC	CLKD
13	B_PE_TXP0	GND	13	A_PE_TXP10	GND	13	NC	GND	13	GND	3.3V
14	B_PE_TXN0	GND	14	A_PE_TXN10	GND	14	NC	GND	14	CLKA	CLKB
15	GND	B_PE_RXP0	15	GND	A_PE_RXP10	15	GND	NC	15	3.3V	GND
16	GND	B_PE_RXN0	16	GND	A_PE_RXN10	16	GND	NC	16	AD31	PME#
17	B_PE_TXP1	GND	17	A_PE_TXP11	GND	17	NC	GND	17	AD29	3.3V
18	B_PE_TXN1	GND	18	A_PE_TXN11	GND	18	NC	GND	18	M6_6_EN	AD30
19	GND	B_PE_RXP1	19	GND	A_PE_RXP11	19	GND	NC	19	AD27	AD28
20	GND	B_PE_RXN1	20	GND	A_PE_RXN11	20	GND	NC	20	AD25	GND
21	B_PE_TXP2	GND	21	A_PE_TXP12	GND	21	A_MDI0P	GND	21	GND	AD26
22	B_PE_TXN2	GND	22	A_PE_TXN12	GND	22	A_MDI0N	GND	22	CBE3#	AD24
23	GND	B_PE_RXP2	23	GND	A_PE_RXP12	23	GND	A_MDI1P	23	AD23	3.3V
24	GND	B_PE_RXN2	24	GND	A_PE_RXN12	24	GND	A_MDI1N	24	GND	AD22
25	B_PE_TXP3	GND	25	A_PE_TXP13	GND	25	A_MDI2P	GND	25	AD21	AD20
26	B_PE_TXN3	GND	26	A_PE_TXN13	GND	26	A_MDI2N	GND	26	AD19	PCIXCAP
27	GND	B_PE_RXP3	27	GND	A_PE_RXP13	27	GND	A_MDI3P	27	+5V	AD18
28	GND	B_PE_RXN3	28	GND	A_PE_RXN13	28	NC	A_MDI3P	28	AD17	AD16
29	REFCLK0	GND	29	A_PE_TXP14	GND	29	IPMB_CLK	GND	29	CBE2#	GND
30	REFCLK0#	GND	30	A_PE_TXN14	GND	30	IPMB_DAT	GND	30	GND	FRAME#
31	GND	REFCLK1#	31	GND	A_PE_RXP14	31	NC	NC	31	IRDY#	TRDY#
32	RSVD-G	REFCLK1	32	GND	A_PE_RXN14	32	NC	NC	32	DEVSEL#	+5V

Connector A		
	Side B	Side A
33	REFCLK2#	GND
34	REFCLK2	GND
35	GND	REFCLK3#
36	RSVD-G	REFCLK3
37	REFCLK4#	GND
38	REFCLK4	GND
39	GND	REFCLK5# PU
40	RSVD-G	REFCLK 5 PU
41	REFCLK6# PU	GND
42	REFCLK6 PU	GND
43	GND	REFCLK7# PU
44	GND	REFCLK7 PU
45	A_PE_TXP0	GND
46	A_PE_TXN0	GND
47	GND	A_PE_RXP0
48	GND	A_PE_RXN0
49	A_PE_TXP1	GND
50	A_PE_TXN1	GND
51	GND	A_PE_RXP1
52	GND	A_PE_RXN1
53	A_PE_TXP2	GND
54	A_PE_TXN2	GND
55	GND	A_PE_RXP2
56	GND	A_PE_RXN2
57	A_PE_TXP3	GND
58	A_PE_TXN3	GND
59	GND	A_PE_RXP3
60	GND	A_PE_RXN3
61	A_PE_TXP4	GND
62	A_PE_TXN4	GND
63	GND	A_PE_RXP4
64	GND	A_PE_RXN4
65	A_PE_TXP5	GND
66	A_PE_TXN5	GND
67	GND	A_PE_RXP5
68	GND	A_PE_RXN5
69	A_PE_TXP6	GND
70	A_PE_TXN6	GND
71	GND	A_PE_RXP6
72	GND	A_PE_RXN6
73	A_PE_TXP7	GND
74	A_PE_TXN7	GND
75	GND	A_PE_RXP7
76	GND	A_PE_RXN7
77	NC	GND
78	3.3V	3.3V
79	3.3V	3.3V
80	3.3V	3.3V
81	3.3V	3.3V
82	NC	NC

Connector B		
	Side B	Side A
33	A_PE_TXP15	GND
34	A_PE_TXN15	GND
35	GND	A_PE_RXP15
36	GND	A_PE_RXN15
37	NC	GND
38	NC	NC
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND
44	+12V	+12V
45	+12V	+12V
46	+12V	+12V
47	+12V	+12V
48	+12V	+12V
49	+12V	+12V

Connector C		
	Side B	Side A
33	NC	NC
34	NC	GND
35	NC	GND
36	GND	NC
37	GND	NC
38	NC	GND
39	NC	GND
40	GND	NC
41	GND	NC
42	3.3V	3.3V
43	3.3V	3.3V
44	3.3V	3.3V
45	3.3V	3.3V
46	3.3V	3.3V
47	3.3V	3.3V
48	3.3V	3.3V
49	3.3V	3.3V
50	3.3V	3.3V
51	GND	GND
52	GND	GND
53	GND	GND
54	GND	GND
55	GND	GND
56	GND	GND
57	GND	GND
58	GND	GND
59	+5V	+5V
60	+5V	+5V
61	+5V	+5V
62	+5V	+5V
63	GND	GND
64	GND	GND
65	GND	GND
66	GND	GND
67	GND	GND
68	GND	GND
69	GND	GND
70	GND	GND
71	GND	GND
72	GND	GND
73	+12V_VRM	+12V_VRM
74	+12V_VRM	+12V_VRM
75	+12V_VRM	+12V_VRM
76	+12V_VRM	+12V_VRM
77	+12V_VRM	+12V_VRM
78	+12V_VRM	+12V_VRM
79	+12V_VRM	+12V_VRM
80	+12V_VRM	+12V_VRM
81	+12V_VRM	+12V_VRM
82	+12V_VRM	+12V_VRM

Connector D		
	Side B	Side A
33	PLOCK#	STOP#
34	PERR#	GND
35	GND	CBE1#
36	PAR	AD14
37	NC	GND
38	GND	AD12
39	AD15	AD10
40	AD13	GND
41	GND	AD9
42	AD11	CBE0#
43	AD8	GND
44	GND	AD6
45	AD7	AD5
46	AD4	GND
47	GND	AD2
48	AD3	AD1
49	AD0	GND

PCI Express Signals Overview

The following table provides a description of the SHB slot signal groups on the PCI Express connectors.

Type	Signals	Description	Connector	Source
Global	GND, +5V, +3.3V, +12V	Power		Backplane
	PSON#	Optional ATX support	A	SHB
	PWRGD, PWRBT#, 5Vaux	Optional ATX support	A and B	Backplane
	TDI	Optional JTAG support	A	Backplane
	TDO	Optional JTAG support	A	SHB
	SMCLK, SMDAT	Optional SMBus support	A	SHB & Backplane
	IPMB_CL, IPMB_DA	Optional IPMB support	C	SHB & Backplane
	CFG[0:3]	PCIe configuration straps	A	Backplane
	SHB_RST#	Optional reset line	A	SHB
	RSVD	Reserved	A and B	
	RSVD-G	Reserved ground	A	Backplane
	WAKE#	Signal for link reactivation	A	Backplane
PCIe	a_PETp[0:15] a_PETn[0:15] a_PERp[0:15] a_PERn[0:15]	Point-to-point from SHB slot through the x16 PCIe connector (A) to the target device(s)	A and B	SHB & Backplane
	b_PETp[0:3] b_PETn[0:3] b_PERp[0:3] b_PERn[0:3]	Point-to-point from SHB slot through the x8 PCIe connector (B) to the target device(s)	A	SHB & Backplane
	REFCLK[0:7]+, REFCLK[0:7]-	Clock synchronization of PCIe expansion slots	A	SHB
	PERST#	PCIe fundamental reset	A	SHB & Backplane
PCI(-X)	AD[0:31], FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, C/BE[0:3], SDONE, SBO#, PAR	Bussed on SHB slot and expansion slots	D	SHB & Backplane
	GNT[0:3], REQ[0:3], CLKA, CLKB, CLKC, CLKD, CLKFO, CLKFI	Point-to-point from SHB slot to each expansion slot	D	SHB & Backplane
	INTA#, INTB#, INTC#, INTD#	Bussed (rotating) on SHB slot and expansion slots	D	Backplane
	M66EN, PCIXCAP	Bussed on SHB slot and expansion slots	D	Backplane
	PCI_PRST#	PCI(-X) present on backplane detect	D	Backplane
	PME#	Optional PCI wake-up event bussed on SHB and backplane expansion slots	A	Backplane
Misc. I/O	USB[0:3]P, USB[0:3]N, USBOC[0:3]#	Optional point-to-point from SHB Connector C to a destination USB device	C	SHB & Backplane
SATA	ESATATX(4:5)P, ESATATX(4:5)N, ESATARX(4:5)P, ESATARX(4:5)N,	Optional point-to-point from SHB Connector C to a destination SATA device Note: These optional SATA connections to the backplane are not available with the TSB7053.	C	SHB & Backplane
Ethernet	a_MDI(0:1)p, a_MDI(0:1)n	Optional point-to-point from SHB Connector C to a destination Ethernet device	C	SHB & Backplane

Optional IOB33 PCI Express Link Expansion

An optional Trenton IOB33 module may be used with the TSB7053 SHB to provide additional PCIe links to a backplane equipped with a PCI Express expansion slot. The Trenton BPG7087 and BPG6600 backplane feature this PCI Express expansion slot. The IOB33 routes an additional PCIe x4 link available from the TSB7053's processor down to a backplane for use in PCI Express link and/or bandwidth expansion. This additional link may operate at the PCIe 1.1 or PCIe 2.0 interface speed depending on the backplane and end-point configuration.

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Chapter 3 TSB7053 System Power Connections

Introduction

The combination of new power supply technologies and the system capabilities defined in the SHB Express® (PICMG® 1.3) specification requires a different approach to connecting system power to a PICMG 1.3 backplane and/or SHB hardware.

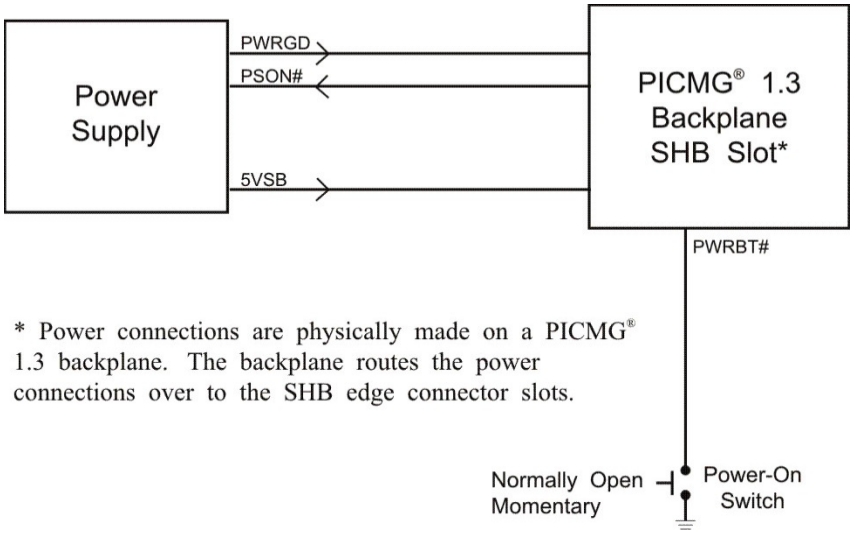
To improve system MTTR (Mean Time To Repair), the PICMG 1.3 specification defines enough power connections to the SHB's edge connectors to eliminate the need to connect auxiliary power to the SHB. All power connections in a PICMG 1.3 system can be made to the PICMG 1.3 backplane. This is true for SHBs that use high-performance processors. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive these high-performance SHBs. Trenton's PICMG 1.3 backplanes define ATX/EPS and +12V connectors that are compatible with ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in this manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

Power Supply and SHB Interaction

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.



Power Supply and SHB Interaction

PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

Electrical Connection Configurations

There are a number of different connector types, such as EPS, ATX or terminal blocks, which can be utilized in wiring power supply and control functions to a PICMG 1.3 backplane. However, there are only two basic electrical connection configurations: **ACPI Connection** and **Legacy Non-ACPI Connection.**

ACPI Connection

The diagram on the previous page shows how to connect an ACPI compliant power supply to an ACPI enabled PICMG 1.3 system. The following table shows the required connections that must be made for soft power control to work.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up.	Power Supply
PWRGD	Power Good. This signal indicates that the power supply's voltages are stable and within tolerance.	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply.	SHB/Backplane
PWRBT#	Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state. If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs.	Power Button

Legacy Non-ACPI Connection

For system integrators that either do not have or do not require an ACPI compliant power supply as described in the section above, an alternative electrical configuration is described in the table on the following page.

Signal	Description	Source
+12	DC voltage for those systems that require it	Power Supply
+5V	DC voltage for those systems that require it	Power Supply
+3.3V	DC voltage for those systems that require it	Power Supply
+5VSB	Not Required	Power Supply
PWRGD	Not Required	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply. If an ATX or EPS power supply is used in this legacy configuration, a shunt must be installed on the backplane from PSON# to signal Ground. This forces the power supply DC outputs on whenever AC to the power supply is active.	Backplane
PWRBT#	Not Used	

In addition to these connections, there is usually a switch controlling AC power input to the power supply.

When using the legacy electrical configuration, the SHB BIOS **Power Supply Shutoff** setting should be set to **Manual shutdown**. Refer to the *General ACPI Configuration* section of the *Advanced Setup* chapter in this manual for details.

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Chapter 4 PCI Express Backplane Usage

Introduction

PCI Express® is a scalable, full-duplex serial interface which consists of multiple communication lanes grouped into links. PCI Express scalability is achieved by grouping these links into multiple configurations. A x1 ("by 1") PCI Express link is made up of one full-duplex link that consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. A x4 configuration is made up of four PCI Express links. The most commonly used PCIe link sizes are x1, x4, x8 and x16.

PCI Express devices with different PCI Express link configurations establish communication with each other using a process called auto-negotiation or link training. For example, a PCI Express device or option card that has a x16 PCI Express interface and is placed into a x16 mechanical/x8 electrical slot on a backplane establishes communication with a PICMG® 1.3 SHB using auto-negotiation. The option card's PCI Express interface will "train down" to establish communication with the SHB via the x8 PCI Express link between the SHB and the backplane option card slot.

SHB Edge Connectors

The PICMG 1.3 specification enables SHB vendors to provide multiple PCI Express configuration options for edge connectors A and B of a particular SHB. These edge connectors carry the PCI Express links and reference clocks down to the SHB slot on the PICMG 1.3 backplane. The potential PCI Express link configurations of an SHB fall into three main classifications: server-class, graphics-class and combo-class. The specific class and PCI Express link configuration of an SHB is determined by the chipset components or Platform Controller Hub (PCH) and the processor(s) used on the board.

In a server-class configuration, the main goal of the SHB is to route as many high-bandwidth PCI Express links as possible down to the backplane. Typically, these links are a combination of x4 and x8 PCI Express links.

A graphics-class configuration should provide a x16 PCI Express link down to the backplane in order to support high-end PCI Express graphics and video cards. Graphics-class SHB configurations also provide as many lower bandwidth (x1 or x4) links as possible.

A combo-class configuration is provided by SHBs like the TSB7053 or JXT6966. These system host board types have PCI Express hardware and software implementations that are capable of combining links to support either server or graphics-class PICMG 1.3 backplane configurations.

The A0, A2 and A3 PCI Express links on the TSB7053 connect to the processor via PCI Express 2.0 link repeaters. These repeaters ensure optimum PCI Express signal integrity between the SHB's processor and the end-point device on the backplane regardless of device's location on the backplane. The A0, A2 and A3 links can operate as either PCI Express 2.0 or PCI Express 1.1 links based on the end-point devices on the backplane that connect to the SHB. In addition to automatically configuring themselves for either PCIe 2.0 or PCIe 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the two x4 links and the one x8 link from the processor; links A0, A2 and A3 can be combined into a single x16 PCIe electrical link or two x8 links on a backplane. (Note: link A0 is a x8 link.) The CPU's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. The PCIe link (B0) is also a PCIe 2.0 or PCIe 1.1 interface and this link comes from the board's Intel® C206 PCH. This x4 link can automatically bifurcate into four, x1 PCIe links.

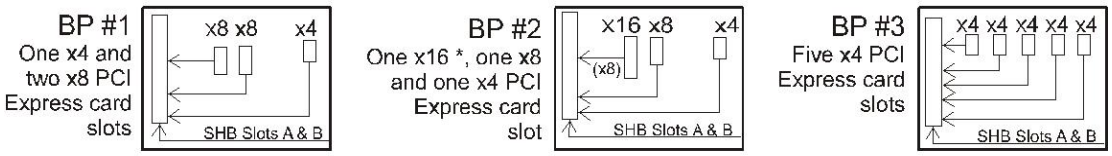
In addition to the standard PICMG 1.3 edge connector PCIe interfaces, the TSB7053 boards also have an additional x4 link available for use on a backplane. This extra x4 link originates at the processor and is routed to the SHB's controlled impedance connector for use with the Trenton IOB33 plug-in option card. The IOB33 routes this x4 PCI Express link down to a physical x4 PCIe edge connector on the board. The IOB33 edge connector mates with a backplane's PCIe Expansion slot. This extra x4 link is useful in supporting an additional system card slot or a PCIe end-point device such a PCI Express switch. Refer to the *Optional IOB Expansion Board – Chapter 5* for more information on the IOB33 and the *PCI Express*

Reference – Chapter 2 for more information on the PCI Express signal routings to the SHB edge connectors.

The figures below show some typical SHB and backplane combinations that would result in successfully establishing communication with the SHB host device. The first figure shows a server-class SHB; the second shows a graphics-class SHB while the third shows a combination that would not work well with the TSB7053 SHB. Three similar graphics-class examples are illustrated in the second group of figures below.

Server-Class SHB:

PCI Express™ Edge Connectors A & B: One x4 and two x8 PCI Express™ Links with five reference clocks

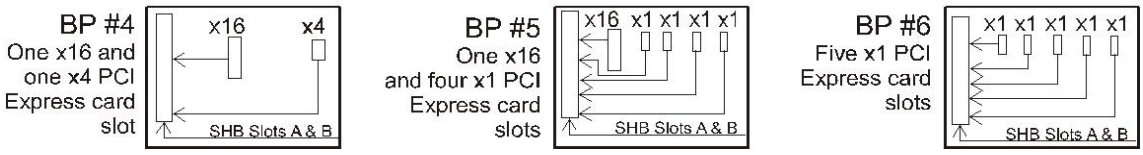


* x16 slot is x16 mech./x8 elec.

Note: A backplane with the BP #3 routing example to edge connectors A & B would not be a good match for the TSB7053 SHB because link A0 is a x8 link that cannot bifurcate into two x4 links. One of these x4 links will not have an interface path available to the TSB7053.

Graphics-Class SHB:

PCI Express™ Edge Connectors A & B: One x16 and one x4 PCI Express™ Link with five reference clocks



Note: All of these graphics class backplane examples will work fine with the TSB7053 SHB because the PCIe link B0 on the board can bifurcate into four x1 PCIe links.

PCI Express link configuration straps for each PCI Express option card slot on a PICMG 1.3 backplane are required as part of the PICMG® 1.3 specification. These configuration straps alert the SHB as to the specific link configuration expected on each PCI Express option card slot. PCI Express communication between the SHB and option card slots is successful only when there are enough available PCI Express links established between the PICMG 1.3 SHB and each PCI Express slot or device on the backplane.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express® System Host Board PCI Express Specification, PICMG® 1.3*.

TSB7053 and Compatible Trenton Backplanes

The TSB7053 is a standard PICMG 1.3 SHB that will function with a wide variety of industry standard PICMG 1.3 backplanes. However, some non-Trenton backplanes may not utilize the full capabilities of the Trenton TSB7053 boards. The table below illustrates the TSB7053 compatibility with the current listing of Trenton PICMG 1.3 backplanes. A "Yes" in the compatible column below means that all slots on the backplane will function with a TSB7053 board. The clarification column explains any limitations of using a TSB7053 single processor SHB with a particular backplane. We are continuously adding backplanes to our product line so contact us or visit our website to learn about the latest Trenton PICMG 1.3 backplane availability listings.

PICMG 1.3 Backplane	Compatible with TSB7053 (i.e. all backplane slots are functional)	Why not or clarification
2U Butterfly Backplanes		
BPC8219	Yes	
BPG6741	Yes	
BPX6736*	Yes	
Multi-Segment Backplanes		
BP6FS6605	No	SHB segment spacing
BP4FS6890	Yes, use Graphics Class configuration	
BP2S6929	Yes	
Combo Backplanes		
BPC7041	No, the TSB7053 does not support the PEX10 for PCIe link expansion	PEX10 needed to provide the links for BP slots PCIe 1 through PCIe4
BPC7009*	Yes	
Server-Class Backplanes		
BPX8093	No, the TSB7053 does not support the PEX10 for PCIe link expansion	PEX10 needed to provide the links for BP slots PCIe1 and PCIe2
BPX6806*	Yes, need IOB33 for PCIe1 slot	TSB7053 provides x4 via IOB33
BPX6620*	Yes, need IOB33 for PCIe1 slot	TSB7053 provides x4 via IOB33
BPX6610*	Yes	
BPX6571*	Yes	
BPX3/14*	No	Short one x4 PCIe link
BPX3/8*	Yes	
BPX6719	Yes, need IOB33 for PCIe1 slot	TSB7053 provides x4 via IOB33
BPX3/2*	Yes	
BPX5*	Yes, need IOB33 for PCIe1 slot	TSB7053 provides x4 via IOB33
Graphics-Class Backplanes		
BPG8150	No, the TSB7053 does not support the PEX10 for PCIe link expansion	PEX10 needed to provide the links for BP slots PCIe 1 and PCIe2
BPG8032	Yes	
BPG7087	Yes, need IOB33 for PCIe1 slot	
BPG6615	Yes	
BPG6600	Yes	
BPG6544	Yes	
BPG6714	Yes, need IOB33 for PCIe1 slot	TSB7053 provides x4 via IOB33
BPG2/2*	Yes	
BPG4*	Yes, need IOB33 for PCIe1 slot	TSB7053 provides x4 via IOB33

*Backplane does not have an SHB edge connector D slot. The backplane will function OK, but the system designer should ensure the exposed SHB edge connector D pins are protected from potential damage.

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Chapter 5 Optional IOB33 Expansion Board Usage

IOB33 Overview

The IOB33 is optional I/O expansion board that may be used on the TSB7053 SHB for the purpose of routing an additional x4 PCIe expansion link from the processor down to the PCIe Expansion Slot on a Trenton backplane.

Most of the legacy I/O interfaces on the IOB33 have been moved down to the TSB7053. Additional legacy I/O IOB33 will be available for use on the TSB7053 with a future BIOS revision of the SHB. The added I/O capabilities will include the following added interfaces for use by the system designer:

- Two - RS232 communication ports
- One - Floppy drive interface
- One - Parallel printer interface
- One – PS/2 Mini-DIN connector for PS/2 keyboard and mouse connections
  - Also includes separate, on-board PS/2 keyboard and mouse headers for systems that require separate PS/2 connections

There are three versions of the Trenton IOB33 I/O expansion board. This optional board is designed for the TSB7053 SHB, but the additional versions may be used on other Trenton SHBs. The chart below identifies the IOB33 version that is compatible with specific Trenton SHBs.

IOB Module	TSB7053 (7053)	T4L (6483)	TML (6490)	TQ9 (6731)	MCG-Series (6680, 6690, 6675, 6695)	NLI / NLT (6313, 6396)	SLT / SLI (6515, 6521)	MCX-Series (6633, 6685, 6638, 6700)	JXT / JXTS (6966)
IOB33JX (7015-004)	X								X
IOB33MC (7015-002)				X	X			X	
IOB33 (7015-000)		X	X			X	X		

IOB33 Models

Model #	Model Name	Description
7015-004	IOB33JX	Includes the I/O Plate for use with the TSB7053, JXT6966 or JXTS6966 System Host Boards
7015-002	IOB33MC	Includes the I/O Plate for use with MCX, MCG and TQ9 system host boards
7015-000	IOB33	Includes the I/O Plate for use with TML, SLT, SLI NLT, NLI and T4L system host boards

IOB33 Features

IOB33 (7015-004, 7015-002, 7015-001)

- I/O plate versions for a variety of Trenton system host boards
- Two serial ports and PS/2 mouse/keyboard mini DIN on the I/O bracket
- PS/2 mouse, keyboard, parallel port and floppy drive connectors
- PCI Express expansion capability for use with PCI Express backplanes
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG®) PCI Express Specification

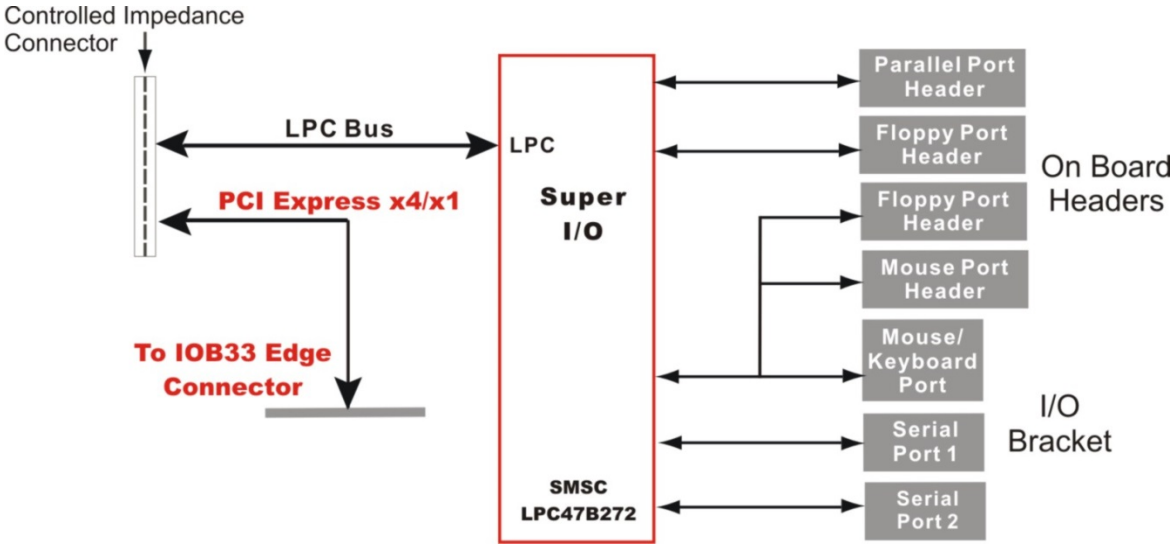
IOB33 Temperature/Environment

Operating Temperature: 0º C. to 60º C.

Storage Temperature: - 40º C. to 70º C.

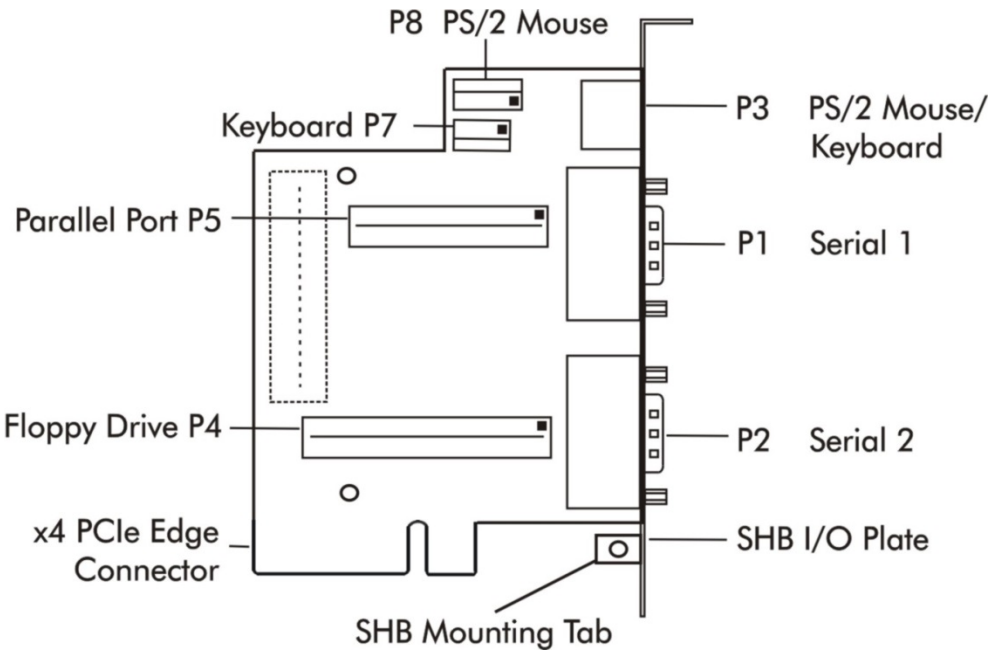
Humidity: 5% to 90% non-condensing

IOB33 (7015-xxx) Block Diagram

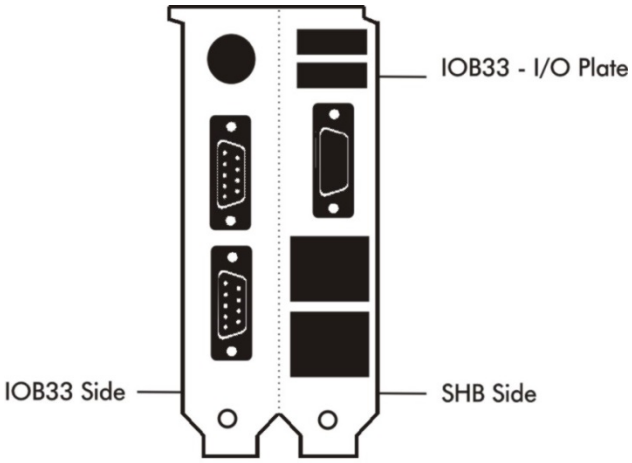


NOTE: When an IOB33 is connected to the TSB7053's P20 I/O expansion connector, a second Super I/O chip is placed into the system by virtue of the LPC Bus routing through the controlled impedance connector. A future TSB7053 BIOS revision will be necessary to use this second Super I/O chip to support the IOB33's on-board headers and I/O bracket port connectors. All of the legacy I/O and serial communication ports featured on the IOB33; with the exception of the floppy and parallel ports, are now available directly on the TSB7053 board itself. The PCIe x4 link routing to a PICMG 1.3 backplane expansion slot works fine with the current TSB7053 BIOS revision.

IOB33 (7015-xxx) Layout Diagram



IOB33 (7015-xxx) I/O Plate Diagram



IOB33 Connectors

NOTE: the square pad on the PCB indicates Pin 1 on the connectors.

P1 - Serial Port Connector

9 position "D" right angle, Spectrum #56-402-001

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-O	8	Clear to Send-
4	Data Terminal Ready-O	9	Ring Indicator-I
5	Signal Gnd		

P2 - Serial Port Connector

9 position "D" right angle, Spectrum #56-402-001

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-O	8	Clear to Send-
4	Data Terminal Ready-O	9	Ring Indicator-I
5	Signal Gnd		

P3 - PS/2 Mouse and Keyboard Connector

6 pin mini DIN, Kycon #KMDG-6S-B4T

Pin	Signal
1	Ms Data
2	Kbd Data
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P4 - Floppy Drive Connector

34 pin dual row header, Amp #103308-7

Pin	Signal	Pin	Signal
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Change

IOB33 Connectors (continued)

P5 - Parallel Port Connector
26 pin dual row header, Amp #103308-6

Pin	Signal	Pin	Signal
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

P7 - Keyboard Header
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self resetting fuse

P8 - PS/2 Mouse Header
6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	Reserved
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

IOB33 Connectors (continued)

P6 - Impedance Connector
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12	2	+5V_STANDBY
3	NC	4	+5V_STANDBY
5	NC	6	+5V_DUAL
7	NC	8	+5V_DUAL
9	NC	10	NC
11	NC	12	NC
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SBMCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP4	48	C_PE_RXP4
49	C_PE_TXN4	50	C_PE_RXN4
51	Gnd	52	Gnd
53	C_PE_TXP3	54	C_PE_RXP3
55	C_PE_TXN3	56	C_PE_RXN3
57	Gnd	58	Gnd
59	C_PE_TXP2	60	C_PE_RXP2
61	C_PE_TXN2	62	C_PE_RXN2
63	Gnd	64	Gnd
65	C_PE_TXP1	66	C_PE_RXP1
67	C_PE_TXN1	68	C_PE_RXN1
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5v

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Appendix A BIOS Messages

Introduction

A status code is a data value used to indicate progress during the boot phase. These codes are outputted to I/O port 80h on the SHB. Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 4.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

[1] Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality in legacy BIOS

BIOS Beep Codes

The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

BIOS Status Codes

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the TSB7053 SHB. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

The HEX to LED chart in the POST Code LEDs section will serve as a guide to interpreting specific BIOS status codes.

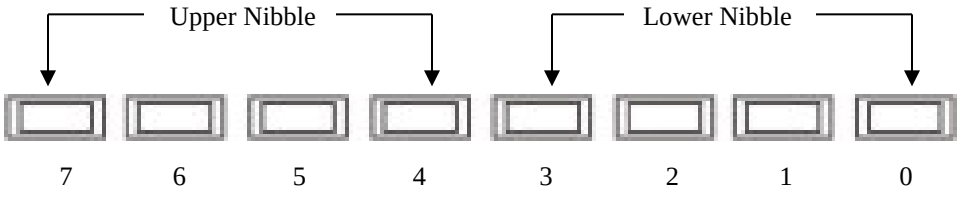
BIOS Status POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the SHB, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the TSB7053 SHB. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED7	LED6	LED5	LED4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3	LED2	LED1	LED0
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



TSB7053 POST Code LEDs

Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

SEC Status Codes

Status Code	Description
0x0	Not used
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

SEC Beep Codes

There are no SEC Beep codes associated with this phase of the Aptio BIOS boot process.

PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started

PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
S3 Resume Error Codes	
0xE8	S3 Resume Failed in PEI
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
7	Reset PPI is not available
4	Recovery failed
4	S3 Resume failed

DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization

0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

DXE Beep Codes

# of Beeps	Description
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
1	Invalid password
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

ACPI/ASL Status Codes

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

OEM-Reserved Status Code Ranges

Status Code	Description
0x5	OEM SEC initialization before microcode loading
0xA	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

Appendix B Certificates of Compliance

Certificate of Compliance – EN61000

Certificate Of Compliance

(Application of Council Directive: 2004/108/EC - EMC Directive)

Standards to which Conformity is Declared:

EN 61000-6-4:2007 including EN 55022:2006 + A1 CLASS A, EN 55022:2006 + A1 CLASS A, EN 61000-3-2:2005, IEC 61000-3-3:2008, EN 61000-6-2:2005 including EN 61000-4-2:2008, EN 61000-4-3:2008 + A1:2010, EN 61000-4-4:2004 + A1:2010, EN 61000-4-5:2005, EN 61000-4-6:2008 EN 61000-4-8:2009 & EN 61000-4-11:2004

Applicant:	Trenton Technology Inc.
Address:	2350 Centennial Drive Gainesville, GA 30504 USA Tel: 770.287.3100 Fax: 770.287.3150
Product(s) Tested:	Host Board (including processor, memory, I/O ports, battery)
Model(s) Tested:	TSB7053
Tested By:	ITC Engineering Services, Inc. 9959 Calaveras Road, PO Box 543 Sunol, California 94586-0543 Tel: (925) 862-2944 Fax: (925) 862-9013 Email: info@itcemc.com http://www.itcemc.com
Date of Issue:	December 21, 2011
Report Number:	20111208-01

I, the undersigned hereby declare that the model(s) listed above was tested and conforms to the Directives and Standards listed above.

Certified By: Date December 21, 201

Mr. Michael Gbadebo, PE
(California License # 11303)
Chief Engineer/Principal Consultant

NVLAP NVLAP Accredited (code 200172-0)

Certificate of Compliance – EN60950

Certificate Of Compliance

(Application of Council Directive: LVD 2006/95/EC – Low Voltage Directive)

Standards to which Conformity is Declared:
EN 60950-1:2005

Applicant:	Trenton Technology Inc.
Address:	2350 Centennial Drive Gainesville, GA 30504 USA Tel: 770.287.3100 Fax: 770.287.3150
Product(s) Tested:	Host Board (including processor, memory, I/O ports, battery)
Model(s) Tested:	TSB7053
Tested By:	ITC Engineering Services, Inc. 9959 Calaveras Road, PO Box 543 Sunol, California 94586-0543 Tel: (925) 862-2944 Fax: (925) 862-9013 Email: info@itcemc.com http://www.itcemc.com
Date of Issue:	December 21, 2011
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I, the undersigned hereby declare that the model(s) listed above was tested and conforms to the Directives and Standards listed above.

Certified By: Date December 21, 2011

Mr. Michael Gbadebo, PE
(California License # 11303)
Chief Engineer/Principal Consultant

NVLAP NVLAP Accredited (code 200172-0)