MCP6792

6792-xxx

No. 87-006795-000 Revision A

TECHNICAL REFERENCE

Manual Revision 1.1

Intel® Core™ 2 Duo

Processor AMC (PrAMC)

WARRANTY

The following is an abbreviated version of Trenton Technology's warranty policy for MicroTCA® (*u*TCA) products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonTechnology.com.

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RETURN POLICY

Products returned for repair must be accompanied by a Return Material Authorization (RMA) number, obtained from Trenton Technology prior to return. Freight on all returned items must be prepaid by the customer, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton Technology via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

TRENTON Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

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E-mail: Support@TrentonTechnology.com
Web: www.TrentonTechnology.com

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HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your AMC card from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the AMC in its static-shielded bag until you are ready to perform your installation.
- Handle the AMC by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the AMC.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

RECOMMENDED BOARD HANDLING PRECAUTIONS

This AMC has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

WE APPRECIATE YOUR INPUT

Let us know if see anything with this product including the manual, our on-line product information or any product specification information that might need improving or correcting. Contact us on our web site at www.TrentonTechnology.com via the Ask Trenton form, by phone at 770-287-3100 or in the U.S. at 800-875-6031 or via e-mail at marketing@TrentonTechnology.com. Thank you for your business and your input in helping to make our products better.

Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your MCP6792 (6792-xxx) AMC Processor. Overall system performance may be affected by incorrect usage of these features.

RECOMMENDED BOARD HANDLING PRECAUTIONS

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- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

AIR FLOW REQUIREMENT

The MCP6792 AMC uses a low-power, dual-core processor capable of a wide range of operating temperatures. These thermal characteristics are invaluable in many AMC applications. AMC module specification requirements require a very low mechanical profile height for the topside of the card. These requirements demand the use of passive heat sink technology, which in turn requires the system designer to ensure that air flows over the module's heat sink and forces the warm air away from the AMC. Trenton recommends a chassis design that provides a 300LFM continuous airflow over the AMC to ensure years of trouble free operation in harsh environments.

DDR3 MEMORY

The DDR3 memory modules used in the MCP6792 must be non-ECC (64-bit) DDR3, unbuffered, SO-DIMMs and must be PC3-6400 or PC3-8500 compliant.

A memory module can be installed in only one SO-DIMM socket. If only one SO-DIMM module is used, it must be populated in SO-DIMM socket 1A. The AMC's memory interface operates at maximum bandwidth with two SO-DIMMs of the same size installed in sockets 1A and 1B and the SO-DIMMs may differ in technology (i.e. component density) and/or device width.

SATA II INTERFACE

The small form factor version of the ICH9M I/O Controller Hub used on the MCP6792 supports two Serial ATA 300 (i.e. SATA II 300) interfaces on the card's edge connector. To maximize the storage capability and efficiency of your system design, use storage devices and cards capable of supporting the SATA II interface. If you must use storage devices that only support the SATA I interface, ensure that the AMC's SATA interface BIOS parameter is configured properly. The AMC's BIOS default setting for the SATA interface is SATA II.

Before You Begin (continued)

PCI EXPRESS LINKS AND MICROTCA BACKPLANES

The current version of the MicroTCA specification that defines PCI Express backplane routings (*PICMG AMC.1 R2.0*) supports a x4 and a x1 PCIe link from an AMC to a *u*TCA backplane. The chipset used on the Trenton MCP6792 allows the x4 PCIe link to be divided into four x1 PCIe links. In this configuration there are a total of five x1 PCI Express links routed from the AMC's edge card connector to a *u*TCA backplane and these additional links could be very useful in customized MicroTCA system applications. SW2 on the AMC is used to set the connector's PCI Express link configuration. The factory default setting is set to the x4 and x1 PCIe link routing supported by the specification. Care must be used if changing these routings because a standard MicroTCA backplane may not function with the AMC if SW2 is set to a PCIe link configuration that is not supported by the backplane.

ETHERNET INTERFACES

The AMC provides two 1000Base-BX Ethernet interfaces (LAN1 and LAN2) on the AMC's edge connector. Two differential signal pairs are used for each 1000Base-BX LAN and the ATCA carrier or *u*TCA backplane must account for this improved and faster Ethernet implementation supported by the MCP6792.

SINGLE-WIDTH, FULL-SIZE FRONT PANEL CONFIGURATION

The full-size front panel configuration of the Trenton MCP6792 AMC provides the following front panel ports and LED indicators:

- 10/100/1000Base-T Ethernet Port
- Video Port
- RS-232 COMM Port
- Two USB 2.0 Ports
- Four diagnostic LEDs and three card status LEDs

SINGLE-WIDTH, MID-SIZE FRONT PANEL CONFIGURATION

The mid-size front panel configuration of the Trenton MCP6792 AMC provides the following front panel ports and LED indicators:

- 10/100/1000Base-T Ethernet Port
- Video Port
- One USB 2.0 Port
- Three card status LEDs

FRONT PANEL MICRO-D CONNECTORS

Industry standard micro-D connectors are used for the front panel's RS-232 serial and video ports. The serial port has a 9-socket position connector and the connector for the video port has 15-socket positions. These AMC ports require standard 9-pin and 15-pin Micro-D connectors for connecting RS-232 and Video cables to the card.

IPMI SUPPORT

The MCP6792 uses the Intelligent Platform Management Interface (IPMI) to monitor key system functions and support various alarming functions. IPMI functionality and implementations are governed by several common industry standards. The card is fully compliant with these industry standards and well as IPMI Ver. 2.0. **In order to take advantage of the AMC's IPMI capabilities, application software that is IPMI-aware must be provided by the end user, system integrator or OEM.**

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections *MCP6792 Technical Reference Manual* (#87-006795-000). The latest revision of may be found on Trenton's website - www.TrentonTechnology.com/ProcessorAMC.

Chapter 1 Specifications

INTRODUCTION

The MCP6792 is an processor AMC card (PrAMC) designed for inserting directly into MicroTCA® backplanes or the AMC slots of an AdvancedTCA® blade or carrier card. The full- or mid-size front panel configuration of the MCP6792 provides support for a broad array of *u*TCA® and ATCA® chassis styles and applications. The AMC's Small Form Factor (SFF), dual-core processor options deliver impressive MCP6792 performance. Processor options for the card include the embedded Intel® Core™ 2 Duo Processor SP9300 SV, SL9400 LV or SU9300 ULV.

The Intel® GS45 Express Chipset is used on the Trenton MCP6792 to enable 4GB of DDR3 memory, multiple PCI Express® links, three Ethernet interfaces and much more. The I/O features on the card route two 1000Base-BX Ethernet interfaces, two SATA II 300 connections and multiple PCI Express links to the edge card connector. A switch on the rear of the card allows the user to select three different PCI Express link configuration options for routing to the card's edge connectors.

The full-size version of the card's front panel supports two USB 2.0 ports, one video port, one COMM port and a 10/100/1000 Base-T Ethernet port. The card supports an optional solid-state data storage capability directly on the card. The MCP6792's Module Management Controller (MMC) or Management Controller supports the Intelligent Platform Management Interface (IPMI) commands to support various system and card-level monitoring functions and alarm messaging.

The MCP6792 is compliant with version 1.2 of the Trusted Computing Group specification for Trusted Platform Modules. The card's TPM, the processor's Intel® Virtualization Technology (Intel® VT) feature and the chipset's Intel® Trusted Execution Technology (Intel® TXT) maximizes the security and integrity of any system design using a Trenton MCP6792 AMC processor card. The Intel® TXT and Intel® VT capabilities coupled with the built in TPM make the Trenton MCP6792 PrAMC a key building block in secure computing applications.

The Trenton MCP6792 installed in either a MicroTCA chassis backplane on the AMC card slot of an AdvancedTCA carrier card enhances the overall flexibility and capability of a *u*TCA/ATCA system design.

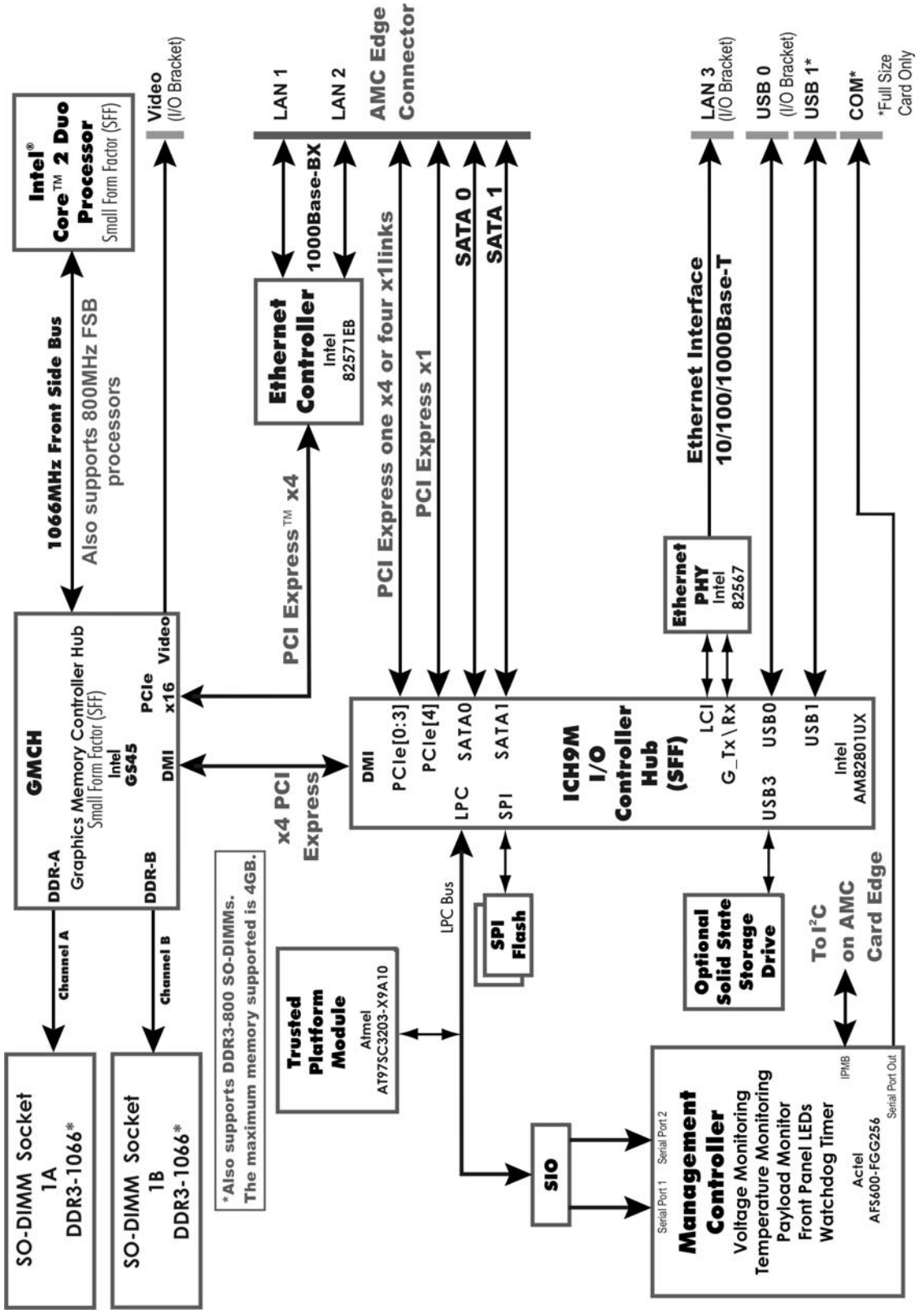
MODELS

Model #	Model Name	Speed	Intel CPU Number
Intel Core 2 Duo Processor SP9300 SV – Dual Core, 1066MHz FSB, 6MB cache, SFF CPU, Full-size I/O plate			
6792-005	MCP6792/2.26SF6	2.26GHz	SP9300
Intel Core 2 Duo Processor SL9400 LV – Dual Core, 1066MHz FSB, 6MB cache, SFF CPU, Full-size I/O plate			
6792-103	MCP6792/1.86LF6	1.86GHz	SL9400
Intel Core 2 Duo Processor SL9400 LV – Dual Core, 1066MHz FSB, 6MB cache, SFF CPU, Mid-size I/O plate			
6792-153	MCP6792/1.86LM6	1.86GHz	SL9400
Intel Core 2 Duo Processor SU9300 ULV – Dual Core, 800MHz FSB, 3MB cache, SFF CPU, Full-size I/O plate			
6792-201	MCP6792/1.2UF3	1.2GHz	SU9300
Intel Core 2 Duo Processor SU9300 ULV – Dual Core, 800MHz FSB, 3MB cache, SFF CPU, Mid-size I/O plate			
6792-251	MCP6792/1.2UM3	1.2GHz	SU9300

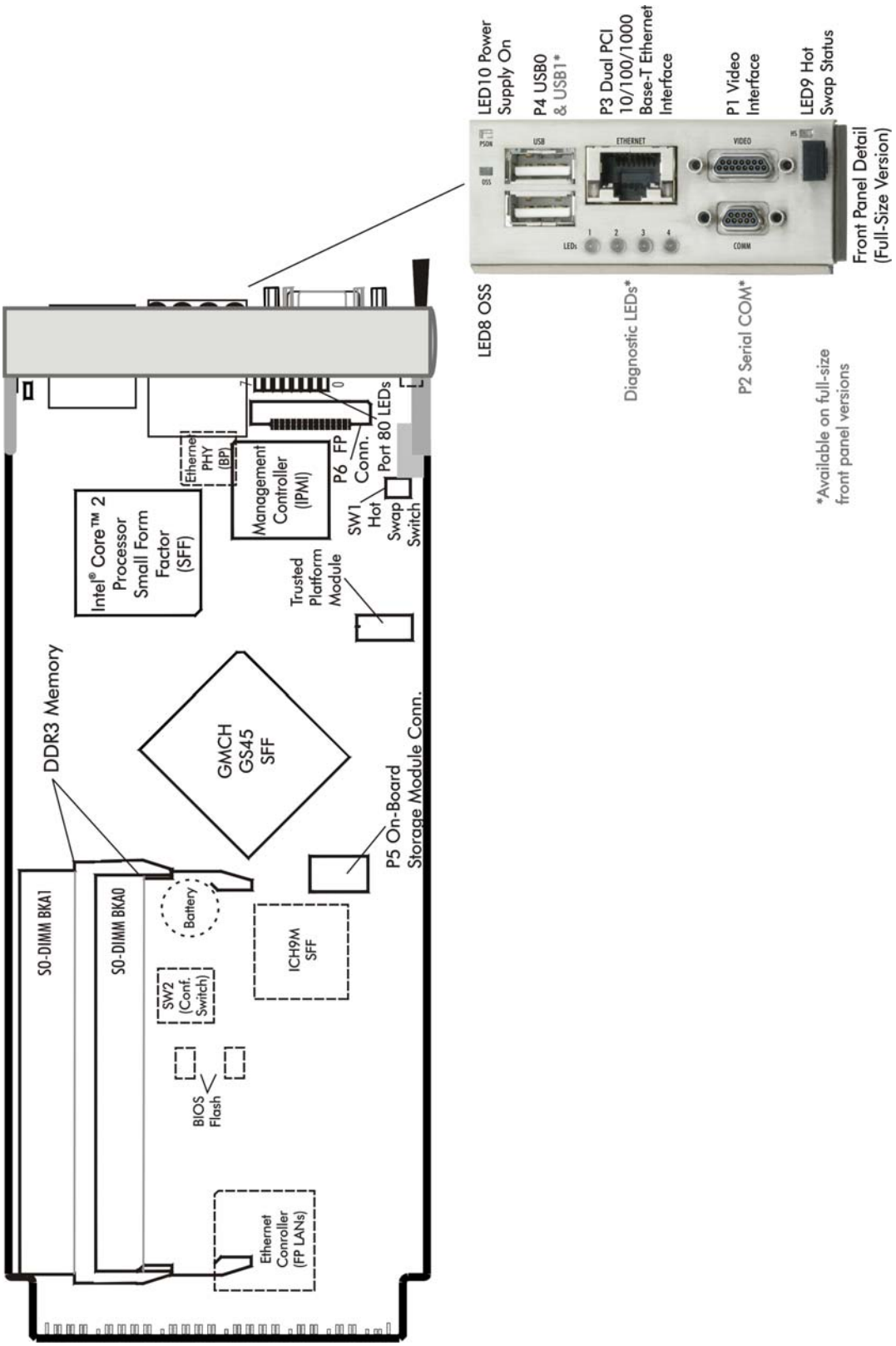
FEATURES

- Intel® Core™ 2 Duo SV, LV or ULV Processors [Penryn Small Form Factor (SFF)]
- Intel® GS45 Express chipset with 800MHz or 1066MHz FSB support
- PCI Express® edge card connector and on-board serial links operating in x4 and x1modes
- Switch selectable PCI Express link configurations to the card's edge connector
- Video interface utilizing the built-in, high-resolution analog display capabilities of the Intel GS45
- Dual 1000Base-BX Ethernet interfaces routed to the card's edge connectors
- Two SATA II 300 interfaces routed to the card's edge connectors
- Full size front panel configuration includes: two USB 2.0 ports, one COMM port, one video port, one 10/100/1000Base-T Ethernet port, four diagnostic LEDs and three status LEDs
- Mid size front panel configuration includes: one USB 2.0 port, one video port, one 10/100/1000Base-T Ethernet port, and three status LEDs
- Front panel Ethernet port supports 10/100/1000Base-T operation
- Supports up to 4GB of Double Data Rate (DDR3-1066) on-board memory via two plug-in SO-DIMM sockets
- Programmable FPGA Board Management Controller (BMC) supports IPMI board and system-level function monitoring and manages alarm indicators
- Trusted Computing Group (TCG) Trusted Platform Module (TPM) Ver. 1.2 compatible
- Optional on-board storage via plug-in USB solid-state drive (SSD) board
- Compatible with various MicroTCA chassis and AdvancedTCA AMC carrier card and blade specifications
    - PICMG® MTCA.0 R1.0 Specification (MicroTCA)
    - PICMG® 3.0, R3.0 Specification (AdvancedTCA)
    - PICMG® AMC.0, R2.0 Specification
    - PICMG® AMC.1, R2.0 Specification (PCI Express Implementation)
    - PICMG® AMC.2 Specification (Ethernet Implementation)
    - PICMG® AMC.3 Specification (Storage Implementation)

MCP6792 (6792-XXX) – AMC BLOCK DIAGRAM



MCP6792 (6792-XXX) – AMC LAYOUT DRAWING



PROCESSOR

- Intel® Core™ 2 Duo Processor SP9300 SV, Intel® Core™ 2 Duo Processor SL9400 LV or Intel® Core™ 2 Duo Processor SU9300 ULV
- SFF (22mm x 22mm) BGA processor package soldered down to the MCP6792 card

SERIAL INTERFACE

PCI Express®

DATA PATH

DDR3 Memory - 64-bit (per channel), 36-bit addressability supported
DMI – x4 PCI Express link

SERIAL INTERFACE SPEEDS

PCI Express x1 or x4 links @ 2.5GHz per lane

PROCESSOR BUS SPEEDS SUPPORTED (FSB)

1066MHz or 800MHz Front Side Bus

MEMORY INTERFACE

Dual Double Data Rate (DDR3) memory channels supports DDR3-1066 or DDR3-800 SO-DIMMS; theoretical memory interface bandwidth is up to 8.533GB/s.

SYSTEM BUS

Intel® GS45 chipset supports the system bus at 1066MHz or 800MHz, which provides a higher bandwidth path for transferring data between main memory/chipset and the processors.

DMA CHANNELS

The AMC is fully PC compatible with six DMA channels, each supporting type F transfers.

INTERRUPTS

The MCP6792 is fully AMC processor card compatible.

BIOS (FLASH)

The BIOS is an AMIBIOS with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. The Flash BIOS resides in the card's 16M-bit serial flash memory (SPI) devices located on the back of the card. There are a variety of methodologies for upgrading the card's BIOS discussed in this manual's BIOS chapters. Custom BIOSs are also available.

TRUSTED PLATFORM MODULE (TPM)

The MCP6792 is compliant with version 1.2 of the Trusted Computing Group specification for Trusted Platform Modules via the use of the Atmel® ATC97SC3203 TPM. The card's TPM and the chipset's Intel® Trusted Execution Technology (Intel® TXT) maximizes the security and integrity of any system design using a Trenton MCP6792 AMC processor card.

CACHE MEMORY

The Intel® Core™ 2 Duo Processor SL9400 LV is a dual core CPU with 6M of L2 cache memory. The Intel® Core™ 2 Duo Processor SU9300 ULV is also a dual core CPU but with a 3M L2 cache. Both processors have 2 x 32 KB L1 Instruction Caches and 2 x 32 KB L1 Data Caches.

DDR3 MEMORY

The Double Data Rate (DDR3) memory interface is a dual-channel interface that supports up to 4GB of memory and supports memory transfer rates of 800MHz or 1066MHz depending on the memory modules used. Each of the channels (DDR-A and DDR-B) terminates at a small outline dual in-line memory module (SO-DIMM) socket. The System BIOS automatically detects memory type, size and speed.

The SHB uses industry standard gold finger memory modules, which must be PC3-6400 or PC3-8500 compliant and have the following features:

- Gold-plated contacts
- Non-ECC (64-bit) DDR3 memory
- Unbuffered configuration

The following SO-DIMM sizes are supported:

FSB	DIMM Type	Width	Component Density
1066	PC3-8500	x8, x16	256MB, 512MB, 1GB, 2GB
800	PC3-6400	x8, x16	256MB, 512MB, 1GB, 2GB

Trenton's MCP6792 supports Interleaved and Asymmetric memory operations. The mode of memory operation is determined by how the SO-DIMMs are populated. Listed below are descriptions of the Interleaved and Asymmetric memory operations.

Interleaved Mode - This is the mode of operation that enables the highest memory interface speed and bandwidth throughput capability. Often times this mode of operation is referred to as "dual-channel mode". Interleaved mode occurs when using two SO-DIMM modules on the MCP6792 card with equal memory capacities. The SO-DIMM technology and device width can vary but the installed memory capacity for each channel must be equal. If different speed SO-DIMMs are used in each channel then the slowest SO-DIMM will determine the memory interface speed.

Asymmetric Mode - A memory module can be installed in only one SO-DIMM socket. If only one SO-DIMM module is used, it must be populated in SO-DIMM socket 1A. From a system operational standpoint, asymmetric mode functions as a "single-channel" memory interface; therefore, on the MCP6792 card asymmetric mode occurs when using a single SO-DIMM module.

The MCP6792's memory interface operates at maximum bandwidth with two SO-DIMMs of the same size installed in SO-DIMM socket 1A and 1B, but the SO-DIMMs may differ in technology (i.e. component density) and/or device width. For example, when using a single PC3-8500 DIMM, the peak memory interface bandwidth is 8.533GB/s. Placing a PC3-8500 DIMM in each memory socket substantially increases the AMC's theoretical peak memory bandwidth.

PCI EXPRESS INTERFACES

The AMC provides a x4 PCI Express link on the card edge connector that may be organized into either a single x4, one x2 and two x1, or four x1 PCIe electrical links. The default configuration for this link is one x4 PCIe electrical link. An additional x1 PCIe link and two PCI Express reference clocks are also included on the card edge connector. These PCI Express links can be used to support a wide variety of devices and plug-in cards within the *u*TCA or ATCA system. Switch SW2 is a six-position switch located on the back of the AMC and is used to organize the x4 PCIe edge connector link into the three possible link configurations used on the uTCA backplane or AMC slot on the ATCA card. Refer to the *Edge Connector Interfaces* chapter of this manual for more information, including edge connector pin assignments and the option settings for SW2. An internal x4 PCI Express interface on the MCP6792 is used to connect the card's GMCH to a dual-channel Ethernet controller. This Ethernet controller supplies its two Ethernet interfaces (LAN1 and LAN2) to the card edge connector.

UNIVERSAL SERIAL BUS (USB)

The AMC supports a maximum of two front-panel USB 2.0 ports when using a full-size version of the card's front panel. One USB port is available with the mid-size version of the front panel.

VIDEO INTERFACE

The AMC supports a direct VGA video connection via the card's Graphics Memory Controller (GMCH) internal video port. Software drivers are available for most popular operating systems.

ETHERNET INTERFACES

A total of three Ethernet interfaces are supplied by the MCP6792. Two 1000Base-BX Ethernet interfaces are located on the AMC's edge connector and are supported by the two independent channels of the Intel® 82571EB Ethernet controller. The third 10/100/1000Base-T Ethernet interface is generated by the LAN Interconnect Interface (LCI) of the ICH and is delivered to the front panel port via the 1.25GHz Ethernet PHY device.

The main components of the card's Ethernet interfaces are:

- Intel® 82571EB for 1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCIe interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connector on the AMC's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the front panel bracket for status indication (See *Ethernet LEDs and Connector* later in this chapter.)

Software drivers are supplied for most popular operating systems.

DMI INTERFACE

The Intel® GS45 Express chipset utilizes a Direct Media Interface (DMI) connection via a x4 PCIe link between the memory controller hub (MCH) and the I/O controller hub (ICH9M). The purpose of the DMI interface is to provide efficient, high-speed communication between chipset components in order to support high-speed I/O applications. The point-to-point DMI interface features a 32-bit downstream address capability.

SERIAL ATA/300 INTERFACES

The two Serial ATA (SATA II) interfaces that support IDE, RAID 0 and RAID 1 implementations are routed from the ICH to the card edge connector. These interfaces comply with the PICMG 1.3 AMC.3 specification for a Storage Client and support two independent SATA storage devices. SATA produces higher performance interfacing by providing data transfer rates up to 300MB per second on each port.

SPI FLASH

Two Atmel® 16M-bit Serial Firmware DataFlash® Memory or SPI Flash memory devices are provided for the storage and data retention of the card's CMOS memory BIOS parameters and card settings. The estimated data retention of these devices under normal operating conditions is twenty years.

BATTERY

BAT1 is a 3V rechargeable battery located on the bottom side of the AMC and is designed to maintain the real time clock functionality. This soldered down coin-cell battery is charged by the presence of the system's 3.3V Management voltage.

When the AMC is used in a typical MicroTCA system, the system's MCH card provides the real time clock functionality. If the AMC is used on an ATCA carrier card, then the carrier card usually provides the real time clock. For stand-alone AMC applications, the card's battery is used to maintain the real time clock functionality during a power loss condition. During a power loss condition the real-time clock will be maintained for approximately 30 days. When the battery voltage discharges below 2.0V the card's real time clock information will have to be reset after system power is restored.

The battery used on the MCP6792 has a rated lifetime of 10 years and 1,000 charge/discharge cycles. Specifically, the battery will be able to maintain the voltage level to within 10% of the battery's total capacity over these 1,000 cycles. In the case of the battery used on the MCP6792 this means that the voltage under load will stay above 2.7V during the usable life of the battery.

POWER REQUIREMENTS

The following are typical values:

Processor Type	Processor Speed	+12V	+3.3V*
CPU Idle State:			
Core 2 Duo SP9300 SV	2.26GHz	1.17A	0.15A
Core 2 Duo SL9400 LV	1.86GHz	1.09A	0.15A
Core 2 Duo SU9300 ULV	1.20GHz	1.16A	0.15A
100% CPU Stress State:			
Core 2 Duo SP9300 SV	2.26GHz	2.70A	0.15A
Core 2 Duo SL9400 LV	1.86GHz	2.08A	0.15A
Core 2 Duo SU9300 ULV	1.20GHz	1.98A	0.15A

Tolerance for all voltages is +/- 5%
All processors are dual core CPUs
4GB of system memory was installed during power testing
*Management Power current draw is typically less than 150mA

CAUTION: Stand-by voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

TEMPERATURE/ENVIRONMENT

Operating Temperature: -5º C. to 55 C.

Minimum Airflow Requirement: 300LFM

Storage Temperature: - 20º C. to 70º C.

Humidity: 5% to 90% non-condensing

CAUTION: To ensure proper card operation airflow of at least 300 linear feet per minute (LFM) must always be flowing past the MCP6792's passive heat sink.

MECHANICAL

The low profile, passive cooling solution used on the MCP6792 card complies with the height and space restrictions defined in various AMC, ATCA and *u*TCA industry specifications. The AMC's overall card dimensions are 7.11" (18.05cm) L x 2.89" (7.34cm) H. The single-width, full-size front panel height dimension is 1.03" (28.00mm) and the height of the single-width, mid-size front panel is 0.709" (18mm).

IPMI MODULE MANAGEMENT CONTROLLER OVERVIEW

The Module Management Controller (MMC) of the card is a factory programmed Actel AFS6000 FPGA. This component functions as the Management Controller and enables the card's IPMI functionality. Here are some of the IPMI functions supported by the card's management module:

- Voltage Monitoring
  - 12V, 5V, 3.3V, 1.5V, 1.05V, 0.75V
  - 1.8V, 1.1V, 1.0V, 3.3MGNT, 1.5MGNT, CPU Voltage
- Temperature Monitoring
  - Inlet air temperature
  - CPU temperature
- Payload Monitoring
  - Hot Swap status
  - General fault conditions
  - IMPI front panel status LEDs

Specific IPMI alarm conditions, error codes and commands are discussed in detail in the *System Monitoring and Alarms* chapter of this manual.

The Actel AFS6000 management is also programmed to monitor the card's Port 80 codes, the SATA activity and Ethernet link status of the card edge LANS. The management module also drives the full-size front panel's diagnostic LEDs and controls the serial port's messaging traffic.

UL RECOGNITION

The MCP6792 AMC is a UL recognized product, contact Trenton for the UL listed file number. This card was investigated and determined to be in compliance under the Bi-National Standard for Information Technology Equipment. This included the Electrical Business Equipment, UL 60950 and CAN/CSA C22.2 No. 60950-00.

NEBS COMPLIANCE

The MCP6792 AMC Processor Card is designed for NEBS compliant systems testing.

ETHERNET LEDS AND CONNECTOR

The front panel Ethernet interface has two LEDs for status indication and an RJ-45 network connector.

LED/Connector	Description
Activity LED	Green LED which indicates network activity. This is the upper LED on the LAN connector (i.e., toward the P4 USB0 port).
Off	Indicates there is no current network transmit or receive activity.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Green LED which identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the P1 video port).
Off	Indicates a valid link at 1000-Mb/s.
Green	Indicates a valid link at 100-Mb/s.
RJ-45 Network Connector	The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection

POST CODE, DIAGNOSTIC AND OPERATING STATUS LEDS

Post Code LEDs
As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0 through 7, which are located directly behind the card's front panel and are numbered from bottom (0) to top (7). Refer to the board layout earlier in this chapter for the exact location of the POST code LEDs. These POST codes may be helpful as a diagnostic tool. Specific error codes are listed in *Appendix A - BIOS Messages*, along with a chart to interpret the LEDs into hexadecimal format.

Front Panel Diagnostic LEDs *(Full-size Front Panel Versions)*
The card's diagnostic LEDs are numbered 1 through 4 as shown on the card's layout diagram on page 1-4 of this manual. These LEDs provide multiplexed status information. During the card's boot-up process or POST a sliding LED pattern is displayed on the full-size front panel's diagnostic LEDs. If a port80 POST code remains constant for a period greater than four seconds the port 80 code will be displayed on the diagnostic LEDS. First the LEDs will be turned off for one second, and then the upper nibble of the port 80 code will be displayed for 0.5 seconds followed by the lower nibble for 0.5 seconds at which point the sequence will recycle with all LEDS off for one sec. If there were an actual POST-code error these LEDs would continually present the error code. There are some non-error port 80 codes that may be valid for greater than four seconds. Examples on the non-error port 80 codes are memory test and SATA device timeout. If a postcode is valid for greater than four seconds and then POST continues, the LEDS will return to the sliding pattern. Once POST has successfully completed, diagnostic LEDs 1 through 4 will turn off. The diagnostic LEDs are then reconfigured to present the following card operating status indications:

Diagnostic LED	LED Status	Description
LED1	On/Flashing	AMC Ethernet Port 0 Activity
LED2	On/Flashing	AMC Ethernet Port 1 Activity
LED3	On/Flashing	AMC SATA Activity (Port 0 or Port1)
LED4	On/Flashing	LED4 On/Flashing = On-board Solid-state Disk Drive (SDD) Activity

Front Panel Operating Status LEDs *(All Front Panel Versions)*
The backplane LAN LED (LED11), which is located at the center bottom of the SHB, indicates the status of communication between the SHB and the backplane. The remaining front panel LEDs and their functions are illustrated below:

Operating Status LED	LED State	Description
PSON (LED10)	Green - On	Indicates the system power supply has provided all of the correct voltage levels to the card.
PSON (LED10)	Green - Off	Indicates the system power supply has not provided all of the correct voltage levels to the card.
HS (LED9)	Blue - On	On condition of the Hot Swap LED is initiated by pulling on the card's ejection level this indicates that the card can be safely removed.
HS (LED9)	Blue - Off	Normal operating mode condition for Hot Swap LED.
Out Of Service (LED8)	Red - On	OSS indicates that an IPMI monitored process or event has triggered a failed IPMI condition. Does not necessarily mean a fault on the AMC.
Out Of Service (LED8)	Red - Off	Normal operating mode condition.

SYSTEM BIOS SETUP UTILITY

The System BIOS is an AMIBIOS with a ROM-resident setup utility. The BIOS Setup Utility allows you to select the following categories of options:

- Main Menu
- Advanced Setup
- Plug and Play (PCIPnP) Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual.

CONNECTORS AND SWITCHES

P1 - Video Interface Connector
Micro-D DB15 connector, Molex 83612-9020

Pin	Signal	Pin	Signal	Pin	Signal
1	Red	6	Gnd	11	NC
2	Green	7	Gnd	12	VGASDA
3	Blue	8	Gnd	13	HSYNC
4	NC	9	+5	14	VSYNC
5	Gnd	10	Gnd	15	VGASCL

Trenton includes a 7" video pigtail Micro-D-to-D-Sub Socket cable assembly with each card shipment (Trenton part number 60-006934-000) and is designed to be used with standard 15-pin video cables. Other video cable and mating connector options are available from Molex for connecting directly to the Micro-D video connector on the card's front panel. Some of these video cable options are listed below, but for a complete up-to-date listing of all the available connection options from Molex go to www.molex.com.

Molex Cable Assembly Part Number	Description
83422-9053	Micro-D to Micro-D, cable assembly, 18" length
83422-9054	Micro-D to Micro-D, cable assembly, 36" length
83422-9055	Micro-D to Micro-D, cable assembly, 72" length
83422-9056	Micro-D to D-Sub Socket, cable assembly, 18" length
83422-9057	Micro-D to D-Sub Socket, cable assembly, 36" length
83422-9058	Micro-D to D-Sub Socket, cable assembly, 72" length
83422-9059	Micro-D to D-Sub Pin, cable assembly, 18" length
83422-9060	Micro-D to D-Sub Pin, cable assembly, 36" length
83422-9061	Micro-D to D-Sub Pin, cable assembly, 72" length

P2 - RS-232 COMM Connector *(Full Size Front Panel Version)*
Micro-D DB9 connector, Molex 83611-9006

Pin	Signal	Pin	Signal	Pin	Signal
1	Carrier Detect (DCD)	4	Request To Send (RTS)	7	Data Terminal Ready DTR
2	Data Set Ready (DSR)	5	Transmitted Data (TxD)	8	Ring Indicator (RI)
3	Received Data (RxD)	6	Clear To Send (CTS)	9	GND

Trenton includes a 7" RS-232 pigtail Micro-D-to-D-Sub pin cable assembly with each card shipment (Trenton part number 60-006935-000) and is designed to be used with standard 9-pin serial communication cables. Other RS232 COMM cable and mating connector options are available from Molex for connecting directly to the Micro-D RS232 connector on the card's full-size front panel. Some of these communication cable options are listed below, but for a complete up-to-date listing of all the available connection options from Molex go to www.molex.com.

Molex Cable Assembly Part Number	Description
83421-9049	Micro-D to Micro-D, cable assembly, 18" length
83421-9050	Micro-D to Micro-D, cable assembly, 36" length
83421-9051	Micro-D to Micro-D, cable assembly, 72" length
83421-9039	Micro-D to D-Sub Socket, cable assembly, 18" length
83421-9040	Micro-D to D-Sub Socket, cable assembly, 36" length
83421-9041	Micro-D to D-Sub Socket, cable assembly, 72" length
83421-9036	Micro-D to D-Sub Pin, cable assembly, 18" length
83421-9037	Micro-D to D-Sub Pin, cable assembly, 36" length
83421-9038	Micro-D to D-Sub Pin, cable assembly, 72" length

CONNECTORS AND SWITCHES (CONTINUED)

P3 - 10/100/1000Base-T Ethernet Connector – LAN3
RJ-45 connector, Pulse #JOG-0009NL
The cable side of the RJ-45 connector is defined as follows:

Pin	Signal	
1	TRP1+	(Card side signal = MDI0+)
2	TRP1-	(Card side signal = MDI0-)
3	TRP2+	(Card side signal = MDI1+)
4	TRP3+	(Card side signal = MDI2+)
5	TRP3-	(Card side signal = MDI2-)
6	TRP2-	(Card side signal = MDI1-)
7	TRP4+	(Card side signal = MDI3+)
8	TRP4-	(Card side signal = MDI3-)

P4 - Dual Stacked Universal Serial Bus (USB) Connector *(Full Size Front Panel Version)*
Dual 4-position connectors within a common right-angle housing, Molex #67298-4091

Pin	Signal	Pin	Signal
1	VCC-USB0	5	VCC-USB1
2	USB0-	6	USB1-
3	USB0+	7	USB1+
4	Gnd-USB0	8	Gnd-USB1

P4 - Universal Serial Bus (USB) Connector *(Mid Size Front Panel Version)*
4-position connector in a right-angle housing, Molex #67643-0910

Pin	Signal
1	VCC-USB0
2	USB0-
3	USB0+
4	Gnd-USB0

P5 - Universal Serial Bus (USB) Flash Drive Connector
10-position vertical header, 2mm, unshrouded, Samtec #TW-05-02-L-D-180-SM

Pin	Signal	Pin	Signal
1	VCC-USB2	6	NC
2	NC	7	Gnd-USB2
3	USB2-	8	NC
4	NC	9	Key
5	USB2+	10	Flash LED

CONNECTORS AND SWITCHES (CONTINUED)

AMC1 - AMC Edge Card Connector

170 position card edge connector, Refer to PICMG AMC.0, R2.0 Specification

Position	Signal	Position	Signal
1	Gnd	170	Gnd
2	+12V	169	TDI*
3	PS1#	168	TDO*
4	MP PWR	167	*TRST#*
5	GA0	166	*TMS*
6	*RSRVD6*	165	*TCK*
7	Gnd	164	Gnd
8	*RSRVD8*	163	*TX20+*
9	+12V	162	*TX20-*
10	Gnd	161	Gnd
11	TX0+ (Ethernet LAN1)	160	*RX20+*
12	TX0- (Ethernet LAN1)	159	*RX20-*
13	Gnd	158	Gnd
14	RX0+ (Ethernet LAN1)	157	*TX19+*
15	RX0- (Ethernet LAN1)	156	*TX19-*
16	Gnd	155	Gnd
17	GA1	154	*RX19+*
18	+12V	153	*RX19-*
19	Gnd	152	Gnd
20	TX1+ (Ethernet LAN2)	151	*TX18+*
21	TX1- (Ethernet LAN2)	150	*TX18-*
22	Gnd	149	Gnd
23	RX1+ (Ethernet LAN2)	148	*RX18+*
24	RX1- (Ethernet LAN2)	147	*RX18-*
25	Gnd	146	Gnd
26	GA2	145	*TX17+*
27	+12V	144	*TX17-*
28	Gnd	143	Gnd
29	TX2+ (SATA0)	142	*RX17+*
30	TX2- (SATA0)	141	*RX17-*
31	Gnd	140	Gnd
32	RX2+ (SATA0)	139	*TCLKD+*
33	RX2- (SATA0)	138	*TCLKD-*
34	Gnd	137	Gnd
35	TX3+ (SATA1)	136	*TCLKC+*
36	TX3- (SATA1)	135	*TCLKC-*
37	Gnd	134	Gnd
38	RX3+ (SATA1)	133	*TX15+*
39	RX3- (SATA1)	132	*TX15-*
40	Gnd	131	Gnd
41	ENABLE# (AMC Enable)	130	*RX15+*
42	+12V	129	*RX15-*
43	Gnd	128	Gnd
44	TX4+ (PCI Express)	127	*TX14+*
45	TX4- (PCI Express)	126	*TX14-*
46	Gnd	125	Gnd
47	RX4+ (PCI Express)	124	*RX14+*
48	RX4- (PCI Express)	123	*RX14-*
49	Gnd	122	Gnd
50	TX5+ (PCI Express)	121	*TX13+*
51	TX5- (PCI Express)	120	*TX13-*

* Pins jumpered together

AMC1 - AMC Edge Card Connector (continued)
170 position card edge connector, Refer to PICMG AMC.0, R2.0 Specification

Position	Signal	Position	Signal
52	Gnd	119	Gnd
53	RX5+ (PCI Express)	118	*RX13+*
54	TX5- (PCI Express)	117	*RX13-*
55	Gnd	116	Gnd
56	SCL_L (IPMB-L Clock)	115	*TX12+*
57	+12V	114	*RX12-*
58	Gnd	113	Gnd
59	TX6+ (PCI Express)	112	*RX12+*
60	TX6- (PCI Express)	111	*RX12-*
61	Gnd	110	Gnd
62	RX6+ (PCI Express)	109	*TX11+*
63	RX6- (PCI Express)	108	*TX11-*
64	Gnd	107	Gnd
65	TX7+ (PCI Express)	106	*RX11+*
66	TX7- (PCI Express)	105	*RX11-*
67	Gnd	104	Gnd
68	RX7+ (PCI Express)	103	*TX10+*
69	RX7- (PCI Express)	102	*TX10-*
70	Gnd	101	Gnd
71	SDA_L (IMPB-L Data)	100	*RX10+*
72	+12V	99	*RX10-*
73	Gnd	98	Gnd
74	*TCLKA+*	97	*TX9+*
75	*TCLKA-*	96	*TX9-*
76	Gnd	95	Gnd
77	*TCLKB+*	94	*RX9+*
78	*TCLKB-*	93	*RX9-*
79	Gnd	92	Gnd
80	FCLKA+ (PCIe Clock)	91	TX8+ (PCI Express)
81	FCLKA- (PCIe Clock)	90	TX8- (PCI Express)
82	Gnd	89	Gnd
83	PS0#	88	RX8+ (PCI Express)
84	+12V	87	RX8- (PCI Express)
85	Gnd	86	Gnd

Italics indicates no connects on the AMC6792 card.

SW2 - PCI Express Backplane Link Configuration Switch & Clear CMOS Reset
6-position dip switch, C&K #TDA06H0SB1

Card Configuration	**SW2 Settings**
Normal Operation (default)	SW2-1 = OFF, *default*
Clear CMOS*	SW2-1 = ON
PCIe Link Org. = 4, x1 PCI Express Ports	SW2-2 = ON & SW2-3 = ON
PCIe Link Org. = 1, x2 & 2, x1 PCIe Ports	SW2-2 = ON & SW2-3 = OFF
Reserved	SW2-2 = OFF & SW2-3 = ON
PCIe Link Org. = 1, x4 PCI Express Port	SW2-2 = OFF & SW2-3 = OFF, *default*
Fabric Clock Select – Normal	SW2-4 = OFF, *default*
Fabric Clock Select – Force AMC CLK Src.	SW2-4 = On
Reserved	SW2-5
Reserved	SW2-6

*Toggle SW2-1 on and then off to effect a Clear CMOS operation. There is no need for the card to be under power to Clear CMOS.

Chapter 2 Edge Connector Interfaces

PCI EXPRESS IMPLEMENTATION

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between cards and a backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between MicroTCA cards or between the AMC processor card and the AdvancedTCA carrier.

A PCI Express link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. The MicroTCA specification supports routing a x4 and a x1 PCI link to the backplane.

The x1 PCIe link provided by the MCP6792 card has a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The card's x4 PCIe link has a full-duplex bandwidth of 2GB/s. This link may be re-configured into four, x1 PCIe links using the card's PCI Express Backplane Link Configuration Switch SW2. The default setting for this PCI Express backplane link is x4 since the four individual x1 PCIe links are not supported in the MicroTCA specification.

One PCI Express fabric clock is also available for use on either the MicroTCA backplane or the AdvancedTCA carrier card slot. Here are the PCI Express link configuration settings available on switch SW2:

Card Configuration	**SW2 Settings**
PCIe Link Org. = 4, x1 PCI Express Ports	SW2-2 = ON & SW2-3 = ON
PCIe Link Org. = 1, x2 & 2, x1 PCIe Ports	SW2-2 = ON & SW2-3 = OFF
PCIe Link Org. = 1, x4 PCI Express Port	SW2-2 = OFF & SW2-3 = OFF*, default*
Fabric Clock Select – Normal	SW2-4 = OFF*, default*
Fabric Clock Select – Force AMC CLK Src.	SW2-4 = On

For more information, refer to the PCI Industrial Manufacturers Group's *PICMG® AMC.0 R2.0 and PICMG® AMC.1 R2.0 Specifications*.

BACKPLANE ETHERNET INTERFACES

Two 1000Base-BX Ethernet interfaces are routed directly to the edge card connector from the card's dual channel Ethernet controller. This Intel® 82571EB Ethernet Controller is driven with a x4 PCI Express link directly from the Graphics Memory Controller Hub or the Intel® GS45. This results in two very efficient and high-speed Ethernet interfaces being available for use on the MicroTCA backplane or on the AMC slot of AdvancedTCA carrier card. Each edge card LAN uses two differential pairs for transmit and receive. LAN1 is located on edge card connector locations 11, 12, 14 and 15 while LAN2 can be found on locations 20, 21, 23 and 24. See the *AMC Edge Card Connector* pin out listing in Chapter 1 for specific Ethernet signal locations on the edge connector of the AMC.

SATA II INTERFACES

The Two Serial ATA/300 (i.e. SATA II 300) interfaces on the MCP6792 are available for use on the AMC's card edge connector. A typical MicroTCA system may have a couple of SATA II storage module cards plugged into the chassis. The interoperability standards defined in the PICMG® AMC.0 R2.0 Mezzanine Module and PICMG® AMC.3 Storage specifications define the locations on the AMC's edge connector that carry the SATA II communication signals in order to ensure that the *u*TCA storage cards communicate to the MCP6792 card. **It is important to note that the MCP6792 supports SATA II signaling and that the storage cards must use SATA II drives or if using SATA I drives, the storage card must be able to accommodate SATA II drive interface signals.** Likewise when using the AMC on an AdvancedTCA carrier card with a SATA drive; the ACTA carrier card must be able to accommodate SATA II drive interface signals. IDE, RAID 0 and RAID 1 drive implementations are supported by the AMC's SATA II interfaces. The AMC's SATA0 transmit and receive signal locations on the edge connector are 11, 12, 14 and 15 while SATA1 interface locations are 20, 21, 23 and 24. See the *AMC Edge Card Connector* pin out listing in Chapter 1 for more detailed SATA II signal location information.

IPMI, POWER, GROUND (GND) AND OTHER CARD CONNECTIONS

There are several edge card signals related to supporting the IPMI capability of the AMC. These signals are as follows:

- SDA_L and SDCL-L – These lines make up the IPMB-L or local IPMI data signals to the card's MMC or Management Controller.
- ENABLE# - This active low input is pulled high when the Management Power (MP PWR) line reaches the correct voltage levels and is inverted on the AMC to create a RESET# signal which tells the MMC that the card is fully inserted and valid power states exist on all card inputs. An ENABLE# that is inactive prevents the card's MMC from reading the geographic addressing (GA) lines or sensing the IPMB-L signals.
- MP PWR - Management Power line
- PS0# and PS1# - The connections are located on opposite sides of the AMC's edge connector and last connections made when inserting the card into a MicroTCA chassis or an AMC slot on an AdvancedTCA carrier cars. These signal lines are used to detect the presence of an AMC card.
- GA0, GA1, GA2 – These are geographic address lines that are read by the card's MMC. These signals carry the specific address of the AMC and let the MMC know which sensors or modules are sending IMPI input information or where the MMC needs to send IMPI commands within the system.

There are several +12V and ground pins on the edge connector and the locations of these inputs are defined by the PICMG specifications.

There are a number of signal locations that are defined, but not needed on the AMC. These signal locations are define by the various specifications for use on other types of AMC card designs and not needed for this AMC processor card design.

A jumper on the AMC is used to connect locations 169 (TDI) and 168 (TDO) together.

See the *AMC Edge Card Connector* pin out listing in Chapter 1 for more detailed signal location information.

Chapter 3 System BIOS

BIOS OPERATION

Chapters 3 through 7 of this manual describe the operation of the American Megatrends AMIBIOS and the BIOS Setup Utility. Refer to *Running AMIBIOS Setup* later in this chapter for standard Setup screens, options and defaults. The available Setup screens, options and defaults may vary if you have a custom BIOS.

When the system is powered on, AMIBIOS performs the Power-On Self Test (POST) routines. These routines are divided into two phases:

1) **System Test and Initialization**. Test and initialize system boards for normal operations.

2) **System Configuration Verification**. Compare defined configuration with hardware actually installed.

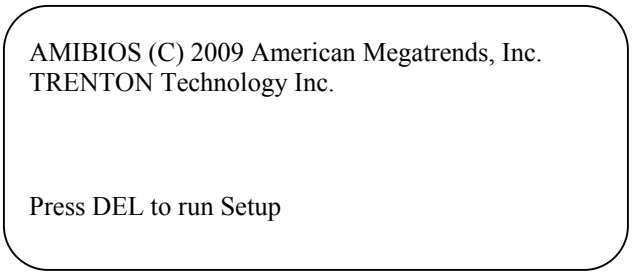
If an error is encountered during the diagnostic tests, the error is reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps are transmitted. If the error occurs after the display device is initialized, the error message is displayed on the screen. See *BIOS Errors* later in this section for more information on error handling.

The following are some of the Power-On Self Tests (POSTs), which are performed when the system is powered on:

- CMOS Checksum Calculation
- Keyboard Controller Test
- CMOS Shutdown Register Test
- 8254 Timer Test
- Memory Refresh Test
- Display Memory Read/Write Test
- Display Type Verification
- Entering Protected Mode
- Memory Size Calculation
- Conventional and Extended Memory Test
- DMA Controller Tests
- System Configuration Verification and Setup

AMIBIOS checks system memory and reports it on both the initial AMIBIOS screen and the AMIBIOS System Configuration screen which appears after POST is completed. AMIBIOS attempts to initialize the peripheral devices and if it detects a fault, the screen displays the error condition(s) which has/have been detected. If no errors are detected, AMIBIOS attempts to load the system from a bootable device, such as a floppy disk or hard disk. Boot order may be specified by the **Boot Device Priority** option on the Boot Setup Menu as described in the *Boot Setup* chapter later in this manual.

Normally, the only POST routine visible on the screen is the memory test. The following is a sample portion of the initial BIOS start-up screen that is displayed when the system is powered on:



Initial Power-On Screen

There are additional status messages and other text displayed on the screen and you have two options:

- Press **<Del>** to access the BIOS Setup Utility.

  This option allows you to change various system parameters such as date and time, disk drives, etc. The *Running AMIBIOS Setup* section of this manual describes the options available.

  You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* later in this section.)

  If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays. (See *Running AMIBIOS Setup* later in this section.)

- Allow the bootup process to continue without invoking the BIOS Setup Utility.

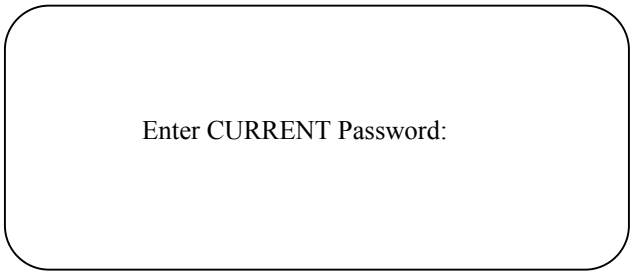
  In this case, after AMIBIOS loads the system, you may be requested to enter a password. (See *Password Entry* later in this section.)

Once the POST routines complete successfully, a screen displays showing the current configuration of your system, including processor type, base and extended memory amounts, hard drive types, display type and peripheral ports.

Password Entry
The system may be configured so that the user is required to enter a password each time the system boots or whenever an attempt is made to enter the BIOS Setup Utility. The password function may also be disabled so that the password prompt does not appear under any circumstances.

The **Password Check** option in the Security Menu allows you to specify when the password prompt displays: **Always** or only when **Setup** is attempted. This option is available only if the supervisor and/or user password(s) have been established. The supervisor and user passwords may be changed using the **Change Supervisor Password** and **Change User Password** options on the Security Menu. If the passwords are null, the password prompt does not display at any time. See the *Security Setup* section of this chapter for details on setting up passwords.

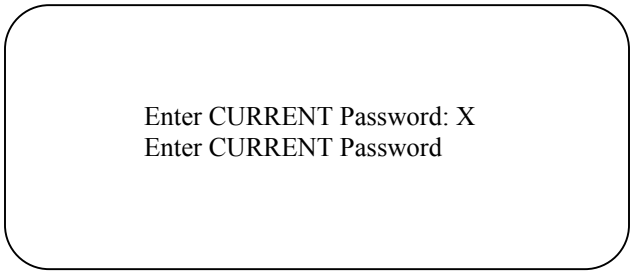
When password checking is enabled, the following password prompt displays:



Type the password and press **<Enter>**.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the password prompt does not display. To set up passwords, you may use the **Change Supervisor Password** and **Change User Password** options on the Security Menu of the BIOS Setup Utility. (See the *Security Setup* section later in this chapter.)

If an incorrect password is entered, the following screen displays:



You may try again to enter the correct password. If you enter the password incorrectly three times, the system responds in one of two different ways, depending on the value specified in the **Password Check** option on the *Security* Menu:

1) If the **Password Check** option is set to **Setup**, and you enter the incorrect password, the system displays the "Password check failed" message and the system does not let you enter Setup, but it does continue the booting process. You must reboot the system manually to retry entering the password in order to enter the BIOS setup menus.

2) If the **Password Check** option is set to **Always**, and you enter the incorrect password, the system locks, displays the "Password check failed" and "Fatal Error…System Halted" messages. You must reboot the system manually to retry entering the password in order to enter the BIOS setup menus.

The BIOS defaults for the supervisor and user passwords are set to "Not Installed".

BIOS ERRORS

If an error is encountered during the diagnostic checks performed when the system is powered on, the error is reported in one of two different ways:

1) If the error occurs before the display device is initialized, a series of signals are transmitted to the post code LEDs on the module and the status LEDs of full-size version of the AMC.

2) If the error occurs after the display device is initialized, the screen displays the error message as well as the module's post code LEDs. In the case of a non-fatal error, a prompt to press the **<F1>** key may also appear on the screen.

Explanations of the post code LEDs and BIOS error messages may be found in *Appendix A - BIOS Messages*.

As the POST routines are performed, test codes are presented on Port 80H. These codes may be helpful as a diagnostic tool and are listed in *Appendix A - BIOS Messages*.

If certain non-fatal error conditions occur, you are requested to run the BIOS Setup Utility. The error messages are followed by this screen:

```
AMIBIOS (C)2008 American Megatrends, Inc.
TRENTON Technology Inc.


Press F1 to Run SETUP
Press F2 to load default values and continue
```

RUNNING AMIBIOS SETUP

The BIOS is an AMIBIOS with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. Two Atmel® 16M-bit Serial Firmware DataFlash® Memory or SPI Flash memory devices are provided for the storage and data retention of the card's CMOS memory BIOS parameters and card settings.

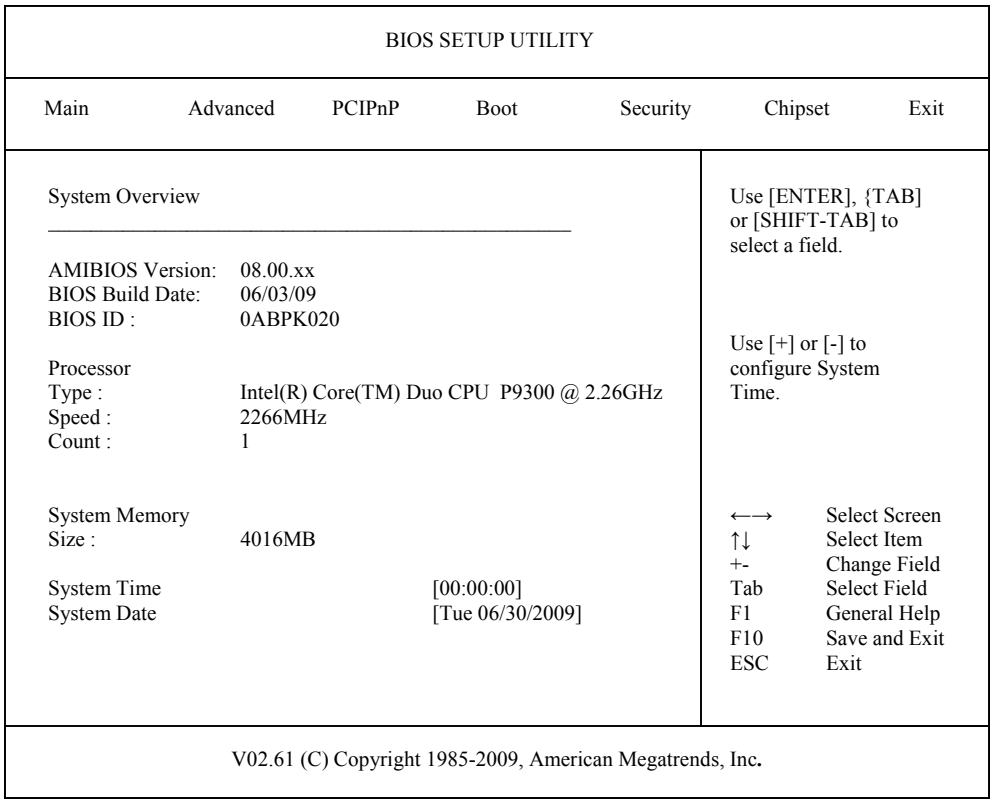
Each time the system is powered on, it is configured with these values, unless the CMOS has been corrupted or is faulty. The BIOS Setup Utility is resident in the module's SPI Flash devices so that it is available each time the computer is turned on. If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file. The estimated data retention of the SPI Flash Memory devices under normal operating conditions is twenty years.

As soon as the system is turned on, the power-on diagnostic routines check memory, attempt to prepare peripheral devices for action, and offer you the option of pressing **<Del>** to run the BIOS Setup Utility.

If certain non-fatal errors occur during the Power-On Self Test (POST) routines that are run when the system is turned on, you may be prompted to run the BIOS Setup Utility by pressing **<F1>**.

BIOS SETUP UTILITY MAIN MENU

When you press **<F1>** in response to an error message received during the POST routines or when you press the **<Del>** key to enter the BIOS Setup Utility, the following screen displays:



BIOS Setup Utility Main Menu

When you display the BIOS Setup Utility Main Menu, the format is similar to the sample shown above. The data displayed on the top portion of the screen details parameters detected by AMIBIOS for your processor board and may not be modified. The system time and date displayed on the bottom portion of the screen may be modified.

BIOS SETUP UTILITY MAIN MENU OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

System Time/System Date

These options allow you to set the correct system time and date. If you do not set these parameters the first time you enter the BIOS Setup Utility, you will receive a "Run SETUP" error message when you boot the system until you set the correct parameters.

The Setup screen displays the system options:

System Time	**[00:00:00]**
System Date	**[Tue 06/30/2009]**

There are three fields for entering the time or date. Use the **<Tab>** key or the **<Enter>** key to move from one field to another in the same line and the **<**↑> and <↓> to move between the System Time and System

Date lines. Type in the correct value for each field and hit enter after each entry. Hit the **F10** key to save the changes and exit. If you enter an invalid value in any field, the screen will revert to the previous value when you move to the next field. When you change the value for the month, day or year field, the day of the week changes automatically when you move to the next field.

BIOS SETUP UTILITY OPTIONS

The BIOS Setup Utility allows you to change system parameters to tailor your system to your requirements. Various options, which may be changed, are listed below. Further explanations of these options and available values may be found in later chapters of this manual, as noted below.

NOTE: Do *not* change the values for any option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Use the **Right Arrow** key to display the desired menu. The following menus are available:

- Select **Advanced** to make changes to Advanced Setup parameters as described in the *Advanced Setup* chapter of this manual. The following options may be modified:
    - CPU Configuration
        - Hardware Prefetcher
        - Adjacent Cache Line Prefetch
        - Max CPUID Value Limit
        - Intel (R) Virtualization Tech
        - Execute-Disable Bit Capability
        - Intel (R) SpeedStep(tm) tech
        - Intel (R) C-STATE tech
        - Enhanced C-States
    - IDE Configuration
        - SATA#1 Configuration
            - Configure SATA#1 as
        - SATA Speed Negotiation Limit
        - Primary IDE Master
        - Secondary IDE Master
        - Hard Disk Write Protect
        - IDE Detect Time Out (Sec)
        - ATA(PI) 80Pin Cable Detection
    - SuperIO Configuration
        - Serial Port1 Address
    - Advanced ACPI Configuration
        - ACPI Version Features
        - ACPI APIC Support
        - AMI OEMB Table
        - Headless Mode

- Chipset ACPI Configuration
    - Energy Lake Feature
    - APIC ACPI SCI IRQ
    - USB Device Wakeup From S3/S4
    - High Performance Event Timer
    - HPET Memory Address
- AHCI Configuration
    - ACHI BIOS Support
    - AHCI CD/DVD Boot Time out
    - AHCI Port 0
        - SATA Port0
        - S.M.A.R.T.
    - AHCI Port 1
        - SATA Port1
        - S.M.A.R.T.
- Intel TXT(LT) Configuration
    - Intel TXT Initialization
- MPS Configuration
    - MPS Revision
- PCI Express Configuration
    - Active State Power-Management
- Smbios Configuration
    - Smbios Smi Support
- Remote Access Configuration
    - Remote Access
- Trusted Computing
    - TCG/TPM Support
- USB Configuration
    - Legacy USB Support
    - USB 2.0 Controller Mode
    - BIOS EHCI Hand-Off

- Select **PCIPnP** to make changes to Advanced PCI Plug and Play Settings as described in the *PCI Plug and Play Setup* chapter of this manual. The following options may be modified:
    - Clear NVRAM
    - Plug & Play O/S
    - Allocate IRQ to PCI VGA
    - Palette Snooping
    - GBE LAN Boot
- Advanced PCI Plug and Play Settings (continued)
    - IRQs 3, 4, 5, 7, 9, 10, 11, 14 and 15
    - DMA Channel 0, 1, 3, 5, 6 and 7

- Select **Boot** to make changes to Boot Setup parameters as described in the *Boot Setup* chapter of this manual. The following options may be modified:
    - Boot Settings Configuration
        - Quick Boot
        - Quiet Boot
        - AddOn ROM Display Mode
        - Bootup Num-Lock
        - PS/2 Mouse Support
        - Wait For 'F1' If Error
        - Hit 'DEL' Message Display
        - Interrupt 19 Capture
    - Boot Device Priority
        - 1st Boot Device
        - 2nd Boot Device
        - 3rd Boot Device
    - Hard Disk Drives
        - 1st Drive

- Select **Security** to establish or change the supervisor or user password or to enable boot sector virus protection. These functions are described later in this chapter. The following options may be modified:
    - Change Supervisor Password
    - Change User Password
    - Clear User Password (Note: shows up only if a user password has been entered.)
    - Boot Sector Virus Protection

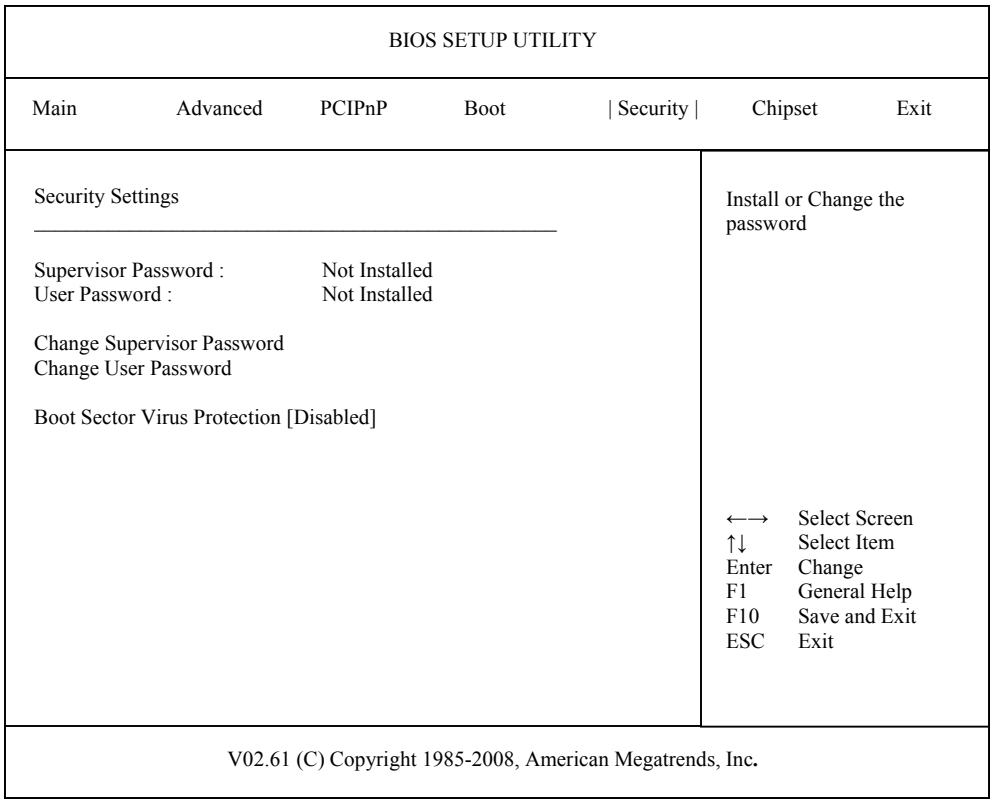
- Select **Chipset** to make changes to Chipset Setup parameters as described in the *Chipset Setup* chapter of this manual. The following options may be modified:
    - North Bridge Chipset Configuration
        - Boots Graphic Adapter Priority
        - Internal Graphics Mode Select
        - Max TOLUD
        - Video Function Configuration
            - DVMT Mode Select
                - DVMT/Fixed Memory
            - Spread Spectrum Clock

- South Bridge Configuration
    - USB Functions
    - USB 2.0 Controller
    - LCI LAN Controller
        - LCI LAN Boot
    - SMBUS Controller
    - Front Panel Serial Port (Full-size front-panel configurations only.)
    - SLP_S4# Min. Assertion Width
    - PCIE Ports Configuration
        - PCIE Port 0
        - PCIE Port 1
        - PCIE Port 2
        - PCIE Port 3
        - PCIE Port 4
        - PCIE High Priority Port
        - PCIE Port 0 IOxAPIC Enable
        - PCIE Port 1 IOxAPIC Enable
        - PCIE Port 2 IOxAPIC Enable
        - PCIE Port 3 IOxAPIC Enable
        - PCIE Port 4 IOxAPIC Enable
        - PCIE Port 5 IOxAPIC Enable

- Select **Exit** to save or discard changes you have made to AMIBIOS parameters or to load the Optimal or Failsafe default settings. These functions are described later in this chapter. The following options are available:
    - Save Changes and Exit
    - Discard Changes and Exit
    - Discard Changes
    - Load Optimal Defaults
    - Load Failsafe Defaults

SECURITY SETUP

When you select **Security** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Security Setup Screen

When you display the Security Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>**.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your AMC. Refer to the explanations below for specific instructions about entering correct information.

SECURITY SETUP OPTIONS

The Security Setup options allow you to establish, change or clear the supervisor or user password and to enable boot sector virus protection.

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

CHANGE SUPERVISOR PASSWORD

This option allows you to establish a supervisor password, change the current password or disable the password prompt by entering a null password. The password is stored in CMOS RAM.

If you have signed on under the user password, this option is *not* available.

The **Change Supervisor Password** feature can be configured so that a password must be entered each time the system boots or just when a user attempts to enter the BIOS Setup Utility.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the "Enter CURRENT Password" prompt is bypassed when you boot the system, and you must establish a new password.

If you select the **Change Supervisor Password** option, the following window displays:

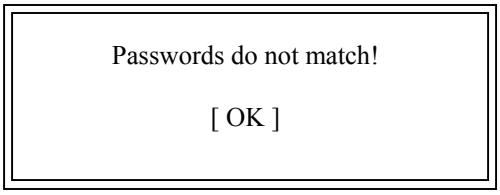
This is the message that displays before you have established a password, or if the last password entered was the null password. If a password has already been established, you are asked to enter the *current* password before being prompted to enter the *new* password.

Type the new password and press **<Enter>**. The password cannot exceed six (6) characters in length. The screen displays an asterisk (*****) for each character you type.

After you have entered the new password, the following window displays:

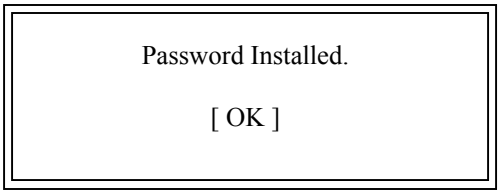
Re-key the new password as described above.

If the password confirmation is miskeyed, AMIBIOS Setup displays the following message:



No retries are permitted; you must restart the procedure.

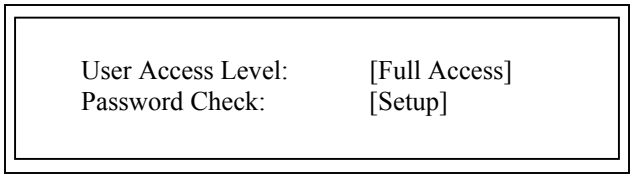
If the password confirmation is entered correctly, the following message displays:



Press the **<Enter>** key to return to the Security screen. **Installed** displays on the screen next to the **Supervisor Password** option, indicating the password has been accepted. This setting will remain in effect until the supervisor password is either disabled or discarded upon exiting the BIOS Setup Utility. If you have created a new password, be sure to select **Exit**, then **Save Changes and Exit** to save the password. The password is then stored in CMOS. The next time the system boots, you are prompted for the password.

NOTE: Be sure to keep a record of the new password each time it is changed.

If a password has been established, the following options and their default values are added to the screen:



User Access Level

This option allows you to define the level of access the user will have to the system.

The Setup screen displays the system option:

User Access Level [Full Access]

Four options are available:

- Select **No Access** to prevent user access to the BIOS Setup Utility.
- Select **View Only** to allow access to the BIOS Setup Utility for viewing, but to prevent the user from changing any of the fields.
- Select **Limited** to allow the user to change only a limited number of options, such as Date and Time.
- Select **Full Access** to allow the user full access to change any option in the BIOS Setup Utility.

Password Check

This option determines when a password is required for access to the system.

The Setup screen displays the system option:

Password Check [Setup]

Two options are available:

- Select **Setup** to have the password prompt appear only when an attempt is made to enter the BIOS Setup Utility program.
- Select **Always** to have the password prompt appear each time the system is powered on.

DISABLING THE SUPERVISOR PASSWORD

To *disable* password checking so that the password prompt does not appear, you may create a null password by selecting the **Change Supervisor Password** function and pressing **<Enter>** without typing in a new password. You will be asked to enter the current password before being allowed to enter the null password. After you press **<Enter>** at the **Enter New Password** prompt, the following message displays:

CHANGE USER PASSWORD

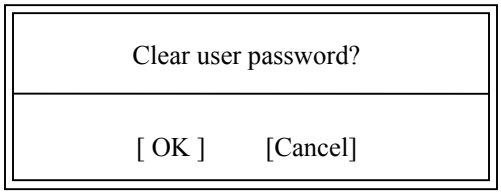
The **Change User Password** option is similar in functionality to the **Change Supervisor Password** and displays the same messages. If you have signed on under the user password, the **Change Supervisor Password** function is not available for modification.

If a user password has been established, the **Password Check** option and its default value is added to the screen. This option determines when a user password is required for access to the system. For details, refer to the description for **Password Check** under the **Change Supervisor Password** heading earlier in this section.

CLEAR USER PASSWORD

This option allows you to clear the user password. It disables the user password by entering a null password.

If you select the **Clear User Password** option, the following window displays:



You have two options:

- Select **Ok** to clear the user password.
- Select **Cancel** to leave the current user password in effect.

BOOT SECTOR VIRUS PROTECTION

This option allows you to request AMIBIOS to issue a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.
The Setup screen displays the system option:

Boot Sector Virus Protection [Disabled]

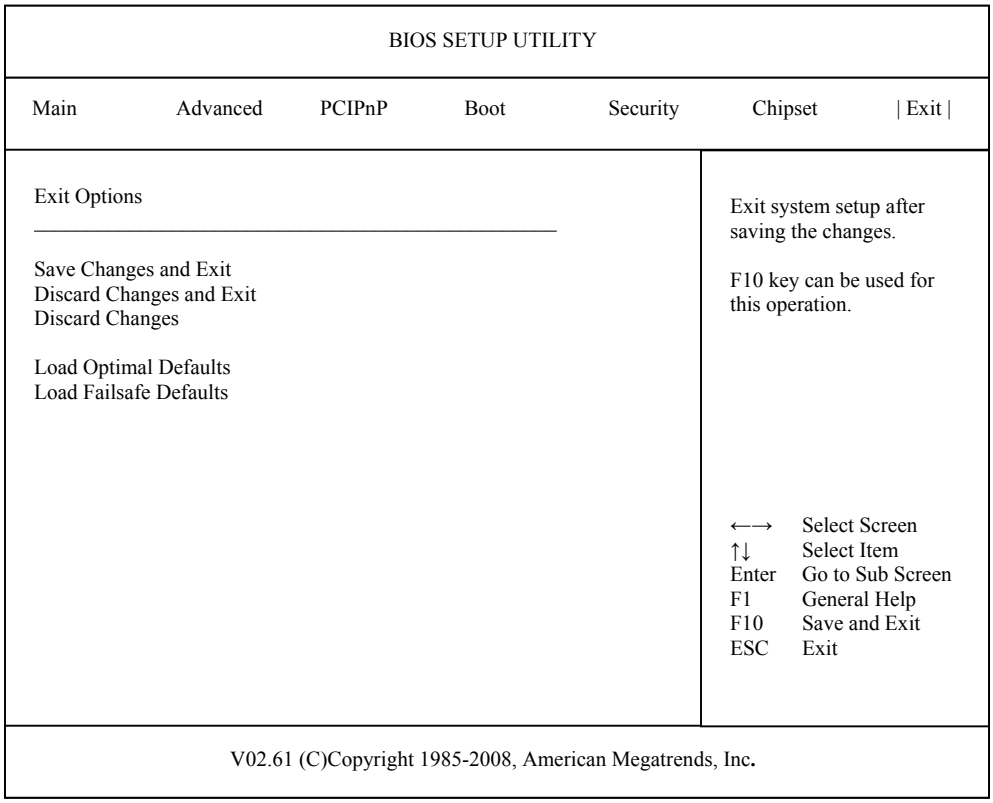
Available options are:

Disabled
Enabled

NOTE: You should *not* enable boot sector virus protection when formatting a hard drive.

EXIT MENU

When you select Exit from the BIOS Setup Utility Main Menu, the following screen displays:



Exit Menu Screen

When you display the Exit Menu screen, the format is similar to the sample shown above. Highlight the option you wish to select and press **<Enter>**.

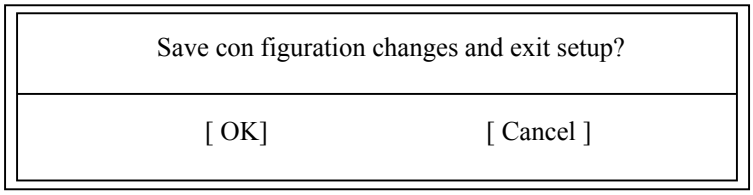
EXIT MENU OPTIONS

When you are running the BIOS Setup Utility program, you may either save or discard changes you have made to AMIBIOS parameters, or you may load the Optimal or Failsafe default settings.

Save Changes and Exit

The features selected and configured in the Setup screens are stored in the CMOS when this option is selected. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the AMIBIOS and the booting process continues, using the new CMOS values.

If you select the **Save Changes and Exit** option, the following window displays:

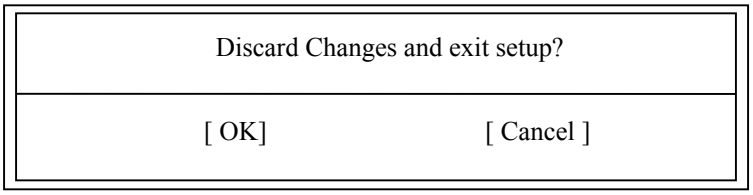


You have two options:

- Select **Ok** to save the system parameters and continue with the booting process.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes and Exit
When the **Discard Changes and Exit** option is selected, the BIOS Setup Utility exits *without* saving the changes in the CMOS. Control is then passed back to AMIBIOS and the booting process continues, using the previous CMOS values.

If you select the **Discard Changes and Exit** option, the following window displays:

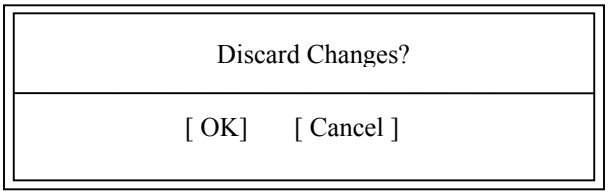


You have two options:

- Select **Ok** to continue the booting process *without* writing any changes to the CMOS.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes
When the Discard Changes option is selected, the BIOS Setup Utility resets any parameters you have changed back to the values at which they were set when you entered the Setup Utility. Control is then passed back to the BIOS Setup Utility screen.

If you select the Discard Changes option, the following window displays:



You have two options:

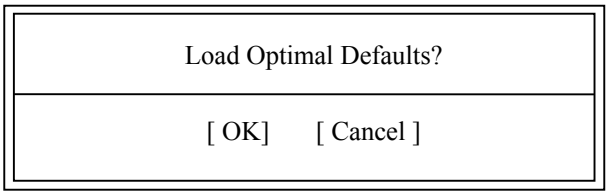
- Select Ok to reset any parameters you have changed back to the values at which they were set when you entered the BIOS Setup Utility. This option then returns you to the BIOS Setup Utility screen.
- Select Cancel to return to the BIOS Setup Utility screen without discarding any changes you have made.

Load Optimal or Failsafe Defaults
Each AMIBIOS Setup option has two default settings (Optimal and Failsafe). These settings can be applied to all AMIBIOS Setup options when you select the appropriate configuration option from the BIOS Setup Utility Main Menu.

You can use these configuration options to quickly set the system configuration parameters which should provide the best performance characteristics, or you can select a group of settings which have a better chance of working when the system is having configuration-related problems.

Load Optimal Defaults
This option allows you to load the Optimal default settings. These settings are best-case values, which should provide the best performance characteristics. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

If you select the **Load Optimal Defaults** option, the following window displays:

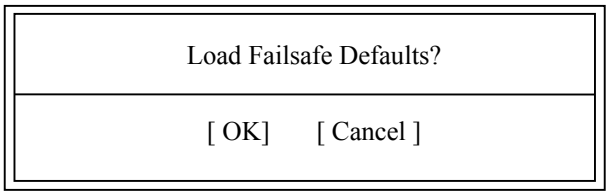


You have two options:

- Select Ok to load the Optimal default settings.
- Select Cancel to leave the current values in effect.

Load Failsafe Defaults This option allows you to load the Failsafe default settings when you cannot boot your computer successfully. These settings are more likely to configure a workable computer. They may not provide optimal performance, but are the most stable settings. You may use this option as a diagnostic aid if your system is behaving erratically. Select the Failsafe settings and then try to diagnose the problem after the computer boots.

If you select the **Load Failsafe Defaults** option, the following window displays:



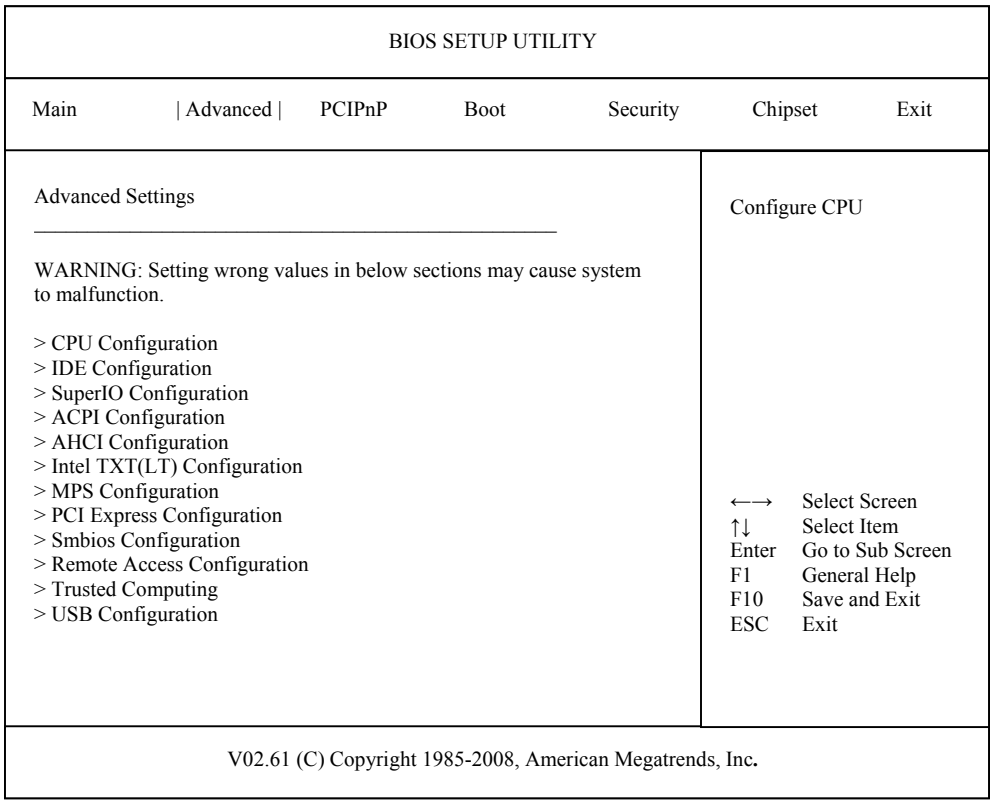
You have two options:

- Select **Ok** to load the Failsafe default settings.
- Select **Cancel** to leave the current values in effect.

Chapter 4 Advanced Setup

ADVANCED SETUP

When you select **Advanced** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



When you display the Advanced Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Advanced Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

ADVANCED SETUP OPTIONS

NOTE: Do *not* change the values for any Advanced Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

CPU Configuration
The **CPU Configuration** subscreen provides you with information about the processor in your system. This top potion of the screen is for informational purposes only and cannot be changed. The following options may be modified:

- CPU Configuration
    - Hardware Prefetcher
    - Adjacent Cache Line Prefetch
    - Max CPUID Value Limit
    - Intel(R) Virtualization Tech
    - Execute-Disable Bit Capability
    - Intel(R) SpeedStep(tm) tech
    - Intel(R) C-STATE tech
    - Enhanced C-States

IDE Configuration
The options on the **IDE Configuration** subscreens allow you to set up or modify parameters for your IDE controller and hard disk drive(s). The following options may be modified:

- IDE Configuration
    - SATA#1 Configuration
        - Configure SATA#1 as
    - SATA Speed Negotiation Limit
    - Primary IDE Master
    - Primary IDE Slave
        - Type
        - LBA/Large Mode
        - Block (Multi-Sector Transfer)
        - PIO Mode
        - DMA Mode
        - S.M.A.R.T.
        - 32Bit Data Transfer
    - Hard Disk Write Protect
    - IDE Detect Time Out (Sec)
    - ATA(PI) 80Pin Cable Detection

SuperIO Configuration
The options on the **SuperIO Configuration** subscreen allow you to set up or modify parameters for AMC's internal serial port routings to the Module Management Controller (MMC). Only on the full-size front panel versions of the AMC have an external serial port. The following options may be modified:

- Serial Port1 Address

ACPI Configuration
The **ACPI Configuration** subscreen allows you to set up or modify the following options:

- ACPI Configuration
    - Advanced ACPI Configuration
        - ACPI Version Features
        - ACPI APIC Support
        - AMI OEMB Table
        - Headless Mode
    - Chipset ACPI Configuration
        - Energy Lake Feature
        - APIC ACPI SCI IRQ
        - USB Device Wakeup From S3/S4
        - High Performance Event Timer
        - HPET Memory Address

AHCI Configuration
The **ACPI Configuration** subscreen allows you to set up or modify the following options:

- AHCI Configuration
    - ACHI BIOS Support
    - AHCI CD/DVD Boot Time out
    - AHCI Port 0
    - AHCI Port 1
        - SATA Port(x)
        - S.M.A.R.T.

Intel TXT(LT) Configuration
The **Intel TXT Configuration** subscreen allows you to enable or disable this AMC feature. The choices illustrated here assume that Intel TXT Initialization is ENABLED:

- Intel TXT Initialization
    - BIOS AC[SCLEAN]
    - BIOS AC[SCHECK]
    - Lock DPR
    - Reset TPM Establishment Flag

MPS Revision MPS Configuration
The **MPS Configuration** subscreen allows you to modify the following option:

- MPS Revision

PCI Express Configuration
The **PCI Express Configuration** allows you to enable or disable the standby power and power conversation features inherent in PCI Express link technology. The subscreen allows you to modify the following option:

- Active State Power-Management

Smbios Configuration
This is where you enable or disable the System Management Interrupt (Smi) capability of the System Management BIOS. The subscreen allows you to modify the following option:

- Smbios Smi Support

Remote Access Configuration
The options on the **Remote Access Configuration** subscreen allow you to set up or modify parameters for configuring remote access type and parameters. The choices illustrated here assume that Remote Access is ENABLED:

- Remote Access
    - Serial Port Number
        - COM1
    - Serial Port Mode
        - 115200 8,n,1
        - 57600 8,n,1
        - 38400 8,n,1
        - 19200 8,n,1
        - 09600 8,n,1
    - Flow Control
        - None
        - Hardware
        - Software
    - Redirection After BIOS POST
        - Disabled
        - Boot Loader
        - Always
    - Terminal Type
        - ANSI
        - VT100
        - VT-UTF8
    - VT-UTF8 Combo Key Support
    - Sredir Memory Display Mode
        - No Delay
    - Sredir Memory Display Mode (continued)
        - Delay 1 Sec
        - Delay 2 Sec
        - Delay 4 Sec

Trusted Computing
Here is where you can elect to use the AMC's on-board Trusted Platform Module (TPM) to support **Trusted Computing** applications. The following options listed assumes that TCG/TPM Support is set to **YES**:

- TCG/TPM Support
    - Execute TPM Command
    - Clearing the TPM
        - TPM Enable/Disable Status
        - TPM Owner Status

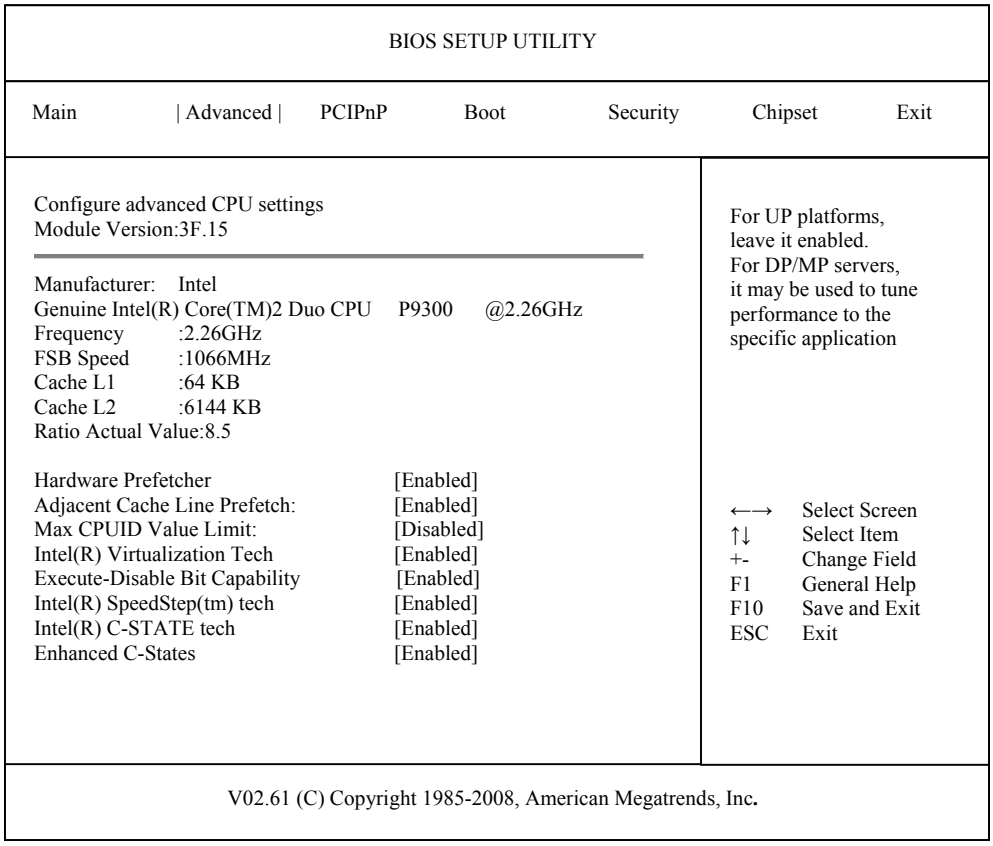
USB Configuration
The options on the **USB Configuration** subscreen allow you to set up or modify parameters for your front panel USB ports. The following options may be modified:

- Legacy USB Support
- USB 2.0 Controller Mode
- BIOS EHCI Hand-Off

Saving and Exiting
When you have made all desired changes to **Advanced** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

CPU CONFIGURATION SETUP

When you select **CPU Configuration** from the Advanced Setup Screen, the following Setup screen displays:



CPU Configuration Screen

When you display the CPU Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

CPU CONFIGURATION SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Advanced Setup. Once you change the settings, the new settings display each time Advanced Setup is run.

Hardware Prefetcher

The Setup screen displays the system option:

Hardware Prefetcher: [Enabled]

Available options are:

Disabled
Enabled

Adjacent Cache Line Prefetch

The Setup screen displays the system option:

Adjacent Cache Line Prefetch: [Enabled]

Available options are:

Disabled
Enabled

Max CPUID Value Limit

The Setup screen displays the system option:

Max CPUID Value Limit: [Disabled]

Available options are:

Disabled
Enabled

Intel(R) Virtualization Technology

The Setup screen displays the system option:

Intel(R) Virtualization Tech: [Enabled]

Available options are:

Disabled
Enabled

Execute-Disable Bit Capability

The Setup screen displays the system option:

Execute-Disable Bit Capability: [Enabled]

Available options are:

Disabled
Enabled

Intel(R) SpeedStep(tm) Technology

The Setup screen displays the system option:

Intel(R) SpeedStep(tm) tech [Enabled]

Available options are:

Disabled
Enabled

Intel(R) C-STATE Technology

The Setup screen displays the system option:

Intel(R) C-STATE tech [Enabled]

Available options are:
Disabled
Enabled

Enhanced C-States

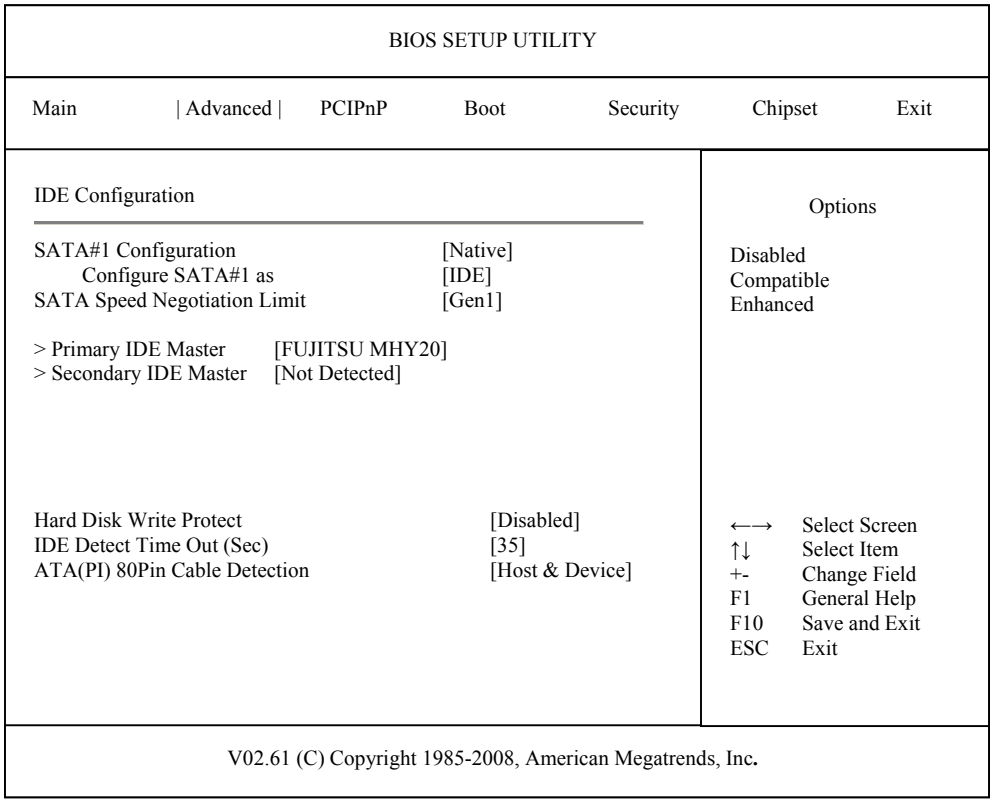
The Setup screen displays the system option:

Enhanced C-States [Enabled]

Available options are:
Disabled
Enabled

IDE CONFIGURATION

When you select **IDE Configuration** from the Advanced Setup Menu, a Setup screen similar to the following displays:



IDE Configuration Screen

When you display the IDE Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

Some of the options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

IDE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

SATA#1 Configuration

The Setup screen displays the system option:

SATA#1 Configuration [Native]

Three options are available:

- Select **Disabled** to disable all interfaces. No drives are displayed on the screen..
- Select **Native** to allow up to two SATA devices
- Select **Enhanced** to allow up to six SATA devices. This mode is not currently supported on the AMC and is reserved for future use.

Configure SATA#1 As

This option allows you specify how to configure the available SATA devices. It is only available if the SATA#1 Configuration option is set to Compatible or Enhanced.

The Setup screen displays the system option:

Configure SATA as [IDE]

Three options are available:

- Select **IDE** to enable the SATA devices as IDE devices.
- Select **RAID** to enable the SATA devices as a RAID device. When RAID is selected:
  - The SATA RAID 0 and 1 implementations will be supported with the AMC's two SATA edge connector interfaces.
  - The SATA#1 Configuration line disappears from the screen when this option is selected.
- Select **AHCI** to enable Native Command Queuing (NCQ) and SATA hot plug capability.
  - The SATA#1 Configuration line disappears from the screen when this option is selected

The next two items on the IDE Configuration BIOS set-up menu are:

► **Primary IDE Master**
► **Secondary IDE Master**

The presence of IDE devices in the system are detected automatically upon entering the BIOS setup and the detection results are presented to the right on the configuration option. For example, in the set-up screen example for the IDE Configuration a Fujuitsu drive was detected as the Primary IDE Master. The Setup screen displays the following options:

Primary IDE Master :[FUJITSU MHY20]
Secondary IDE Master :[Not Detected]

Here are the options in the lower portion of this set-up screen:

Type :[Auto]
LBA/Large Mode :[Auto]
Block (Multi-Sector Transfer) :[Auto]
PIO Mode :[Auto]
DMA Mode :[Auto]
S.M.A.R.T Mode :[Auto]
32Bit Data Transfer :[Enable]

To view and/or change any device parameter, press **<Enter>** to proceed to the IDE Device Setup screen. There are short descriptions of each parameter located in the upper right section of the

BIOS setup screen. A detailed discussion of the IDE Device Setup screen setting is located in the following section of this chapter.

Hard Disk Write Protect
This option allows you to disable or enable device write protection. Write protection will be effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Hard Disk Write Protect [Disabled]

Available options are:

Disabled
Enabled

IDE Detect Time Out (Sec)

This option allows you to select the time-out value (in seconds) for detecting an ATA/ ATAPI device.

The Setup screen displays the system option:
IDE Detect Time Out (Sec) [35]

Available options are:
0
5
10
15
20
25
30
35

ATA(PI) 80Pin Cable Detection

This option allows you to select the mechanism for detecting an 80-pin ATA(PI) cable.

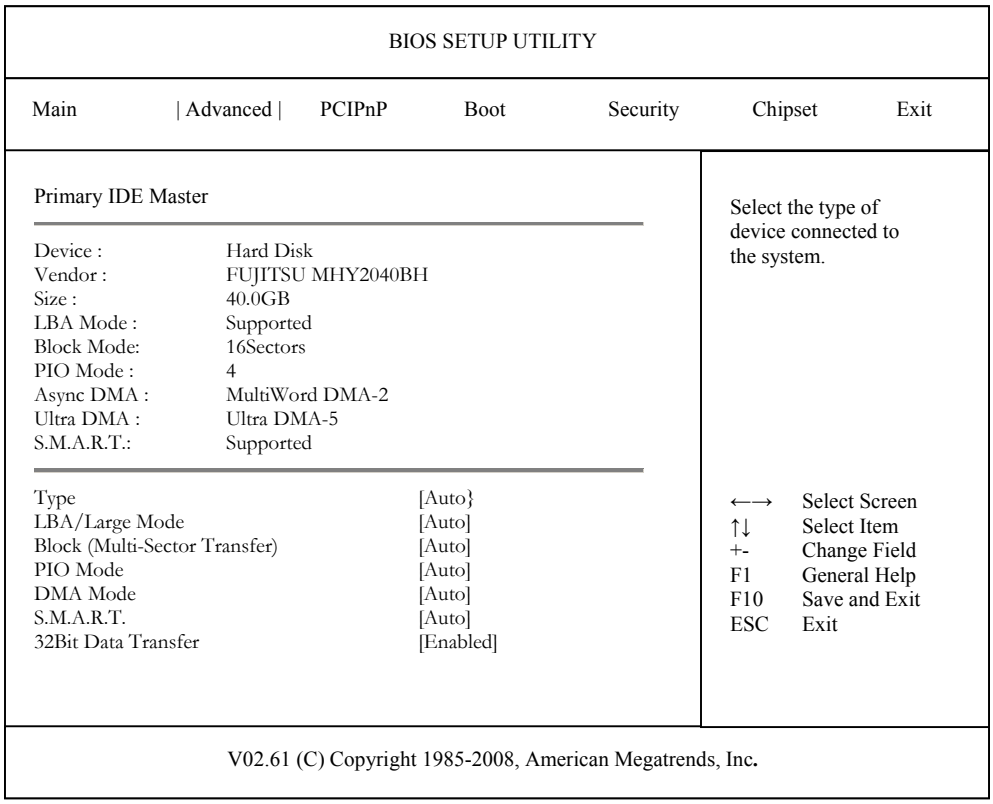
The Setup screen displays the system option:

ATA(PI) 80Pin Cable Detection [Host & Device]

Available options are:
Host & Device
Host
Device

IDE DEVICE SETUP

When you select one of the IDE devices from the **IDE Configuration** screen, a Setup screen similar to the following displays:



IDE Device Screen

When you display the IDE Device subscreen, the format is similar to the sample shown above. The data displayed on the top portion of the screen details the parameters detected by AMIBIOS for the specified device and may not be modified. Entering the Primary IDE Master option in this example yields specific device information about the Fujuitsu drive in the top of the screen. The data displayed on the bottom portion of the screen may be modified; however, most applications will require the automatic mode.

IDE DEVICE SETUP OPTIONS

The following options are available for each of the IDE devices on the primary and secondary IDE controllers:

Type

This option allows you to specify what type of device is on the IDE controller.

The Setup screen displays the system option:

Type [Auto]

Available options are:

Not Installed
Auto
CD/DVD
ARMD

If **Not Installed** is selected, the other options on the bottom portion of this screen do not display.

LBA/Large Mode

This option allows you to enable IDE LBA (Logical Block Addressing) Mode for the specified IDE drive. Data is accessed by block addresses rather than by the traditional cylinder-head-sector format. This allows you to use drives larger than 528MB.

The Setup screen displays the system option:

LBA/Large Mode [Auto]

Two options are available:

- Select **Disabled** to have AMIBIOS use the physical parameters of the hard disk and do no translation to logical parameters. The operating system, which uses the parameter table, will then see only 528MB of hard disk space even if the drive contains more than 528MB.
- Select **Auto** to enable LBA mode and translate the physical parameters of the drive to logical parameters. LBA Mode must be supported by the drive and the drive must have been formatted with LBA Mode enabled.

Block (Multi-Sector Transfer) Mode

This option supports transfer of multiple sectors to and from the specified IDE drive. Block mode boosts IDE drive performance by increasing the amount of data transferred during an interrupt.

If **Block Mode** is set to **Disabled**, data transfers to and from the device occur one sector at a time.

The Setup screen displays the system option:

Block (Multi-Sector Transfer) [Auto]

Available options are:
Disabled
Auto

PIO Mode

IDE Programmed I/O (PIO) Mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Set the **PIO Mode** option to **Auto** to have AMIBIOS select the PIO mode used by the IDE drive being configured. If you select a specific value for the PIO mode, you must make *absolutely* certain that you are selecting the PIO mode supported by the IDE drive being configured.

The Setup screen displays the system option:

PIO Mode [Auto]

Available options are:

Auto
0
1
2
3
4

DMA Mode

This option allows you to select DMA Mode for the device.

The Setup screen displays the system option:

DMA Mode [Auto]

Available options are:

Auto	
SWDMA0	(SingleWord DMA 0 - 2)
SWDMA1	
SWDMA2	
MWDMA0	(MultiWord DMA 0 - 2)
MWDMA1	
MWDMA2	
UDMA0	(UltraDMA 0 - 5)
UDMA1	
UDMA2	
UDMA3	
UDMA4	
UDMA5	

S.M.A.R.T.

This option allows AMIBIOS to use the SMART (Self-Monitoring Analysis and Reporting Technology) protocol for reporting server system information over a network.

The Setup screen displays the system option:

S.M.A.R.T. [Auto]

Available options are:

Auto
Disabled
Enabled

32Bit Data Transfer
If the **32Bit Data Transfer** parameter is set to **Enabled**, AMIBIOS enables 32-bit data transfers. If the host controller does not support 32-bit transfer, this feature *must* be set to **Disabled**.

The Setup screen displays the system option:

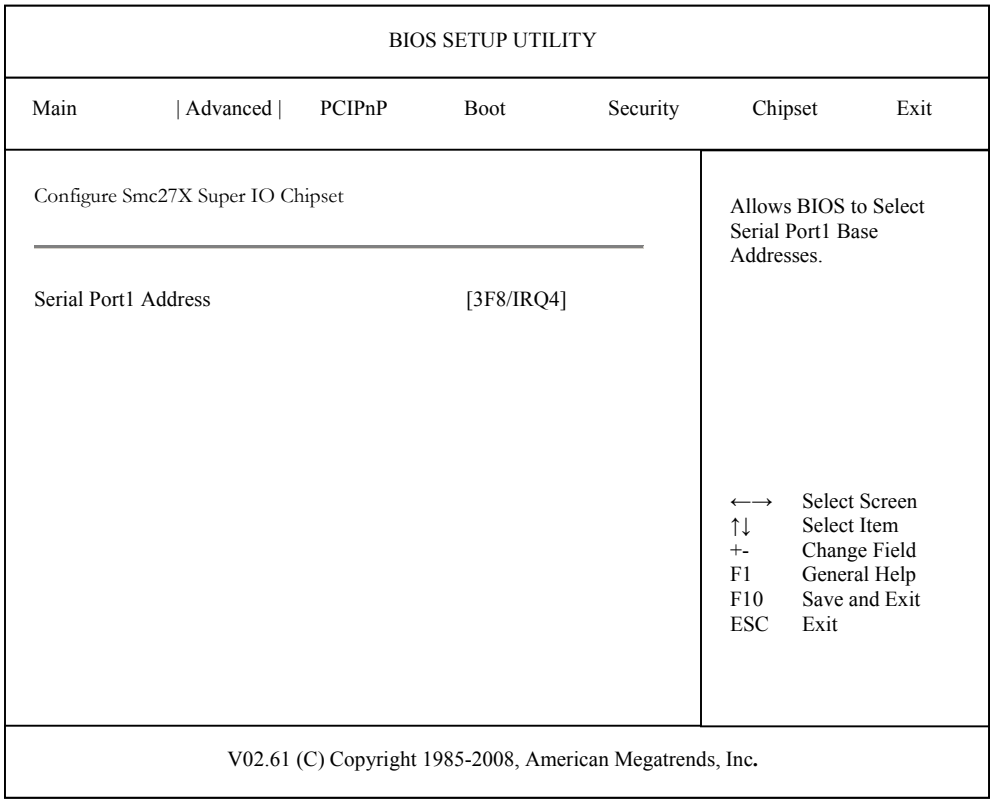
32Bit Data Transfer [Enabled]

Available options are:

Disabled
Enabled

SUPERIO CONFIGURATION

When you select **SuperIO Configuration** from the Advanced Setup Menu, the following Setup screen displays.



SuperIO Configuration Screen

When you display the SuperIO Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

The drive information; which displays the first time the BIOS Setup Utility is run, indicates the drive(s) on your system that have been detected by the AMIBIOS upon initial bootup.

SUPERIO CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Serial Port1 Address

Each of these options enables the specified serial port on the AMC that are connected to the Module Management Controller (MMC) and establishes the base I/O address and the number of the interrupt request for the port.

The Setup screen displays the system option:

Serial Port1 Address [3F8/IRQ4]

Serial Port1 Address Configuration (Continued)

Available options are:

Disabled
3F8/IRQ4
3E8/IRQ4
2E8/IRQ3

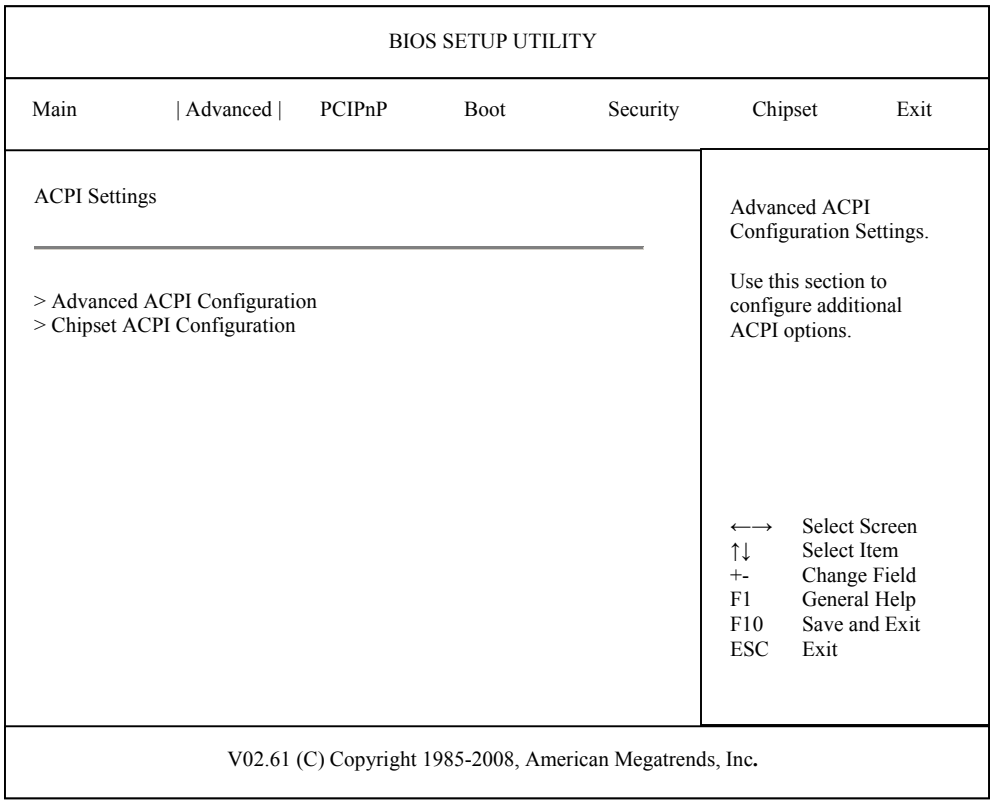
If the system has off-board serial ports that are configured to specific starting I/O ports, AMIBIOS configures the on-board serial ports to avoid conflicts.

When AMIBIOS checks serial port 1, any off-board serial ports found are left at their assigned addresses. Serial Port1 is configured with the first available address. The default address assignment order is 3F8H, 2F8H, 3E8H, 2E8H. Note that this same assignment order is used by AMIBIOS to place the active serial port addresses in lower memory (BIOS data area) for configuration as logical COM devices.

For example, if there is one off-board serial port and its address is set to 3E8H, Serial Port1 is assigned address 3F8H.

ACPI CONFIGURATION

When you select **ACPI Configuration** from the Advanced Setup Menu, the following Setup screen displays.



ACPI Configuration Screen

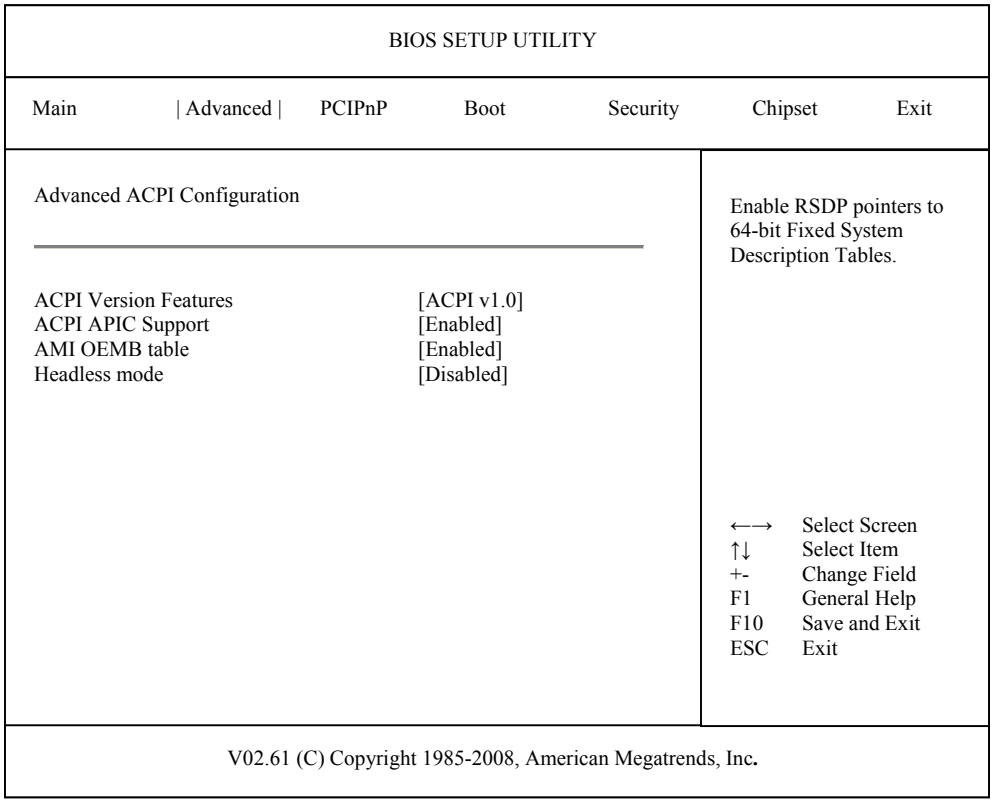
When you display the ACPI Configuration screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the ACPI Configuration options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

The subscreens allow you to set up or modify the following options:

- Advanced ACPI Configuration
  - ACPI Version Features
  - ACPI APIC Support
  - AMI OEMB Table
  - Headless Mode
- Chipset ACPI Configuration
  - Energy Lake Feature
  - APIC ACPI SCI IRQ
  - USB Device Wakeup From S3/S4
  - High Performance Event Timer
  - HPET Memory Address

ADVANCED ACPI CONFIGURATION

When you select **Advanced ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:



Advanced ACPI Configuration Screen

When you display the Advanced ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

ADVANCED ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

ACPI Version Features

The Setup screen displays the system option:

ACPI Version Features [ACPI v1.0]

Available options are:

ACPI v1.0
ACPI v2.0
ACPI v3.0

ACPI APIC Support

The Setup screen displays the system option:

ACPI APIC Support [Enabled]

Available options are:
Disabled
Enabled

AMI OEMB Table

The Setup screen displays the system option:

AMI OEMB Table [Enabled]

Available options are:
Disabled
Enabled

Headless Mode

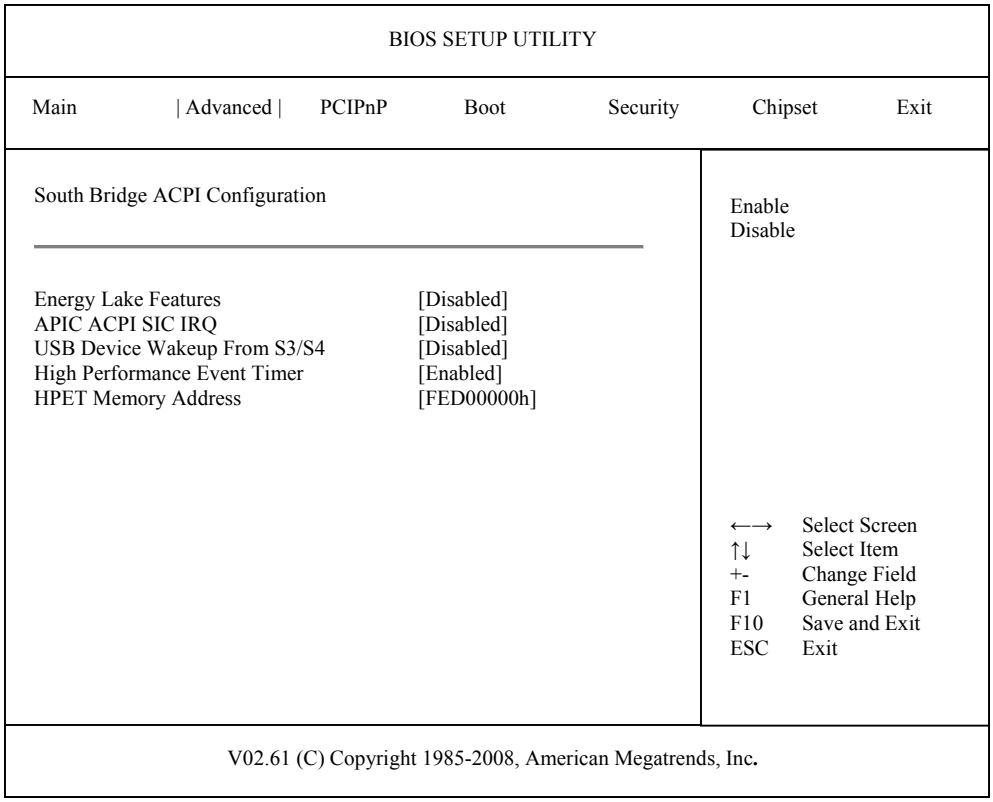
The Setup screen displays the system option:

Headless Mode [Disabled]

Available options are:
Disabled
Enabled

CHIPSET ACPI CONFIGURATION

When you select **Chipset ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:



Chipset ACPI Configuration Screen

When you display the Chipset ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

CHIPSET ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Energy Lake Feature

The Setup screen displays the system option:

Energy Lake Feature [Disabled]

Available options are:

Disabled
Enabled

APIC ACPI SCI IRQ

The Setup screen displays the system option:

APIC ACPI SCI IRQ [Disabled]

Available options are:

Disabled
Enabled

USB Device Wakeup From S3/S4

The Setup screen displays the system option:

USB Device Wakeup From S3/S4 [Disabled]

Available options are:

Disabled
Enabled

High Performance Event Timer

The Setup screen displays the system option:

High Performance Event Timer [Enabled]

Available options are:

Disabled
Enabled

HPET Memory Address

The Setup screen displays the system option:

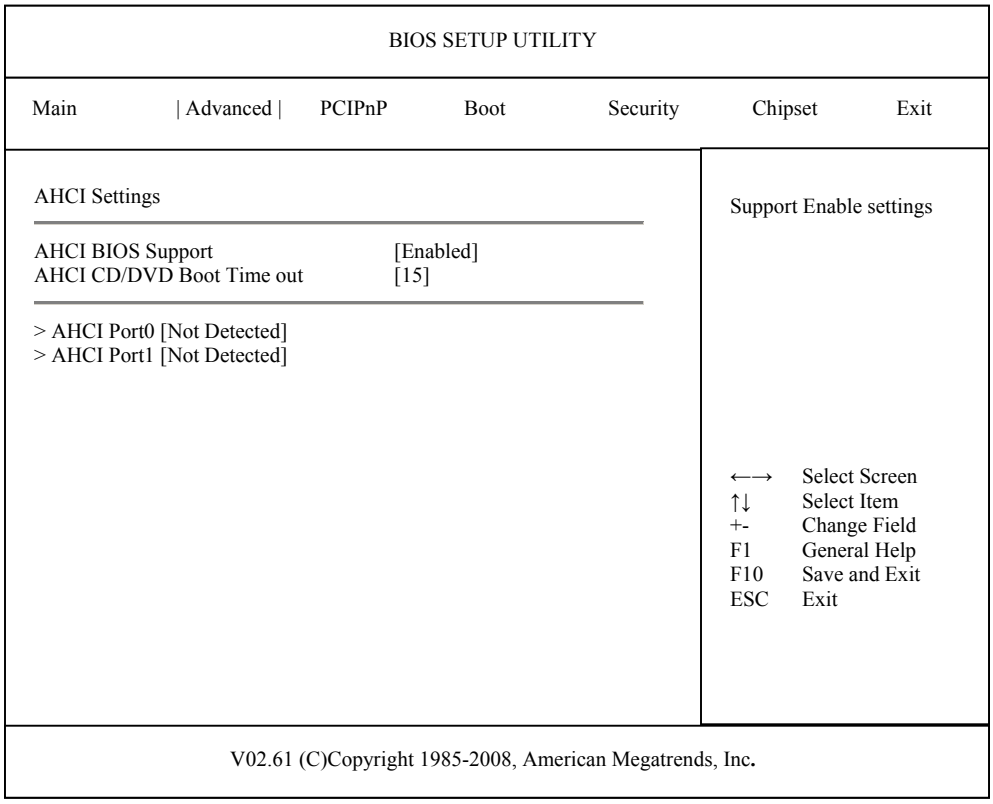
HPET Memory Address [FED00000h]

Available options are:

FED00000h
FED01000h
FED02000h
FED03000h

AHCI CONFIGURATION

When you select **AHCI Configuration** from the Advanced Setup Menu, the following Setup screen displays:



AHCI Configuration Screen

When you display the AHCI Configuration screen, the format is similar to the sample shown above. You may highlight the option you wish to change, press enter to display the available options and then press **<Enter>** again to accept the highlighted value you chose.

Other options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

AHCI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

AHCI BIOS Support

The Setup screen displays the system option:

AHCI BIOS Support [Enabled]

Available options:
- Disabled
- Enabled

AHCI configuration options (continued)

AHCI CD/DVD Boot Time out

The Setup screen displays the system option:

AHCI CD/DVD Boot Time out [35]

Available Options are:

0
5
10
15
20
25
30
35

AHCI PORT 0, 1

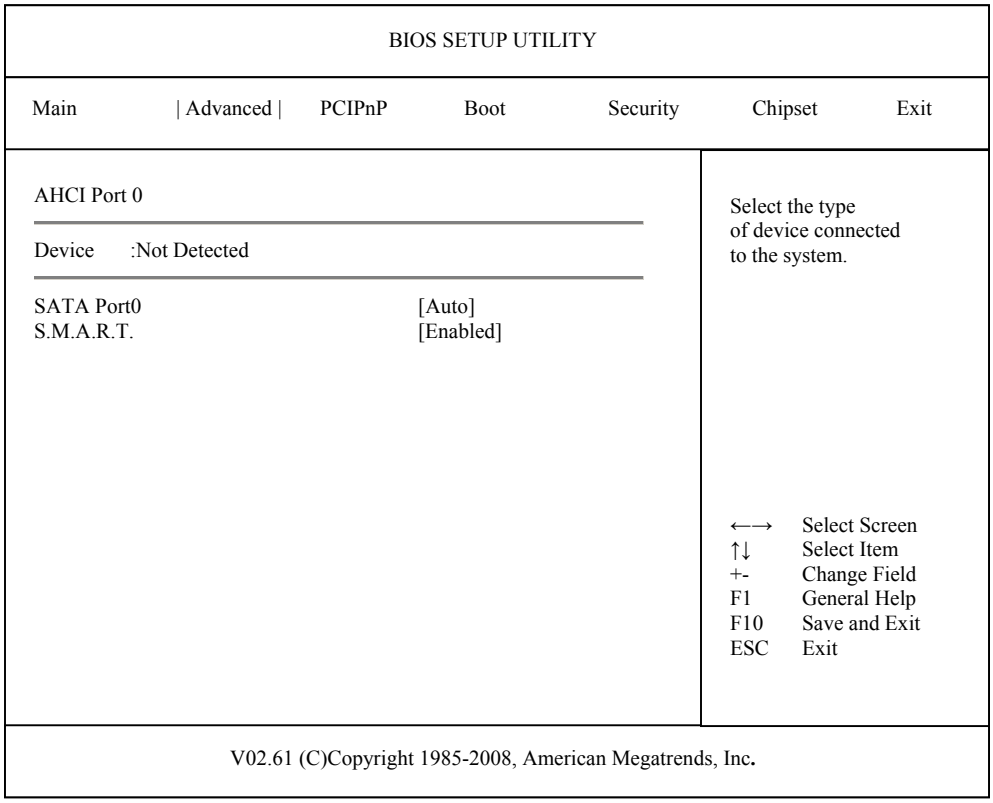
The Setup screen displays the system options:

AHCI Port 0 [Not Detected]
AHCI Port 1 [Not Detected]

This is an example of the screen. To view and/or change parameters for any of the devices, press <ENTER> to proceed to the IDE Device Setup screen.

AHCI PORT CONFIGURATION

When you select an **AHCI Port x** option from the **AHCI Configuration Menu**, the following Setup screen will display for each **AHCI Port x** option:



AHCI Port Configuration Screen

When you display the AHCI Port Configuration screen **for any of the 2 AHCI Ports listed on the AHCI Configuration screen**, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

AHCI PORT CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run. The AHCI Port screen is the same for all 6 AHCI Ports listed on the AHCI Configuration screen.

SATA Port0

The Setup screen displays the system option:

SATA Port0 [Disabled]

Available options are:

Auto
Not Installed

S.M.A.R.T.

The Setup screen displays the system option:

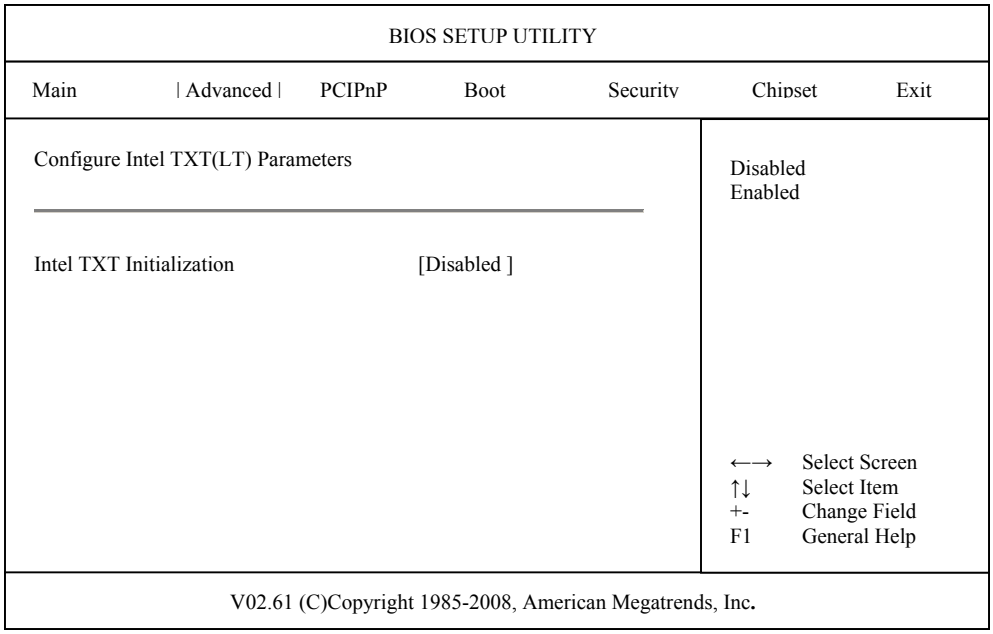
S.M.A.R.T. [Enabled]

Available options are:

Disabled
Enabled

INTEL® TXT CONFIGURATION

When you select **Intel® TXT Configuration** from the Advanced Setup Screen, the following Setup screen displays:



Intel TXT Configuration Screen

When you display the Intel® TXT Configuration screen, the format is similar to the sample shown above. Highlight the option to change it and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

INTEL® TXT CONFIGURATION SETUP OPTIONS

The description for the system option listed below shows the value as it appears if you have not yet run Advanced Setup. Once you change the setting, the new setting displays each time Advanced Setup is run.

Intel TXT Initialization

The Setup screen displays the system option:

Intel TXT Initialization [Disabled]

Available options are:

Disabled
Enabled

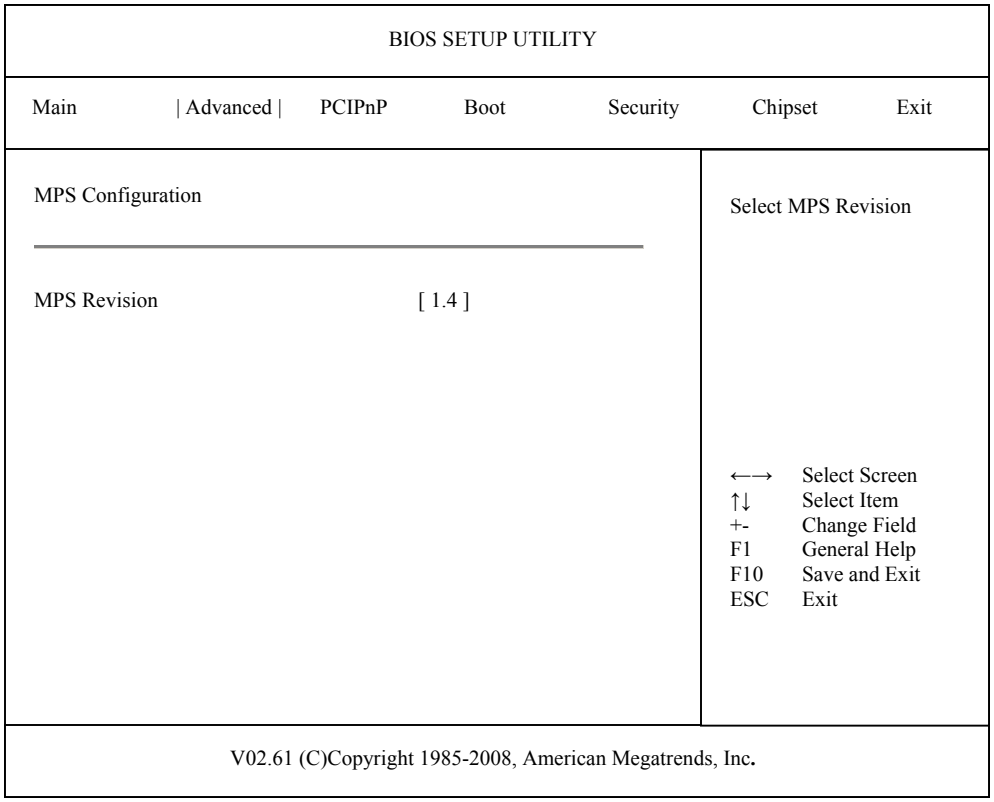
If the initialization enable option is selected, the following options are displayed:

BIOS AC[SCLEAN]	[Enabled]
BIOS AC[SCHECK]	[Enabled]
Lock DPR	[Enabled]
Reset TPM Establishment Flag	[Enabled]

These settings are factory set to enabled when choosing to use the Intel TXT Initialization feature.

MPS CONFIGURATION

When you select **MPS Configuration** from the Advanced Setup Screen, the following Setup screen displays:



MPS Configuration Screen

When you display the MPS Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

MPS CONFIGURATION SETUP OPTIONS

The description for the system option listed below shows the value as it appears if you have not yet run Advanced Setup. Once you change the setting, the new setting displays each time Advanced Setup is run.

MPS Revision

The Setup screen displays the system option:

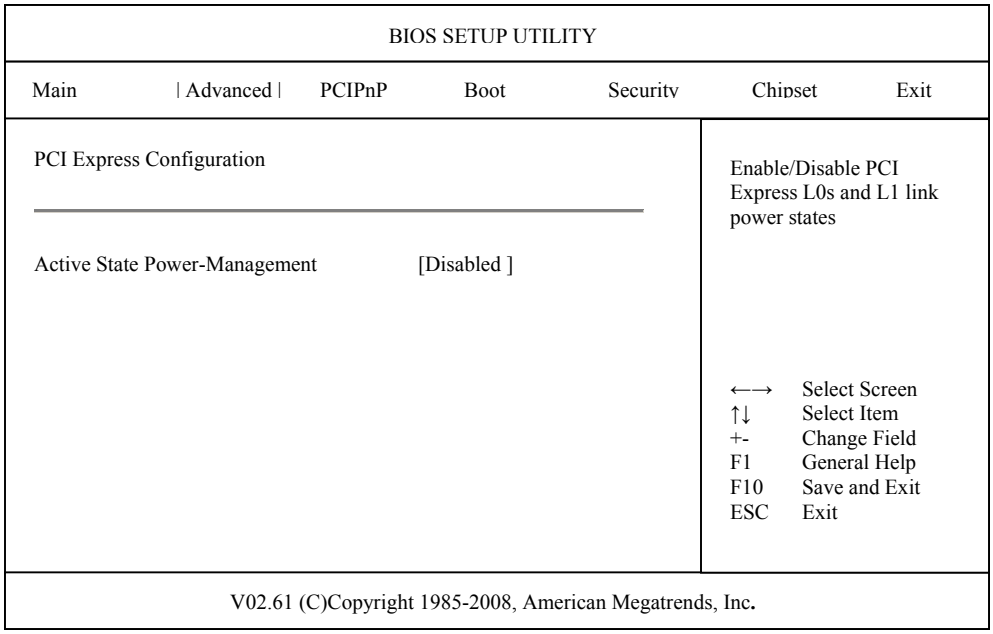
MPS Revision [1.4]

Available options are:

1.1
1.4

PCI EXPRESS® CONFIGURATION

When you select **PCI Express® Configuration** from the Advanced Setup Screen, the following Setup screen displays:



PCI Express Configuration Screen

When you display the PCI Express® Configuration screen, the format is similar to the sample shown above. Highlight the option to change it and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

PCI EXPRESS® CONFIGURATION SETUP OPTION

The description for the system option listed below shows the value as it appears if you have not yet run Advanced Setup. Once you change the setting, the new setting displays each time Advanced Setup is run.

Active State Power Management

The Setup screen displays the system option:

Active State Power Management [Enabled]

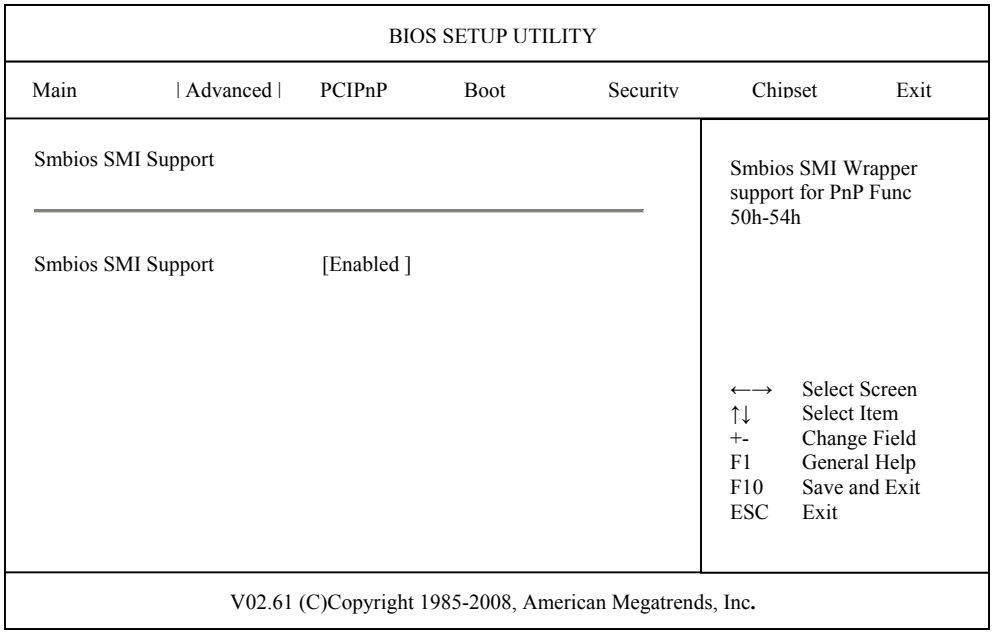
Available options are:

Disabled
Enabled

Active state power management is the ability of the AMC's PCI Express hardware controller inside the module's ICH9M to power-manage links. PCIe links L0s and L1 are used in active state power management where L0s can be configured to reduce power consumption between PCIe link activities and L1 can be configured to reduce power consumption when there are no outstanding requests or pending transactions on the AMC's PCI Express links. L0s support is mandatory in PCI Express implementations, but L1 support is optional. To use the active state power management feature the PCIe devices connected to the link must support both L0s and L1.

SMBIOS CONFIGURATION

When you select **SmbiosConfiguration** from the Advanced Setup Screen, the following Setup screen displays:



Smbios Configuration Screen

When you display the Smbios Configuration screen, the format is similar to the sample shown above. Highlight the option to change it and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

SMBIOS CONFIGURATION SETUP OPTIONS

The description for the system option listed below shows the value as it appears if you have not yet run Advanced Setup. Once you change the setting, the new setting displays each time Advanced Setup is run.

Smbio SMI Support

The Setup screen displays the system option:

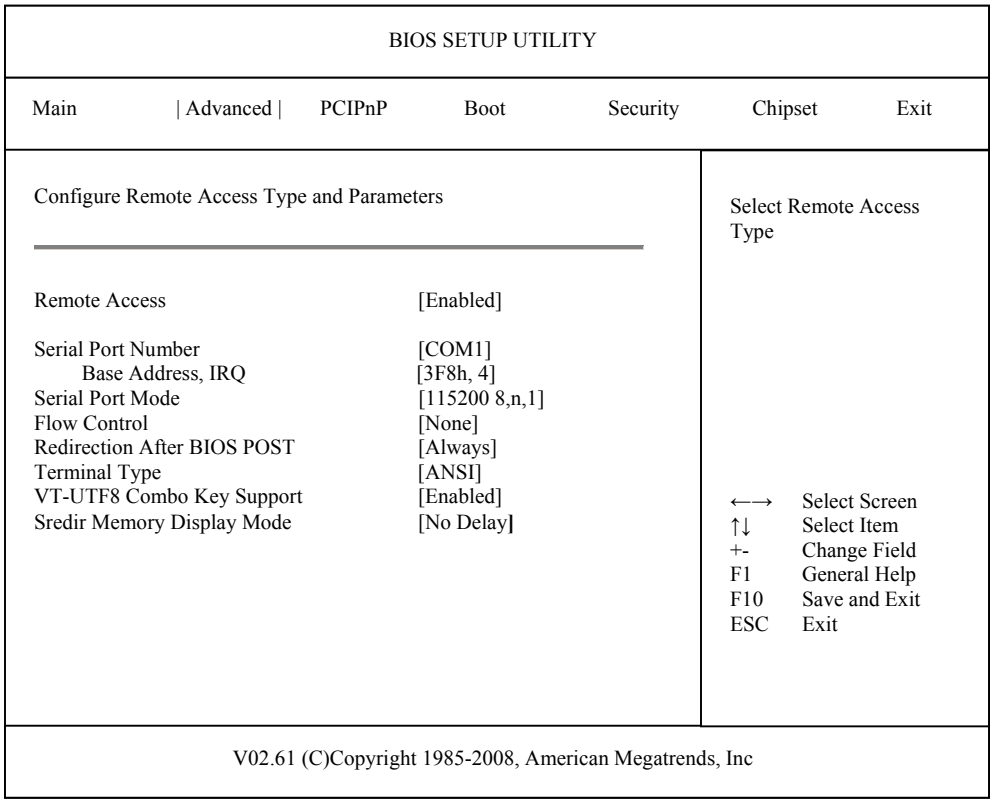
Smbio SMI Support [Disabled]

Available options are:

Disabled
Enabled

REMOTE ACCESS CONFIGURATION

When you select **Remote Access Configuration** from the Advanced Setup Menu, the following Setup screen displays.



Remote Access Configuration Screen

When you display the Remote Access Configuration screen, the format is similar to the sample shown above if you have enabled **Remote Access**. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

REMOTE ACCESS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Advanced Setup. Once values have been defined, they display each time Advanced Setup is run.

Remote Access

This option allows you to use a terminal connected to a serial port on an I/O expansion board to control changes to the BIOS settings.

The sample above shows the appearance of the screen if **Remote Access** is set to **Enabled**. If this option is set to **Disabled**, which is the default, the other options on this screen do not display. The Setup screen displays the system option:

Remote Access [Enabled]

Remote Access (continued)

Available options are:

Disabled
Enabled

Serial Port Number

This option specifies the serial port on which remote access is to be enabled. If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Serial Port Number [COM1]

Available option is:
COM1
The base address and IRQ for COM1 is set by the BIOS and displayed for informational purposes.

Serial Port Mode

This option specifies settings for the serial port on which remote access is enabled. The settings indicate baud rate, eight bits per character, no parity and one stop bit. If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Serial Port Mode [115200 8,n,1]

Available options are:
115200 8,n,1
57600 8,n,1
38400 8,n,1
19200 8,n,1
09600 8,n,1

Flow Control

This option allows you to select flow control for console redirection.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Flow Control [None]

Available options are:

None
Hardware
Software

Redirection After BIOS POST

This option specifies when redirection should be active.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Redirection After BIOS POST [Always]

Three options are available:

- Select **Disabled** to turn off the redirection after POST.
- Select **Boot Loader** to keep redirection active during POST and during Boot Loader.
- Select **Always** to always keep redirection active. Note that some operating systems may not work properly if this option is set to **Always**.

Terminal Type

This option allows you to select the target terminal type.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Terminal Type [ANSI]

Available options are:

ANSI
VT100
VT-UTF8

VT-UTF8 Combo Key Support

This option allows you to enable VT-UTF8 combination key support for ANSI or VT100 terminals.

If the **Remote Access** option is set to **Disabled** or the **Terminal Type** option is set to **VT-UTF8**, this option is not available.

The Setup screen displays the system option:

VT-UTF8 Combo Key Support [Enabled]

Available options are:
Disabled
Enabled

Sredir Memory Display Mode

This option indicates the delay in seconds to display memory information.

The Setup screen displays the system option:

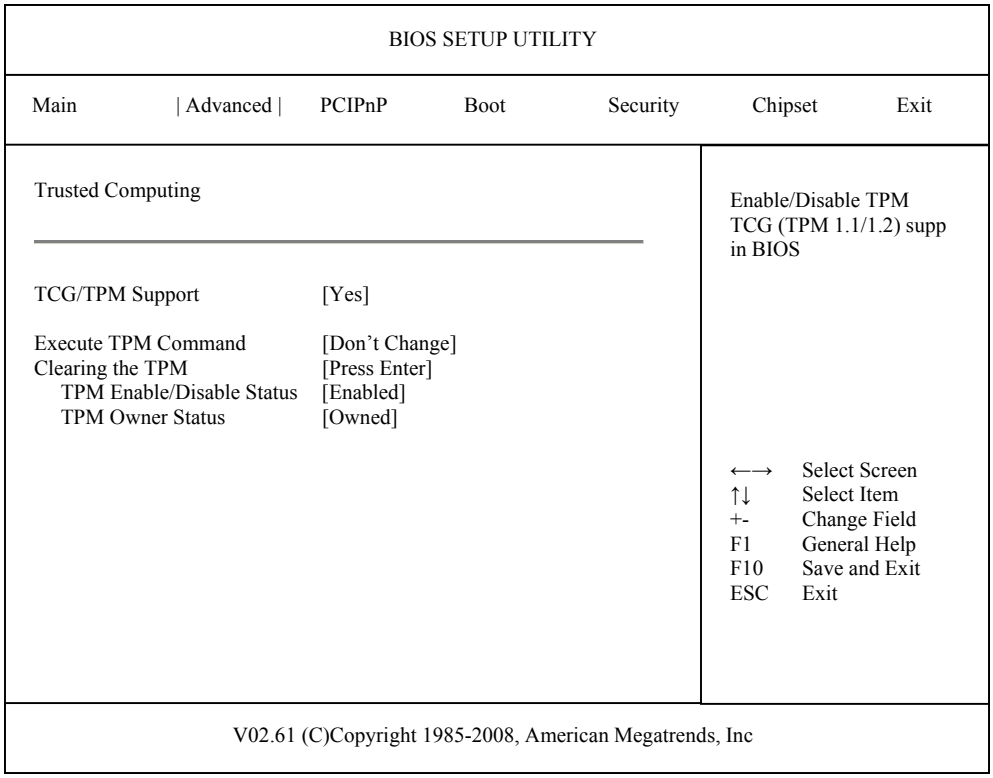
Sredir Memory Display Mode [No Delay]

Available options are:

No Delay
Delay 1 Sec
Delay 2 Sec
Delay 4 Sec

TRUSTED COMPUTING CONFIGURATION

When you select **Trusted Computing Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Trusted Computing Configuration Screen

When you display the Trusted Computing Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

TRUSTED COMPUTING CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you select **Yes** on the TCG/TPM Support line in the set-up screen example shown. When the BIOS default setting of **No** is displayed, the following set-up parameter options are hidden.

Execute TPM Command

This option allows you to enable (activate) or disable (deactivate) support for TPM commands issued to the board's trusted platform module. The third option called **Don't Change** ensures that the TPM will function in its factory default mode.
The Setup screen displays the system option:

Execute TPM Command [Don't Change]

Available options are:
- Don't Change
- Disabled
- Enabled

Trusted Computing Configuration (continued)

Clearing the TPM Command

This is a powerful command that must be used with care. Executing this command will re-set the AMC's TPM back to the factory defaults. Any platform ownership status, i.e. TPM passwords, activation keys and/or data access keys that were set via TPM commands and not recorded and stored in a secure location could be lost. If this happens the system could be rendered useless. Do not agree to clear the TPM by choosing the OK option if you are unsure.

Clearing the TPM [Press Enter]

CAUION: There are no set-up options with this parameter. Pressing enter will pull up a caution menu informing you that the AMC is about to clear the TPM and that the system's platform owner may change as a result. ***Do not agree to clear the TPM*** by choosing the **[OK]** option if you are unsure about the platform ownership status and any related TPM passwords, activation keys and/or data access key settings. Choose the **[Cancel]** option or hit the **[ESC]** key to exit this setting if you are unsure about the platform owner status.

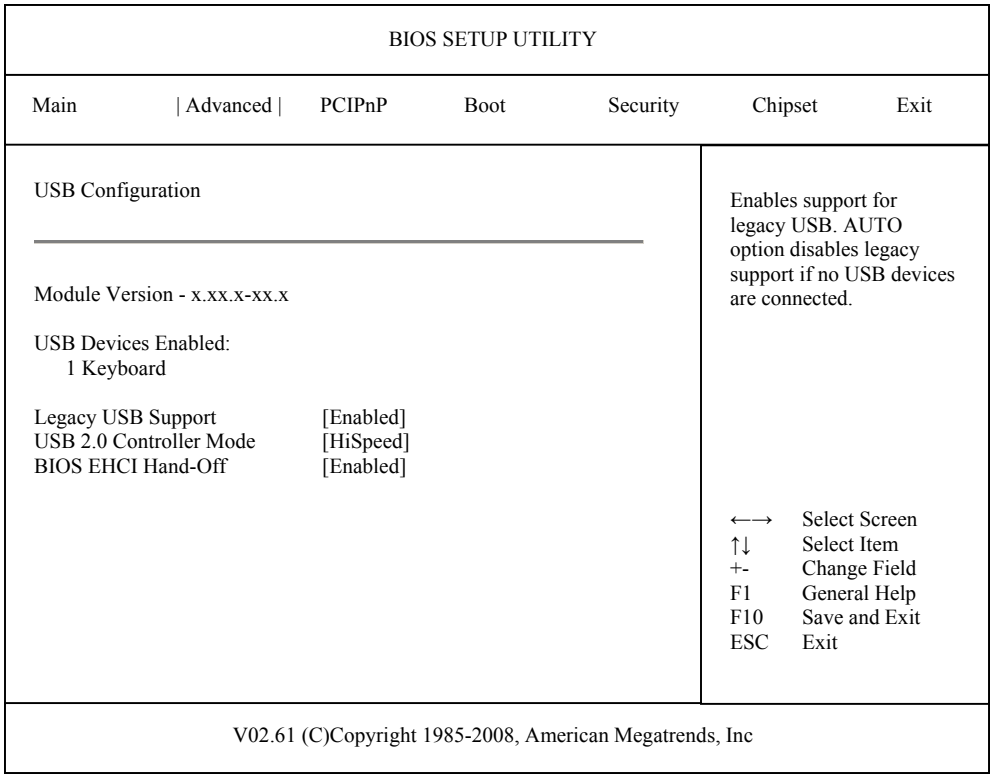
TPM Enable/Disable Status and **TPM Owner Status**

These two status lines are displayed below the Clearing the TPM command line. These lines reflect the current state of the AMC's Trusted Platform Module. In the following example, the TPM is enabled and there has been a platform owner identified in the O/S and/or the TPM application software.

TPM Enable/Disable Status [Enabled]
TPM Owner Status [Owned]

USB CONFIGURATION

When you select **USB Configuration** from the Advanced Setup Menu, the following Setup screen displays:



USB Configuration Screen

When you display the USB Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

USB CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Legacy USB Support

This option allows you to enable support for older USB devices. The **Auto** option disables legacy support if no USB devices are connected. If this option is set to **Disabled**, the remaining three options are not available.

The Setup screen displays the system option:

Legacy USB Support [Enabled]

Available options are:

Disabled
Enabled
Auto

USB 2.0 Controller Mode

This option configures the USB 2.0 controller to high-speed (480Mbps) or full-speed (12Mbps) mode. If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

USB 2.0 Controller Mode [HiSpeed]

Available options are:

FullSpeed
HiSpeed

BIOS EHCI Hand-Off

This option is a work-around for operating systems without EHCI hand-off support. If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

BIOS EHCI Hand-Off [Enabled]

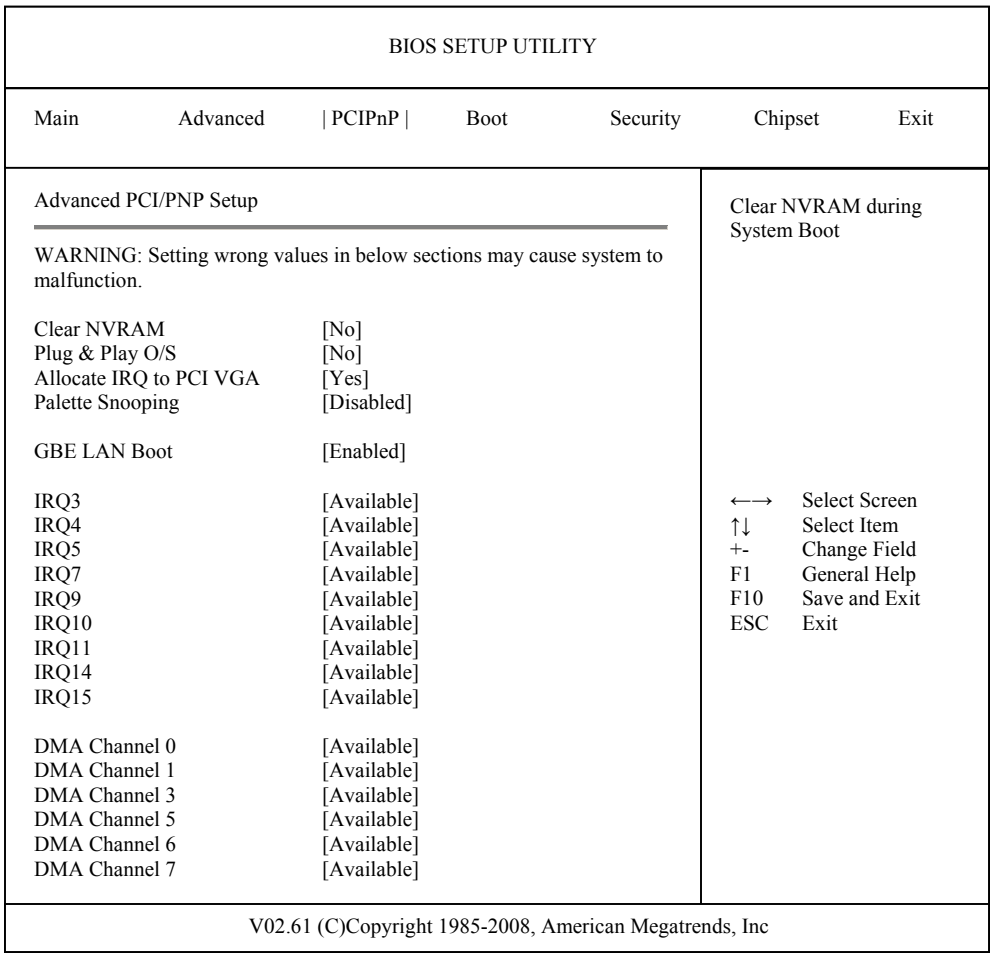
Available options are:

Disabled
Enabled

Chapter 5 PCI Plug and Play Setup (PCIPnP)

PLUG AND PLAY SETUP

When you select **PCIPnP** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



PCIPnP Setup Screen

When you display the PCIPnP Setup screen, the format is similar to the sample shown above, except the screen does not display all of the options at one time. If you need to change other options, use the down arrow key to locate the appropriate option. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The values on the PCIPnP Setup screen do not necessarily reflect the values appropriate for your AMC. Refer to the explanations below for specific instructions about entering correct information.

PCIPnP Setup Options

The descriptions for the system options listed below show the values as they appear if you have not yet run PCIPnP Setup. Once values have been defined, they display each time PCIPnP Setup is run.

NOTE: Do not change the values for any PCIPnP Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Clear NVRAM

This option allows you to clear NVRAM during system boot.

The Setup screen displays the system option:

Clear NVRAM [No]

Available options are:

No
Yes

Plug & Play O/S

This option indicates whether or not the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP adapter cards which are required for system boot. An operating system which is PnP-aware detects and enables all other PnP-aware adapter cards. Set this option to **No** if the operating system (such as DOS or OS/2) does *not* use PnP.

NOTE: You *must* set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

The Setup screen displays the system option:

Plug & Play O/S [No]

Two options are available:

- Select **No** to allow AMIBIOS to configure the devices in the system.
- Select **Yes** if your system has a Plug and Play operating system and you want to allow the operating system to configure all Plug and Play (PnP) devices which are not required for bootup.

PCIPnP Setup Options (continued)

Allocate IRQ to PCI VGA

This option allows you to assign an IRQ to a PCI VGA card if the card requests an IRQ.

The Setup screen displays the system option:

Allocate IRQ to PCI VGA [Yes]

Available options are:

Yes
No

Palette Snooping

This option, when set to **Enabled**, indicates to the PCI devices that a graphics device is installed in the system so the card will function correctly.

The Setup screen displays the system option:

Palette Snooping [Disabled]

Available options are:

Disabled
Enabled

GBE LAN Boot

This option, when set to **Enabled**, indicates that the option ROM for the on-board Gigabit LANs is to be executed. This option should remain **Disabled** if you are not booting from a LAN device.

The Setup screen displays the system option:

GBE LAN Boot ROM [Enabled]

Available options are:

Disabled
Enabled

IRQ3/IRQ4/IRQ5/IRQ7/IRQ9/IRQ10/IRQ11/IRQ14/IRQ15

These options indicate whether the specified interrupt request (IRQ) is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices. This allows you to specify IRQs for use by legacy adapter cards.

The IRQ setup options indicate whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices.

PCIPnP Setup Options (continued)

The Setup screen displays the system option:

IRQ# [Available]

where # is the number of the interrupt request (IRQ)

Two options are available:

- Select **Available** to make the specified IRQ available for use by PCI/PnP devices. •
- Select **Reserved** to reserve the specified IRQ for use by legacy devices.

DMA Channels 0, 1, 3, 5, 6 and 7

These options indicate whether the specified DMA channel is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices.

The Setup screen displays the system option:

DMA Channel # [Available]

where # is the DMA Channel number

Two options are available:

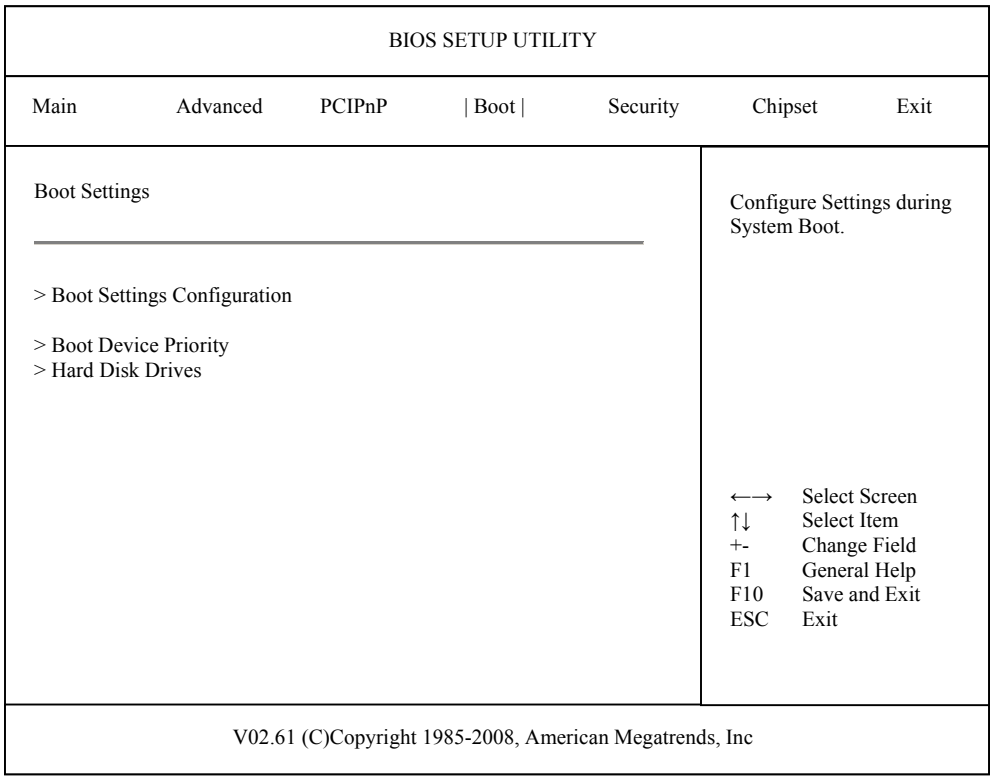
- **Available** indicates that the specified DMA channel is available for use by PCI/PnP devices.
- **Reserved** indicates the specified DMA channel is reserved for use by legacy devices.

Saving and Exiting

When you have made all desired changes to **PCIPnP** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

Chapter 6 Boot Setup

BOOT SETUP



Boot Setup Screen

When you display the Boot Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Boot Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: If no device is found for one of the device types, the line item for that device type does not display.

BOOT SETUP OPTIONS

The descriptions for the system option listed below show the values as they appear if you have not yet run Boot Setup. Once values have been changed, they display each time Boot Setup is run. You may also continue to subscreens to specify boot parameters and the boot sequence of bootable devices in your system.

Boot Settings Configuration

The options on the **Boot Settings Configuration** subscreen allow you to set up or modify parameters for boot procedures.

The following options may be modified:

- Quick Boot
- Quiet Boot
- AddOn ROM Display Mode
- Bootup Num-Lock
- PS/2 Mouse Support
- Wait For 'F1' If Error
- Hit 'DEL' Message Display
- Interrupt 19 Capture

Boot Device Priority

The options on the **Boot Device Priority** subscreen specify the order in which AMIBIOS attempts to boot devices available in the system. It allows you to select the drive which will be booted first, second, third, etc.

Hard Disk Drives

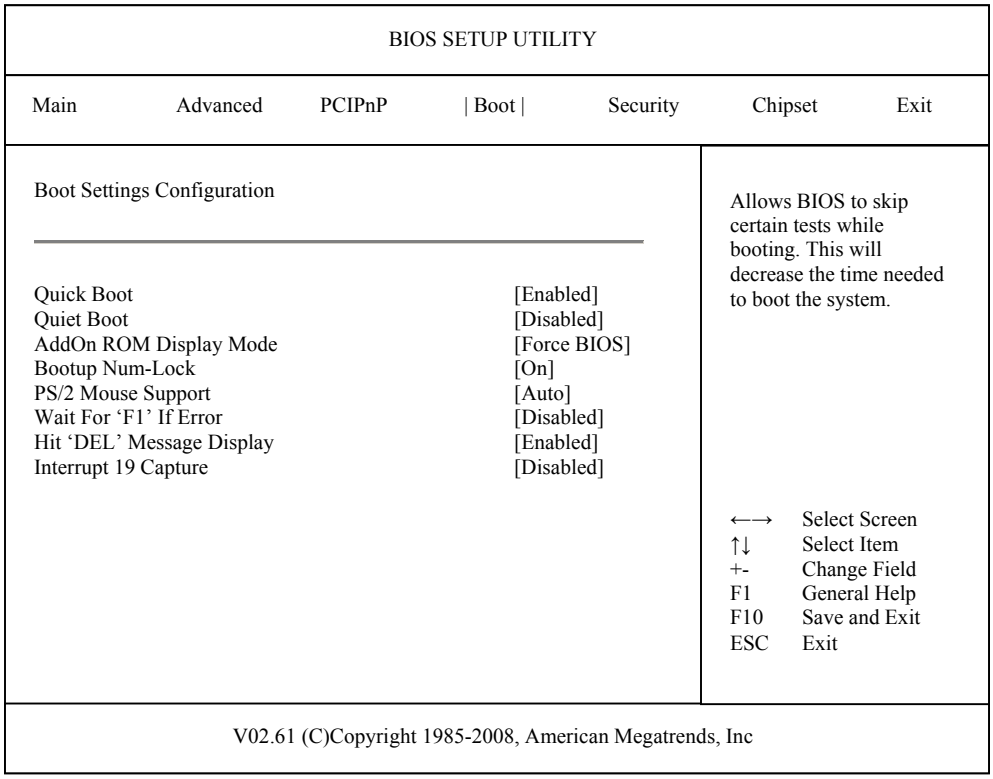
The **Hard Disk Drives** subscreen specifies the boot sequence of the hard drives available in the system.

Saving and Exiting

When you have made all desired changes to **Boot** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

BOOT SETTING CONFIGURATION

When you select **Boot Settings Configuration** from the Boot Setup Menu, the following Setup screen displays:



Boot Settings Configuration Screen

When you display the Boot Settings Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

BOOT SETTINGS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Quick Boot

This option allows you to have the AMIBIOS boot quickly when the computer is powered on or go through more complete testing. If you set the **Quick Boot** option to **Enabled**, the BIOS skips certain tests while booting and decreases the time needed to boot the system.

The Setup screen displays the system option:

Quick Boot [Enabled]

Boot Settings Configuration (continued)

Available options are:

Disabled
Enabled

Quiet Boot

This option specifies what will be displayed on the screen while the system is performing the POST routines when the computer is powered on or a soft reboot is performed.

The Setup screen displays the system option:

Quiet Boot [Disabled]

Two options are available:

- Select **Disabled** to display normal POST messages.
- Select **Enabled** to display the OEM logo instead of the POST messages.

AddOn ROM Display Mode

This option specifies the system display mode which is set at the time the AMIBIOS post routines initialize an optional option ROM.

The Setup screen displays the system option:

AddOn ROM Display Mode [Force BIOS]

Two options are available:

Select **Force BIOS** to use the display mode currently being used by AMIBIOS.
Select **Keep Current** to use the current display mode.

BootUp Num-Lock

This option enables you to turn off the Num-Lock option on the enhanced keyboard when the system is powered on. If Num-Lock is turned off, the arrow keys on the numeric keypad can be used, as well as the other set of arrow keys on the enhanced keyboard.

The Setup screen displays the system option:

BootUp Num-Lock [Off]

Available options are:

Off
On

Boot Settings Configuration (continued)

PS/2 Mouse Support

This option indicates whether or not a PS/2-type mouse is supported.

The Setup screen displays the system option:

PS/2 Mouse Support [Auto]

Available options are:

Disabled
Enabled
Auto

Wait For 'F1' If Error

Before the system boots up, the AMIBIOS executes the Power-On Self Test (POST) routines, a series of system diagnostic routines. If any of these tests fail but the system can still function, a non-fatal error has occurred. The AMIBIOS responds with an appropriate error message followed by:

Press F1 to RESUME

If this option is set to **Disabled**, a non-fatal error does not generate the "Press F1 to RESUME" message. The AMIBIOS still displays the appropriate message, but continues the booting process without waiting for the **<F1>** key to be pressed. This eliminates the need for any user response to a non-fatal error condition message. Non-fatal error messages are listed in *Appendix A - BIOS Messages*.

The Setup screen displays the system option:

Wait For 'F1' If Error [Disabled]

Available options are:
Disabled
Enabled

Hit 'DEL' Message Display

The "Hit DEL to run Setup" message displays when the system boots up. Disabling this option prevents the message from displaying.

The Setup screen displays the system option:

Hit 'DEL' Message Display [Enabled]

Available options are:
Disabled
Enabled

Boot Settings Configuration (continued)

Interrupt 19 Capture

This option allows option ROMs to trap Interrupt 19.

The Setup screen displays the system option:

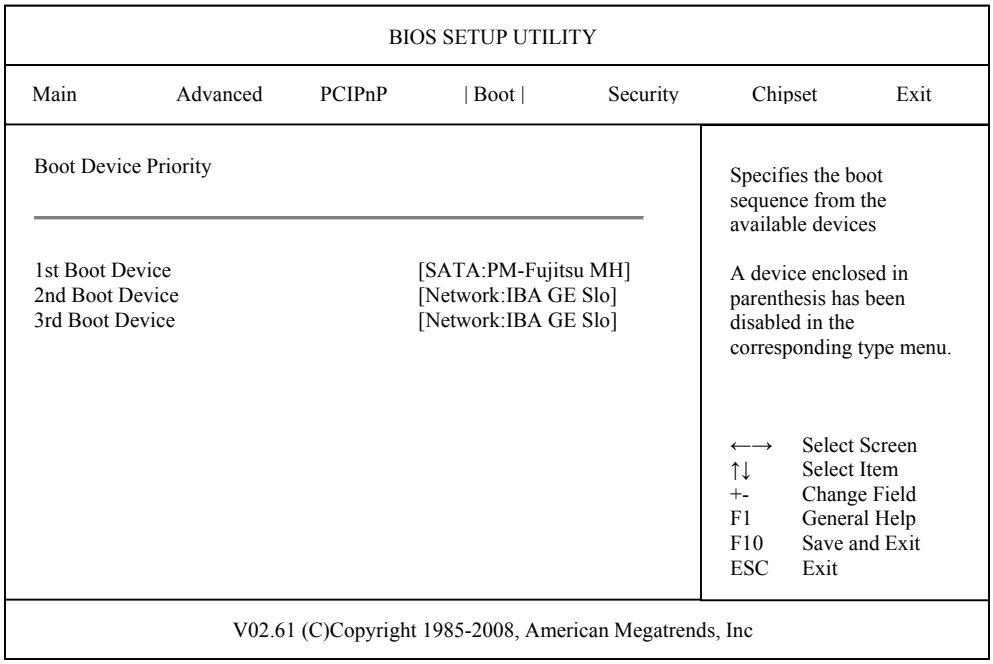
Interrupt 19 Capture [Disabled]

Available options are:

Disabled
Enabled

BOOT DEVICE PRIORITY

When you select **Boot Device Priority** from the Boot Setup Menu, a Setup screen similar to the following displays:



Boot Device Priority Screen

When you display the Boot Device Priority screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen may vary depending on the number of bootable devices available on your system.

BOOT DEVICE PRIORITY OPTIONS

1st Boot Device through the 3rd Boot Device

These options specify the order in which AMIBIOS attempts to boot the devices after the POST routines complete. The setting for each boot device line item is the description of the bootable device. The number of line items on this screen is dynamic. If new system devices are added, the new devices are displayed at the end of the list as additional line items.

The AMC supports bootup from a LAN device. In the sample screen above, the 2nd Boot Device and 3rd Boot Device line items are boot from LAN options.

Boot Device Priority (continued)

The Setup screen displays the system option(s):

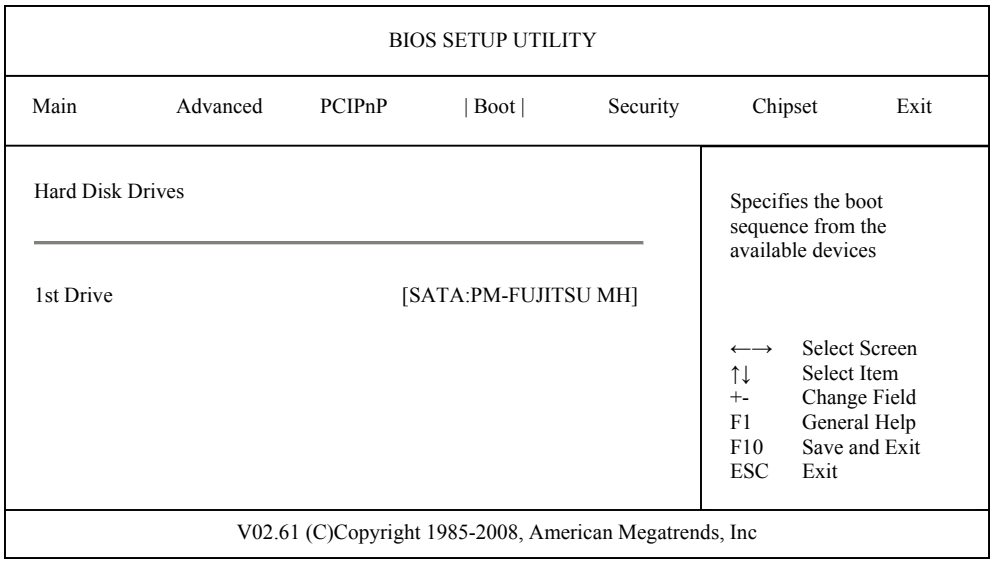
Boot Device [xxxxxxxxx]

where ### is the boot order and xxxxxxxxx is the description of the device.

NOTE: Disabled is also available as an option if you do not want a particular device to be included in the boot sequence. Setting a device to **Disabled** will eliminate unnecessary delays during the bootup process.

HARD DISK DRIVES

When you select **Hard Disk Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:



Hard Disk Drives Screen

When you display the Hard Disk Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen is determined by the number of hard disk drives available.

HARD DISK DRIVES OPTIONS

The AMC supports two SATA hard disk drives in IDE master configuration of the AMC's ICH9M primary and secondary SATA drive controller.

1st Drive/2nd Drive

When the system boots up, it searches for all hard drives and displays the description of each disk drive it has detected.

If you have more than one hard disk drive, you may change the order in which the system will attempt to boot the available hard drives by changing these line items. The number of options displayed for each line item depends on the number of hard disk drives in your system.

Disabled is also available as an option if you do not want a particular drive to be included in the boot sequence.

The Setup screen displays the system option(s):

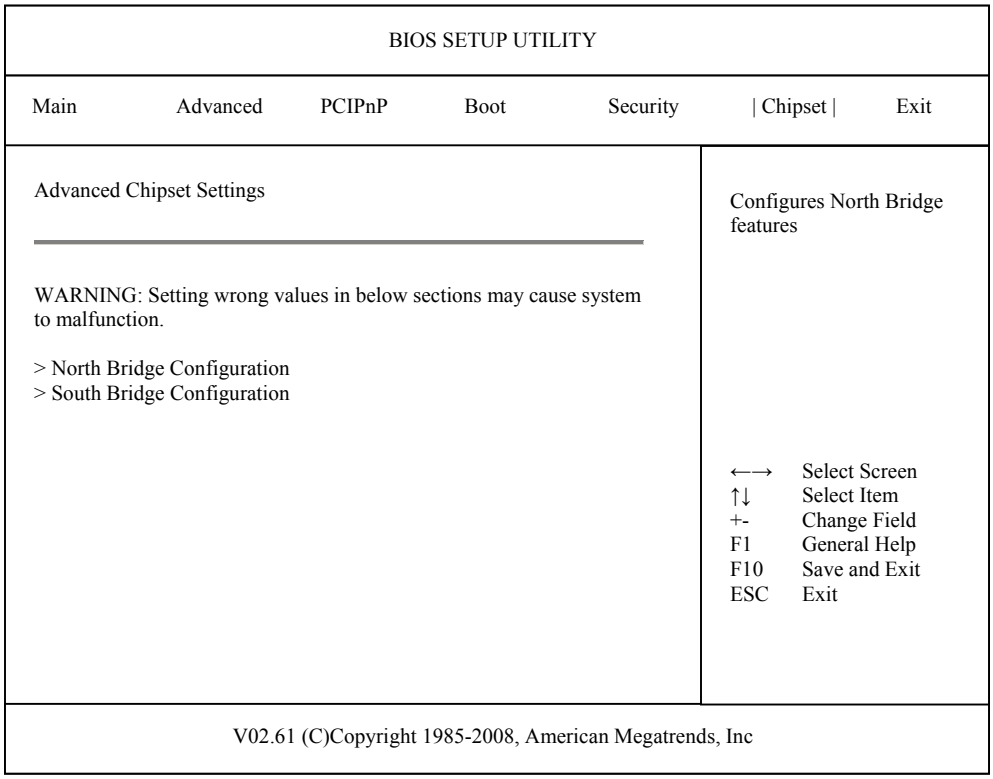
Drive [xxxxxxxxx]

where ### is the boot order and xxxxxxxxx is the description of the hard disk drive.

Chapter 7 Chipset Setup

CHIPSET SETUP

When you select **Chipset** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Chipset Setup Screen

When you display the Chipset Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Chipset Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: The values on the Chipset Setup subscreens do not necessarily reflect the values appropriate for your SHB. Refer to the explanations following the screens for specific instructions about entering correct information.

CHIPSET SETUP OPTIONS

NOTE: Do *not* change the values for any Chipset Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

North Bridge Configuration

The options on the **North Bridge Configuration** subscreen allow you to set up or modify parameters to configure the Intel® GS45 Graphics Memory Controller Hub

The following options may be modified:

- Boots Graphic Adapter Priority
- Internal Graphics Mode Select
- Max TOLUD (Top of Low Usage DRAM)
- Video Function – DVMT Mode
- Video Function – Spread Spectrum Clock

South Bridge Configuration

The options on the **South Bridge Configuration** subscreen allow you to set up or modify parameters to configure the Intel® ICH9M I/O Controller Hub.

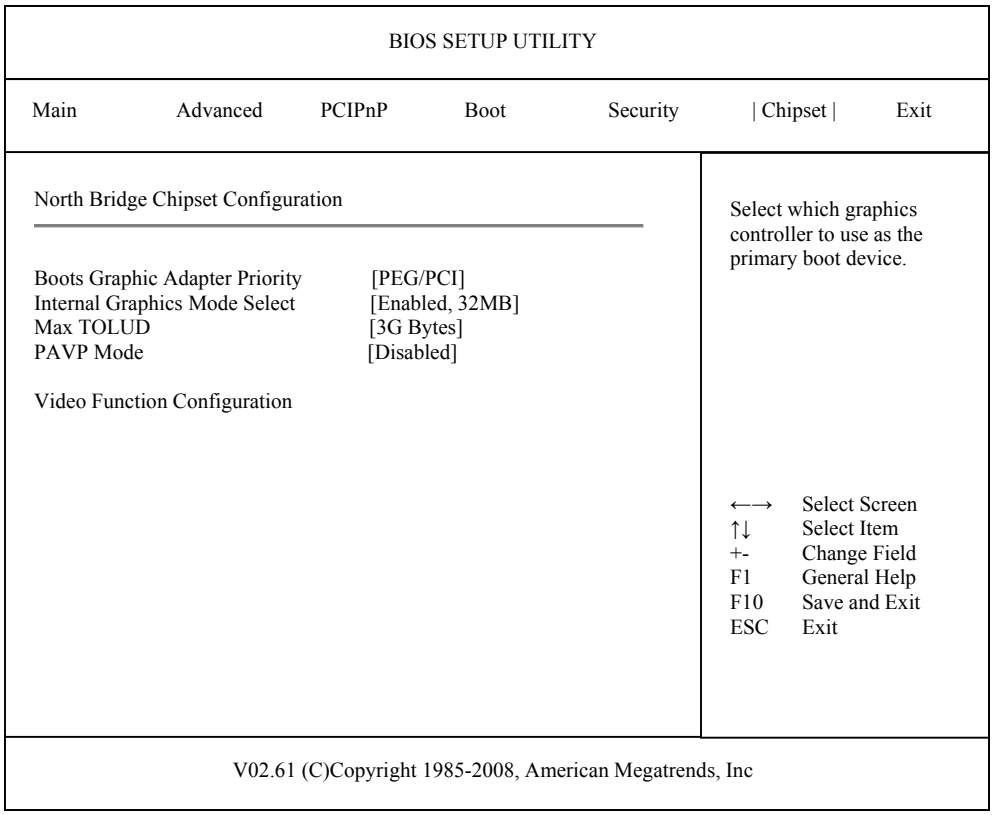
The following options may be modified:

- USB Functions
- USB Port Configure
- USB 2.0 Controller
- LCI LAN Controller
- SMBUS Controller
- Front Panel Serial Port
- PCI Express Configurations

Saving and Exiting When you have made all desired changes to **Chipset** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

NORTH BRIDGE CONFIGURATION

When you select **North Bridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:



North Bridge Configuration Screen

When you display the North Bridge Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NORTH BRIDGE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

Boots Graphic Adapter Priority

The Setup screen displays the system option:

Boots Graphic Adapter Priority [PEG/PCI]

Available options are:

IGD
PCI/IGD
PCI/PEG
PEG/IGD
PEG/PCI

North Bridge Configuration Options (continued)

Internal Graphics Mode Select

The Setup screen displays the system option:

Internal Graphic Mode Select [Enabled, 32MB]

Available options are:

Disabled
Enabled, 32MB
Enabled, 64MB
Enabled, 128MB

Max TOLUD

The Setup screen displays the system option:

Max TOLUD [3G Bytes]

Available options are:

3G Bytes
2.5G Bytes
2G Bytes

PAVP Mode

The Setup screen displays the system option:

PAVP Mode [Disabled]

Available options are:

Disabled
Lite
High

Video Function Configurations
The video setup screen provides two configuration options for DVMT mode selection and spread spectrum clock operation.

DVMT Mode Select

The Setup screed displays the system option:

DVMT Mode Select [DVMT Mode]

Available options are:

Fixed Mode
DVMT Mode

Video Function Configurations (continued)

DVMT/FIXED Memory

The Setup screed displays the system option:

DVMT/FIXED Memory [256MB]

Available options are:

128MB
256MB
Maximum DVMT

Spread Spectrum Clock

The Setup screed displays the system option:

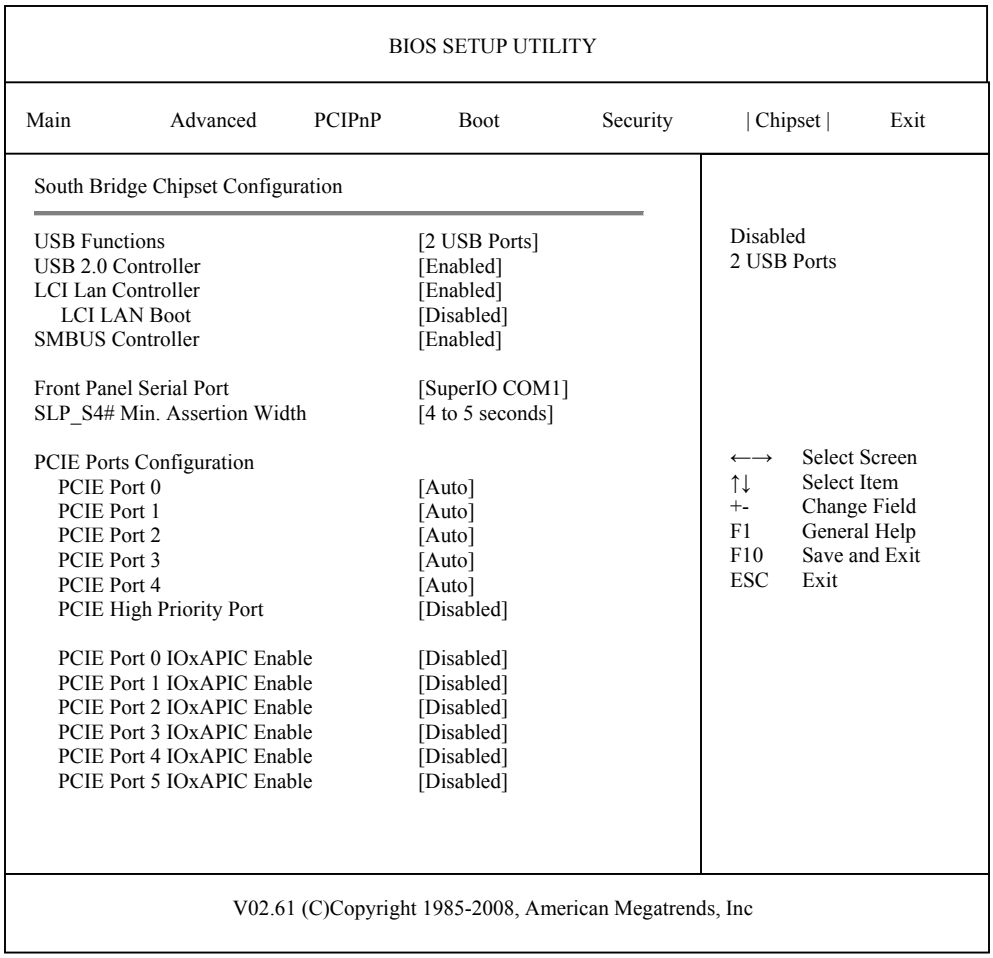
Spread Spectrum Clock [Disabled]

Available options are:

Disabled
Enabled

SOUTH BRIDGE CONFIGURATION

When you select **South Bridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:



South Bridge Configuration Screen

When you display the South Bridge Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

SOUTH BRIDGE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

USB Functions

This option specifies the number of Universal Serial Bus (USB) ports to be used.

The Setup screen displays the system option:

USB Functions [2 USB Ports]

Available options are:

Disabled
2 USB Ports

USB 2.0 Controller

This Option can only be changed from its default if USB Functions is set to Disabled.
The Setup screen displays the system option:

USB 2.0 Controller [Enabled]

Available options are:
Enabled
Disabled

LCI LAN Controller

The Setup screen displays the system option:

LCI LAN Controller [Enabled]

Available options are:

Disabled
Enabled

LCI LAN Boot

The Setup screen displays the system option in the LCI LAN controller selection is **Enabled**:

LCI LAN Boot Controller [Disabled]

Available options are:

Enabled
Disabled

SMBUS Controller

The Setup screen displays the system option:

SMBUS Controller [Enabled]

Available options are:

Enabled
Disabled

Front Panel Serial Port

This option specifies where the AMC's serial port is to be routed.

The Setup screen displays the system option:

Front Panel Serial Port [SuperIO COM1]

Available options are:

SuperIO COM1
MMC (Module Management Controller)

SLP_S4# MIN. Assertion Width

The Setup screen displays the system option:

SLP_S4# MIN. Assertion Width [4 to 5 seconds]

Available options are:

4 to 5 seconds
3 to 4 seconds
2 to 3 seconds
1 to 2 seconds

PCIE Ports Configuration

PCIE Port 0, 1, 2, 3 and 4

The Setup screen displays the system option:

PCIE Port (x) [Auto]

Available options for each port are:

Auto
Enabled
Disabled

PCIE High Priority Port

The Setup screen displays the system option:

PCIE High Priority Port [Disabled]

Available options for each port are:

Disabled
PCIE Port 0, 1, 2, 3 or 4

PCIE Ports Configuration (continued)

PCIE Port 0, 1, 2, 3 and 4 IOxAPIC Enable

The Setup screen displays the system option:

PCIE Port (x) IOxAPCI Enable [Disabled]

Available options for each port are:

Disabled
Enabled

Chapter 8 System Monitoring and Alarms

OVERVIEW

The MCP6792 uses the Intelligent Platform Management Interface (IPMI) to monitor key system functions and support various alarming functions. IPMI functionality and implementation are governed by several common industry standards. The card supports IPMI Ver. 2.0 and the specific specification details can be found at http://www.intel.com/design/servers/ipmi. The card's factory programmed Module Management Controller (MMC) is an Actel AFS6000 FPGA and houses the AMC's IPMI firmware. The card's FPGA functions as the Management Controller that enables the MCP6792's IPMI functionality. Here are higher level IPMI functions supported by the card's management module:

- Voltage Monitoring
- Temperature Monitoring
- Payload Monitoring
- FRU (Field Replacement Unit) Monitoring and Support Functions
- Logging and System Recover Functions

IPMI functions and commands are supported and executed in the card's MMC and are therefore independent of the card's processor, BIOS or operating system. In order to take advantage of the AMC's IPMI capabilities, application software must be provided by the end user, system integrator or OEM that is IPMI-aware.

SUPPORTED IPMI COMMANDS

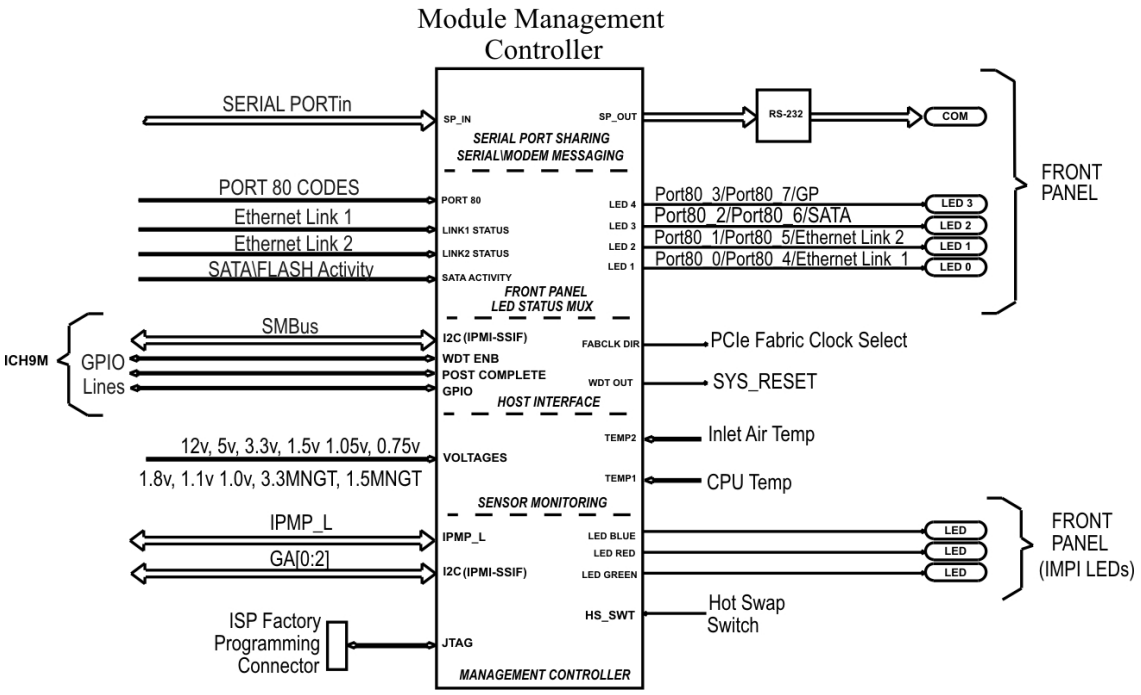
Listed below are the specific IPMI commands supported by the AMC's Module Management Controller.

Command	IPMI Ver 2.0, PICMG 3.0 or AMC.0 Spec. Reference	NetFn	CMD	MMC Spec. Requirement
IPM Device "Global Commands				
Get Device ID	Section 20.1	App	01h	Mandatory
Broadcast "Get Device ID"	Section 20.9	App	01h	Mandatory
Event Commands				
Set Event Receiver	Section 29.1	S/E	00h	Mandatory
Get Event Receiver	Section 29.2	S/E	01h	Mandatory
Platform Event ("Event Message")	Section 29.3	S/E	02h	Mandatory
Sensor Device Commands				
Get Device SDR Information	Section 35.2	S/E	20h	Mandatory
Get Device SDR	Section 35.3	S/E	21h	Mandatory
Reserve Device SDR Repository	Section 35.4	S/E	22h	Mandatory
Get Sensor Reading	Section 35.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Information	Section 34.1	Storage	10h	Mandatory
Read FRU Data	Section 34.2	Storage	11h	Mandatory
Write FRU Data	Section 34.3	Storage	12h	Mandatory
AdvancedTCA Commands	**PICMG 3.0 Spec**			
Get PICMG Properties	Table 3-9	PICMG	00h	Mandatory
FRU Control	Table 3-22	PICMG	04h	Mandatory
Get FRU LED Properties	Table 3-24	PICMG	05h	Mandatory
Get LED Color Capabilities	Table 3-25	PICMG	06h	Mandatory
Set FRU LED State	Table 3-26	PICMG	07h	Mandatory
Get FRU LED State	Table 3-27	PICMG	08h	Mandatory
Get Device Locator Record ID	Table 3-29	PICMG	0Dh	Mandatory
AMC Commands	**AMC.0 Spec**			
Set AMC Port State	Table 3-27 of AMC.0	PICMG	19h	Mandatory
Get AMC Port State	Table 3.28 of AMC.0	PICMG	1Ah	Mandatory

IPMI commands are sent to the card's Module Management Controller and the MMC in turn replies with an IPMI response. Every command has a response. Some commands and responses may have data and all responses have at least one data byte that holds the completion code for the specific command sent to the MMC.

Using the IPMI-aware application software, these commands may be sent to the MMC of the MCP6792 by other cards and/or devices in the system via the IPMB_L management bus and the Geographic Address (GA[0:2]) signal lines. The GA lines are used by the card's MMC to determine where a command is coming from and where the response needs to be sent. Voltage, chassis air temperature and CPU temperature sensor lines are connected to the card's MMC to support the IMPI sensor and event commands. The figure below illustrates the connection details for the rest of the IPMI signal lines and other function lines used by the card's Module Management Controller.

IPMI SIGNAL LINE DETAIL DIAGRAM – MODULE MANAGEMENT CONTROLLER



HOT SWAP OPERATION

Removing the MCP6792 AMC is controlled by the hot swap IPMI logic in the card's MMC and either a MicroTCA chassis' MCH or an AdvancedTCA's carrier card. The blue hot swap (HS) LED on the card's front panel indicates the specific states of the AMC's hot swap IPMI logic.

When the card's front panel latch is pulled out to position 2 as shown in Figure 7-A, SW1on the card sends a signal to the MMC indicating that the card latch has been opened. The MCC then sends out an IPMI Hot Swap event message on the IPMB_L bus. In a MicroTCA application the system's MCH reads this message and clears the deactivation-locked bit and sends a message back to the MMC along the IPMB-L bus to blink the card's HS LED. Several other commands and messages are generated in a specific sequence to prepare the system for the safe removal of the AMC.

Once the hot swap logic execution is completed, the blue LED will be turned to the full on condition. This is your indication to pull the card's front panel latch to position 3 in Figure 7-1 in order to remove the MCP6792 from the system. Make sure to follow the recommended card handling and proper anti-static procedures explained in this manual and in the *Before Your Begin* in order to prevent damage to the card.

MCP6792 FRONT PANEL LATCH DETAIL – FIGURE 7-A

Position 1 -
AMC Locked

Position 2 -
Requesting HS Removal

Position 3 –
Full extension for AMC Removal

Hot Swap Sensor Record – IPMI Sensor Number 0x0F

This sensor for the AMC's Hot Swap switch returns the three possible states of the H/S switch:

Position 1 H/S Switch Closed	–	"HOTSWAP_STATE_CLOSED"
Position 2 H/S Switch Removal Request	–	"HOTSWAP_STATE_QUISCED"
Position 3 H/S Switch Opened	–	"HOTSWAP_STATE_OPENED"

GENERAL IPMI COMMAND AND RESPONSE MESSAGE FORMATS

NetFN means Network Function and it describes the function group of a specific IPMI command. The NetFNcolumn in the *Supported IPMI Commands* table lists the NetFN function group for each supported IPMI command request along with the Command (CMD) hexadecimal code number for a specific IPMI command supported by the MMC on the Trenton MCP6792 card. Remember that every IPMI request and response has a NetFN and a command number. Just about all IPMI commands within a specific NetFN have the same NetFN number. The command number is a number within the NetFN that is specific for a particular IPMI command. The response data packets to IPMI requests come back to the card's management controller (MMC) with a one added to the NetFN number and the same command number of the IPMI request along with any response data and/or status information. Listed below are overviews of each IPMI command supported by the AMC and the IPMI message request and response formats sent or received by the MMC on the MCP6792.

IPM DEVICE GLOBAL COMMANDS

The AMC supports two commands with this NetFN Application group: Get Device ID and Broadcast Get Device ID.

Get Device ID - This command is used to get a device's hardware, software or firmware revision information. The command can also retrieve Sensor and Event Interface Command specification revision information.

MMC Message Request – NetFN = 06h, CMD = 01h (h = hexadecimal notation)
MMC Message Response – NetFN = 07h, CMD = 01h + Response Data Field

Get Device ID Response Data

Byte	Response Data Field
1	Completion Code
2	Device ID (00h = unspecified)
3	Device Revision Data [7] 1 = device supports SDRs (Sensor Data Records) 0 = device does not support SDRs [6:4] reserved, returned as 0 [3:0] Device Revision, binary encoded
4	Firmware Revision 1 [7] Device available: 0 = normal operation, 1 = device firmware [6:0] Major Firmware Revision, binary encoded
5	Firmware Revision 2 – Minor Firmware Revision, binary encoded
6	IPMI Version – Supported IPMI Command Specification Revision, BCD encoded, e.g. 02h indicates IPMI v2.0 and 51h indicates IPMI v1.5
7	Additional Device Support [7] Chassis Device that function per ICMB spec [6] Bridge *Notes: ICMB – Int. Chassis Mgmt. Bus* [5] IPMB Event Generator *IPMB – Int. Plat. Management B.* [4] IPMB Event Receiver *FRU – Field Replacement Unit.* [3] FRU inventor Device *SEL – System Event Log* [2] SEL Device *SDR – System Data Record* [1] SDR Repository Device [0] Sensor Device
8:10	Manufacturer ID Number
11:12	Product ID Number
13:16	Auxiliary Firmware Revision Information

Refer to section 20.1 of the IPMI Ver. 2.0 specification for more details on the **Get Device ID** command request and response at http://www.intel.com/design/servers/ipmi.

Broadcast Get Device ID

This command is similar to Get Device ID, but is used to broadcast requests to discover all of the intelligent devices connected to the IPMB. The command is helpful when you do not know the physical address (i.e. geographic address) of each of the devices in the system. To perform a complete discovery function using this command, multiple Broadcast Get Device ID requests need to be sent to the MMC over the card's SMBus. Each request will have different physical address information in the slave address parameter field of the command. Each device on the bus responds to the MCC command once that particular device's address is sent. Logic will need to be part of the IPMI application software provided by the end user, system integrator or OEM so that the card's MMC does not keep broadcasting command requests with addresses for devices that do not exist on the IPMB.

See section 20.9 of the IPMI Ver. 2.0 specification at http://www.intel.com/design/servers/ipmi for more details on using the **Broadcast Get Device ID** command.

EVENT COMMANDS

The IPMI event commands are classified as Sensor/Event network functions. There are three event commands supported by the AMC: Set Event Receiver, Get Event Receiver and Platform Event/ Event Message.

Set Event Receiver - Instructs the MMC where to send event messages.

MMC Message Request – NetFN = 04h, CMD = 00h + address and logical unit number
MMC Message Response – NetFN = 05h, CMD = 00h + Response Data Field

Set Event Request Data

Byte	Request Data Field
1	Event Receiver Slave Address – 0FFh disables Event Message generation, Otherwise: [7:1] IPMB (I^2C) Slave Address [0] always 0b when [7:1] holds I^2C slave address
2	[7:1] reserved [1] Event Receiver LUN (Logical Unit Number)

Set Event Response Data

Byte	Response Data Field
1	Completion Code

Get Event Receiver - Retrieves the current setting for an event receiver slave address and the receiver's local unit number.

MMC Message Request – NetFN = 04h, CMD = 01h
MMC Message Response – NetFN = 05h, CMD = 01h + Response Data Field

Get Event Response Data

Byte	Response Data Field
1	Completion Code
2	Event Receiver Slave Address – 0FFh disables Event Message generation, Otherwise: [7:1] IPMB (I^2C) Slave Address [0] always 0b(inary) when [7:1] holds I^2C slave address
3	[7:1] reserved [1] Event Receiver LUN (Logical Unit Number)

Platform Event/ Event Message – Requests for the system's BMC to process the event data and associated command.

MMC Message Request – NetFN = 04h, CMD = 02h + Request Data Field
MMC Message Response – NetFN = 05h, CMD = 02h + Response Data Field

Platform Event/ Event Message Data Fields

IPMB Messaging (IPMB, LAN, Serial/Modem, etc.)		**System Interface**	
Request Data		**Request Data**	
Byte	Data Field	**Byte**	**Data Field**
-	Generator ID (Address, LUN)	1	Generator ID
1	Event Message Revision	2	Event Message Revision
2	Sensor Type	3	Sensor Type
3	Sensor Number	4	Sensor Number
4	Event Direction | Event Type	5	Event Direction | Event Type
5	Event Data 1	6	Event Data 1
6	Event Data 2	7	Event Data 2
7	Event Data 3	8	Event Data 3
Response Data		**Response Data**	
1	Completion Code	1	Completion Code

See sections 29.1, 29.2 and 29.3 of the IPMI Ver. 2.0 specification at http://www.intel.com/design/servers/ipmi for more details on using the **Event Commands**.

SENSOR DEVICE COMMANDS

As the name implies, this class of NetFN commands are classified as Sensor/Event network functions. The MCP6792 supports the Get Device SDR Information, Get Device SDR, Reserve Device SDR Repository and Get Sensor Reading sensor device commands. *Note: SDR means Sensor Data Record.*

Get Device SDR Information – This command gets information about the collection of sensors that make up a system's Dynamic Sensor Device. Dynamic Sensor Devices are usually discovered by the Broadcast Get Device ID command. The Broadcast Get Device ID provides all of the slave addresses of the sensors making up the Dynamic Sensor Device. These sensor addresses are needed by the Get Device SDR Information command, therefore the Get Device SDR Information is usually implemented in an IPMI system after the MMC issues a Broadcast Get Device ID command.

MMC Message Request – NetFN = 04h, CMD = 20h + address and logical unit number
MMC Message Response – NetFN = 05h, CMD = 20h + Response Data Field

Get Device SDR Information Data Fields

Request Data	
(1)	Operation (optional) [7:1] reserved [0] 1b = Get SDR count. This returns the total number of Sensor Data Records in the device. 0b = Get sensor Count. This returns the number of sensors implemented on LUN this command was addressed to.
Response Data	
1	Competition Code
2	For Operation = "Get Sensor Count" (or if byte 1 not present in request): Number of sensors in device for LUN this command was addressed to. For Operating = "Get Sensor Count" Total number of SDRs in the device
3	Flags: [7] 0b = static sensor population. Indicates a fixed number of sensors. 1b = dynamic sensor population. Indicates that the sensor population may vary during system run time. [6:4] reserved [3] 1b = LUN 3 has sensors [2] 1b = LUN 2 has sensors [1] 1b = LUN 1 has sensors [0] 1b = LUN 0 has sensors
4:7	Sensor Population Change Indicator

Get Device SDR Command – This is an optional command for Static Sensor Devices and a mandatory command for Dynamic Sensor Devices. The command itself returns Sensor Data Record (SDR) information. The Reservation ID portion of the command alerts the MMC that a sensor record changed during a multi-part read command sequence.

MMC Message Request – NetFN = 04h, CMD = 21h + Request Data Field
MMC Message Response – NetFN = 05h, CMD = 21h + Response Data Field

Get Device SDR Command Data Fields

Request Data	
1	Reservation ID (LS Byte)
2	Reservation ID (MS Byte)
3	Record ID of record to Get (LS Byte)
4	Record ID of record to Get (MS Byte)
5	Offset into record
6	Bytes to read (FFh means read the entire record)
Response Data	
1	Competition Code (80h = record changed)
2	Record ID for next record (LS Byte)
3	Record ID for next record (MS Byte)
4:3+N	Requested bytes from record

Reserve Device SDR Repository – This is the command used to get the Reservation ID of a Sensor Data Record or SDR.

MMC Message Request – NetFN = 04h, CMD = 22h
MMC Message Response – NetFN = 05h, CMD = 22h + Response Data Field

Get Device SDR Command Data Fields

Response Data	
Byte	Response Data Field
1	Competition Code
2	Reservation ID (LS Byte)
3	Reservation ID (MS Byte)

Get Sensor Reading Command – This command does exactly what is says; it gets the current reading from a specific sensor. Depending on the sensor type, the sensor may return a stored value reading or it may go out a perform a scan function to obtain an updated reading after receiving the Get Sensor Reading command.

MMC Message Request – NetFN = 04h, CMD = 2Dh + Sensor Number
MMC Message Response – NetFN = 05h, CMD = 2Dh + Response Data Field

Get Sensor Reading Command Data Fields

Request Data	
1	Sensor number (FFh is reserved)
Response Data	
1	Competition Code
2	Sensor Reading
3	[7] 0b = All Event Messages disabled from this sensor [6] 0b = Sensor scanning disabled [5] 1b = Reading/state unavailable [4:0] reserved
4	For threshold-based sensors [7:6] reserved [5] 1b = ≥ upper non-recoverable threshold sensor value [4] 1b = ≥ upper critical threshold sensor value [3] 1b = ≥ upper non-critical threshold sensor value [2] 1b = ≤ lower non-recoverable threshold sensor value [1] 1b = ≤ lower critical threshold sensor value [0] 1b = ≤ lower non-critical threshold sensor value For discrete reading sensors [7] 1b = state 7 asserted [6] 1b = state 6 asserted [5] 1b = state 5 asserted [4] 1b = state 4 asserted [3] 1b = state 3 asserted [2] 1b = state 2 asserted [1] 1b = state 1 asserted [0] 1b = state 0 asserted
5	For discrete reading sensors (optional) 00h Otherwise: [7] 1b = state 14 asserted [6] 1b = state 13 asserted [5] 1b = state 12 asserted [4] 1b = state 11 asserted [3] 1b = state 10 asserted [2] 1b = state 9 asserted [1] 1b = state 8 asserted [0] 1b = state 7 asserted

See sections 35.2, 35.3, 35.4 and 35.14 of the IPMI Ver. 2.0 specification at http://www.intel.com/design/servers/ipmi for more details on using the **Sensor Device Commands**.

FRU (FIELD REPLACEMENT UNIT) DEVICE COMMANDS

Each Field Replacement Unit or FRU in a system has associated FRU inventory data that contains information such as serial number, part number, asset tag, and other descriptive information. An FRU is a logical device that may be a separate physical device or the FRU inventory information contained within the SDR Repository Device for a larger component of the system such as the system host board or the chassis. Separate FRU Inventory devices could also be implemented on the IPMB that contain FRU information for replacement modules such as memory DIMMs. The AMC supports the Get FRU Inventory Area Information, Read FRU Data and Write FRU Data commands.

Get FRU Inventory Area Information - This command returns the size of the FRU inventory area. contained with a specific device.

MMC Message Request – NetFN = 0Ah, CMD = 10h + Request Data Field
MMC Message Response – NetFN = 0Bh, CMD = 10h + Response Data Field

Get FRU Inventory Area Information Data Fields

Request Data	
Byte	Request Data Field
1	FRU Device ID (FFh is reserved)
Response Data	
Byte	Response Data Field
1	Competition Code
2	FRU Inventory area size in bytes (LS Byte)
3	FRU Inventory area size in bytes (MS Byte)
4	Requested bytes from record

Read FRU Data - This is the command used to read the FRU data from the FRU Inventory Information area contained within the target device. Specific logical offsets with a device and FRU physical address locations are used with this command to gather the device's FRU data. Typically FRU data is stored in flash at address 1234h and offset 0000h is used to access start of the FRU data. A device's specific offset can be obtained with the GET FRU Inventory Area Information command.

MMC Message Request – NetFN = 0Ah, CMD = 11h + Request Data Field
MMC Message Response – NetFN = 0Bh, CMD = 11h + Response Data Field

Read FRU Data Fields

Request Data	
Byte	Request Data Field
1	FRU Device ID (FFh is reserved)
2	FRU Inventory Offset to read, LS Byte
3	FRU Inventory Offset to read, MS Byte
4	Count to read
Response Data	
Byte	Response Data Field
1	Competition Code – Generic plus command specific, 81h = FRU Device Busy
2	Count returned
3:2+N	Requested data

Write FRU Data - Use this command to write specific data into the device's FRU Inventory Information area. The same FRU address and offset information is needed with this command to ensure the data is placed into the desired location within the information area.

MMC Message Request – NetFN = 0Ah, CMD = 12h + Request Data Field
MMC Message Response – NetFN = 0Bh, CMD = 12h + Response Data Field

Write FRU Data Fields

Request Data	
Byte	Request Data Field
1	FRU Device ID (FFh is reserved)
2	FRU Inventory Offset to read, LS Byte
3	FRU Inventory Offset to read, MS Byte
4:3+N	Data to write
Response Data	
Byte	Response Data Field
1	Competition Code – Generic plus command specific: 80h = Write-protected Offset, instruction could not be completed 81h = FRU Device Busy
2	Count written

See sections 34.1, 34.2 and 34.3 of the IPMI Ver. 2.0 specification at http://www.intel.com/design/servers/ipmi for more details on using the **FRU Device Commands**.

PICMG 3.0 OR ADVANCEDTCA/MICROTCA COMMANDS

The shelf management principles first defined in chapter three of the *PICMG 3.0 R2.0 AdvancedTCA Base Specification* apply to IPMI implementations in both AdvancedTCA and MicroTCA systems. The MCP6792 supports the mandatory PICMG/AdvancedTCA IPMI commands of Get PICMG Properties, FRU Control, Get FRU LED Properties, Get LED Color Capabilities, Set FRU LED State, Get FRU LED State and Get Device Locator Record ID.

Get PICMG Properties - This command provides a method to find out the maximum supported FRU Device ID supported by the card's MMC.

MMC Message Request – NetFN = 2Ch, CMD = 00h
MMC Message Response – NetFN = 2Dh, CMD = 00h + Response Data Field

Get PICMG Properties Data Fields

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h
3	PICMG Extension Version [7:4] = BCD encoded minor version [3:0] = BCD encoded major version
4	Max FRU Device ID
5	FRU Device ID for MMC

FRU Control - This command provides a method to enable base level control of a FRU's primary function or payload. If a device receiving the control option request does not support a particular FRU control option then the device will respond with a CCh completion code, which means "Invalid Data Field Request".

MMC Message Request – NetFN = 2Ch, CMD = 04h + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 04h + Response Data Field

FRU Control Data Fields

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	FRU Device ID
3	FRU Control Option: 00h = Cold Reset 01h = Warm Reset 02h = Reboot 03h = Issue Diagnostic Reboot 04h –FFh = reserved
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h

Get FRU LED Properties - This command allows the system software to find out which LEDs are under the control of the AMC's management module. In the case of the MCP6792 the IPMI-related front panel FLT, PSON and HS are controlled by the MMC. LEDs 1,2, 3 and 4 are examples of application specific LEDs under control of the card's MMC.

MMC Message Request – NetFN = 2Ch, CMD = 05h + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 05h + Response Data Field

Get FRU LED Properties Data Fields

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	FRU Device ID
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h
3	General Status LED Properties: [7:4] Reserved, set to 0 [3] LED3 [2] LED2 [2] LED1 [0] Blue LED
4	Application Specific LED Count 00h-FB Number of LEDs controlled by MMC, none = 00h FCh-FFh Reserved

Get LED Color Capabilities – When using multi-color LEDs it is beneficial to know the supported colors on a specific LED before issuing a Set FRU LED State command.

MMC Message Request – NetFN = 2Ch, CMD = 06h + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 06h + Response Data Field

Get LED Color Capabilities Data Fields

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	FRU Device ID
3	LED ID FFh Reserved
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h
3	LED Color Capabilities: [7] Reserved, set to 0 [6] LED supports white [5] LED supports orange [4] LED supports amber [3] LED supports green [2] LED supports red [1] LED supports blue [0] Reserved, set to 0
4	Default LED Color in Local Control State [7:4] Reserved, set to 0 [3:0] Consists of: 0h = Reserved 1h = Blue 2h = Red 3h = Green 4h = Amber 5h = Orange 6h = White 7h-Fh = Reserved
5	Default LED Color in Override State [7:4] Reserved, set to 0 [3:0] Consists of: 0h = Reserved 1h = Blue 2h = Red 3h = Green 4h = Amber 5h = Orange 6h = White 7h-Fh = Reserved

Set FRU LED State – This command enables the MMC to control the on/off states of the front panel LEDs on the MCP6792. The command includes codes that control the duty cycle of the LEDs and lamp test functions.

MMC Message Request – NetFN = 2Ch, CMD = 07h + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 07h + Response Data Field

Set FRU LED State Data Fields

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	FRU Device ID
3	LED ID 00h Blue LED 01h LED1 02h LED2 03h LED3 04h-FEh OEM Defined LEDs FFh Lamp Test
4	LED Function 00h LED off override 01h-FAh LED blinking override FBh Lamp test state FCh LED state restore FDh-FEh Reserved FFh LED on override
5	On-duration, see PICMG 3.0 spec., table 3-26 for details on acceptable values
6	Color when illuminated [7:4] Reserved, set to 0 [3:0] Consists of: 0h = Reserved 1h = Blue 2h = Red 3h = Green 4h = Amber 5h = Orange 6h = White 7h-Dh = Reserved Eh = Do not change Fh = Use default color
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h

Get FRU LED State – Use this command to find out the state of a specific LED or if a particular control state is supported on a particular LED.

MMC Message Request – NetFN = 2Ch, CMD = 08h + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 08h + Response Data Field

Get FRU LED State Data Fields

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	FRU Device ID
3	LED ID 00h Blue LED 01h LED1 02h LED2 03h LED3 04h-FEh OEM Defined LEDs FFh Reserved
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h
3	LED States [7:3] Reserved [2] 1b if Lamp Test enabled [1] 1b if override state enabled [0] 1b MMC has a Local Control state
4	Local Control LED Function 00h LED off 01h – FAh LED blinking, see PICMG 3.0 spec for value definations FBh – FEh Reserved FFh LED on
5	Local Control On-duration, see PICMG 3.0 spec for value definations
6	Local Control Color [7:4] Reserved, set to 0 [3:0] Consists of: 0h = Reserved 4h = Amber 1h = Blue 5h = Orange 2h = Red 6h = White 3h = Green 7h-Fh = Reserved
[7]	Override State LED Function 00h LED off 01h – FAh LED blinking, see PICMG 3.0 spec for value definations FBh – FEh Reserved FFh LED on
[8]	Override State On-duration, see PICMG 3.0 spec for value definations
[9]	Overide State Color [7:4] Reserved, set to 0 [3:0] Consists of: 0h = Reserved 4h = Amber 1h = Blue 5h = Orange 2h = Red 6h = White 3h = Green 7h-Fh = Reserved
[10]	Lamp Test Duration, see PICMG 3.0 spec for value definations

Get Device Locator Record ID - Provides information to the AdvancedTCA's shelf manager or the MicroTCA's MCH that makes it easier for these components to quickly access the specific sensor or FRU records it needs to perform various system-level IMPI functions.

MMC Message Request – NetFN = 2Ch, CMD = 0Dh + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 0Dh + Response Data Field

Get Device Locator Record ID

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	FRU Device ID, see PICMG 3.0 spec. for value information
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h
3	Record ID LS – Least significant byte of the Record ID for the requested Device Locator SDR
4	Record ID MS – Most significant byte of the Record ID for the requested Device Locator SDR

See tables 3-9, 3-22, 3-24, 3-25, 3-26, 3-37 and 3-29 in the ***PICMG 3.0 R2.0 AdvancedTCA Base Specification*** for the detailed information necessary to fully implement these IPMI commands. The commands are fully supported on the Trenton MCP6782 and you may need some additional information from the specification to successfully use the commands in your specific IPMI implementation. These commands may prove essential in certain AdvancedTCA and MicroTCA system applications.

AMC COMMANDS FOR IPMI

The PICMG AMC.0 specification requires defines two mandatory IPMI commands that are supported on the MCP6792: Set AMC Port State and Get AMC Port State.

Set AMC Port State – This command enables or disables ports that are linked to an AMC channel using the link descriptor information contained within the AMC's point-to-point connectivity record. Link descriptors are used by AMCs that have configurable interfaces. Typically, this command is only used for trouble shooting purposes. The MCP6792 has a configurable PCI Express interface routed to the edge card connector of the AMC. It's conceivable that the user's supplied IPMI application software could use this command to trouble shoot PCI Express devices that are connected to the PCIe interface of the card.

MMC Message Request – NetFN = 2Ch, CMD = 19h + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 19h + Response Data Field

Set AMC Port State

Request Data	
Byte	**Request Data Field**
1	PICMG Identifier, value must be 00h
2 -5	Link Descriptor Information [31:24] Link Grouping ID [23:20] Link Type Extension [19:12] Link Type [11] Lane 3 Bit Flag [10] Lane 2 Bit Flag [9] Lane 1 Bit Flag [8] Lane 0 Bit Flag [7:0] AMC Channel ID
6	State 00h = Disable 01h = Enable
(7)	Only exits if the AMC Channel ID points to an ATCA carrier device [7:4] Reserved – write as 0h [3:0] ID of a device located on the ATCA carrier
Response Data	
Byte	**Response Data Field**
1	Competition Code
2	PICMG Identifier, value must be 00h

Get AMC Port State - This is a query command that allows you to find out the state of a particular link on a specific AMC channel.

MMC Message Request – NetFN = 2Ch, CMD = 1Ah + Request Data Field
MMC Message Response – NetFN = 2Dh, CMD = 1Ah + Response Data Field

Get AMC Port State

Request Data	
Byte	Request Data Field
1	PICMG Identifier, value must be 00h
2	AMC Channel ID
(3)	Only exits if the AMC Channel ID points to an ATCA carrier device [7:4] Reserved – write as 0h [3:0] ID of a device located on the ATCA carrier
Response Data	
Byte	Response Data Field
1	Competition Code
2	PICMG Identifier, value must be 00h
(3:5)	Link Info 1, LS byte first, only present if the channel ID has the defined link [23:16] Link Grouping ID [15:12] Link Type Extension [11:4] Link Type [3] Lane 3 Port [2] Lane 2 Port [1] Lane 1 Port [0] Lane 0 Port
(6)	State 1, only present if Link Info 1 is present 00h = Disable 01h = Enable
(7:9)	Link Info 2, LS byte first
(10)	State 2
(11:13)	Link Info 3, LS byte first
(14)	State 3
(15:17)	Link Info 4, LS byte first
(18)	State 4

See tables 3-27 and 3-28 in the ***PICMG AMC.0 Advanced Mezzanine Card Base Specification*** for the detailed information necessary to fully implement these IPMI commands. The commands are fully supported on the Trenton MCP6782 and you may need some additional information from the specification to successfully use the commands in your specific IPMI implementation. These commands may prove essential in certain AdvancedTCA and MicroTCA system applications.

SENSOR DATA RECORDS

The following tables list some of the most common IPMI voltage and temperature sensor commands supported in the Module Management Controller on the MCP6792 PrAMC.

The sensor ID numbers are Hexadecimal values and the values returned by these sensors are Base 10 numeric numbers. These numbers go into a formula to produce the value indicated in the "What the returned data means" column. Contact Trenton for detailed information on this calculation.

Processor Die Temperature

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrTempHPT	
SENSOR_ASCII_NAME	CPU TEMP (info)	
SENSOR_NUMBER	0x01 (data)	
SENSOR_TYPE	SENSOR_TYPE_TEMP (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA94 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA94 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	155 (data received example)	CPU Die temp = 115° C
THRESHOLD_UpperCritical	140 (data received example)	CPU Die temp = 100° C
THRESHOLD_UpperNonCritical	125 (data received example)	CPU Die temp = 85° C
THRESHOLD_LowerNonCritical	55 (data received example)	CPU Die temp = 15° C
THRESHOLD_LowerrCritical	45 (data received example)	CPU Die temp = 5° C
THRESHOLD_LowerNonRecoverable	30 (data received example)	CPU Die temp = -10° C
NORMAL_MAX	125 (info)	85° C
NORMAL_READING	95 (info)	50° C
NORMAL_MIN	50 (info)	10° C

Ambient Board Temperature

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrTempIAT	
SENSOR_ASCII_NAME	Ambient TEMP (info)	
SENSOR_NUMBER	0x02 (data)	
SENSOR_TYPE	SENSOR_TYPE_TEMP (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA80 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA80 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	100 (data received example)	Ambient temp = 60° C
THRESHOLD_UpperCritical	95 (data received example)	Ambient temp = 55° C
THRESHOLD_UpperNonCritical	85 (data received example)	Ambient temp = 45° C
THRESHOLD_LowerNonCritical	50 (data received example)	Ambient temp = 10° C
THRESHOLD_LowerrCritical	40 (data received example)	Ambient temp = 0° C
THRESHOLD_LowerNonRecoverable	35 (data received example)	Ambient temp = -5° C
NORMAL_MAX	85 (info)	45° C
NORMAL_READING	65 (info)	25° C
NORMAL_MIN	40 (info)	0° C

3.3V Management Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVoltM3V3	
SENSOR_ASCII_NAME	MP_3V3 (info)	
SENSOR_NUMBER	0x03 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	226 (data received example)	MP3.3V Level = 3.616V
THRESHOLD_UpperCritical	218 (data received example)	MP3.3V Level = 3.488V
THRESHOLD_UpperNonCritical	215 (data received example)	MP3.3V Level = 3.440V
THRESHOLD_LowerNonCritical	198 (data received example)	MP3.3V Level = 3.168V
THRESHOLD_LowerrCritical	195 (data received example)	MP3.3V Level = 3.120V
THRESHOLD_LowerNonRecoverable	187 (data received example)	MP3.3V Level = 2.992V
NORMAL_MAX	215 (info)	3.440V
NORMAL_READING	206 (info)	3.296V
NORMAL_MIN	198 (info)	3.168V

1.5V Management Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVoltM1V5	
SENSOR_ASCII_NAME	MP_1V5 (info)	
SENSOR_NUMBER	0x04 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	165 (data received example)	MP1.5V Level = 1.650V
THRESHOLD_UpperCritical	161 (data received example)	MP1.5V Level = 1.610V
THRESHOLD_UpperNonCritical	157 (data received example)	MP1.5V Level = 1.570V
THRESHOLD_LowerNonCritical	143 (data received example)	MP1.5V Level = 1.430V
THRESHOLD_LowerrCritical	139 (data received example)	MP1.5V Level = 1.390V
THRESHOLD_LowerNonRecoverable	135 (data received example)	MP1.5V Level = 1.350V
NORMAL_MAX	157 (info)	1.570V
NORMAL_READING	150 (info)	1.500V
NORMAL_MIN	143 (info)	1.430V

12V Payload Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVoltP12V	
SENSOR_ASCII_NAME	PP_12V (info)	
SENSOR_NUMBER	0x05 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	219 (data received example)	PP12V Level = 14.016V
THRESHOLD_UpperCritical	212 (data received example)	PP12V Level = 13.568V
THRESHOLD_UpperNonCritical	205 (data received example)	PP12V Level = 13.120V
THRESHOLD_LowerNonCritical	169 (data received example)	PP12V Level = 10.816V
THRESHOLD_LowerrCritical	162 (data received example)	PP12V Level = 10.368V
THRESHOLD_LowerNonRecoverable	152 (data received example)	PP12V Level = 9.728V
NORMAL_MAX	205 (info)	13.120V
NORMAL_READING	188 (info)	12.032V
NORMAL_MIN	169 (info)	10.816V

5.0V Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt5V0	
SENSOR_ASCII_NAME	5V0 (info)	
SENSOR_NUMBER	0x06 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	172 (data received example)	5.0V Level = 5.500V
THRESHOLD_UpperCritical	164 (data received example)	5.0V Level = 5.250V
THRESHOLD_UpperNonCritical	162 (data received example)	5.0V Level = 5.175V
THRESHOLD_LowerNonCritical	151 (data received example)	5.0V Level = 4.825V
THRESHOLD_LowerrCritical	148 (data received example)	5.0V Level = 4.750V
THRESHOLD_LowerNonRecoverable	141 (data received example)	5.0V Level = 4.500V
NORMAL_MAX	162 (info)	5.175V
NORMAL_READING	156 (info)	5.000V
NORMAL_MIN	151 (info)	4.825V

3.3V Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt3V3	
SENSOR_ASCII_NAME	3V3 (info)	
SENSOR_NUMBER	0x07 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	227 (data received example)	3.3V Level = 3.630V
THRESHOLD_UpperCritical	217 (data received example)	3.3V Level = 3.465V
THRESHOLD_UpperNonCritical	213 (data received example)	3.3V Level = 3.416V
THRESHOLD_LowerNonCritical	199 (data received example)	3.3V Level = 3.185V
THRESHOLD_LowerrCritical	196 (data received example)	3.3V Level = 3.135V
THRESHOLD_LowerNonRecoverable	186 (data received example)	3.3V Level = 2.970V
NORMAL_MAX	213 (info)	3.416V
NORMAL_READING	206 (info)	3.300V
NORMAL_MIN	199 (info)	3.185V

1.5V Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt1V5	
SENSOR_ASCII_NAME	1V5 (info)	
SENSOR_NUMBER	0x08 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	204 (data received example)	1.5V Level = 1.635V
THRESHOLD_UpperCritical	197 (data received example)	1.5V Level = 1.575V
THRESHOLD_UpperNonCritical	194 (data received example)	1.5V Level = 1.553V
THRESHOLD_LowerNonCritical	181 (data received example)	1.5V Level = 1.448V
THRESHOLD_LowerrCritical	178 (data received example)	1.5V Level = 1.425V
THRESHOLD_LowerNonRecoverable	171 (data received example)	1.5V Level = 1.365V
NORMAL_MAX	194 (info)	1.553V
NORMAL_READING	188 (info)	1.500V
NORMAL_MIN	181 (info)	1.448V

1.05V Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt1V05	
SENSOR_ASCII_NAME	1V05 (info)	
SENSOR_NUMBER	0x09 (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	143 (data received example)	1.05V Level = 1.145V
THRESHOLD_UpperCritical	138 (data received example)	1.05V Level = 1.103V
THRESHOLD_UpperNonCritical	136 (data received example)	1.05V Level = 1.087V
THRESHOLD_LowerNonCritical	127 (data received example)	1.05V Level = 1.013V
THRESHOLD_LowerrCritical	125 (data received example)	1.05V Level = 0.998V
THRESHOLD_LowerNonRecoverable	119 (data received example)	1.05V Level = 0.956V
NORMAL_MAX	136 (info)	1.087V
NORMAL_READING	131 (info)	1.050V
NORMAL_MIN	127 (info)	1.013V

0.75V Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt0V75	
SENSOR_ASCII_NAME	0V75 (info)	
SENSOR_NUMBER	0x0A (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	204 (data received example)	0.75V Level = 0.818V
THRESHOLD_UpperCritical	197 (data received example)	0.75V Level = 0.788V
THRESHOLD_UpperNonCritical	194 (data received example)	0.75V Level = 0.776V
THRESHOLD_LowerNonCritical	181 (data received example)	0.75V Level = 0.724V
THRESHOLD_LowerrCritical	178 (data received example)	0.75V Level = 0.713V
THRESHOLD_LowerNonRecoverable	171 (data received example)	0.75V Level = 0.683V
NORMAL_MAX	194 (info)	0.776V
NORMAL_READING	188 (info)	0.750V
NORMAL_MIN	181 (info)	0.724V

VCCore CPU Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVoltVCCORE	
SENSOR_ASCII_NAME	VCPU (info)	
SENSOR_NUMBER	0x0B (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	177 (data received example)	VCCore Level = 1.418V
THRESHOLD_UpperCritical	171 (data received example)	VCCore Level = 1.365V
THRESHOLD_UpperNonCritical	164 (data received example)	VCCore Level = 1.313V
THRESHOLD_LowerNonCritical	98 (data received example)	VCCore Level = 0.788V
THRESHOLD_LowerrCritical	92 (data received example)	VCCore Level = 0.735V
THRESHOLD_LowerNonRecoverable	85 (data received example)	VCCore Level = 0.683V
NORMAL_MAX	177 (info)	1.418V
NORMAL_READING	131 (info)	1.050V
NORMAL_MIN	85 (info)	0.683V

1.8V LAN Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt1V8LAN	
SENSOR_ASCII_NAME	1V8LAN (info)	
SENSOR_NUMBER	0x0C (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	123 (data received example)	1.8V LAN = 1.962V
THRESHOLD_UpperCritical	118 (data received example)	1.8V LAN = 1.890V
THRESHOLD_UpperNonCritical	116 (data received example)	1.8V LAN = 1.863V
THRESHOLD_LowerNonCritical	109 (data received example)	1.8V LAN = 1.737V
THRESHOLD_LowerrCritical	107 (data received example)	1.8V LAN = 1.710V
THRESHOLD_LowerNonRecoverable	102 (data received example)	1.8V LAN = 1.638V
NORMAL_MAX	116 (info)	1.863V
NORMAL_READING	113 (info)	1.800V
NORMAL_MIN	109 (info)	1.737V

1.1V LAN Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt1V1LAN	
SENSOR_ASCII_NAME	1V1LAN (info)	
SENSOR_NUMBER	0x0D (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	150 (data received example)	1.1V LAN = 1.199V
THRESHOLD_UpperCritical	144 (data received example)	1.1V LAN = 1.155V
THRESHOLD_UpperNonCritical	142 (data received example)	1.1V LAN = 1.139V
THRESHOLD_LowerNonCritical	133 (data received example)	1.1V LAN = 1.062V
THRESHOLD_LowerrCritical	131 (data received example)	1.1V LAN = 1.045V
THRESHOLD_LowerNonRecoverable	125 (data received example)	1.1V LAN = 1.001V
NORMAL_MAX	142 (info)	1.139V
NORMAL_READING	138 (info)	1.100V
NORMAL_MIN	133 (info)	1.062V

1.05V LAN Power

Sensor Data Record Parameter	Sensor Info / Data Sent or Received	What the returned data means
SENSOR_NAME	SdrVolt1V05LAN	
SENSOR_ASCII_NAME	1V05LAN (info)	
SENSOR_NUMBER	0x0E (data)	
SENSOR_TYPE	SENSOR_TYPE_VOLTAGE (data)	
LOWER_THRESHOLD_READING_MASK	0x7 (data)	
ASSERTION_EVENT_MASK	0xA95 (data)	
UPPER_THRESHOLD_READING_MASK	0x7 (data)	
DEASSERTION_EVENT_MASK	0xA95 (data)	
SETTABLE_THRESHOLD_MASK	0x00 (data)	
READABLE_THRESHOLD_MASK	0x3F (data)	
THRESHOLD_UpperNonRecoverable	143 (data received example)	1.05V LAN = 1.145V
THRESHOLD_UpperCritical	138 (data received example)	1.05V LAN = 1.103V
THRESHOLD_UpperNonCritical	136 (data received example)	1.05V LAN = 1.087V
THRESHOLD_LowerNonCritical	127 (data received example)	1.05V LAN = 1.013V
THRESHOLD_LowerrCritical	125 (data received example)	1.05V LAN = 0.998V
THRESHOLD_LowerNonRecoverable	119 (data received example)	1.05V LAN = 0.956V
NORMAL_MAX	136 (info)	1.087V
NORMAL_READING	131 (info)	1.050V
NORMAL_MIN	127 (info)	1.013V

The sensor ID numbers are Hexadecimal values and the values returned by these sensors are Base 10 numeric numbers. These numbers go into a formula to produce the value indicated in the “What the returned data means” column. Contact Trenton for detailed information on this calculation.

Appendix A BIOS Messages

BIOS BEEP CODES

Errors may occur during the POST (Power-On Self Test) routines which are performed each time the system is powered on.

Non-fatal errors are those which, in most cases, allow the system to continue the bootup process. The error message normally appears on the screen. See *BIOS Error Messages* later in this section for descriptions of these messages.

Fatal errors are those which will not allow the system to continue the bootup procedure.

These fatal errors are usually communicated through a series of audible beeps. Each error message has its own specific beep code, defined by the number of beeps following the error detection. The following table lists the errors which are communicated audibly.

Beep Codes	Description
1	Memory refresh timer error
2	Parity Error
3	Main memory read/write test error
4	Timer not operational
5	Processor error
6	Keyboard controller BAT test error
7	General exception error
8	Display memory error
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

BIOS BEEP CODE TROUBLESHOOTING

Beep Counts	Description
1, 2 or 3	Reseat the memory or replace with known good modules.
4-7, 9-11	Fatal error. Perform the following steps before calling Technical Support. Remove all expansion cards and try to reboot. If the beep code is still generated, call Technical Support. If the beep code is not generated, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem recurs. This will indicate the malfunctioning card.
8	The board may be faulty. Call Technical Support.

BIOS ERROR MESSAGES

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press F1 to Resume

Note the error message and press the **<F1>** key to continue with the bootup procedure.

NOTE: If the **Wait for 'F1' If Any Error** option in the Advanced Setup portion of the BIOS Setup Program has been set to **Disabled**, the "Press F1 to Resume" prompt will not appear on the last line. The bootup procedure will continue without waiting for operator response.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing an ERROR Message Line 2, the text will be "RUN SETUP UTILITY." Pressing the **<F1>** key will invoke the BIOS Setup Utility.

A description of each error message appears below.

Memory Errors

Message	Description
Gate20 Error	The BIOS is unable to properly control the SBC's Gate A20 function, which controls access to memory over 1MB. This may indicate a problem with the board.
Multi-Bit ECC Error	This message only occurs on systems using ECC enabled memory modules. ECC memory has the ability to correct singlebit errors that may occur from faulty memory modules. A multiple bit corruption of memory has occurred, and the ECC memory algorithm cannot correct it. This may indicate a defective memory module.
Parity Error	Fatal memory parity error. System halts after displaying this message.

Boot Errors

Message	Description
Boot Failure	This is a generic message indicating the BIOS could not boot from a particular device. This message is usually followed by other information concerning the device.
Invalid Boot Diskette	A diskette was found in the drive, but it is not configured as a bootable diskette.
Drive Not Ready	The BIOS was unable to access the drive because it indicated it was not ready for data transfer. This is often reported by drives when no media is present.

BIOS ERROR MESSAGES (CONTINUED)

Boot Errors (Continued)

Message	Description
A: Drive Error	The BIOS attempted to configure the A: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive.
B: Drive Error	The BIOS attempted to configure the B: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive.
Insert BOOT diskette in A:	The BIOS attempted to boot from the A: drive, but could not find a proper boot diskette.
Reboot and Select proper Boot device or Insert Boot Media in selected Boot device	BIOS could not find a bootable device in the system and/or removable media drive does not contain media.
NO ROM BASIC	This message occurs on some systems when no bootable device can be detected.

Storage Device Errors

Message	Description
The following errors are typically displayed when the BIOS is trying to detect and configure IDE/ ATAPI devices in POST.	
XXXXXX Hard Disk Error XXXXXX - ATAPI Incompatible	Messages in this format indicate that the specified device could not be properly initialized by the BIOS. Possible message are: Primary Master Hard Disk Error Primary Slave Hard Disk Error Secondary Master Hard Disk Error Secondary Slave Hard Disk Error Primary Master Drive - ATAPI Incompatible Primary Slave Drive - ATAPI Incompatible Secondary Master Drive - ATAPI Incompatible Secondary Slave Drive - ATAPI Incompatible
The following messages can be reported by an ATAPI device using the S.M.A.R.T. error reporting standard. The S.M.A.R.T. failure message may indicate the need to replace the hard disk.	
S.M.A.R.T. Capable but Command Failed	The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed.
S.M.A.R.T. Command Failed	The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed.
S.M.A.R.T. Status BAD, Backup and Replace	A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure.
S.M.A.R.T. Capable and Status BAD	A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure.

BIOS ERROR MESSAGES (CONTINUED)

Virus Related Errors

Message	Description
The following messages only display if Virus Detection is enabled in the BIOS Setup Utility.	
BootSector Write !!	The BIOS has detected software attempting to write to a drive's boot sector. This is flagged as possible virus activity.
VIRUS: Continue (Y/N)?	The BIOS has detected possible virus activity.

System Configuration Errors

Message	Description
DMA-2 Error	Error initializing secondary DMA controller. This is a fatal error, often indicating a problem with system hardware.
DMA Controller Error	POST error while trying to initialize the DMA controller. This is a fatal error, often indicating a problem with system hardware.
Checking NVRAM..Update Failed	BIOS could not write to the NVRAM block. This message appears when the FLASH part is write-protected or if there is no FLASH part (system uses a PROM or EPROM).
Microcode Error	BIOS could not find or load the CPU Microcode Update to the processor. This message only applies to Intel processors. The message is most likely to appear when a brand new processor is installed in an SBC with an outdated BIOS. In this case, the BIOS must be updated to include the Microcode Update for the new processor.
NVRAM Checksum Bad, NVRAM Cleared	There was an error while validating the NVRAM data. This causes POST to clear the NVRAM data..
Resource Conflict	More than one system device is trying to use the same non-shareable resources (memory or I/O).
NVRAM Ignored	The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST.
NVRAM Bad	The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST due to a data error.
Static Resource Conflict	Two or more static devices are trying to use the same resource space (usually memory or I/O).
PCI I/O Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI ROM Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI IRQ Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI IRQ Routing Table Error	BIOS POST (DIM code) found a PCI device in the system but was unable to figure out how to route an IRQ to the device. Usually this error is caused by an incomplete description of the PCI Interrupt Routine of the system.

BIOS ERROR MESSAGES (CONTINUED)

System Configuration Errors

Message	Description
Timer Error	Indicates an error while programming the count register of channel 2 of the 8254 timer. This may indicate a problem with system hardware.
Interrupt Controller-1 Error	BIOS POST could not initialize the Master Interrupt Controller. This may indicate a problem with system hardware.
Interrupt Controller-2 Error	BIOS POST could not initialize the Slave Interrupt Controller. This may indicate a problem with system hardware.

CMOS Errors

Message	Description
CMOS Date/Time Not Set	The CMOS Date and/or Time are invalid. This error can be resolved by readjusting the system time in the BIOS Setup Utility.
CMOS Battery Low	CMOS Battery is low. This message usually indicates that the CMOS battery needs to be replaced. It could also appear when the user intentionally discharges the CMOS battery.
CMOS Settings Wrong	CMOS settings are invalid. This error can be resolved by using the BIOS Setup Utility.
CMOS Checksum Bad	CMOS contents failed the Checksum check. Indicates that the CMOS data has been changed by a program other than the BIOS or that the CMOS is not retaining its data due to malfunction. This error can typically be resolved by using the BIOS Setup Utility.

Miscellaneous Errors

Message	Description
Keyboard Error	Keyboard is not present or the hardware is not responding when the keyboard controller is initialized.
Keyboard/Interface Error	Keyboard Controller failure. This may indicate a problem with system hardware.
System Halted	The system has been halted. A reset or power cycle is required to reboot the machine. This message appears after a fatal error has been detected.

BOOTBLOCK INITIALIZATION CODE CHECKPOINTS

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the Bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable cache before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Reenable cache. Verify that flat mode is enabled.
D4	Test base 512K memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See the Bootblock Recovery Code Checkpoints section of this appendix for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copy Main BIOS into memory. Leave all RAM below 1MB Read/Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (Execute POSTKernel). See the POST Code Checkpoints section of this appendix for more information.

BOOTBLOCK RECOVERY CODE CHECKPOINTS

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

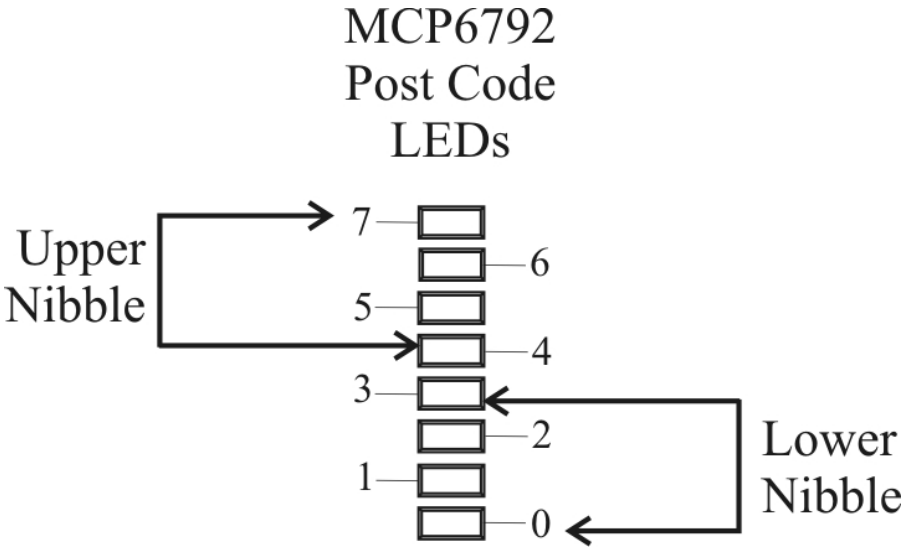
Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
E9 or Ea	Determine information about root directory of recovery media.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

POST CODE LEDS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the MCP6792. The LEDs are located behind the I/O plate of the AMC and to the right of the full-size front panel ribbon connector header. The board LEDs and are numbered from top (7) to bottom (0). Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED7 FP 1	LED6 FP 2	LED5 FP 3	LED4 FP 4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On

Lower Nibble (LN)				
Hex. Value	LED3 FP 1	LED2 FP 2	LED1 FP 3	LED0 FP 4
0	Off	Off	Off	Off
1	Off	Off	Off	On
2	Off	Off	On	Off
3	Off	Off	On	On
4	Off	On	Off	Off
5	Off	On	Off	On
6	Off	On	On	Off
7	Off	On	On	On
8	On	Off	Off	Off
9	On	Off	Off	On
A	On	Off	On	Off
B	On	Off	On	On
C	On	On	Off	Off
D	On	On	Off	On
E	On	On	On	Off
F	On	On	On	On



POST CODE CHECKPOINTS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The table below describes the type of checkpoints that may occur during the POST portion of the BIOS. Refer to the chart in the previous section to interpret the hexadecimal values of POST code LEDs 1 through 8.

Checkpoint	Description
03	Disable NMI, parity, video for EGA and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialize CMOS as mentioned in the Kernel Variable “wCMOSFlags.”
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables that are based on CMOS setup questions. Initialize both the 8259 compatible PICs in the system.
05	Initialize the interrupt controlling hardware (generally OPIC) and interrupt vector table.
06	Do read/write test to CH-2 count register. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock.”
08	Initialize the processor. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after auto detection of keyboard/mouse using AMI KB-5.
0A	Initialize the 8042 compatible keyboard controller.
0B	Detect the presence of PS/2 mouse.
0C	Detect the presence of keyboard in KBC port.
0E	Testing and initialization of different input devices. Also, update the Kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo and silent logo modules.
13	Early POST initialization of chipset registers
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initialize different devices through DIM. See *DIM Code Checkpoints* section of this appendix for more information.
2C	Initialize different devices. Detects and initializes the video adapter installed in the system.
2E	Initialize all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initialize the silent boot module. Set the window for displaying text information.
37	Display sign-on message, processor information, setup key message and any OEM specific information.

POST CODE CHECKPOINTS (CONTINUED)

Checkpoint	Description
38	Initialize different devices through DIM. See DIM Code Checkpoints section of this appendix for more information.
39	Initialize DMAC-1 and DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (parallel ports, serial ports and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDA, etc.
50	Program the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initialize NUM-LOCK status and program the keyboard Typematic rate.
75	Initialize INT13 and prepare for IPL detection.
78	Initialize IPL devices controlled by BIOS and option ROMs.
7A	Initialize remaining option ROMs.
7C	Generate and write contents of ESCD in NVRAM.
84	Log errors encountered during POST.
85	Display errors to the user and get the user response for error.
87	Execute BIOS setup if needed/requested.
8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/disable NMI as selected.
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initialize the Microsoft IRQ Routing Table. Prepare the runtime language module. Disable the system configuration display if needed.
A4	Initialize runtime language module.

POST CODE CHECKPOINTS (CONTINUED)

Checkpoint	Description
A7	Display system configuration screen if enabled. Initialize the processor before boot, which includes the programming of the MTRRs.
A8	Prepare processor for OS boot, including final MTRR values.
A9	Wait for user input at configuration display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitialize the ADM module.
AB	Prepare BBS for INT19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Pass control to OS Loader (typically INT19h)

DIM CODE CHECKPOINTS

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different buses. The following table describes the main checkpoints where the DIM module is accessed:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices and PnP ISA cards. It also assigns PCI Bus numbers. Function 1 initializes all static devices, which include manually configured on-board peripherals, memory and I/O decode windows in PCI-to-PCI bridges and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI or AGP video drivers.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all on-board peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

ADDITIONAL CHECKPOINTS

While control is in the different functions, additional checkpoints are output to Port 80H as word values to identify the routines being executed.

The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two sets of information. The details of the high byte of these checkpoints are detailed in the following table:

High Byte XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 8.

0	Function 0. Disable all devices on the bus.
1	Function 1. Initialize static devices on the bus.
2	Function 2. Initialize output devices on the bus.
3	Function 3. Initialize input devices on the bus.
4	Function 4. Initialize IPL devices on the bus.
5	Function 5. Initialize general devices on the bus.
6	Function 6. Error reporting for the bus.
7	Function 7. Initialize add-on ROMs for all buses.
8	Function 8. Initialize BBS ROMs for all buses.

The lower nibble 'Y' indicates the bus on which the different routines are being executed. 'Y' can be from 0 to 5.

0	Generic DIM (Device Initialization Manager)
1	On-board system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices