MCX Series

6633-xxx - MCXT

6685-xxx - MCXT-E

6638-xxx - MCXI

6700-xxx - MCXI-E

No. 87-006636-000 Revision D

TECHNICAL REFERENCE

Intel® Dual-Core Xeon®

Intel® Quad-Core Xeon®

PROCESSOR-BASED

Server-Class SHB

WARRANTY

The following is an abbreviated version of Trenton Technology's warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonTechnology.com.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Technology Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Technology's discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Technology Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Technology Inc. Trenton Technology Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Technology Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Technology Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Technology Inc.

RETURN POLICY

Products returned for repair must be accompanied by a Return Material Authorization (RMA) number, obtained from Trenton Technology prior to return. Freight on all returned items must be prepaid by the customer, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton Technology via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

TRENTON Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

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Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your MCXT (6633-xxx), MCXT-E (6685-xxx), MCXI (6638-xxx) or MCXI-E (6700-xxx) SHB. Overall system performance may be affected by incorrect usage of these features.

PS/2 REQUIREMENTS DURING BOOT-UP

Certain operating systems require a PS/2 keyboard during boot-up. Since the SHB itself does not have a PS/2 keyboard connector, you may need Trenton's IOB30MC (6391-001) or IOB31 (6474-000) I/O board in your system to provide this functionality. If your operating system is not included below, contact Trenton for the latest information regarding IOB30MC/IOB31 requirements.

Trenton has determined that an IOB30MC or IOB31 *is* required when using the following operating systems: RedHat Enterprise Linux (RHEL) V4.0 ES 64-bit and 32-bit; QNX Neutrino 6.3.0; Fedora Core 6.0 64-bit and 32-bit; SUSE Linux 9.0 Linux Enterprise Server 64-bit and 32-bit; Sun® Solaris™ 10.0. An IOB30MC or IOB31 is *not* required when using the following operating systems: Microsoft® Windows® Vista 64-bit and 32-bit; Microsoft® Windows® 2000; Microsoft® Windows® XP 64-bit and 32-bit; Microsoft® Windows® 2003 Server 64-bit and 32-bit.

VIDEO START-UP

The first video display image could be delayed 10-30 seconds while the MCX-series SHB performs start-up diagnostics and advanced technology sequencing during system power-up. Post-code LEDs on the SHB provide a visual indication of normal board operation. The specific length of this delay depends on the amount of installed system memory and the overall system configuration.

DDR2 MEMORY

The 240-pin DDR2 memory modules used on the SHB must be industry standard 72-bit wide ECC registered memory modules. The FB-DIMMs must be PC2-4200 or PC2-5300 (DDR2-533 or DDR2-667) and comply with the JEDEC Rev. 2.0 specifications.

NOTE: All memory modules must have gold contacts.

With the bracket end of the board to the right, the four FB-DIMM sockets available on the MCXT and MCXI SHBs are numbered BK0A, BK1A, BK0B and BK1B, from top to bottom. On the extended-memory MCXT-E and MCXI-E SHBs, there are an additional four FB-DIMM sockets. The upper sockets are BK2A and BK2B, from left to right, and the lower sockets are BK3A and BK3B. These socket definitions are illustrated in the board layouts in the *Specifications* chapter of the MCXT/MCXI manual.

A minimum of one 512MB FB-DIMM is required and must be populated in DIMM socket BK0A. When using more than one FB-DIMM, the memory sockets must be populated in multiples of two in order to maximize the speed and performance of the memory interface. To take full advantage of the four-channel memory interface of the SHB's memory controller hub, the FB-DIMMs in sockets BK0A and BK1A must be identical in manufacturing, speed, timing and organization. FB-DIMMs in sockets BK0B and BK1B must also be identical. FB-DIMMs in sockets contained within the same memory channel (e.g., BK0A and BK2A) do not have to be identical.

The FB-DIMMs must be installed in the SHB's FB-DIMM sockets using prescribed population rules to ensure proper memory interface operation and performance. Refer to the DDR2 Memory section of the *Specifications* chapter of the MCXT/MCXI manual for more details.

POWER SUPPLY

The MCX-series SHB requires a power supply with a minimum of 450 watts. If the power supply does not provide a minimum of 2.0 Amps of 5-volt standby current *and* 18.0 Amps of +12V current, the system may not boot. Ensure that the system supply can safely deliver adequate power to meet all remaining system requirements.

The default system shutdown option is set to **Manual Shutdown**. This prompts a shutdown screen after the operating system shuts down, which requires a manual power off in A/C power. To automatically shut down the SHB after operating system shutdown, change **Manual Shutdown** to **Auto**. This puts the SHB in S5 power-off state and does not require that a manual power off be done in order to keep the SHB off.

A/C power should always be powered off when any parts are being removed from or connected to the SHB or backplane. Failure to do so may result in serious damage to the SHB or backplane.

POWER CONNECTION

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The MCX-series SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used. Refer to *Appendix B - Power Connection* in the MCXT/MCXI manual to determine the method that will work best for a specific system design.

SATA PORTS

SATA ports 0, 1, 2 and 3 are accessible in IDE mode. Ports 4 and 5 are only accessible when either AHCI or RAID configurations have been enabled. Your operating system may need a driver in order to install SATA in AHCI or RAID configurations. Once these configurations have been enabled, all six SATA ports are fully accessible.

MOUSE/KEYBOARD "Y" CABLE

If you have an IOB30MC I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections of the *MCXT/MCXI Technical Reference Manual* (#87-006636-000). The latest revision of this manual may be found on Trenton's website - www.TrentonTechnology.com.
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HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins. Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

SOLDER-SIDE COMPONENTS

This SHB has components on both sides of the PCB. It is important for you to observe the following precautions when handling or storing the board to prevent solder-side components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

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Chapter 1 Specifications

INTRODUCTION

The MCX series processor boards are full-featured server-class system host boards (SHBs). The MCXT (506633-xxx) features two dual- or quad-core Intel® Xeon® microprocessors; the MCXI (506638-xxx) has one dual- or quad-core Intel® Xeon® microprocessor. Both SHBs provide a 1066MHz or 1333MHz system bus, ATI Technologies® video interface, support for 16GB DDR2 memory, PCI Express™ bus, cache memory, an Ultra ATA/100 drive interface, support for three Gigabit Ethernet interfaces, six Serial ATA ports, support for up to seven USB ports and a speaker port. These single-slot high performance SHBs plug into PICMG® 1.3 backplanes and provide full PC compatibility for the system expansion slots.

The MCXT-E (506685-xxx) and MCXI-E (506700-xxx) are extended-memory models which have all of the features of the MCXT/MCXI and support up to 32GB of DDR2 memory.

NOTE: In the model number/name tables below, "xG" indicates memory size (0G = 0GB memory, 1G = 1GB memory, etc.)

MCXT (506633-XXX) MODELS

MCXT Models -- Two Processors, Standard Memory (up to 16GB):

Model #	Model Name	Speed
MCXT - Dual-Core Processors:		
Intel® Xeon® Processors - 1066MHz FSB/4MB cache:		
506633-005-xG	MCXT/1.86DH	1.86GHz
506633-004-xG	MCXT/1.6DH	1.6GHz
Intel® Xeon® Processors - 1333MHz FSB/4MB cache:		
506633-112-xG	MCXT/3.0DK	3.0GHz
506633-110-xG	MCXT/2.66DK	2.66GHz
506633-108-xG	MCXT/2.33DK	2.33GHz
506633-106-xG	MCXT/2.0DK	2.0GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/4MB cache:		
506633-308-xG	MCXT/2.33LK	2.33GHz
Intel® Xeon® Processors - 1333MHz FSB/6MB cache:		
506633-132-xG	MCXT/3.0FK	3.0GHz
506633-128-xG	MCXT/2.33FK	2.33GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/6MB cache:		
506633-232-xG	MCXT/3.0FLK	3.0GHz
506633-230-xG	MCXT/2.66FLK	2.66GHz
Intel® Xeon® Processors - Extreme - 1333MHz FSB/6MB cache:		
506633-363-xG	MCXT/3.5FX	3.5GHz
506633-362-xG	MCXT/3.33FX	3.33GHz

Model #	Model Name	Speed
MCXT - Quad-Core Processors:		
Intel® Xeon® Processors - 1066MHz FSB/2x4MB cache:		
506633-405-xG	MCXT/1.86QH	1.86GHz
506633-404-xG	MCXT/1.6QH	1.6GHz
Intel® Xeon® Processors - Low Voltage - 1066MHz FSB/2x4MB cache:		
506633-605-xG	MCXT/1.86QLH	1.86GHz
506633-604-xG	MCXT/1.6QLH	1.6GHz
506633-603-xG	MCXT/1.6aQLH	1.6GHz (ATCA)
Intel® Xeon® Processors - Extreme - 1066MHz FSB/2x4MB cache:		
506633-573-xG	MCXT/2.66QX	2.66GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x4MB cache:		
506633-706-xG	MCXT/2.0QLK	2.0GHz
Intel® Xeon® Processors - 1333MHz FSB/2x4MB cache:		
506633-508-xG	MCXT/2.33QK	2.33GHz
506633-506-xG	MCXT/2.0QK	2.0GHz
Intel® Xeon® Processors - 1333MHz FSB/2x6MB cache:		
506633-812-xG	MCXT/3.0RK	3.0GHz
506633-811-xG	MCXT/2.83RK	2.83GHz
506633-810-xG	MCXT/2.66RK	2.66GHz
506633-809-xG	MCXT/2.5RK	2.5GHz
506633-808-xG	MCXT/2.33RK	2.33GHz
506633-806-xG	MCXT/2.0RK	2.0GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x6MB cache:		
506633-910-xG	MCXT/2.66RLK	2.66GHz
506633-909-xG	MCXT/2.5RLK	2.5GHz
506633-908-xG	MCXT/2.33RLK	2.33GHz
Intel® Xeon® Processors - Extreme - 1333MHz FSB/2x6MB cache:		
506633-874-xG	MCXT/3.33RX	3.33GHz
506633-873-xG	MCXT/3.16RX	3.16GHz
506633-872-xG	MCXT/3.0RX	3.0GHz

MCXT-E (506685-xxx) Models

MCXT-E Models - Two Processors, Extended Memory (up to 32GB):

Model #	Model Name	Speed
MCXT-E - Dual-Core Processors:		
Intel® Xeon® Processors - 1066MHz FSB/4MB cache:		
506685-005-xG	MCXT-E/1.86DH	1.86GHz
506685-004-xG	MCXT-E/1.6DH	1.6GHz
Intel® Xeon® Processors - 1333MHz FSB/4MB cache:		
506685-112-xG	MCXT-E/3.0DK	3.0GHz
506685-110-xG	MCXT-E/2.66DK	2.66GHz
506685-108-xG	MCXT-E/2.33DK	2.33GHz
506685-106-xG	MCXT-E/2.0DK	2.0GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/4MB cache:		
506685-308-xG	MCXT-E/2.33LK	2.33GHz
Intel® Xeon® Processors - 1333MHz FSB/6MB cache:		
506685-132-xG	MCXT-E/3.0FK	3.0GHz
506685-128-xG	MCXT-E/2.33FK	2.33GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/6MB cache:		
506685-232-xG	MCXT-E/3.0FLK	3.0GHz
506685-230-xG	MCXT-E/2.66FLK	2.66GHz
Intel® Xeon® Processors - Extreme - 1333MHz FSB/6MB cache:		
506685-363-xG	MCXT-E/3.5FX	3.5GHz
506685-362-xG	MCXT-E/3.33FX	3.33GHz
MCXT-E - Quad-Core Processors:		
Intel® Xeon® Processors - 1066MHz FSB/2x4MB cache:		
506685-405-xG	MCXT-E/1.86QH	1.86GHz
506685-404-xG	MCXT-E/1.6QH	1.6GHz
Intel® Xeon® Processors - Low Voltage - 1066MHz FSB/2x4MB cache:		
506685-605-xG	MCXT-E/1.86QLH	1.86GHz
506685-604-xG	MCXT-E/1.6QLH	1.6GHz
506685-603-xG	MCXT-E/1.6aQLH	1.6GHz (ATCA)
Intel® Xeon® Processors - Extreme - 1066MHz FSB/2x4MB cache:		
506685-573-xG	MCXT-E/2.66QX	2.66GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x4MB cache:		
506685-706-xG	MCXT-E/2.0QLK	2.0GHz

Intel® Xeon® Processors - 1333MHz FSB/2x4MB cache:

506685-508-xG	MCXT-E/2.33QK	2.33GHz
506685-506-xG	MCXT-E/2.0QK	2.0GHz

Intel® Xeon® Processors - 1333MHz FSB/2x6MB cache:

506685-812-xG	MCXT-E/3.0RK	3.0GHz
506685-811-xG	MCXT-E/2.83RK	2.83GHz
506685-810-xG	MCXT-E/2.66RK	2.66GHz
506685-809-xG	MCXT-E/2.5RK	2.5GHz
506685-808-xG	MCXT-E/2.33RK	2.33GHz
506685-806-xG	MCXT-E/2.0RK	2.0GHz

Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x6MB cache:

506685-910-xG	MCXT-E/2.66RLK	2.66GHz
506685-909-xG	MCXT-E/2.5RLK	2.5GHz
506685-908-xG	MCXT-E/2.33RLK	2.33GHz

Intel® Xeon® Processors - Extreme - 1333MHz FSB/2x6MB cache:

506685-874-xG	MCXT-E/3.33RX	3.33GHz
506685-873-xG	MCXT-E/3.16RX	3.16GHz
506685-872-xG	MCXT-E/3.0RX	3.0GHz

MCXI (506638-XXX) MODELS

MCXI Models -- One Processor, Standard Memory (up to 16GB):

Model #	Model Name	Speed

MCXI - Dual-Core Processor:

Intel® Xeon® Processor - 1066MHz FSB/4MB cache:

506638-045-xG	MCXI/1.86DH	1.86GHz
506638-044-xG	MCXI/1.6DH	1.6GHz

Intel® Xeon® Processor - 1333MHz FSB/4MB cache:

506638-152-xG	MCXI/3.0DK	3.0GHz
506638-150-xG	MCXI/2.66DK	2.66GHz
506638-148-xG	MCXI/2.33DK	2.33GHz
506638-146-xG	MCXI/2.0DK	2.0GHz

Intel® Xeon® Processor - Low Voltage - 1333MHz FSB/4MB cache:

506638-348-xG	MCXI/2.33LK	2.33GHz

Intel® Xeon® Processors - 1333MHz FSB/6MB cache:

506638-172-xG	MCXI/3.0FK	3.0GHz
506638-168-xG	MCXI/2.33FK	2.33GHz

MCXI (506638-XXX) MODELS (CONTINUED)

MCXI Models -- One Processor, Standard Memory (up to 16GB) (cont'd):

Model #	Model Name	Speed
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/6MB cache:		
506638-272-xG	MCXI/3.0FLK	3.0GHz
506638-270-xG	MCXI/2.66FLK	2.66GHz
Intel® Xeon® Processors - Extreme - 1333MHz FSB/6MB cache:		
506638-369-xG	MCXI/3.5FX	3.5GHz
506638-368-xG	MCXI/3.33FX	3.33GHz

MCXI - Quad-Core Processor:

Intel® Xeon® Processor - 1066MHz FSB/2x4MB cache:		
506638-445-xG	MCXI/1.86QH	1.86GHz
506638-444-xG	MCXI/1.6QH	1.6GHz
Intel® Xeon® Processors - Low Voltage - 1066MHz FSB/2x4MB cache:		
506638-645-xG	MCXI/1.86QLH	1.86GHz
506638-644-xG	MCXI/1.6QLH	1.6GHz
506638-643-xG	MCXI/1.6aQLH	1.6GHz (ATCA)
Intel® Xeon® Processors - Extreme - 1066MHz FSB/2x4MB cache:		
506638-578-xG	MCXI/2.66QX	2.66GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x4MB cache:		
506638-746-xG	MCXI/2.0QLK	2.0GHz
Intel® Xeon® Processor - 1333MHz FSB/2x4MB cache:		
506638-548-xG	MCXI/2.33QK	2.33GHz
506638-546-xG	MCXI/2.0QK	2.0GHz
Intel® Xeon® Processors - 1333MHz FSB/2x6MB cache:		
506638-852-xG	MCXI/3.0RK	3.0GHz
506638-851-xG	MCXI/2.83RK	2.83GHz
506638-850-xG	MCXI/2.66RK	2.66GHz
506638-849-xG	MCXI/2.5RK	2.5GHz
506638-848-xG	MCXI/2.33RK	2.33GHz
506638-846-xG	MCXI/2.0RK	2.0GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x6MB cache:		
506638-950-xG	MCXI/2.66RLK	2.66GHz
506638-949-xG	MCXI/2.5RLK	2.5GHz
506638-948-xG	MCXI/2.33RLK	2.33GHz

Model #	Model Name	Speed
Intel® Xeon® Processors - Extreme - 1333MHz FSB/2x6MB cache:		
506638-879-xG	MCXI/3.33RX	3.33GHz
506638-878-xG	MCXI/3.16RX	3.16GHz
506638-877-xG	MCXI/3.0RX	3.0GHz

MCXI-E (506700-XXX) MODELS

MCXI-E Models - One Processor, Extended Memory (up to 32GB):

Model #	Model Name	Speed
MCXI-E - Dual-Core Processor:		
Intel® Xeon® Processor - 1066MHz FSB/4MB cache:		
506700-045-xG	MCXI-E/1.86DH	1.86GHz
506700-044-xG	MCXI-E/1.6DH	1.6GHz
Intel® Xeon® Processor - 1333MHz FSB/4MB cache:		
506700-152-xG	MCXI-E/3.0DK	3.0GHz
506700-150-xG	MCXI-E/2.66DK	2.66GHz
506700-148-xG	MCXI-E/2.33DK	2.33GHz
506700-146-xG	MCXI-E/2.0DK	2.0GHz
Intel® Xeon® Processor - Low Voltage - 1333MHz FSB/4MB cache:		
506700-348-xG	MCXI-E/2.33LK	2.33GHz
Intel® Xeon® Processors - 1333MHz FSB/6MB cache:		
506700-172-xG	MCXI-E/3.0FK	3.0GHz
506700-168-xG	MCXI-E/2.33FK	2.33GHz
Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/6MB cache:		
506700-272-xG	MCXI-E/3.0FLK	3.0GHz
506700-270-xG	MCXI-E/2.66FLK	2.66GHz
Intel® Xeon® Processors - Extreme - 1333MHz FSB/6MB cache:		
506700-369-xG	MCXI-E/3.5FX	3.5GHz
506700-368-xG	MCXI-E/3.33FX	3.33GHz

MCXI-E - Quad-Core Processor:

Intel® Xeon® Processor - 1066MHz FSB/2x4MB cache:

506700-445-xG	MCXI-E/1.86QH	1.86GHz
506700-444-xG	MCXI-E/1.6QH	1.6GHz

Intel® Xeon® Processors - Low Voltage - 1066MHz FSB/2x4MB cache:

506700-645-xG	MCXI-E/1.86QLH	1.86GHz
506700-644-xG	MCXI-E/1.6QLH	1.6GHz
506700-643-xG	MCXI-E/1.6aQLH	1.6GHz (ATCA)

Intel® Xeon® Processors - Extreme - 1066MHz FSB/2x4MB cache:

506700-578-xG	MCXI-E/2.66QX	2.66GHz

Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x4MB cache:

506700-746-xG	MCXI-E/2.0QLK	2.0GHz

Intel® Xeon® Processor - 1333MHz FSB/2x4MB cache:

506700-548-xG	MCXI-E/2.33QK	2.33GHz
506700-546-xG	MCXI-E/2.0QK	2.0GHz

Intel® Xeon® Processors - 1333MHz FSB/2x6MB cache:

506700-852-xG	MCXI-E/3.0RK	3.0GHz
506700-851-xG	MCXI-E/2.83RK	2.83GHz
506700-850-xG	MCXI-E/2.66RK	2.66GHz
506700-849-xG	MCXI-E/2.5RK	2.5GHz
506700-848-xG	MCXI-E/2.33RK	2.33GHz
506638-846-xG	MCXI-E/2.0RK	2.0GHz

Intel® Xeon® Processors - Low Voltage - 1333MHz FSB/2x6MB cache:

506700-950-xG	MCXI-E/2.66RLK	2.66GHz
506700-949-xG	MCXI-E/2.5RLK	2.5GHz
506700-948-xG	MCXI-E/2.33RLK	2.33GHz

Intel® Xeon® Processors - Extreme - 1333MHz FSB/2x6MB cache:

506700-879-xG	MCXI-E/3.33RX	3.33GHz
506700-878-xG	MCXI-E/3.16RX	3.16GHz
506700-877-xG	MCXI-E/3.0RX	3.0GHz

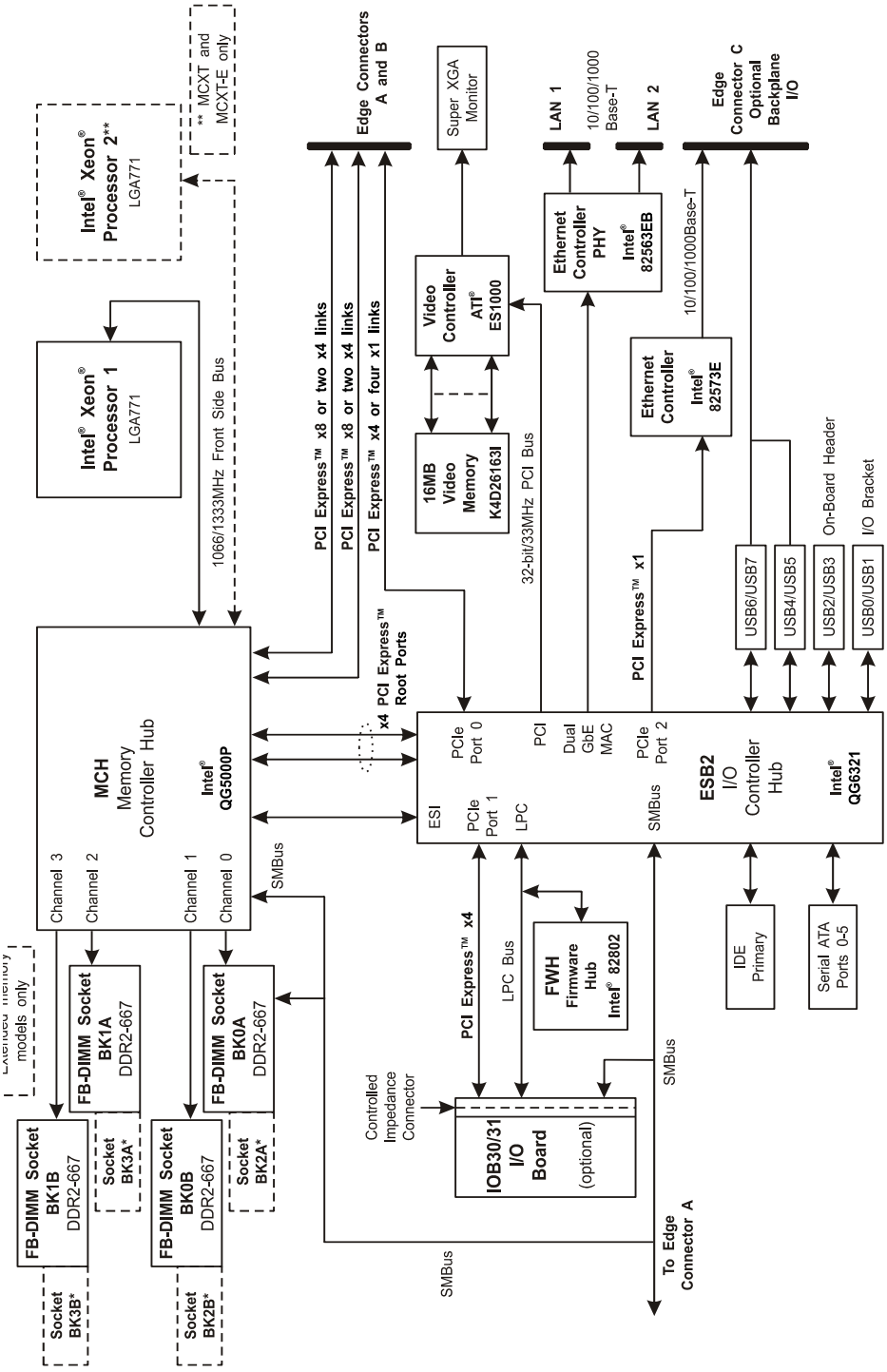
FEATURES

- Two Intel® Xeon® microprocessors (MCXT/MCXT-E) or one Intel® Xeon® microprocessor (MCXI/MCXI-E)
- Dual-core or quad-core processors

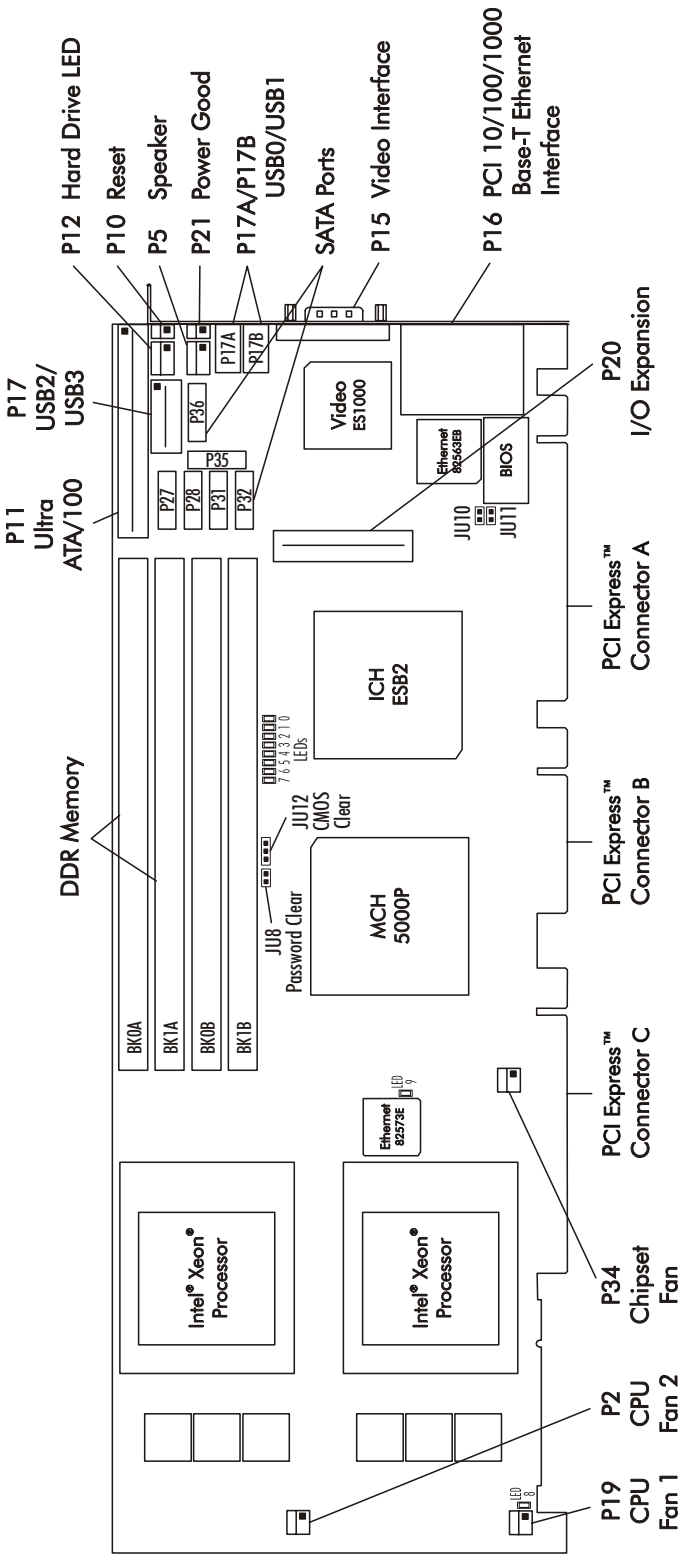
FEATURES (CONTINUED)

- MCXT and MCXI models support up to 16GB of Double Data Rate (DDR2) on-board memory; extended-memory MCXT-E and MCXI-E models support up to 32GB of DDR2 memory
- Intel® 5000P chipset with 1066/1333MHz system bus
- PCI Local Bus operating in 32-bit/33MHz mode and PCI Express™ Bus operating in x4 and x8 modes
- Super XGA on-board video interface (ATI Technologies®)
- Supports three Ethernet interfaces for use with 10/100/1000Base-T networks
- Six Serial ATA ports support independent SATA I and SATA II storage devices
- Memory error checking and correction (ECC) support
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG®) 1.3 Specification
- Ultra ATA/100 drive interface supports two drives in a master/slave configuration
- Universal Serial Bus (USB 2.0) support
- Automatic or manual peripheral configuration
- Full PC compatibility

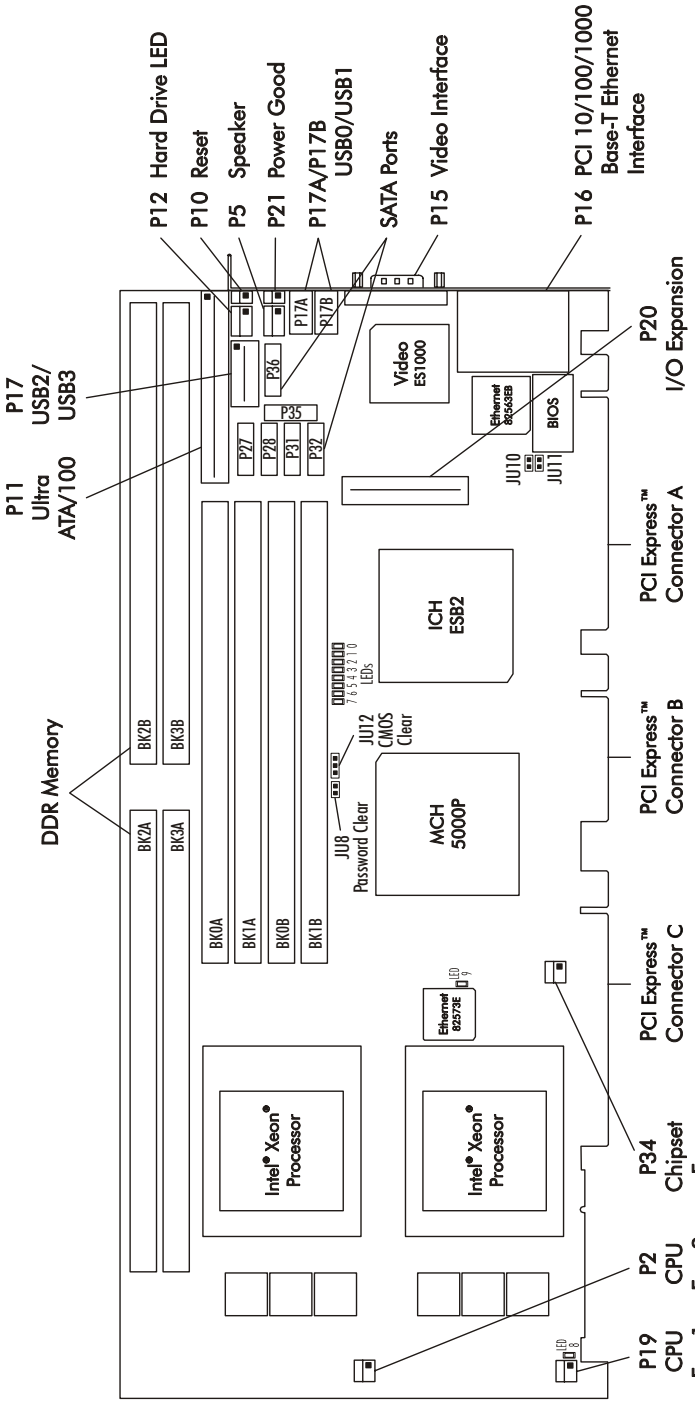
MCX SERIES
SHB BLOCK
DIAGRAM



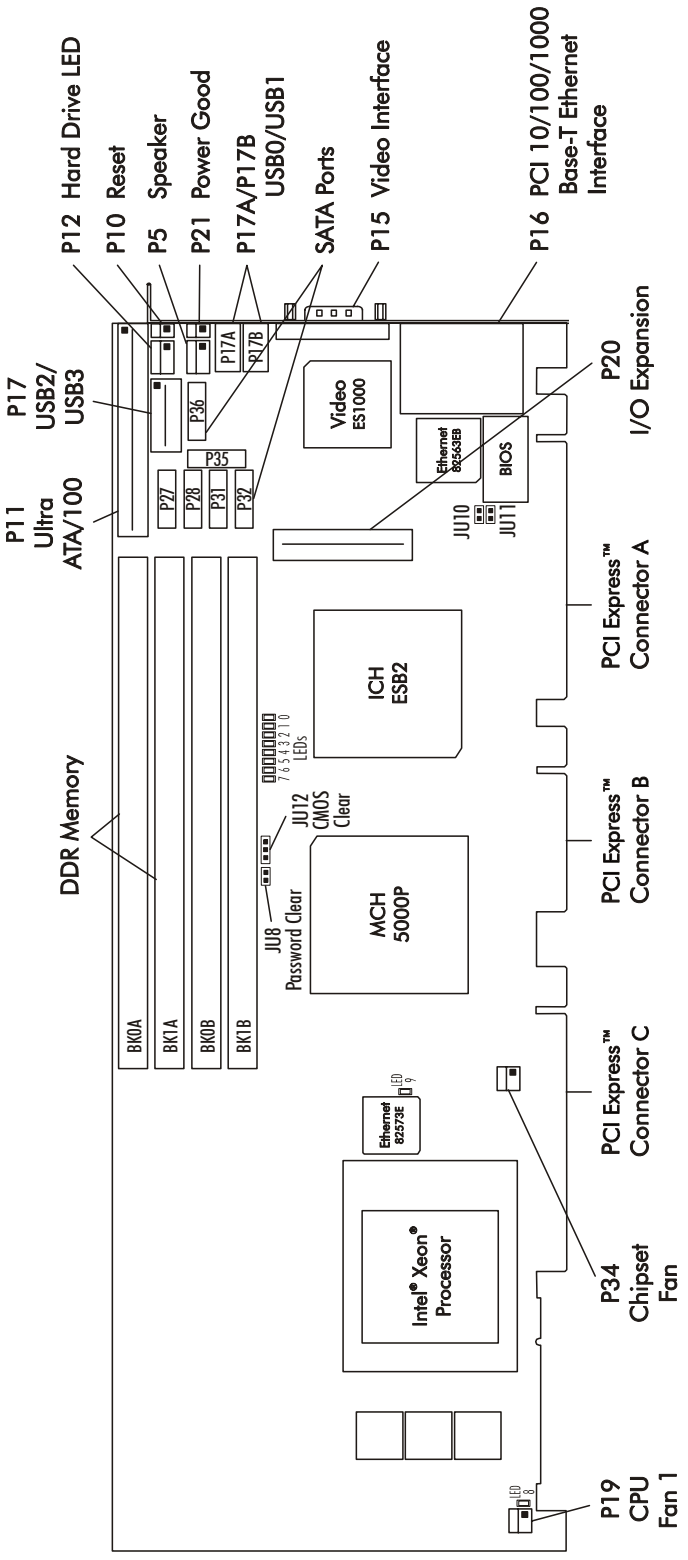
MCXT (506633-XXX) SHB BOARD LAYOUT



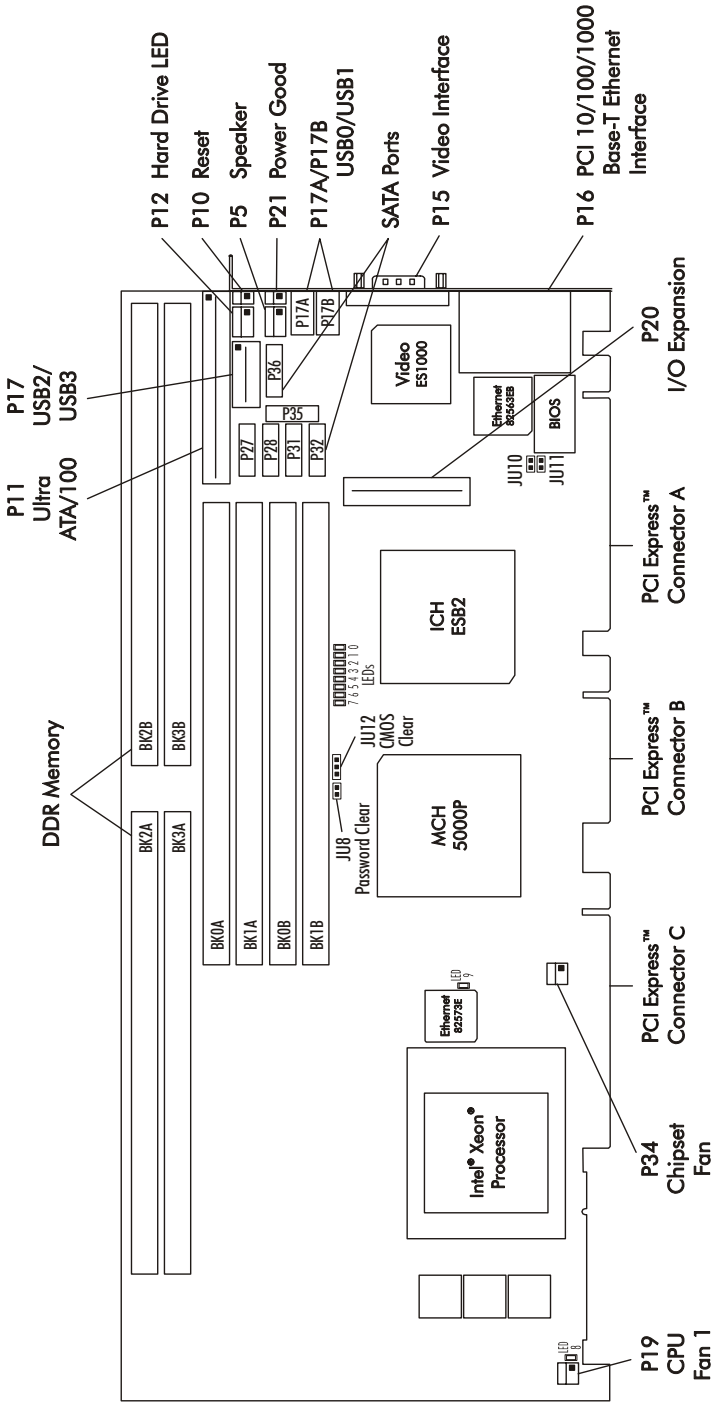
MCXT-E
(506685-XXX)
SHB BOARD
LAYOUT



MCXI (506638-XXX) SHB BOARD LAYOUT



MCXI-E
(506700-XXX)
SHB BOARD
LAYOUT



PROCESSORS	• Two Intel® Xeon® microprocessors (MCXT/MCXT-E) or one Intel® Xeon® microprocessor (MCXI/MCXI-E) • Dual-core or quad-core processors • Processors use the LGA771 (Socket J) packaging
BUS INTERFACES	PCI Local Bus compatible
DATA PATH	DDR2 Memory - 64-bit (per channel) PCI Bus - 32-bit
BUS SPEEDS	PCI - 33MHz (on-board only) PCI Express - 2.5GHz per lane
BUS SPEED - SYSTEM	1066MHz or 1333MHz Front Side Bus
MEMORY INTERFACE	The SHB uses Double Data Rate (DDR2) memory. Theoretical memory interface bandwidth is a maximum of 8.0GB/s when using PC2-5300 DIMMs
SYSTEM BUS	Intel® 5000P chipset supports the system bus at 1066MHz or 1333MHz, which provides a higher bandwidth path for transferring data between main memory/chipset and the processors.
DMA CHANNELS	The SHB is fully PC compatible with seven DMA channels, each supporting type F transfers.
INTERRUPTS	The SHB is fully PC compatible with interrupt steering for PCI plug and play compatibility.
BIOS (FLASH)	The BIOS is an AMIBIOS with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. The Flash BIOS resides in the Intel® 82802AC Firmware Hub (FWH). The BIOS may be upgraded from floppy disk by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the floppy disk in drive A:. Custom BIOSs are available.
CACHE MEMORY	The processors include integrated on-die, 8-way set associative level two (L2) cache, which implements the Advanced Transfer Cache architecture and runs at the full speed of the processor core. The dual-core Intel® Xeon® processors have 4M of shared L2 cache memory; the quad-core processors have 2 x 4M of L2 cache memory. Both types of processors have 32K level 1 (L1) instruction cache and 32K L1 data cache per core.

DDR2 MEMORY

The Double Data Rate (DDR2) memory interface on the MCXT and MCXI SHBs supports up to 16GB of memory; the MCXT-E and MCXI-E models support up to 32GB of memory.

The SHB uses industry standard 72-bit wide ECC gold finger memory modules in four (MCXT/MCXI) or eight (MCXT-E/MCXI-E) 240-pin sockets. The FB-DIMMs must be PC2-4200 or PC2-5300 (DDR2-533 or DDR2-667) and comply with the JEDEC Rev. 2.0 specifications.

FB-DIMMs have "Advanced Memory Buffer" chips that provide enhanced signal integrity and improved error detection that help reduce soft memory errors. FB-DIMM memory technology improves overall system reliability by extending the current ECC capability to include protection of command and address data. FB-DIMMs feature automatic retries when a memory error is detected, which results in uninterrupted system operation in the event of transient errors.

The following FB-DIMM sizes are supported:

DIMM Size	DIMM Type	ECC
512MB	Registered	64M x 72
1GB	Registered	128M x 72
2GB	Registered	256M x 72
4GB	Registered	512M x 72

NOTE: With the bracket end of the board to the right, the four FB-DIMM sockets available on the MCXT and MCXI SHBs are numbered BK0A, BK1A, BK0B and BK1B, from top to bottom. On the extended-memory MCXT-E and MCXI-E SHBs, there are an additional four FB-DIMM sockets. The upper sockets are BK2A and BK2B, from left to right, and the lower sockets are BK3A and BK3B. These socket definitions are illustrated in the board layouts earlier in this chapter. All memory modules must have gold contacts.

A minimum of one 512MB FB-DIMM is required and must be populated in DIMM socket BK0A. When using more than one FB-DIMM, the memory sockets must be populated in multiples of two in order to maximize the speed and performance of the memory interface.

To take full advantage of the four-channel memory interface of the SHB's memory controller hub, the FB-DIMMs in sockets BK0A and BK1A must be identical in manufacturing, speed, timing and organization. FB-DIMMs in sockets BK0B and BK1B must also be identical. FB-DIMMs in sockets contained within the same memory channel (e.g., BK0A and BK2A) do not have to be identical.

The following table illustrates the FB-DIMM population rules:

	FB-DIMM Sockets (All Models)				FB-DIMM Sockets (MCXT-E/MCXI-E)			
Number of FB-DIMM Modules	BK0A *	BK1A	BK0B	BK1B	BK2A	BK2B	BK3A	BK3B
One	DIMM	Empty	Empty	Empty	Empty	Empty	Empty	Empty
Two	DIMM	DIMM	Empty	Empty	Empty	Empty	Empty	Empty
Four	DIMM	DIMM	DIMM	DIMM	Empty	Empty	Empty	Empty
Six	DIMM	DIMM	DIMM	DIMM	DIMM	DIMM	Empty	Empty
Eight	DIMM	DIMM	DIMM	DIMM	DIMM	DIMM	DIMM	DIMM

* BK0A is the top-most DIMM on the MCXT and MCXI models.

ERROR CHECKING AND CORRECTION

The memory interface supports ECC modes via BIOS setting for multiple-bit error detection and correction of all errors confined to a single nibble.

BUS INTERFACES

The PCI Local Bus, which is 32 bits wide and runs at 33MHz, interfaces to the ATI Technologies ES1000 video controller.

The SHB provides two x8 PCI Express links, one x4 PCI Express link and eight PCI Express reference clocks on Edge Connectors A and B. Each of the x8 links can be bifurcated into two x4 PCIe links; the single x4 PCIe link can be divided into four x1 PCIe links. The SHB also provides a x4 link to the controlled impedance connector for use with PCI Express plug-in option cards. Refer to the *PCI Express Reference* chapter of this manual for more information, including edge connector pin assignments.

UNIVERSAL SERIAL BUS (USB)

The SHB supports up to eight high-speed USB 2.0 ports. Connectors for two of the USB ports (0 and 1) are on the I/O bracket; two ports (2 and 3) are available via a header on the SHB. USB ports 4, 5, 6 and 7 are routed to edge connector C of the SHB for use on a PICMG 1.3 backplane which supports the optional PICMG 1.3 USB interface capability.

SUPER XGA INTERFACE

The ATI Technologies ES1000 video controller provides 16MB of on-board video memory via an external memory chip. The video controller supports pixel resolutions up to 1280 x 1024 (SXGA).

Software drivers are available for most popular operating systems.

ETHERNET INTERFACES

The SHB provides three Ethernet interfaces, each supporting up to 1Gb/s transfers.

Two of the Ethernet interfaces are implemented using an Intel® 82563EB Ethernet controller with two channels. These interfaces support Gigabit, 10Base-T and 100Base-TX Fast Ethernet modes and are compliant with the IEEE 802.3 Specification.

The Intel® 82563EB Ethernet controller provides:

- Integrated RJ-45/Magnetics module connectors on the SHB's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.

- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

The third LAN is supported by the ESB2 I/O controller hub via a x1 PCI Express bus to an Intel® 82573E Ethernet controller. This 10/100/1000Base-T Ethernet interface is routed to the PICMG 1.3 backplane via edge connector C of the SHB.

Software drivers are supplied for most popular operating systems.

SERIAL ATA/300 PORTS

The six Serial ATA (SATA) ports on the SHB comply with the SATA specification and support six independent SATA I or SATA II storage devices such as hard disks and CD-RW devices. SATA produces higher performance interfacing by providing data transfer rates up to 300MB per second on each port. The SHB supports RAID 0, 1, 5 and 10 array configurations.

ENHANCED IDE INTERFACE

The high performance PCI Bus Master EIDE interface is capable of supporting two IDE disk drives in a master/slave configuration. The interface supports Ultra ATA/100 with synchronous ATA mode transfers up to 100MB per second. Ultra ATA/100 cables must be used with Ultra ATA/100 drives.

BATTERY

A built-in lithium battery is provided, for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

POWER REQUIREMENTS

The following are typical values *:

Processor Speed	+5V	+12V	+3.3V	-12V
100% CPU Idle State - 4GB of system memory:				
2.0GHz **	1.75 Amps	7.50 Amps	3.00 Amps	< 100 mAmps
2.33GHz	1.75 Amps	5.90 Amps	3.00 Amps	< 100 mAmps
2.0GHz	1.75 Amps	5.80 Amps	3.00 Amps	< 100 mAmps
2.33GHz (LV)	1.75 Amps	5.70 Amps	3.00 Amps	< 100 mAmps
100% CPU Stress State - 4GB of system memory:				
2.0GHz **	2.00 Amps	15.60 Amps	3.20 Amps	< 100 mAmps
2.33GHz	2.00 Amps	12.80 Amps	3.20 Amps	< 100 mAmps
2.0GHz	2.00 Amps	12.70 Amps	3.20 Amps	< 100 mAmps
2.33GHz (LV)	2.00 Amps	12.50 Amps	3.20 Amps	< 100 mAmps

* Values stated are when using the MCXT-E extended-memory SHB with dual processors.

** Quad-core processors

Tolerance for all voltages is +/- 5% and must be applied by the PICMG 1.3 backplane to edge connector C.

Each 1GB of additional FB-DIMM system memory will typically draw an additional 0.5A of +12V.

POWER SUPPLY

The MCX-series SHB requires a power supply with a minimum of 450 watts. If the power supply does not provide a minimum of 2.0 Amps of 5-volt standby current, the system may not boot.

The default system shutdown option is set to **Manual Shutdown**. This prompts a shutdown screen after the operating system shuts down, which requires a manual power off in A/C power. To automatically shut down the SHB after operating system shutdown, change **Manual Shutdown** to **Auto**. This puts the SHB in S5 power-off state and does not require that a manual power off be done in order to keep the SHB off.

A/C power should always be powered off when any parts are being removed from or connected to the SHB or backplane. Failure to do so may result in serious damage to the SHB or backplane.

TEMPERATURE/ ENVIRONMENT

Operating Temperature:	0^{o} C. to 55^{o} C. (2.33GHz LV processors) 0^{o} C. to 45^{o} C. (all other processors)
Airflow Requirement:	300 LFM continuous airflow when using the SHB's standard heat sink
Storage Temperature:	- 40^{o} C. to 70^{o} C.
Humidity:	5% to 90% non-condensing

UL RECOGNITION

This SHB is a UL recognized product listed in file #E208896.

This board was investigated and determined to be in compliance under the Bi-National Standard for Information Technology Equipment. This included the Electrical Business Equipment, UL 1950, Third Edition, and CAN/CSA C22.22 No. 950-95.

MEAN TIME BETWEEN FAILURE (MTBF)

186,261 POH (Power-On Hours) at 40^{o} C., per Bellcore.

CONFIGURATION JUMPERS

The setup of the configuration jumpers on the SHB is described below. * indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "RIGHT" is toward the bracket end of the board; "LEFT" is toward the processor(s).

Jumper Description

JU8 Password Clear

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

JU10/JU11 System Flash ROM Operational Modes

The Flash ROM has two programmable sections: the Boot Block for “flashing” in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

	JU10	JU11
All Blocks Write Enabled	Remove *	Remove *
Boot Block Write Protected	Install	Remove
Block 2-16 Write Protected	Remove	Install

JU12 CMOS Clear

Install on the LEFT to clear.
Install on the RIGHT to operate. *

NOTE: To clear the CMOS, power down the system and install the jumper on the LEFT. Wait for at least two seconds, move the jumper back to the RIGHT and turn the power on. When AMIBIOS displays the "CMOS Settings Wrong" message, press F1 to go into the BIOS Setup Utility, where you may reenter your desired BIOS settings, load optimal defaults or load failsafe defaults.

JU13 AT Power Supply Operation

Install when using an AT-style system power supply.
Remove for all other system power supplies.*

ETHERNET LEDS AND CONNECTORS

Each of the two Ethernet interfaces on the SHB's I/O bracket has two LEDs for status indication and an RJ-45 network connector.

LED/Connector	Description
Activity LED	Green LED which indicates network activity. This is the upper LED on the LAN connector (i.e., toward the memory sockets).
Off	Indicates that there is no valid link.
On (solid)	Indicates a valid link, but no current network transmit or receive activity.
On (flashing)	Indicates a valid link with network transmit or receive activity.
Speed LED	Green LED which identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors).
Off	Indicates a valid link at 100-Mb/s or 10-Mb/s.
On (solid)	Indicates a valid link at 1000-Mb/s.
RJ-45 Network Connector	The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection.

LAN3 Link Status LED

The LAN3 link status LED (LED9), which is located to the right of the Intel 82573E Ethernet controller, indicates the link status of the 10/100/1000Base-T Ethernet connection which is routed to the PICMG 1.3 backplane via edge connector C of the SHB. Status can be determined as shown below:

LED Status	Description
Off	Indicates that there is no valid link.
On (solid)	Indicates a valid link, but no current network transmit or receive activity.
On (flashing)	Indicates a valid link with network transmit or receive activity.

STATUS LEDS

POST Code LEDs

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0 through 7, which are located below the memory banks and are numbered from right (0) to left (7). Refer to the board layouts earlier in this chapter for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. Specific error codes are listed in *Appendix A - BIOS Messages*, along with a chart to interpret the LEDs into hexadecimal format.

CPU Throttling LED

The CPU throttling LED (LED8), which is located in the lower left corner of the SHB to the right of CPU Fan 1 (P19), indicates the status of CPU thermal shutdown, as shown below:

LED Status	Description
Off	Indicates the CPU is operating within acceptable thermal levels.
On (flashing)	Indicates the CPU is throttling down to a lower operating speed due to rising CPU temperature.
On (solid)	Indicates the CPU has reached the thermal shutdown threshold limit. The SHB is still operating, but a thermal shutdown may soon occur.

NOTE: When a thermal shutdown occurs, the LED will stay on in systems using non-ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the SHB. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all SHB LEDs will turn off; however, stand-by power will still be present.

SYSTEM BIOS SETUP UTILITY

The System BIOS is an AMIBIOS with a ROM-resident setup utility. The BIOS Setup Utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- PCIPnP Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual.

CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P2 - CPU Fan 2 (MCXT and MCXT-E only)
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

P5 - Speaker Port Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	Speaker Data
2	Key
3	Gnd
4	+5V

P10 - External Reset Connector
2 pin single row header, Amp #640456-2

Pin	Signal
1	External Reset In (Low Active)
2	Gnd

P11 - Primary IDE Hard Drive Connector
40 pin dual row header, Amp #1-1761610-3

Pin	Signal	Pin	Signal
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 0	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDP
29	DACK 0	30	Gnd
31	IRQ 14	32	NC
33	Add 1	34	PCBL DET *

CONNECTORS (CONTINUED)

P11 - Primary IDE Hard Drive Connector (continued)

Pin	Signal	Pin	Signal
35	Add 0	36	Add 2
37	CS 1P	38	CS 3P
39	IDEACTP	40	Gnd

* For ATA/66 and ATA/100 drives, which should be set for Cable Select for proper speed operation. If other drives are detected, pin definition is Gnd.

P12 - Hard Drive LED Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	LED +
2	LED -
3	LED -
4	LED +

P15 - Video Interface Connector
15 pin connector, Kycon #K31X-E15S-N

Pin	Signal	Pin	Signal	Pin	Signal
		6	Gnd		
1	Red			11	NC
		7	Gnd		
2	Green			12	EEDI
		8	Gnd		
3	Blue			13	HSYNC
		9	+5V		
4	NC			14	VSYNC
		10	Gnd		
5	Gnd			15	EECS

P16 - 10/100/1000Base-T Ethernet Connectors - LAN1/LAN2
Dual RJ-45 connector, Pulse #JG0-0024NL
Each individual RJ-45 connector is defined as follows:

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

CONNECTORS (CONTINUED)

P17 - Universal Serial Bus (USB) Connector
8 pin dual row header, Molex #702-46-08-01
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P17A - Universal Serial Bus (USB) Connector
USB vertical connector, Molex #47500-0001
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB0
2	USB0-
3	USB0+
4	Gnd-USB0

P17B - Universal Serial Bus (USB) Connector
USB vertical connector, Molex #47500-0001
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB1
2	USB1-
3	USB1+
4	Gnd-USB1

P19 - CPU Fan 1
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

P20 - I/O Expansion Mezzanine Card Connector
76 pin connector, Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12V	2	+5V_STANDBY
3	NC	4	+5V_STANDBY
5	NC	6	+5V_DUAL
7	NC	8	+5V_DUAL
9	NC	10	NC

CONNECTORS (CONTINUED)

P20 - I/O Expansion Mezzanine Card Connector
76 pin connector, Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
11	NC	12	NC
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SMBCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP4	48	C_PE_RXP4
49	C_PE_TXN4	50	C_PE_RXN4
51	Gnd	52	Gnd
53	C_PE_TXP3	54	C_PE_RXP3
55	C_PE_TXN3	56	C_PE_RXN3
57	Gnd	58	Gnd
59	C_PE_TXP2	60	C_PE_RXP2
61	C_PE_TXN2	62	C_PE_RXN2
63	Gnd	64	Gnd
65	C_PE_TXP1	66	C_PE_RXP1
67	C_PE_TXN1	68	C_PE_RXN1
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5V

P21 - Power Good LED
2 pin single row header, Amp #640456-2

Pin	Signal
1	LED -
2	LED +

CONNECTORS (CONTINUED)

P27 - SATA Port 0
7 pin vertical connector, Molex #67491-0031

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

P28 - SATA Port 1
7 pin vertical connector, Molex #67491-0031

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

P31 - SATA Port 2
7 pin vertical connector, Molex #67491-0031

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

P32 - SATA Port 3
7 pin vertical connector, Molex #67491-0031

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

CONNECTORS (CONTINUED)

P34 - Chipset Fan
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

P35 - SATA Port 4
7 pin vertical connector, Molex #67491-0031

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

P36 - SATA Port 5
7 pin vertical connector, Molex #67491-0031

Pin	Signal
1	Gnd
2	TX+
3	TX-
4	Gnd
5	RX-
6	RX+
7	Gnd

Chapter 2 PCI Express™ Reference

INTRODUCTION

PCI Express™ is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

PCI EXPRESS LINKS

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion. A link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. The bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	250MB/s	500MB/s
x4	1GB/s	2GB/s
x8	2GB/s	4GB/s
x16	4GB/s	8GB/s

Scalability is a core feature of PCI Express. Some chipsets allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. In addition, although a board with a higher number of lanes will not function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) because the connectors are mechanically and electrically incompatible, the reverse configuration will function. A board with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot). The link auto-negotiates between the PCI Express devices to establish communication. The mechanical option card slots on a PICMG 1.3 backplane must have PCI Express configuration straps that alert the SHB to the PCI

Express electrical configuration expected. The SHB can then reconfigure the PCIe links for optimum system performance.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

SHB CONFIGURATIONS

There are two classes of PCI Express SHB configurations: server-class and graphics-class. Server applications require multiple, high-bandwidth PCIe links, and therefore the server-class SHB configuration is identified by multiple x8 and x4 links to the SHB edge connectors.

SHBs which require high-end video or graphics cards generally use a x16 PCI Express link. The graphics-class SHB configuration is identified by one x16 PCIe link and one x4 or four x1 links to the edge connectors. As PCI Express chipsets continue to evolve, it is possible that more x4 and/or x1 links could be supported in graphics-class SHBs. Currently, most video or graphics cards communicate to the SHB at an effective x1, x4 or x8 PCI Express data rate and do not actually make use of all of the signal lanes in a x16 connector.

NOTE: Server-class SHBs should always be used with server-class PICMG 1.3 backplanes and graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes. Combining incompatible SHBs and backplanes will not cause damage to the option cards or SHB, but one or more of the slots may not function and may result in one or more PCI Express option cards on the backplane being non-functional. This is due to the fact that there will not be enough available links to properly connect all of the PCI Express option card slots to the SHB.

PCI Express Edge Connector Pin Assignments

Trenton's MCXT/MCXI server-class SHBs use edge connectors A, B and C only. Optional I/O signals are defined in the PICMG 1.3 specification and if implemented must be located on edge connector C of the SHB. The MCXT/MCXI makes the Intelligent Platform Management Bus (IPMB) signals available to the user. The MCX series also enables the USB0, USB1, USB2 and USB3 ports and one Ethernet port for use on edge connector C.

The following table shows pin assignments for the PCI Express edge connectors on the MCX series of SHBs.

* Pins 3 and 4 of Side B of Connector A (TDI and TDO) are jumpered together.

Connector A			Connector B			Connector C		
	Side B	Side A		Side B	Side A		Side B	Side A
1	SMCLK	SMDAT	1	+5Vaux	+5Vaux	1	USB0P	GND
2	GND	GND	2	GND	RSVD	2	USB0N	GND
3	TDI *	NC	3	a_PETp8	GND	3	GND	USB1P
4	TDO *	NC	4	a_PETn8	GND	4	GND	USB1N
5	NC	WAKE#	5	GND	a_PERp8	5	USB2P	GND
6	PWRBT#	PME#	6	GND	a_PERn8	6	USB2N	GND
7	PWRGD	PSON#	7	a_PETp9	GND	7	GND	USB3P
8	SHB_RST#	PERST#	8	a_PETn9	GND	8	GND	USB3N
9	CFG0	CFG1	9	GND	a_PERp9	9	USBOC0#	GND
10	CFG2	CFG3	10	GND	a_PERn9	10	GND	USBOC1#
11	RSVD	GND	11	RSVD	GND	11	USBOC2#	GND
Mechanical Key			Mechanical Key			Mechanical Key		
12	GND	RSVD	12	GND	RSVD	12	GND	USBOC3#
13	b_PETp0	GND	13	a_PETp10	GND	13	NC	GND
14	b_PETn0	GND	14	a_PETn10	GND	14	NC	GND
15	GND	b_PERp0	15	GND	a_PER10	15	GND	NC
16	GND	b_PERn0	16	GND	a_PERn10	16	GND	NC
17	b_PETp1	GND	17	a_PETp11	GND	17	NC	GND
18	b_PETn1	GND	18	a_PETn11	GND	18	NC	GND
19	GND	b_PERp1	19	GND	a_PERp11	19	GND	NC
20	GND	b_PERn1	20	GND	a_PERn11	20	GND	NC
21	b_PETp2	GND	21	a_PETp12	GND	21	a_MDI0p	GND
22	b_PETn2	GND	22	a_PETn12	GND	22	a_MDI0n	GND
23	GND	b_PERp2	23	GND	a_PERp12	23	GND	a_MDI1p
24	GND	b_PERn2	24	GND	a_PERn12	24	GND	a_MDI1n
25	b_PETp3	GND	25	a_PETp13	GND	25	a_MDI2p	GND
26	b_PETn3	GND	26	a_PETn13	GND	26	a_MDI2n	GND
27	GND	b_PERp3	27	GND	a_PERp13	27	GND	a_MDI3p
28	GND	b_PERn3	28	GND	a_PERn13	28	GND	a_MDI3n
29	REFCLK0+	GND	29	a_PETp14	GND	29	IPMB_CL	GND
30	REFCLK0-	GND	30	a_PETn14	GND	30	IPMB_DA	GND
31	GND	REFCLK1+	31	GND	a_PERp14	31	NC	NC
32	RSVD-G	REFCLK1-	32	GND	a_PERn14	32	NC	NC
33	REFCLK2+	GND	33	a_PETp15	GND	33	NC	NC
34	REFCLK2-	GND	34	a_PETn15	GND	34	NC	GND
35	GND	REFCLK3+	35	GND	a_PERp15	35	NC	GND
36	RSVD-G	REFCLK3-	36	GND	a_PERn15	36	GND	NC
37	REFCLK4+	GND	37	RSVD	GND	37	GND	NC
38	REFCLK4-	GND	38	RSVD	RSVD	38	NC	GND

PCI EXPRESS EDGE CONNECTOR PIN ASSIGNMENTS (CONTINUED)

Connector A		Connector B		Connector C	
Side B	Side A	Side B	Side A	Side B	Side A
39 GND	REFCLK5+	39 GND	GND	39 NC	GND
40 RSVD-G	REFCLK5-	40 GND	GND	40 GND	NC
41 REFCLK6+	GND	41 GND	GND	41 GND	NC
42 REFCLK6-	GND	42 GND	GND	42 +3.3V	+3.3V
43 GND	REFCLK7+	43 GND	GND	43 +3.3V	+3.3V
44 GND	REFCLK7-	44 +12V	+12V	44 +3.3V	+3.3V
45 a_PETp0	GND	45 +12V	+12V	45 +3.3V	+3.3V
46 a_PETn0	GND	46 +12V	+12V	46 +3.3V	+3.3V
47 GND	a_PERp0	47 +12V	+12V	47 +3.3V	+3.3V
48 GND	a_PERn0	48 +12V	+12V	48 +3.3V	+3.3V
49 a_PETp1	GND	49 +12V	+12V	49 +3.3V	+3.3V
50 a_PETn1	GND			50 +3.3V	+3.3V
51 GND	a_PERp1			51 GND	GND
52 GND	a_PERn1			52 GND	GND
53 a_PETp2	GND			53 GND	GND
54 a_PETn2	GND			54 GND	GND
55 GND	a_PERp2			55 GND	GND
56 GND	a_PERn2			56 GND	GND
57 a_PETp3	GND			57 GND	GND
58 a_PETn3	GND			58 GND	GND
59 GND	a_PERp3			59 +5V	+5V
60 GND	a_PERn3			60 +5V	+5V
61 a_PETp4	GND			61 +5V	+5V
62 a_PETn4	GND			62 +5V	+5V
63 GND	a_PERp4			63 GND	GND
64 GND	a_PERn4			64 GND	GND
65 a_PETp5	GND			65 GND	GND
66 a_PETn5	GND			66 GND	GND
67 GND	a_PERp5			67 GND	GND
68 GND	a_PERn5			68 GND	GND
69 a_PETp6	GND			69 GND	GND
70 a_PETn6	GND			70 GND	GND
71 GND	a_PERp6			71 GND	GND
72 GND	a_PERn6			72 GND	GND
73 a_PETp7	GND			73 +12V	+12V
74 a_PETn7	GND			74 +12V	+12V
75 GND	a_PERp7			75 +12V	+12V
76 GND	a_PERn7			76 +12V	+12V
77 RSVD	GND			77 +12V	+12V
78 +3.3V	+3.3V			78 +12V	+12V
79 +3.3V	+3.3V			79 +12V	+12V
80 +3.3V	+3.3V			80 +12V	+12V
81 +3.3V	+3.3V			81 +12V	+12V
82 NC	NC			82 +12V	+12V

PCI EXPRESS SIGNALS OVERVIEW

The following table provides a description of the SHB slot signal groups on the PCI Express connectors.

Type	Signals	Description	Connector	Source
Global	GND, +5V, +3.3V, +12V	Power		Backplane
	PSON#	Optional ATX support	A	SHB
	PWRGD, PWRBT#, +5Vaux	Optional ATX support	A and B	Backplane
	TDI	Optional JTAG support	A	Backplane
	TDO	Optional JTAG support	A	SHB
	SMCLK, SMDAT	Optional SMBus support	A	SHB & Backplane
	IPMB_CL, IPMB_DA	Optional IPMB support	C	SHB & Backplane
	CFG[0:3]	PCIe configuration straps	A	Backplane
	SHB_RST#	Optional reset line	A	SHB
	RSVD	Reserved	A and B	
	RSVD-G	Reserved ground	A	Backplane
	WAKE#	Signal for link reactivation	A	Backplane
PCIe	a_PETp[0:15] a_PETn[0:15] a_PERp[0:15] a_PERn[0:15]	Point-to-point from SHB slot through the x16 PCIe connector (A) to the target device(s)	A and B	SHB & Backplane
	b_PETp[0:3] b_PETn[0:3] b_PERp[0:3] b_PERn[0:3]	Point-to-point from SHB slot through the x8 PCIe connector (B) to the target device(s)	A	SHB & Backplane
	REFCLK[0:7]+ REFCLK[0:7]-	Clock synchronization of PCIe expansion slots	A A	SHB
	PERST#	PCIe fundamental reset		SHB & Backplane
PCI(-X)	PME#	Optional PCI wake-up event bussed on SHB and backplane expansion slots	A	Backplane
Misc. I/O	USB[0:3]P, USB[0:3]N, USBOC[0:3]#	Optional point-to-point from SHB Connector C to destination USB devices	C	SHB & Backplane
	a_MDI[0]p a_MDI[0]n b_MDI[0]p b_MDI[0]n	Optional point-to-point from SHB Connector C to a destination Ethernet device	C	SHB & Backplane

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Chapter 3 System BIOS

BIOS OPERATION

Chapters 3 through 7 of this manual describe the operation of the American Megatrends AMIBIOS and the BIOS Setup Utility. Refer to *Running AMIBIOS Setup* later in this chapter for standard Setup screens, options and defaults. The available Setup screens, options and defaults may vary if you have a custom BIOS.

When the system is powered on, AMIBIOS performs the Power-On Self Test (POST) routines. These routines are divided into two phases:

1) **System Test and Initialization**. Test and initialize system boards for normal operations.
2) **System Configuration Verification**. Compare defined configuration with hardware actually installed.

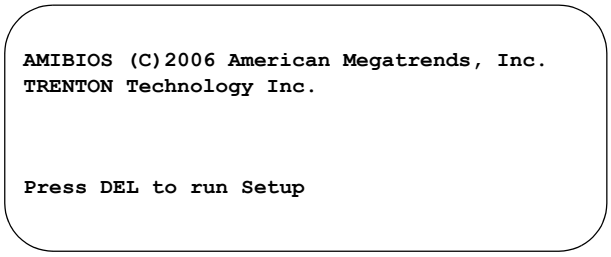
If an error is encountered during the diagnostic tests, the error is reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps is transmitted. If the error occurs after the display device is initialized, the error message is displayed on the screen. See *BIOS Errors* later in this section for more information on error handling.

The following are some of the Power-On Self Tests (POSTs) which are performed when the system is powered on:

- CMOS Checksum Calculation
- Keyboard Controller Test
- CMOS Shutdown Register Test
- Memory Refresh Test
- Display Memory Read/Write Test
- Display Type Verification
- Entering Protected Mode
- Memory Size Calculation
- Conventional and Extended Memory Test
- DMA Controller Tests
- Keyboard Test
- System Configuration Verification and Setup

AMIBIOS checks system memory and reports it on both the initial AMIBIOS screen and the AMIBIOS System Configuration screen which appears after POST is completed. AMIBIOS attempts to initialize the peripheral devices and if it detects a fault, the screen displays the error condition(s) which has/have been detected. If no errors are detected, AMIBIOS attempts to load the system from a bootable device, such as a floppy disk or hard disk. Boot order may be specified by the **Boot Device Priority** option on the Boot Setup Menu as described in the *Boot Setup* chapter later in this manual.

Normally, the only POST routine visible on the screen is the memory test. The following screen displays when the system is powered on:



Initial Power-On Screen

You have two options:

- Press **<Del>** to access the BIOS Setup Utility.

  This option allows you to change various system parameters such as date and time, disk drives, etc. The *Running AMIBIOS Setup* section of this manual describes the options available.

  You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* later in this section.)

  If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays. (See *Running AMIBIOS Setup* later in this section.)

- Allow the bootup process to continue without invoking the BIOS Setup Utility.

  In this case, after AMIBIOS loads the system, you may be requested to enter a password. (See *Password Entry* later in this section.)

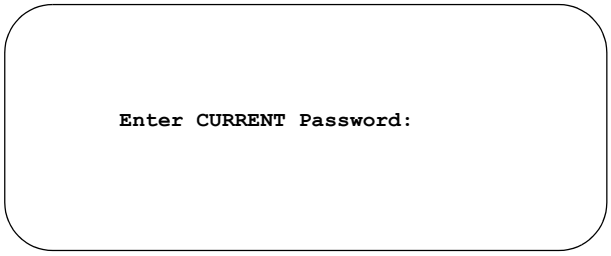
Once the POST routines complete successfully, a screen displays showing the current configuration of your system, including processor type, base and extended memory amounts, floppy and hard drive types, display type and peripheral ports.

Password Entry

The system may be configured so that the user is required to enter a password each time the system boots or whenever an attempt is made to enter the BIOS Setup Utility. The password function may also be disabled so that the password prompt does not appear under any circumstances.

The **Password Check** option in the Security Menu allows you to specify when the password prompt displays: **Always** or only when **Setup** is attempted. This option is available only if the supervisor and/or user password(s) have been established. The supervisor and user passwords may be changed using the **Change Supervisor Password** and **Change User Password** options on the Security Menu. If the passwords are null, the password prompt does not display at any time. See the *Security Setup* section of this chapter for details on setting up passwords.

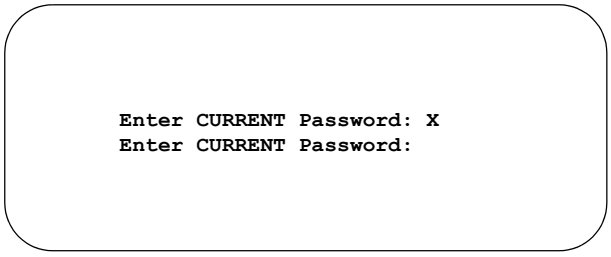
When password checking is enabled, the following password prompt displays:



Type the password and press **<Enter>**.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the password prompt does not display. To set up passwords, you may use the **Change Supervisor Password** and **Change User Password** options on the Security Menu of the BIOS Setup Utility. (See the *Security Setup* section later in this chapter.)

If an incorrect password is entered, the following screen displays:



You may try again to enter the correct password. If you enter the password incorrectly three times, the system responds in one of two different ways, depending on the value specified in the **Password Check** option on the *Security* Menu:

1) If the **Password Check** option is set to **Setup**, the system does not let you enter Setup, but does continue the booting process. You must reboot the system manually to retry entering the password.

2) If the **Password Check** option is set to **Always**, the system locks and you must reboot. After rebooting, you will be requested to enter the password.

Once the password has been entered correctly, you are allowed to continue.

BIOS Errors

If an error is encountered during the diagnostic checks performed when the system is powered on, the error is reported in one of two different ways:

1) If the error occurs before the display device is initialized, a series of beeps is transmitted.

2) If the error occurs after the display device is initialized, the screen displays the error message. In the case of a non-fatal error, a prompt to press the **<F1>** key may also appear on the screen.

Explanations of the beep codes and BIOS error messages may be found in *Appendix A - BIOS Messages*.

As the POST routines are performed, test codes are presented on Port 80H. These codes may be helpful as a diagnostic tool and are listed in *Appendix A - BIOS Messages*.

If certain non-fatal error conditions occur, you are requested to run the BIOS Setup Utility. The error messages are followed by this screen:

```
AMIBIOS (C)2006 American Megatrends, Inc.
TRENTON Technology Inc.



Press F1 to Run SETUP
Press F2 to load default values and continue
```

Press **<F1>**. You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* earlier in this section.)

If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays.

RUNNING AMIBIOS SETUP

AMIBIOS Setup keeps a record of system parameters, such as date and time, disk drives and other user-defined parameters. The Setup parameters reside in the Read Only Memory Basic Input/Output System (ROM BIOS) so that they are available each time the system is turned on. The BIOS Setup Utility stores the information in the complementary metal oxide semiconductor (CMOS) memory. When the system is turned off, a backup battery retains system parameters in the CMOS memory.

Each time the system is powered on, it is configured with these values, unless the CMOS has been corrupted or is faulty. The BIOS Setup Utility is resident in the ROM BIOS so that it is available each time the computer is turned on. If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file.

As soon as the system is turned on, the power-on diagnostic routines check memory, attempt to prepare peripheral devices for action, and offer you the option of pressing **<Del>** to run the BIOS Setup Utility.

If certain non-fatal errors occur during the Power-On Self Test (POST) routines which are run when the system is turned on, you may be prompted to run the BIOS Setup Utility by pressing **<F1>**.

BIOS SETUP UTILITY MAIN MENU

When you press **<F1>** in response to an error message received during the POST routines or when you press the **<Del>** key to enter the BIOS Setup Utility, the following screen displays:

```
                              BIOS SETUP UTILITY
 Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

System Overview                                    Use [ENTER], {TAB]
_____________________________________________      or [SHIFT-TAB] to
                                                   select a field.
AMIBIOS Version: 08.00.xx
BIOS Build Date: 04/16/07                          Use [+] or [-] to
BIOS ID        : 0ABLX018                          configure System
                                                   Time.
Processor
Type           : Intel(R)Xeon(R)CPU 5148 @ 2.33GHz
Speed          : 2333MHz
Count          : 2

System Memory                                      ←→   Select Screen
Size           : 2048MB                            ↑↓   Select Item
                                                   +-   Change Field
System Time                  [00:00:00]            Tab  Select Field
System Date                  [Wed 01/01/2002]      F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit

        vxx.xx (C)Copyright 1985-2006, American Megatrends, Inc.
```

BIOS Setup Utility Main Menu

When you display the BIOS Setup Utility Main Menu, the format is similar to the sample shown above. The data displayed on the top portion of the screen details parameters detected by AMIBIOS for your processor board and may not be modified. The system time and date displayed on the bottom portion of the screen may be modified.

BIOS SETUP UTILITY MAIN MENU OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

System Time/System Date

These options allow you to set the correct system time and date. If you do not set these parameters the first time you enter the BIOS Setup Utility, you will receive a "Run SETUP" error message when you boot the system until you set the correct parameters.

The Setup screen displays the system options:

System Time	**[00:00:00]**
System Date	**[Wed 01/01/2002]**

There are three fields for entering the time or date. Use the **<Tab>** key or the **<Enter>** key to move from one field to another and type in the correct value for the field.

If you enter an invalid value in any field, the screen will revert to the previous value when you move to the next field. When you change the value for the month, day or year field, the day of the week changes automatically when you move to the next field.

BIOS SETUP UTILITY OPTIONS

The BIOS Setup Utility allows you to change system parameters to tailor your system to your requirements. Various options which may be changed are listed below. Further explanations of these options and available values may be found in later chapters of this manual, as noted below.

NOTE: Do *not* change the values for any option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Use the **Right Arrow** key to display the desired menu. The following menus are available:

- Select **Advanced** to make changes to Advanced Setup parameters as described in the *Advanced Setup* chapter of this manual. The following options may be modified:
    - CPU Configuration
        - Adjacent Cache Line Prefetch
        - Max CPUID Value Limit
        - PECI
        - Intel SpeedStep (R) Technology
    - IDE Configuration
        - ATA/IDE Configuration
            - Configure SATA As
            - Legacy IDE Channels
        - Primary IDE Master/Primary IDE Slave
          Secondary IDE Master/Secondary IDE Slave
          Third IDE Master/Third IDE Slave
            - Type
            - LBA/Large Mode
            - Block (Multi-Sector Transfer)
            - PIO Mode
            - DMA Mode
            - S.M.A.R.T.
            - 32Bit Data Transfer
        - Hard Disk Write Protect

- IDE Detect Time Out (Sec)
- ATA(PI) 80Pin Cable Detection

- Floppy Configuration
  - Floppy A/Floppy B
- SuperIO Configuration
  - OnBoard Floppy Controller
  - Serial Port1 Address/Serial Port2 Address
  - Parallel Port Address
    - Parallel Port Mode
    - Parallel Port IRQ
- ACPI Configuration
  - Advanced ACPI Configuration
    - ACPI Version Features
    - ACPI APIC Support
    - AMI OEMB Table
    - Headless Mode
  - Chipset ACPI Configuration
    - APIC ACPI SCI IRQ
    - USB Device Wakeup From S3/S4
  - Power Supply Shutoff
  - AHCI Settings
    - APCI Port0 through Port5
- MPS Configuration
  - MPS Revision
- USB Configuration
  - Legacy USB Support
  - Port 64/60 Emulation
  - USB 2.0 Controller Mode
  - BIOS EHCI Hand-Off

- Select **PCIPnP** to make changes to PCI Plug and Play Setup parameters as described in the *PCI Plug and Play Setup* chapter of this manual. The following options may be modified:
    - Clear NVRAM
    - Plug & Play O/S
    - PCI Latency Timer
    - Allocate IRQ to PCI VGA
    - Palette Snooping
    - PCI IDE BusMaster
    - OffBoard PCI/ISA IDE Card
        - OffBoard PCI IDE Primary IRQ
        - OffBoard PCI IDE Secondary
    - Onboard VGA Controllers
        - Onboard VGA Controller mode
        - Backplane LAN Boot ROM
    - PCI Express Link Width Setting
    - IRQs 3, 4, 5, 7, 9, 10, 11, 14 and 15
    - DMA Channels 0, 1, 3, 5, 6 and 7
    - Reserved Memory Size
    - Reserve Memory Address

- Select **Boot** to make changes to Boot Setup parameters as described in the *Boot Setup* chapter of this manual. The following options may be modified:
    - Boot Settings Configuration
        - Quick Boot
        - Quiet Boot
        - AddOn ROM Display Mode
        - Bootup Num-Lock
        - PS/2 Mouse Support
        - Wait For ‘F1’ If Error
        - Hit ‘DEL’ Message Display
        - Interrupt 19 Capture
    - Boot Device Priority
    - Removable Drives

- Select **Security** to establish or change the supervisor or user password or to enable boot sector virus protection. These functions are described later in this chapter. The following options may be modified:
    - Change Supervisor Password
    - User Access Level
    - Change User Password
    - Password Check
    - Boot Sector Virus Protection
- Select **Chipset** to make changes to Chipset Setup parameters as described in the *Chipset Setup* chapter of this manual. The following options may be modified:
    - South Bridge Configuration
        - Onboard LAN Boot ROM
        - USB 2.0 Controller
        - Restore on AC Power Loss
        - ESB2 PCI-X Hub Configuration
            - PCI Bus Frequency
            - I/O Port Decode
            - RAS Sticky Error Handling
            - VGA 16-Bit Decode
- Select **Exit** to save or discard changes you have made to AMIBIOS parameters or to load the Optimal or Failsafe default settings. These functions are described later in this chapter. The following options are available:
    - Save Changes and Exit
    - Discard Changes and Exit
    - Discard Changes
    - Load Optimal Defaults
    - Load Failsafe Defaults

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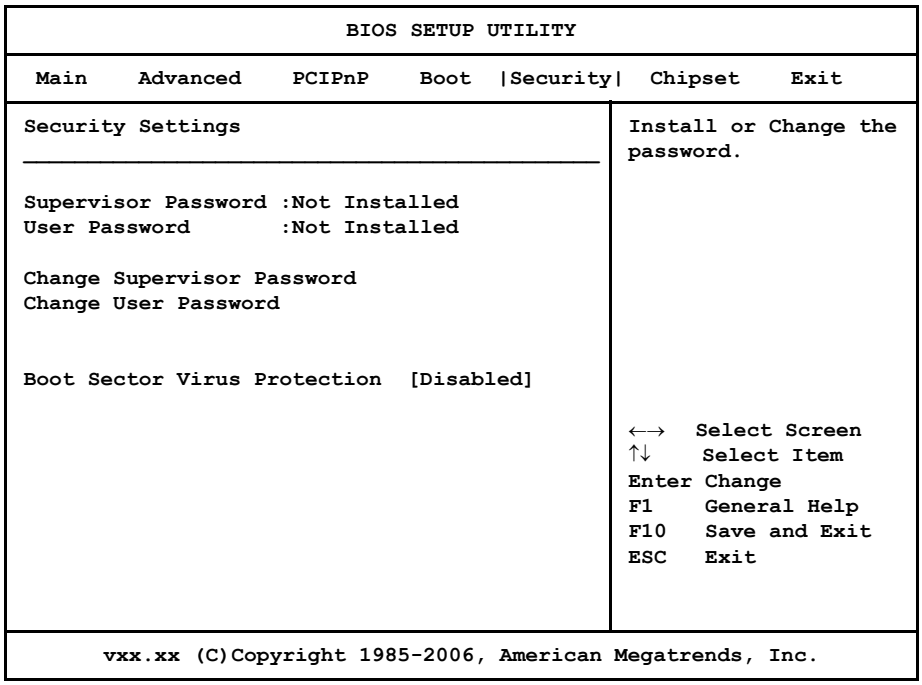
SECURITY SETUP

When you select **Security** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Security Setup Screen

When you display the Security Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>**.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SHB. Refer to the explanations below for specific instructions about entering correct information.

SECURITY SETUP OPTIONS

The Security Setup options allow you to establish, change or clear the supervisor or user password and to enable boot sector virus protection.

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

CHANGE SUPERVISOR PASSWORD

This option allows you to establish a supervisor password, change the current password or disable the password prompt by entering a null password. The password is stored in CMOS RAM.

If you have signed on under the user password, this option is *not* available.

The **Change Supervisor Password** feature can be configured so that a password must be entered each time the system boots or just when a user attempts to enter the BIOS Setup Utility.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the "Enter CURRENT Password" prompt is bypassed when you boot the system, and you must establish a new password.

If you select the **Change Supervisor Password** option, the following window displays:

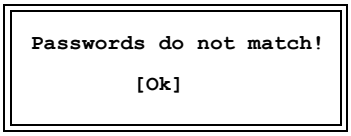
This is the message which displays before you have established a password, or if the last password entered was the null password. If a password has already been established, you are asked to enter the *current* password before being prompted to enter the *new* password.

Type the new password and press **<Enter>**. The password cannot exceed six (6) characters in length. The screen displays an asterisk (*) for each character you type.

After you have entered the new password, the following window displays:

Re-key the new password as described above.

If the password confirmation is miskeyed, AMIBIOS Setup displays the following message:



No retries are permitted; you must restart the procedure.

If the password confirmation is entered correctly, the following message displays:

Press the **<Enter>** key to return to the Security screen. **Installed** displays on the screen next to the **Supervisor Password** option, indicating the password has been accepted. This setting will remain in effect until the supervisor password is either disabled or discarded upon exiting the BIOS Setup Utility.

If you have created a new password, be sure to select **Exit**, then **Save Changes and Exit** to save the password. The password is then stored in CMOS RAM. The next time the system boots, you are prompted for the password.

NOTE: Be sure to keep a record of the new password each time it is changed. If you forget it, use the Password Clear jumper to reset it to the default (null password). See the *Specifications* chapter of this manual for details.

If a password has been established, the following options and their default values are added to the screen:

```
User Access Level          [Full Access]
Password Check             [Setup]
```

User Access Level

This option allows you to define the level of access the user will have to the system.

The Setup screen displays the system option:

User Access Level **[Full Access]**

Four options are available:

- Select **No Access** to prevent user access to the BIOS Setup Utility.
- Select **View Only** to allow access to the BIOS Setup Utility for viewing, but to prevent the user from changing any of the fields.
- Select **Limited** to allow the user to change only a limited number of options, such as Date and Time.
- Select **Full Access** to allow the user full access to change any option in the BIOS Setup Utility.

Password Check

This option determines when a password is required for access to the system.

The Setup screen displays the system option:

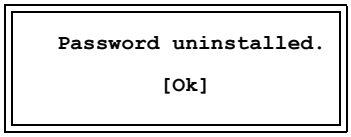
Password Check **[Setup]**

Two options are available:

- Select **Setup** to have the password prompt appear only when an attempt is made to enter the BIOS Setup Utility program.
- Select **Always** to have the password prompt appear each time the system is powered on.

DISABLING THE SUPERVISOR PASSWORD

To *disable* password checking so that the password prompt does not appear, you may create a null password by selecting the **Change Supervisor Password** function and pressing **<Enter>** without typing in a new password. You will be asked to enter the current password before being allowed to enter the null password. After you press **<Enter>** at the **Enter New Password** prompt, the following message displays:



CHANGE USER PASSWORD

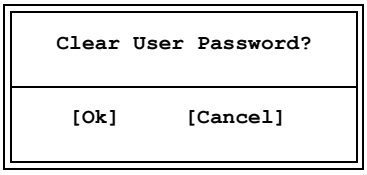
The **Change User Password** option is similar in functionality to the **Change Supervisor Password** and displays the same messages. If you have signed on under the user password, the **Change Supervisor Password** function is not available for modification.

If a user password has been established, the **Password Check** option and its default value is added to the screen. This option determines when a user password is required for access to the system. For details, refer to the description for **Password Check** under the **Change Supervisor Password** heading earlier in this section.

CLEAR USER PASSWORD

This option allows you to clear the user password. It disables the user password by entering a null password.

If you select the **Clear User Password** option, the following window displays:



You have two options:

- Select **Ok** to clear the user password.
- Select **Cancel** to leave the current user password in effect.

BOOT SECTOR VIRUS PROTECTION

This option allows you to request AMIBIOS to issue a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

The Setup screen displays the system option:

Boot Sector Virus Protection [Disabled]

Available options are:

Disabled
Enabled

NOTE: You should *not* enable boot sector virus protection when formatting a hard drive.

EXIT MENU

When you select **Exit** from the BIOS Setup Utility Main Menu, the following screen displays:

```
                        BIOS SETUP UTILITY
 Main    Advanced    PCIPnP    Boot    Security    Chipset    |Exit|
Exit Options                                  Exit system setup
_____________________________________________ after saving the
                                              changes.
Save Changes and Exit
Discard Changes and Exit                      F10 key can be used
Discard Changes                               for this operation.
Load Optimal Defaults
Load Failsafe Defaults

                                              ←→   Select Screen
                                              ↑↓   Select Item
                                              Enter Go to Sub Screen
                                              F1   General Help
                                              F10  Save and Exit
                                              ESC  Exit
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```

Exit Menu Screen

When you display the Exit Menu screen, the format is similar to the sample shown above. Highlight the option you wish to select and press **<Enter>**.

EXIT MENU OPTIONS

When you are running the BIOS Setup Utility program, you may either save or discard changes you have made to AMIBIOS parameters, or you may load the Optimal or Failsafe default settings.

Save Changes and Exit

The features selected and configured in the Setup screens are stored in the CMOS when this option is selected. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the AMIBIOS and the booting process continues, using the new CMOS values.

If you select the **Save Changes and Exit** option, the following window displays:

```
  Save configuration changes and exit setup?

        [Ok]              [Cancel]
```

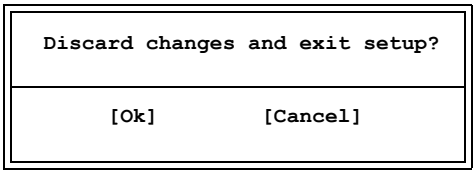
You have two options:

- Select **Ok** to save the system parameters and continue with the booting process.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes and Exit

When the **Discard Changes and Exit** option is selected, the BIOS Setup Utility exits *without* saving the changes in the CMOS. Control is then passed back to AMIBIOS and the booting process continues, using the previous CMOS values.

If you select the **Discard Changes and Exit** option, the following window displays:



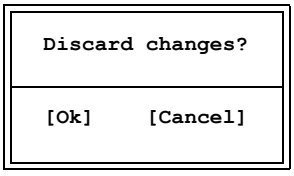
You have two options:

- Select **Ok** to continue the booting process *without* writing any changes to the CMOS.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes

When the **Discard Changes** option is selected, the BIOS Setup Utility resets any parameters you have changed back to the values at which they were set when you entered the Setup Utility. Control is then passed back to the BIOS Setup Utility screen.

If you select the **Discard Changes** option, the following window displays:



You have two options:

- Select **Ok** to reset any parameters you have changed back to the values at which they were set when you entered the BIOS Setup Utility. This option then returns you to the BIOS Setup Utility screen.
- Select **Cancel** to return to the BIOS Setup Utility screen *without* discarding any changes you have made.

Load Optimal or Failsafe Defaults

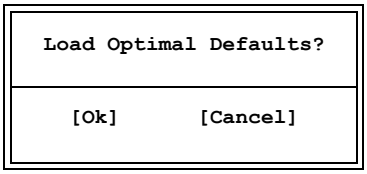
Each AMIBIOS Setup option has two default settings (Optimal and Failsafe). These settings can be applied to all AMIBIOS Setup options when you select the appropriate configuration option from the BIOS Setup Utility Main Menu.

You can use these configuration options to quickly set the system configuration parameters which should provide the best performance characteristics, or you can select a group of settings which have a better chance of working when the system is having configuration-related problems.

Load Optimal Defaults

This option allows you to load the Optimal default settings. These settings are best-case values which should provide the best performance characteristics. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

If you select the **Load Optimal Defaults** option, the following window displays:



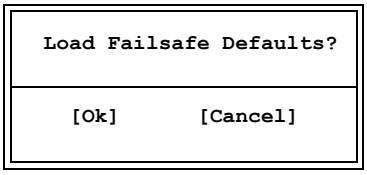
You have two options:

- Select **Ok** to load the Optimal default settings.
- Select **Cancel** to leave the current values in effect.

Load Failsafe Defaults

This option allows you to load the Failsafe default settings when you cannot boot your computer successfully. These settings are more likely to configure a workable computer. They may not provide optimal performance, but are the most stable settings. You may use this option as a diagnostic aid if your system is behaving erratically. Select the Failsafe settings and then try to diagnose the problem after the computer boots.

If you select the **Load Failsafe Defaults** option, the following window displays:



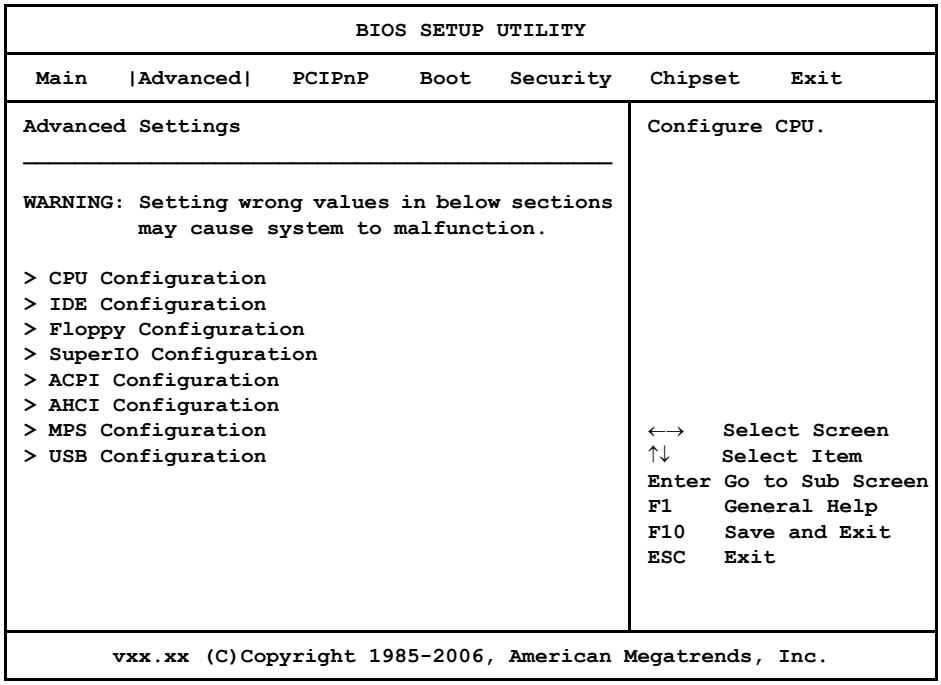
You have two options:

- Select **Ok** to load the Failsafe default settings.
- Select **Cancel** to leave the current values in effect.

Chapter 4 Advanced Setup

ADVANCED SETUP

When you select **Advanced** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Advanced Setup Screen

When you display the Advanced Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Advanced Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: The **Floppy Configuration** and **SuperIO Configuration** options appear only if an I/O board such as the IOB30MC (6391-001) or IOB31 (6474-000) is connected to the SHB. Otherwise, these line items are not available.

The values on the Advanced Setup subscreens do not necessarily reflect the values appropriate for your SHB. Refer to the explanations following each screen for specific instructions about entering correct information.

ADVANCED SETUP OPTIONS

NOTE: Do *not* change the values for any Advanced Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

CPU Configuration

The **CPU Configuration** subscreen provides you with information about the processor in your system. The following options may be modified:

- CPU Configuration
    - Adjacent Cache Line Prefetch
    - Max CPUID Value Limit
    - PECI
    - Intel SpeedStep® Technology

IDE Configuration

The options on the **IDE Configuration** subscreens allow you to set up or modify parameters for your IDE controller and hard disk drive(s). The following options may be modified:

- ATA/IDE Configuration
    - Configure SATA As
    - Legacy IDE Channels
- Primary IDE Master/Primary IDE Slave
  Secondary IDE Master/Secondary IDE Slave
  Third IDE Master/Third IDE Slave
    - Type
    - LBA/Large Mode
    - Block (Multi-Sector Transfer)
    - PIO Mode
    - DMA Mode
    - S.M.A.R.T.
    - 32Bit Data Transfer
- Hard Disk Write Protect
- IDE Detect Time Out (Sec)
- ATA(PI) 80Pin Cable Detection

Floppy Configuration

The options on the **Floppy Configuration** subscreen allow you to set up or modify parameters for your floppy disk drive(s). The following options may be modified:

- Floppy A/Floppy B

SuperIO Configuration

The options on the **SuperIO Configuration** subscreen allow you to set up or modify parameters for your on-board peripherals. The following options may be modified:

- OnBoard Floppy Controller
- Serial Port1 Address/Serial Port2 Address
- Parallel Port Address
    - Parallel Port Mode
    - Parallel Port IRQ

ACPI Configuration

The **ACPI Configuration** subscreen allows you to set up or modify the following options:

- Advanced ACPI Configuration
    - ACPI Version Features
    - ACPI APIC Support
    - AMI OEMB Table
    - Headless Mode
- Chipset ACPI Configuration
    - APIC ACPI SCI IRQ
    - USB Device Wakeup From S3/S4
- Power Supply Shutoff

AHCI Settings

The **AHCI Settings** subscreen allows you to set up or modify the following options:

- AHCI Ports 0 through 5

MPS Configuration

The **MPS Configuration** subscreen allows you to modify the following option:

- MPS Revision

USB Configuration

The options on the **USB Configuration** subscreen allow you to set up or modify parameters for your on-board USB ports. The following options may be modified:

- Legacy USB Support
- Port 64/60 Emulation
- USB 2.0 Controller Mode
- BIOS EHCI Hand-Off

Saving and Exiting

When you have made all desired changes to **Advanced** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

CPU CONFIGURATION SETUP

When you select **CPU Configuration** from the Advanced Setup Screen, the following Setup screen displays:

```
                              BIOS SETUP UTILITY
          |Advanced|
Configure advanced CPU settings                  This should be enabled
Module Version:3E.01                             in order to enable or
                                                 disable the Adjacent
Manufacturer      : Intel                        Cache Line Prefetch
Brand String      : Intel(R) Xeon(R)CPU  5148    Disabel Feature.
Frequency         : 2.33GHz
FSB Speed         : 1333MHz
Cache L1          : 64 KB
Cache L2          : 4096 KB
Ratio Status      : Unlocked (Min:06, Max:07)
Ratio Actual Value: 7                            ←→   Select Screen
                                                 ↑↓   Select Item
Adjacent Cache Line Prefetch:  [Enabled]         +-   Change Option
Max CPUID Value Limit:         [Disabled]        F1   General Help
PECI:                          [Enabled]         F10  Save and Exit
Intel SpeedStep(R) Technology: [Minimum Speed]   ESC  Exit
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```

CPU Configuration Screen

When you display the CPU Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

CPU CONFIGURATION SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Advanced Setup. Once you change the settings, the new settings display each time Advanced Setup is run.

Adjacent Cache Line Prefetch

The Setup screen displays the system option:

Adjacent Cache Line Prefetch: [Enabled]

Available options are:

Disabled
Enabled

Max CPUID Value Limit

This Setup screen displays the system option

Max CPUID Value Limit: [Disabled]

Available options are:

Disabled
Enabled

PECI

This Setup screen displays the status of the PECI or Platfrom Environment Control Interface. PECI is an optional interface that may be used when a communication link is needed between the processor's thermal sensor and external temperature monitoring software applications.

PECI: [Enabled]

Available options are:

Disabled
Enabled

Intel SpeedStep(R) Technology

This option allows you to enable or disable the processor's Intel SpeedStep Technology feature. The maximum setting runs the processor or processors at the maximum CPU speed, likewise the minimum setting runs the procesor at the lowest possible speed. In the automatic mode the processor speed is controlled by the operating system. The disabled setting runs the processor at the default CPU speed.

The Setup screen displays the system option:

Intel SpeedStep(R) Technology: [Maximum Speed]

Available options are:

Maximum Speed
Minimum Speed
Automatic
Disabled

IDE CONFIGURATION

When you select **IDE Configuration** from the Advanced Setup Menu, a Setup screen similar to the following displays:

```
                        BIOS SETUP UTILITY
        |Advanced|
IDE Configuration                                    Options
_____________________________________________

ATA/IDE Configuration          [Enhanced]            Disabled
 Configure SATA as             [IDE]                 Compatible
                                                     Enhanced
> Primary IDE Master     [Not Detected]
> Primary IDE Slave      [ATAPI CDROM]
> Secondary IDE Master   [Not Detected]
> Secondary IDE Slave    [ATAPI CDROM]
> Third IDE Master       [Hard Disk]
> Third IDE Slave        [Hard Disk]

Hard Disk Write Protect       [Disabled]           ←→   Select Screen
IDE Detect Time Out (Sec)     [35]                 ↑↓   Select Item
ATA(PI) 80Pin Cable Detection [Host & Device]      +-   Change Option
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit

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```

IDE Configuration Screen

When you display the IDE Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

Some of the options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

IDE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

ATA/IDE Configuration

This option specifies which IDE ports are available for use. The line items which display below the **ATA/IDE Configuration** option vary depending on the setting of this option.

The Setup screen displays the system option:

ATA/IDE Configuration [Enhanced]

Three options are available:

- Select **Disabled** to disable all ports. No drives are displayed on the screen.
- Select **Compatible** to allow up to four devices, two parallel and two serial. The **Legacy IDE Channels** and **Primary** and **Secondary Master/Slave** line items display on the screen.
- Select **Enhanced** to allow up to eight devices, two parallel and six serial. The **Configure SATA As** and **Primary**, **Secondary** and **Third Master/ Slave** line items display on the screen. The Secondary and Third Master/ Slave line items refer to the four SATA ports (0 through 5).

Configure SATA As

This option allows you specify how to configure the available SATA devices. It is only available if the **ATA/IDE Configuration** option is set to **Enhanced**.

The Setup screen displays the system option:

Configure SATA as [IDE]

Three options are available:

- Select **IDE** to enable the SATA devices as IDE devices. The **Primary**, **Secondary** and **Third IDE Master/Slave** line items display.
- Select **RAID** to enable the SATA devices as a RAID device. The **Primary**, **Secondary** and **Third IDE Master/Slave** line items display.
- Select **AHCI** to enable Native Command Queuing (NCQ) and SATA hot plug capability. The **Primary**, **Secondary** and **Third IDE Master/Slave** line items display.

Legacy IDE Channels

This option allows you specify how to configure the available primary IDE and SATA devices. It is only available if the **ATA/IDE Configuration** option is set to **Compatible**, which allows access to up to four devices, which can be a combination of IDE and serial ATA devices.

The Setup screen displays the system option:

Legacy IDE Channels [PATA Pri, SATA Sec]

Four options are available:

- Select **SATA Only** to enable up to six SATA devices.
- Select **PATA Pri, SATA Sec** to have the system access the primary IDE devices before the SATA devices. The two devices on the primary IDE are then defined as primary master/slave and two of the serial ATA devices are secondary master/slave.

- Select **SATA Pri, PATA Sec** to have the system access the SATA devices before the primary IDE devices. Two of the serial ATA devices are then defined as primary master/slave and the devices on the primary IDE are secondary master/slave.
- Select **PATA Only** if only the two primary IDE devices are available.

Primary IDE Master/Primary IDE Slave
Secondary IDE Master/Secondary IDE Slave
Third IDE Master/Third IDE Slave

The SHB has an enhanced IDE (EIDE) interface which can support two IDE disk drives in a master/slave configuration (P11). Each of the drives may be a different type. Six serial ATA devices can also be supported (P28, P31, P32, P34, P35 and P36).

Devices attached to the primary controller and the serial ATA ports are detected automatically by AMIBIOS and displayed on the IDE Configuration screen. The line items which display are determined by the settings of the **ATA/IDE Configuration**, **Configure SATA as** and **Legacy IDE Channels** options described above. The values for the line items depend on the devices detected by AMIBIOS.

The Setup screen displays the system options:

Primary IDE Master	**[Not Detected]**
Primary IDE Slave	**[ATAPI CDROM]**
Secondary IDE Master	**[Not Detected]**
Secondary IDE Slave	**[ATAPI CDROM]**
Third IDE Master	**[Hard Disk]**
Third IDE Slave	**[Hard Disk]**

This is an example of the screen when the maximum of eight devices are enabled, with the **ATA/IDE Configuration[Enhanced]** and **Configure SATA as** options set as shown in the screen sample at the beginning of this section.

To view and/or change parameters for any of the devices, press **<Enter>** to proceed to the IDE Device Setup screen, which is described later in this section.

Hard Disk Write Protect

This option allows you to disable or enable device write protection. Write protection will be effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Hard Disk Write Protect **[Disabled]**

Available options are:

Disabled
Enabled

IDE Detect Time Out (Sec)

This option allows you to select the time-out value (in seconds) for detecting an ATA/ ATAPI device.

The Setup screen displays the system option:

IDE Detect Time Out (Sec) [35]

Available options are:

0
5
10
15
20
25
30
35

ATA(PI) 80Pin Cable Detection

This option allows you to select the mechanism for detecting an 80-pin ATA(PI) cable.

The Setup screen displays the system option:

ATA(PI) 80Pin Cable Detection [Host & Device]

Available options are:

Host & Device
Host
Device

IDE DEVICE SETUP

When you select one of the IDE devices from the **IDE Configuration** screen, a Setup screen similar to the following displays:

```
                        BIOS SETUP UTILITY
         |Advanced|
Primary IDE Master                                  Select the type
_____________________________________________       of device connected
Device    :Hard Disk                                to the system.
Vendor    :ST380823-A
Size      :80.0GB
LBA Mode  :Supported
Block Mode:16Sectors
PIO Mode  :4
Async DMA :MultiWord DMA-2
Ultra DMA :Ultra DMA-5
S.M.A.R.T.:Supported
_____________________________________________
Type                            [Auto}      ←→   Select Screen
LBA/Large Mode                  [Auto]      ↑↓   Select Item
Block (Multi-Sector Transfer)   [Auto]      +-   Change Option
PIO Mode                        [Auto]      F1   General Help
DMA Mode                        [Auto]      F10  Save and Exit
S.M.A.R.T.                      [Auto]      ESC  Exit
32Bit Data Transfer             [Disabled]

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```

IDE Device Screen

When you display the IDE Device subscreen, the format is similar to the sample shown above. The data displayed on the top portion of the screen details the parameters detected by AMIBIOS for the specified device and may not be modified. The data displayed on the bottom portion of the screen may be modified.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which AMIBIOS detected upon initial bootup.

IDE DEVICE SETUP OPTIONS

The following options are available for each of the IDE devices on the primary and secondary IDE controllers:

Type

This option allows you to specify what type of device is on the IDE controller.

The Setup screen displays the system option:

Type [Auto]

Available options are:

Not Installed
Auto
CD/DVD
ARMD

If **Not Installed** is selected, the other options on the bottom portion of this screen do not display.

LBA/Large Mode

This option allows you to enable IDE LBA (Logical Block Addressing) Mode for the specified IDE drive. Data is accessed by block addresses rather than by the traditional cylinder-head-sector format. This allows you to use drives larger than 528MB.

The Setup screen displays the system option:

LBA/Large Mode [Auto]

Two options are available:

- Select **Disabled** to have AMIBIOS use the physical parameters of the hard disk and do no translation to logical parameters. The operating system which uses the parameter table will then see only 528MB of hard disk space even if the drive contains more than 528MB.
- Select **Auto** to enable LBA mode and translate the physical parameters of the drive to logical parameters. LBA Mode must be supported by the drive and the drive must have been formatted with LBA Mode enabled.

Block (Multi-Sector Transfer) Mode

This option supports transfer of multiple sectors to and from the specified IDE drive. Block mode boosts IDE drive performance by increasing the amount of data transferred during an interrupt.

If **Block Mode** is set to **Disabled**, data transfers to and from the device occur one sector at a time.

The Setup screen displays the system option:

Block (Multi-Sector Transfer) [Auto]

Available options are:

Disabled
Auto

PIO Mode

IDE Programmed I/O (PIO) Mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Set the **PIO Mode** option to **Auto** to have AMIBIOS select the PIO mode used by the IDE drive being configured. If you select a specific value for the PIO mode, you must make *absolutely* certain that you are selecting the PIO mode supported by the IDE drive being configured.

The Setup screen displays the system option:

PIO Mode **[Auto]**

Available options are:

Auto
0
1
2
3
4

DMA Mode

This option allows you to select DMA Mode for the device.

The Setup screen displays the system option:

DMA Mode **[Auto]**

Available options are:

Auto

S.M.A.R.T.

This option allows AMIBIOS to use the SMART (Self-Monitoring Analysis and Reporting Technology) protocol for reporting server system information over a network. The Setup screen displays the system option:

S.M.A.R.T. **[Auto]**

Available options are:

Auto
Disabled
Enabled

32Bit Data Transfer

If the **32Bit Data Transfer** parameter is set to **Enabled**, AMIBIOS enables 32-bit data transfers. If the host controller does not support 32-bit transfer, this feature *must* be set to **Disabled**.

The Setup screen displays the system option:

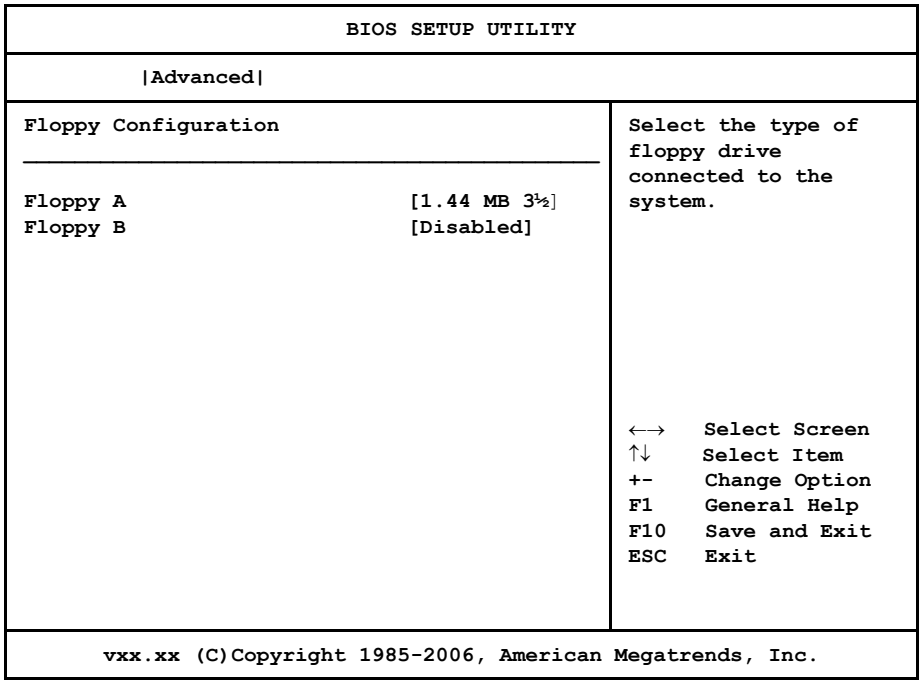
32Bit Data Transfer [Disabled]

Available options are:

Disabled
Enabled

FLOPPY CONFIGURATION

When you select **Floppy Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Floppy Configuration Screen

When you display the Floppy Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The **Floppy Configuration** subscreen is available only if an I/O board such as the IOB30MC (6391-001) or IOB31 (6474-000) is connected to the SHB.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which AMIBIOS detected upon initial bootup.

FLOPPY CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Floppy A/Floppy B

The floppy drive(s) in your system can be configured using these options. The **Disabled** option can be used for diskless workstations.

The Setup screen displays the system options:

Floppy A	**[1.44 MB 3½"]**
Floppy B	**[Disabled]**

Available options are:

Disabled
360 KB 5¼"
1.2 MB 5¼"
720 KB 3½"
1.44MB 3½"
2.88MB 3½"

SUPERIO CONFIGURATION

When you select **SuperIO Configuration** from the Advanced Setup Menu, the following Setup screen displays:

```
                    SuperIO Chipset Smc27X

          |Advanced|

Configure Smc27X Super IO Chipset              Allows BIOS to enable
_____________________________________          or disable floppy
                                               controller.
OnBoard Floppy Controller    [Enabled]
Serial Port1 Address         [3F8/IRQ4]
Serial Port2 Address         [2F8/IRQ3]
Parallel Port Address        [378]
  Parallel Port Mode         [Normal]
  Parallel Port IRQ          [IRQ7]


                                               ←→   Select Screen
                                               ↑↓   Select Item
                                               +-   Change Option
                                               F1   General Help
                                               F10  Save and Exit
                                               ESC  Exit

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```

SuperIO Configuration Screen

When you display the SuperIO Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The **SuperIO Configuration** subscreen is available only if an I/O board such as the IOB30MC (6391-001) or IOB31 (6474-000) is connected to the SHB.

SUPERIO CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

OnBoard Floppy Controller

The on-board floppy drive controller may be enabled or disabled using this option.

The Setup screen displays the system option:

OnBoard Floppy Controller [Enabled]

Available options are:

Disabled
Enabled

Serial Port1 Address/Serial Port2 Address

Each of these options enables the specified serial port on the SBC and establishes the base I/O address and the number of the interrupt request for the port.

The Setup screen displays the system option:

Serial Port1 Address	**[3F8/IRQ4]**
Serial Port2 Address	**[2F8/IRQ3]**

Available options are:

Disabled
3F8/IRQ4
3E8/IRQ4
2F8/IRQ3
2E8/IRQ3

NOTE: The values available for each on-board serial port may vary, depending on the setting previously selected for the other on-board serial port and any off-board serial ports. If an I/O address is assigned to another serial port, AMIBIOS automatically omits that address from the values available.

If the system has off-board serial ports which are configured to specific starting I/O ports via jumper settings, AMIBIOS configures the on-board serial ports to avoid conflicts.

When AMIBIOS checks serial ports, any off-board serial ports found are left at their assigned addresses. Serial Port1, the first on-board serial port, is configured with the first available address and Serial Port2, the second on-board serial port, is configured with the next available address. The default address assignment order is 3F8H, 2F8H, 3E8H, 2E8H. Note that this same assignment order is used by AMIBIOS to place the active serial port addresses in lower memory (BIOS data area) for configuration as logical COM devices.

For example, if there is one off-board serial port and its address is set to 2F8H, Serial Port1 is assigned address 3F8H and Serial Port2 is assigned address 3E8H. Configuration is then as follows:

COM1 - Serial Port1 (at 3F8H)
COM2 - off-board serial port (at 2F8H)
COM3 - Serial Port2 (at 3E8H)

Parallel Port Address

This option enables the parallel port on the SBC and establishes the base I/O address for the port.

The Setup screen displays the system option:

Parallel Port Address [378]

Available options are:

Disabled
378
278
3BC

When AMIBIOS checks for parallel ports, any off-board parallel ports found are left at their assigned addresses. The on-board Parallel Port is automatically configured with the first available address not used by an off-board parallel port.

If this option is set to **Disabled**, the **Parallel Port Mode** and **Parallel Port IRQ** options are not available.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes which adhere to the IEEE P1284 specifications.

If the **Parallel Port Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

Parallel Port Mode [Normal]

Four options are available:

- Select **Normal** to use normal parallel port mode.
- Select **SPP Bi-Directional** to use bi-directional parallel port mode.
- Select **EPP + SPP** to allow the parallel port to be used with devices which adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
  When you select **EPP + SPP** or **ECP + EPP** mode, the **EPP Version** line item displays. Valid version options are 1.7 and 1.9.
- Select **ECP** to allow the parallel port to be used with devices which adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5MB/second. ECP provides symmetric bidirectional communication.

When you select **ECP** or **EPP + ECP** mode, the **ECP Mode DMA Channel** line item displays. Valid DMA channel options are DMA1 and DMA3; the default is DMA3.

Parallel Port IRQ

This option specifies the interrupt request (IRQ) which is used by the parallel port.

If the **Parallel Port Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

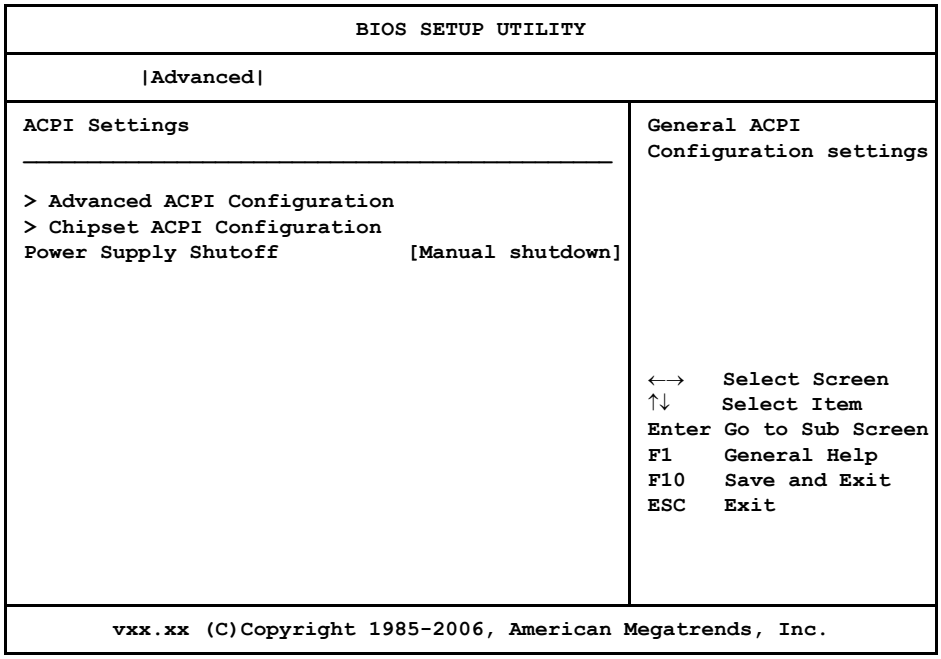
Parallel Port IRQ [IRQ7]

Available options are:

IRQ5
IRQ7

ACPI CONFIGURATION

When you select **ACPI Configuration** from the Advanced Setup Menu, the following Setup screen displays:



ACPI Configuration Screen

When you display the ACPI Configuration screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the ACPI Configuration options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

The subscreens allow you to set up or modify the following options:

- Advanced ACPI Configuration
    - ACPI Version Features
    - ACPI APIC Support
    - AMI OEMB Table
    - Headless Mode
- Chipset ACPI Configuration
    - APIC ACPI SCI IRQ
    - USB Device Wakeup From S3/S4
- Power Supply Shutoff

Power Supply Shutoff

This option should be set to **Auto** if the power supply can turn off automatically on Windows shutdown.

The Setup screen displays the system option:

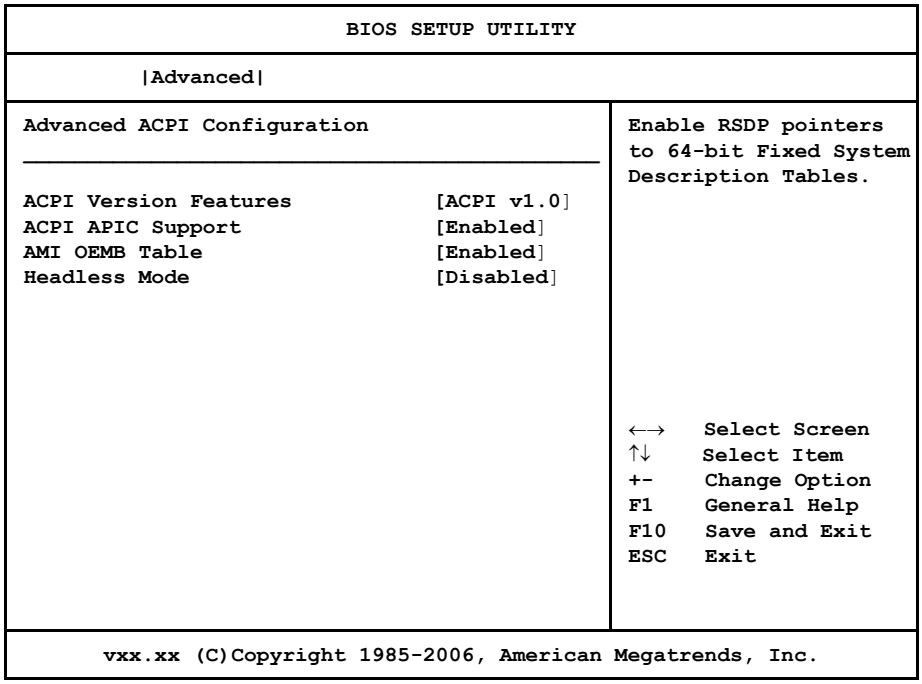
Power Supply Shutoff [Manual shutdown]

Two options are available:

- Select **Auto** to have the system automatically shut down when commanded by the operating system.
- Select **Manual shutdown** to require that the user manually shut down the system. After successful shutdown, the system displays the message "It is now safe to turn off your computer." The power supply may then be turned off manually.

ADVANCED ACPI CONFIGURATION

When you select **Advanced ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:



Advanced ACPI Configuration Screen

When you display the Advanced ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

ADVANCED ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

ACPI Version Features

The Setup screen displays the three ACPI version options:

ACPI Version Features [ACPI v1.0]

Available options are:

ACPI v1.0
ACPI v2.0
ACPI v3.0

ACPI APIC Support

The Setup screen displays the system option:

ACPI APIC Support [Enabled]

Available options are:

Disabled
Enabled

AMI OEMB Table

The Setup screen displays the system option:

AMI OEMB Table [Enabled]

Available options are:

Disabled
Enabled

Headless Mode

The Setup screen displays the system option:

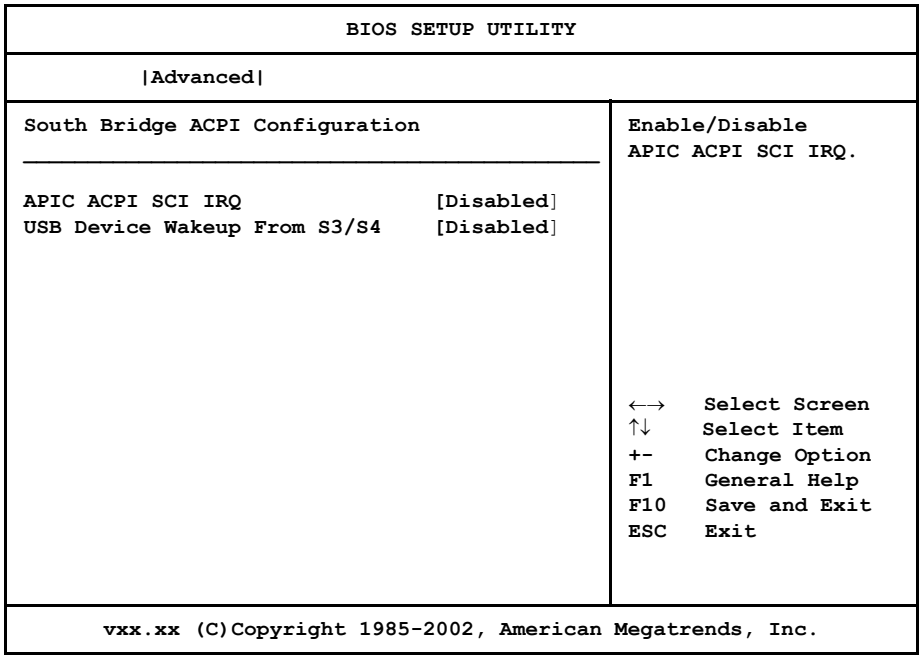
Headless Mode [Disabled]

Available options are:

Disabled
Enabled

CHIPSET ACPI CONFIGURATION

When you select **Chipset ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:



Chipset ACPI Configuration Screen

When you display the Chipset ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

CHIPSET ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

APIC ACPI SCI IRQ

The Setup screen displays the system option:

APIC ACPI SCI IRQ [Disabled]

Available options are:

Disabled
Enabled

USB Device Wakeup From S3/S4

The Setup screen displays the system option:

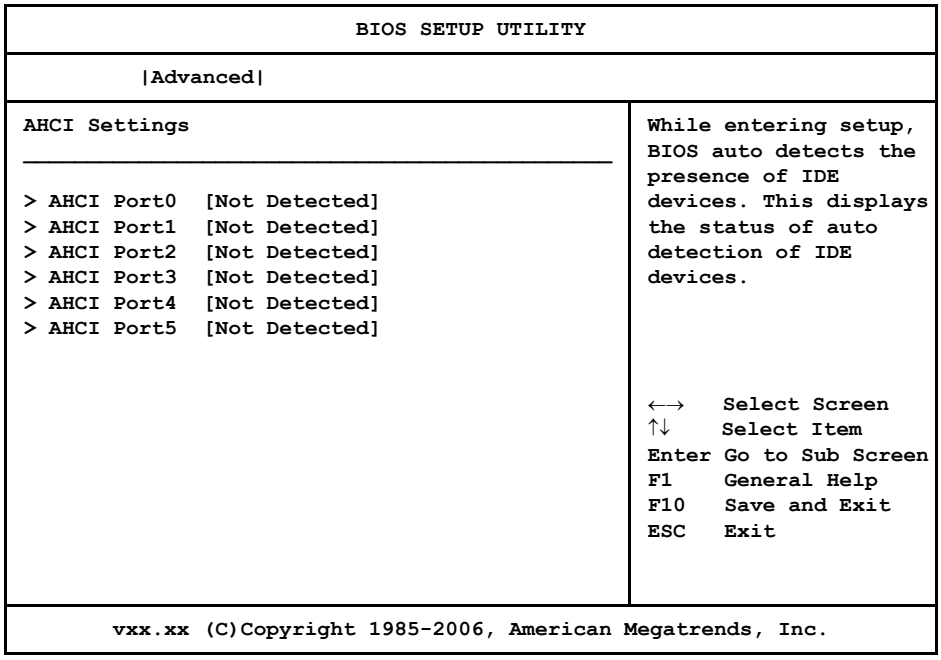
USB Device Wakeup From S3/S4 [Enabled]

Available options are:

Disabled
Enabled

AHCI CONFIGURATION

When you select **AHCI Configuration** from the Advanced Setup Menu, the following Setup screen displays:



AHCI Configuration Screen

When you display the AHCI Configuration screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change the BIOS detection parameter for each SATA device connected to the SHB's south bridge. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

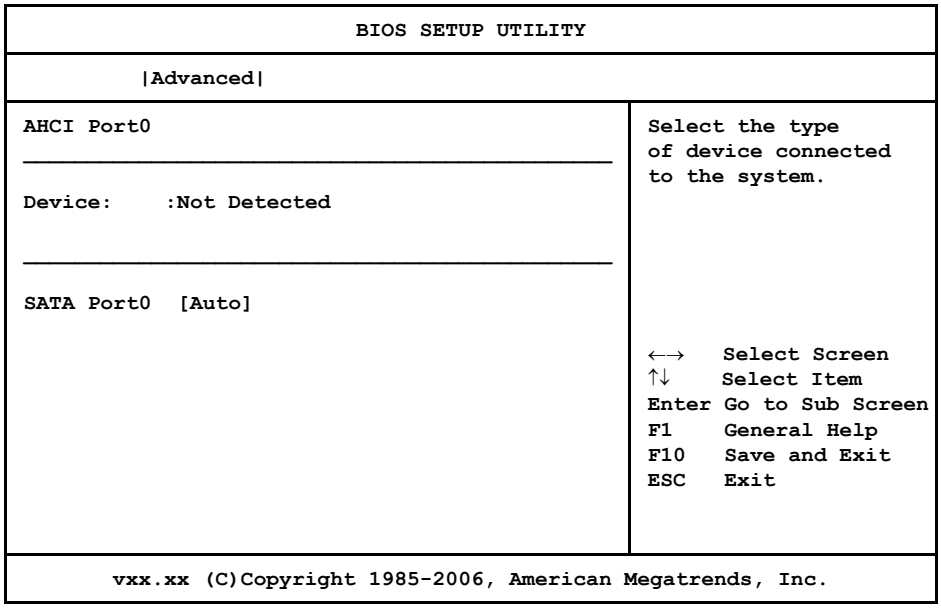
The subscreens allow you to set up or modify the following options:

- AHCI Settings
    - AHCI Port0
    - AHCI Port1
    - AHCI Port2
    - AHCI Port3
    - AHCI Port5

NOTE: This configuration menu only applies if the AHCI or RAID option is selected in the **Configure SATA as** line located on the **IDE Configuration Screen**. SATA drives configured as IDE devices will be displayed on the **IDE Configuration Screen**.

AHCI PORT 0

When you select **AHCI Port0** from the AHCI Settings Menu, the following Setup screen displays:



AHCI Port0

The Setup screen displays the system option:

SATA Port0 **[Auto]**

Available options are:

Auto

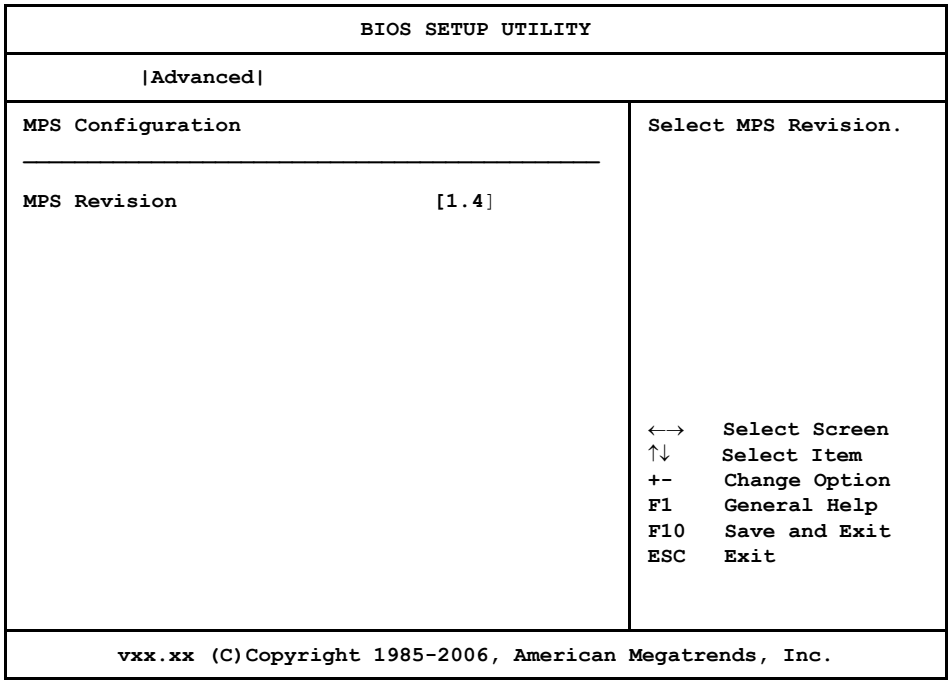
Not Installed

The setup screens will display the same information for each AHCI Port selected on the AHCI Configuration screen. Selecting AHCI Port1 is used to change the settings for SATA Port1 and likewise through the slection of AHCI Port5 that is used to change the settings of SATA Port5.

NOTE: While documentating this BIOS feature, a SATA device was not connected to AHCI Port0. In the example above, this is why the Device :Not Detected message is displayed above the SATA Port0 set-up selection line.

MPS CONFIGURATION SETUP

When you select **MPS Configuration** from the Advanced Setup Screen, the following Setup screen displays:



MPS Configuration Screen

When you display the MPS Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

MPS CONFIGURATION SETUP OPTION

The description for the system option listed below shows the value as it appears if you have not yet run Advanced Setup. Once you change the setting, the new setting displays each time Advanced Setup is run.

MPS Revision

The Setup screen displays the system option:

MPS Revision [1.4]

Available options are:

1.1
1.4

USB CONFIGURATION

When you select **USB Configuration** from the Advanced Setup Menu, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
          |Advanced|
USB Configuration                          | Enables support for
_____________________________________      | legacy USB. AUTO
                                           | option disables
Module Version - x.xx.x-xx.x               | legacy support if
                                           | no USB devices are
USB Devices Enabled:                       | connected.
  1 keyboard,  1 mouse
Legacy USB Support          [Enabled]
Port 64/60 Emulation        [Enabled]
USB 2.0 Controller Mode     [HiSpeed]      ←→   Select Screen
BIOS EHCI Hand-Off          [Enabled]      ↑↓   Select Item
                                           +-   Change Option
                                           F1   General Help
                                           F10  Save and Exit
                                           ESC  Exit
    vxx.xx (C)Copyright 1985-2006, American Megatrends, Inc.
```

USB Configuration Screen

When you display the USB Configuration screen, the format is similar to the sample shown above that illustrates one USB keyboard and one USB mouse connected to the SHB. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

USB CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Legacy USB Support

This option allows you to enable support for older USB devices. The **Auto** option disables legacy support if no USB devices are connected. If this option is set to **Disabled**, the remaining three options are not available.

The Setup screen displays the system option:

Legacy USB Support [Enabled]

Available options are:

Disabled
Enabled
Auto

Port 64/60 Emulation

This option allows you to enable or disable I/O port 60h/64h emulation support. This option should be set to **Enabled** for complete USB keyboard legacy support for operating systems which are not USB-aware.

If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Port 64/60 Emulation [Enabled]

Available options are:

Disabled
Enabled

USB 2.0 Controller Mode

This option configures the USB 2.0 controller to high-speed (480Mbps) or full-speed (12Mbps) mode.

If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

USB 2.0 Controller Mode [HiSpeed]

Available options are:

FullSpeed
HiSpeed

BIOS EHCI Hand-Off

This option is a work-around for operating systems without EHCI hand-off support.

If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

BIOS EHCI Hand-Off [Enabled]

Available options are:

Disabled
Enabled

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Chapter 5 Plug and Play Setup

PLUG AND PLAY SETUP

When you select **PCIPnP** from the BIOS Setup Utility Main Menu, the following Setup screen displays:

```
                              BIOS SETUP UTILITY
 Main    Advanced   |PCIPnP|   Boot   Security   Chipset    Exit
Advanced PCI/PnP Settings                          Clear NVRAM during
_____________________________________________      System Boot.

WARNING: Setting wrong values in below sections
         may cause system to malfunction.

Clear NVRAM                       [No]
Plug & Play O/S                   [No]
PCI Latency Timer                 [64]
Allocate IRQ to PCI VGA           [Yes]
Palette Snooping                  [Disabled]
PCI IDE BusMaster                 [Disabled]
OffBoard PCI/ISA IDE Card         [Auto]
Backplane LCI LAN                 [Enabled]
Onboard VGA Controller            [Enabled]
 Onbd VGA Controller mode         [Disabled]
 Backplane LAN Boot ROM           [Disabled]
PCI Express Link Width Setting    [BP Strapping]

IRQ3                            [Available]
IRQ4                            [Available]
IRQ5                            [Available]
IRQ6                            [Available]
IRQ7                            [Available]
IRQ9                            [Available]
IRQ10                           [Available]
IRQ11                           [Available]
IRQ14                           [Available]
IRQ15                           [Available]      ←→   Select Screen
                                                 ↑↓   Select Item
DMA Channel 0                   [Available]      +-   Change Option
DMA Channel 1                   [Available]      F1   General Help
DMA Channel 3                   [Available]      F10  Save and Exit
DMA Channel 5                   [Available]      ESC  Exit
DMA Channel 6                   [Available]
DMA Channel 7                   [Available]

Reserved Memory Size            [16k]
Reserved Memory Address         [C8000]

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```

PCIPnP Setup Screen

When you display the PCIPnP Setup screen, the format is similar to the sample shown above, except the screen does not display all of the options at one time. If you need to change other options, use the down arrow key to locate the appropriate option. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The values on the PCIPnP Setup screen do not necessarily reflect the values appropriate for your SHB. Refer to the explanations below for specific instructions about entering correct information.

PCIPnP Setup Options

The descriptions for the system options listed below show the values as they appear if you have not yet run PCIPnP Setup. Once values have been defined, they display each time PCIPnP Setup is run.

NOTE: Do not change the values for any PCIPnP Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Clear NVRAM

This option allows you to clear NVRAM during system boot.

The Setup screen displays the system option:

Clear NVRAM [No]

Available options are:

No
Yes

Plug & Play O/S

This option indicates whether or not the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP adapter cards which are required for system boot. An operating system which is PnP-aware detects and enables all other PnP-aware adapter cards. Set this option to **No** if the operating system (such as DOS or OS/2) does *not* use PnP.

NOTE: You *must* set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

The Setup screen displays the system option:

Plug & Play O/S [No]

Two options are available:

- Select **No** to allow AMIBIOS to configure the devices in the system.
- Select **Yes** if your system has a Plug and Play operating system and you want to allow the operating system to configure all Plug and Play (PnP) devices which are not required for bootup.

PCI Latency Timer

This option specifies the latency of all PCI devices on the PCI Local Bus. The settings are in units equal to PCI clocks.

The Setup screen displays the system option:

PCI Latency Timer [64]

Available options are:

32	160
64	192
96	224
128	248

Allocate IRQ to PCI VGA

This option allows you to assign an IRQ to a PCI VGA card if the card requests an IRQ.

The Setup screen displays the system option:

Allocate IRQ to PCI VGA [Yes]

Available options are:

Yes
No

Palette Snooping

This option, when set to **Enabled**, indicates to the PCI devices that a graphics device is installed in the system so the card will function correctly.

The Setup screen displays the system option:

Palette Snooping [Disabled]

Available options are:

Disabled
Enabled

PCI IDE BusMaster

This option specifies whether the IDE controller on the PCI Local Bus has bus mastering capability for reading and writing to IDE drives. The IDE drive(s) must support PCI bus mastering.

The Setup screen displays the system option:

PCI IDE BusMaster [Disabled]

Available options are:

Disabled
Enabled

OffBoard PCI/ISA IDE Card

This option specifies the PCI expansion slot on the SHB where the off-board PCI IDE controller is installed, if any.

The Setup screen displays the system option:

OffBoard PCI/ISA IDE Card [Auto]

Available options are:

Auto
PCI Slot1
PCI Slot2
PCI Slot3
PCI Slot4
PCI Slot5
PCI Slot6

If you select any value other than **Auto**, the following options and their default values are added to the screen:

Onboard VGA Controller

When Enabled this setting instructs the SHB to use the on-board VGA controller to display video. Disabling the on-board VGA controller assumes that the system is using an external video card or is a system without the need of a video display during normal operations. The **OnBd VGA Controller Mode** allows the on-board video controller to act as either the primary or secondary provider of video when an off-board video card is found in the system. This option is not available if the **Onboard VGA Controller** is set to **Disable**.

The **Backplane LAN Boot ROM** setting is set to **Enable** when the option ROM for the backplane LAN is needed by the system.

The Setup screen displays the system options:

OnBoard VGA Controller [Enabled]

Available options are:

Disabled
Enabled

The Setup screen displays the system options:

OnBd VGA Controller mode [Primary]

Available options are:

Primary
Secondary

This option is not available if the **Onboard VGA Controller** is set to **Disable**.

The Setup screen displays the system options:

Backplane LAN Boot ROM [Disabled]

Available options are:

Disabled
Enabled

NOTE: When the setting for this option has been changed and saved, the system should be powered down and powered up in order for the new setting to take effect.

PCI Express Link Width Setting

This option, when set to **Auto**, instructs the SHB to configure the PCI Express links to the backplane slots or devices using auto-negotiation. When the option is set to **BP Strapping** the SHB will read the PCI Express link straps on the backplane and configure the PCI Express links accordingly. Trenton recommends using the **BP Strapping** option setting, which implies that the PICMG 1.3 backplane used with the SHB complies to the PICMG 1.3 specification requirements for PCI Express link strap implementations.

The Setup screen displays the system option:

PCI Express Link Width Setting [BP Strapping]

Available options are:

BP Strapping
Auto

IRQ3/IRQ4/IRQ5/IRQ7/IRQ9/IRQ10/IRQ11/IRQ14/IRQ15

These options indicate whether the specified interrupt request (IRQ) is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices. This allows you to specify IRQs for use by legacy adapter cards.

The IRQ setup options indicate whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices.

The Setup screen displays the system option:

IRQ# [Available]

where # is the number of the interrupt request (IRQ)

Two options are available:

- Select **Available** to make the specified IRQ available for use by PCI/PnP devices.
- Select **Reserved** to reserve the specified IRQ for use by legacy devices.

DMA Channels 0, 1, 3, 5, 6 and 7

These options indicate whether the specified DMA channel is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices.

The Setup screen displays the system option:

DMA Channel # [Available]

where # is the DMA Channel number

Two options are available:

- **Available** indicates that the specified DMA channel is available for use by PCI/PnP devices.
- **Reserved** indicates the specified DMA channel is reserved for use by legacy devices.

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy devices.

If this option is set to **Disabled**, the **Reserved Memory Address** option is not available.

The Setup screen displays the system option:

Reserved Memory Size [Disabled]

Available options are:

Disabled
16k
32k
64k

Reserved Memory Address

This option specifies the beginning address (in hexadecimal) of the ROM memory area reserved for use by legacy devices.

If the **Reserved Memory Size** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Reserved Memory Address [C8000]

Available options are:

C0000	D0000
C4000	D4000
C8000	D8000
CC000	DC000

Saving and Exiting

When you have made all desired changes to **PCIPnP** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

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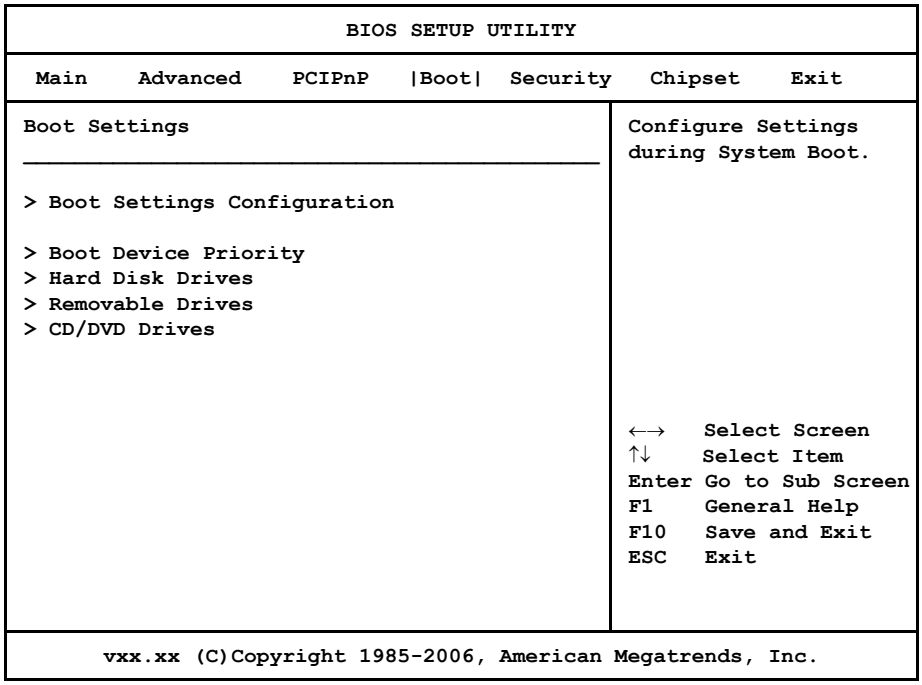
Chapter 6 Boot Setup

BOOT SETUP

When you select **Boot** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Boot Setup Screen

When you display the Boot Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Boot Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: If no device is found for one of the device types, the line item for that device type does not display.

BOOT SETUP OPTIONS

The descriptions for the system option listed below show the values as they appear if you have not yet run Boot Setup. Once values have been changed, they display each time Boot Setup is run. You may also continue to subscreens to specify boot parameters and the boot sequence of bootable devices in your system.

Boot Settings Configuration

The options on the **Boot Settings Configuration** subscreen allow you to set up or modify parameters for boot procedures. The following options may be modified:

- Quick Boot
- Quiet Boot
- AddOn ROM Display Mode
- Bootup Num-Lock
- PS/2 Mouse Support
- Wait For 'F1' If Error
- Hit 'DEL' Message Display
- Interrupt 19 Capture

Boot Device Priority

The options on the **Boot Device Priority** subscreen specify the order in which AMIBIOS attempts to boot devices available in the system. It allows you to select the drive which will be booted first, second, third, etc.

Hard Disk Drives

The **Hard Disk Drives** subscreen specifies the boot sequence of the hard drives available in the system.

Removable Drives

The **Removable Drives** subscreen specifies the boot sequence of the removable devices available in the system.

CD/DVD Drives

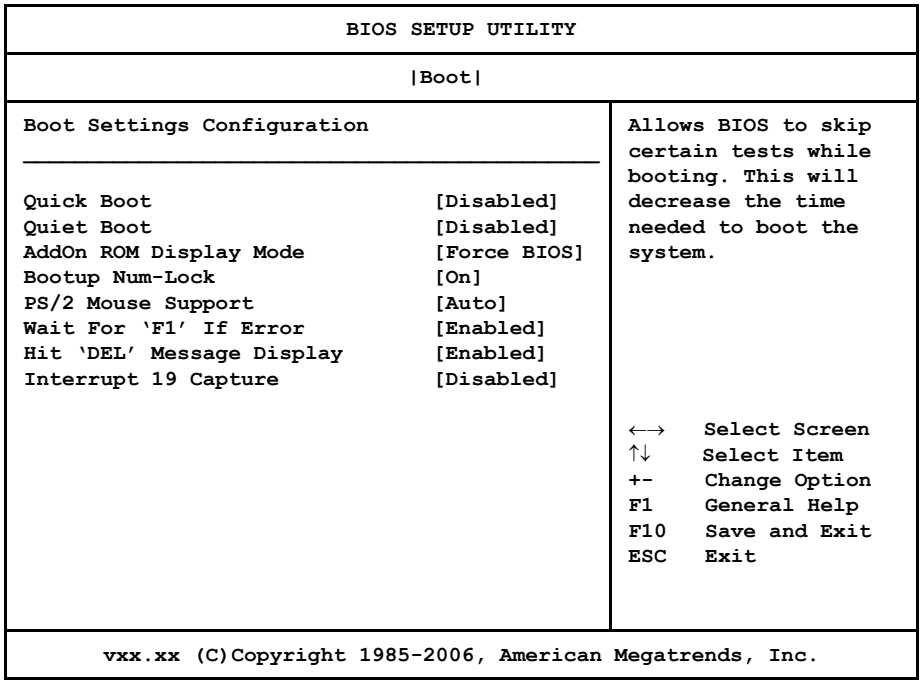
The **CD/DVD Drives** subscreen specifies the boot sequence of the CDROM and DVD devices available in the system.

Saving and Exiting

When you have made all desired changes to **Boot** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

BOOT SETTINGS CONFIGURATION

When you select **Boot Settings Configuration** from the Boot Setup Menu, the following Setup screen displays:



Boot Settings Configuration Screen

When you display the Boot Settings Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

BOOT SETTINGS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Quick Boot

This option allows you to have the AMIBIOS boot quickly when the computer is powered on or go through more complete testing. If you set the **Quick Boot** option to **Enabled**, the BIOS skips certain tests while booting and decreases the time needed to boot the system.

The Setup screen displays the system option:

Quick Boot **[Disabled]**

Available options are:

Disabled
Enabled

Quiet Boot

This option specifies what will be displayed on the screen while the system is performing the POST routines when the computer is powered on or a soft reboot is performed.

The Setup screen displays the system option:

Quiet Boot [Disabled]

Two options are available:

- Select **Disabled** to display normal POST messages.
- Select **Enabled** to display the OEM logo instead of the POST messages.

AddOn ROM Display Mode

This option specifies the system display mode which is set at the time the AMIBIOS post routines initialize an optional option ROM.

The Setup screen displays the system option:

AddOn ROM Display Mode [Force BIOS]

Two options are available:

- Select **Force BIOS** to use the display mode currently being used by AMIBIOS.
- Select **Keep Current** to use the current display mode.

BootUp Num-Lock

This option enables you to turn off the Num-Lock option on the enhanced keyboard when the system is powered on. If Num-Lock is turned off, the arrow keys on the numeric keypad can be used, as well as the other set of arrow keys on the enhanced keyboard.

The Setup screen displays the system option:

BootUp Num-Lock [On]

Available options are:

Off
On

PS/2 Mouse Support

This option indicates whether or not a PS/2-type mouse is supported.

The Setup screen displays the system option:

PS/2 Mouse Support [Auto]

Available options are:

Disabled
Enabled
Auto

Wait For 'F1' If Error

Before the system boots up, the AMIBIOS executes the Power-On Self Test (POST) routines, a series of system diagnostic routines. If any of these tests fail but the system can still function, a non-fatal error has occurred. The AMIBIOS responds with an appropriate error message followed by:

Press F1 to RESUME

If this option is set to **Disabled**, a non-fatal error does not generate the "Press F1 to RESUME" message. The AMIBIOS still displays the appropriate message, but continues the booting process without waiting for the **<F1>** key to be pressed. This eliminates the need for any user response to a non-fatal error condition message. Non-fatal error messages are listed in *Appendix A - BIOS Messages*.

The Setup screen displays the system option:

Wait For 'F1' If Error [Enabled]

Available options are:

Disabled
Enabled

Hit 'DEL' Message Display

The "Hit DEL to run Setup" message displays when the system boots up. Disabling this option prevents the message from displaying.

The Setup screen displays the system option:

Hit 'DEL' Message Display [Enabled]

Available options are:

Disabled
Enabled

Interrupt 19 Capture

This option allows option ROMs to trap Interrupt 19.

The Setup screen displays the system option:

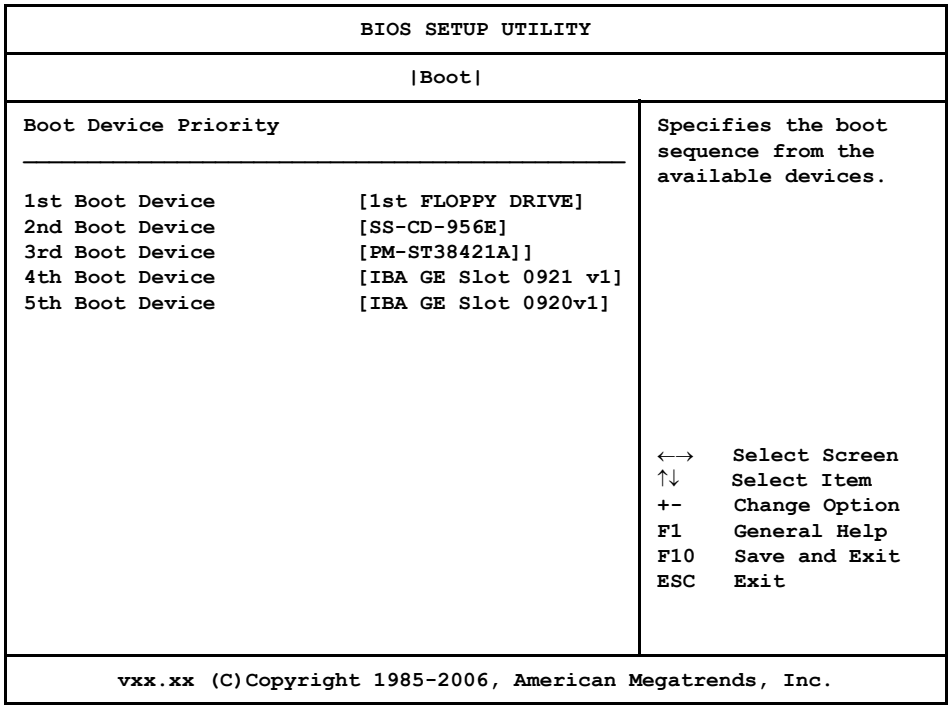
Interrupt 19 Capture [Disabled]

Available options are:

Disabled
Enabled

BOOT DEVICE PRIORITY

When you select **Boot Device Priority** from the Boot Setup Menu, a Setup screen similar to the following displays:



Boot Device Priority Screen

When you display the Boot Device Priority screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen may vary depending on the number of bootable devices available on your system.

BOOT DEVICE PRIORITY OPTIONS

1st Boot Device through Nth Boot Device

These options specify the order in which AMIBIOS attempts to boot the devices after the POST routines complete. The setting for each boot device line item is the description of the bootable device. The number of line items on this screen is dynamic. If new system devices are added, the new devices are displayed at the end of the list as additional line items.

The SHB supports bootup from a LAN device. In the sample screen above, the 4th Boot Device and 5th Boot Device line items are boot from LAN options.

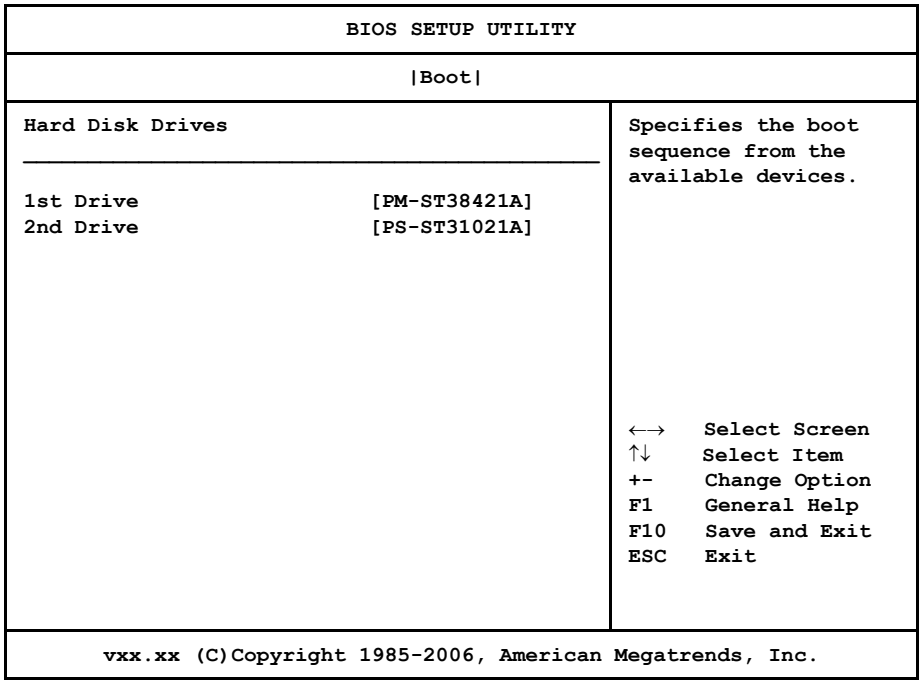
The Setup screen displays the system option(s):

Boot Device [xxxxxxxxx]

where ### is the boot order and xxxxxxxxx is the description of the device.

NOTE: Disabled is also available as an option if you do not want a particular device to be included in the boot sequence. Setting a device to **Disabled** will eliminate unnecessary delays during the bootup process.

HARD DISK DRIVES When you select **Hard Disk Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:



Hard Disk Drives Screen

When you display the Hard Disk Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen is determined by the number of hard disk drives available.

HARD DISK DRIVES OPTIONS The SHB supports up to eight hard disk drives by means of the board's SATA controller and the primary and secondary IDE controller in a master/slave configuration.

1st Drive/2nd Drive

When the system boots up, it searches for all hard drives and displays the description of each disk drive it has detected.

If you have more than one hard disk drive, you may change the order in which the system will attempt to boot the available hard drives by changing these line items. The number of options displayed for each line item depends on the number of hard disk drives in your system.

Disabled is also available as an option if you do not want a particular drive to be included in the boot sequence.

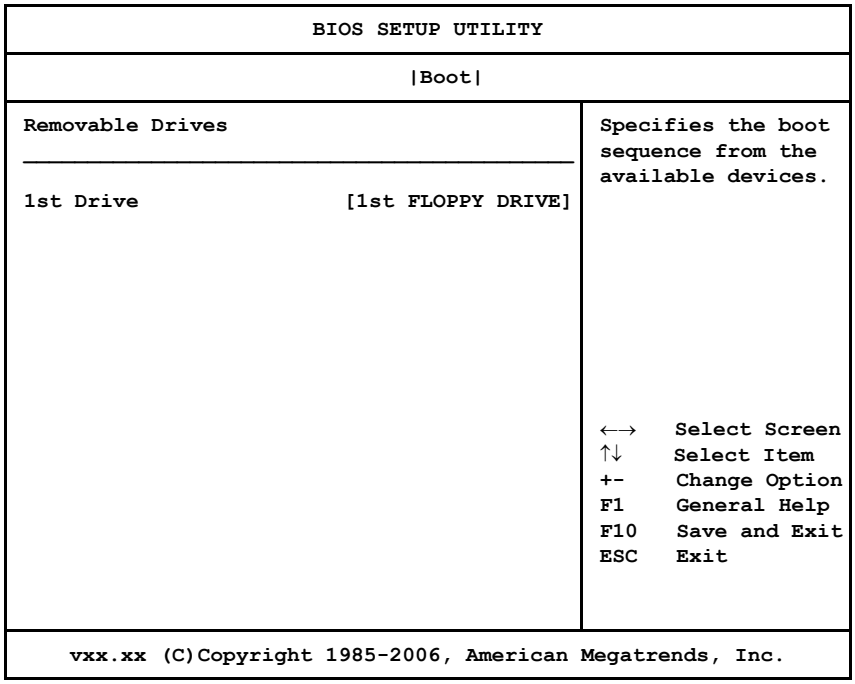
The Setup screen displays the system option(s):

Drive [xxxxxxxxx]

where ### is the boot order and xxxxxxxxx is the description of the hard disk drive.

REMOVABLE DRIVES

When you select **Removable Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:



Removable Drives Screen

When you display the Removable Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen is determined by the number of removable devices available. This menu option is only available if a removable drive has been detected.

REMOVABLE DRIVES OPTIONS

The SHB and the optional IOB30MC and IOB31 modules support multiple removable drives and allows you to change the boot sequence of these devices.

1st Drive/2nd Drive

When the system boots up, it searches for all removable devices and displays the description of each device it has detected.

If you have more than one removable device, you may change the order in which the system will attempt to boot the available devices by changing these line items. The number of options displayed for each line item depends on the number of removable devices in your system.

Disabled is also available as an option if you do not want a particular device to be included in the boot sequence.

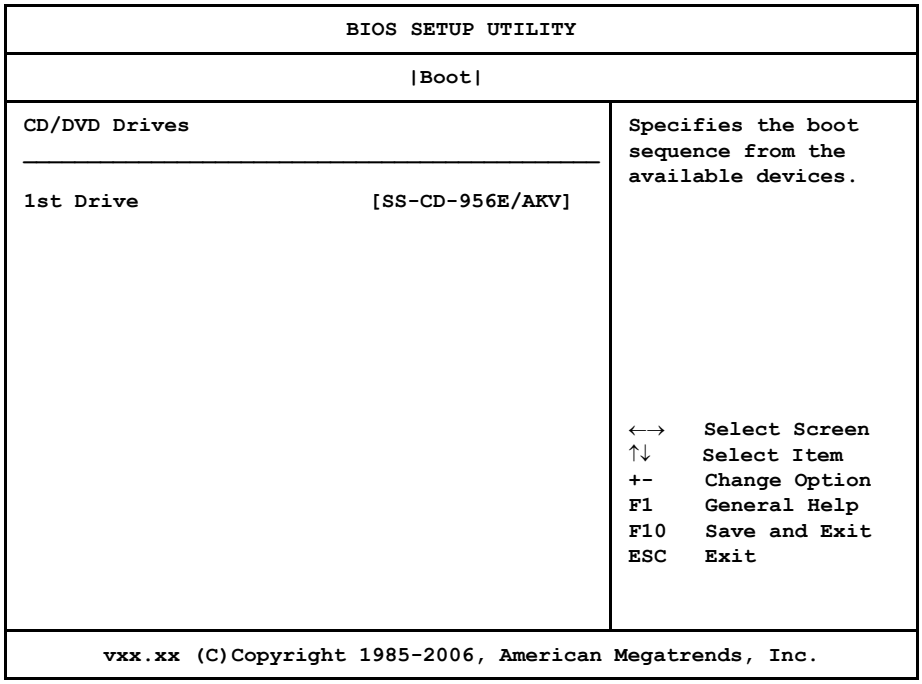
The Setup screen displays the system option(s):

Drive [xxxxxxxxx]

where ### is the boot order and xxxxxxxxx is the description of the removable drive.

CD/DVD DRIVES

When you select **CD/DVD Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:



CD/DVD Drives Screen

When you display the CD/DVD Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen is determined by the number of CDROM and DVD drives available. This menu option is only available if a CD/DVD drive has been detected.

CD/DVD DRIVES OPTIONS

The SHB supports multiple CDROM and DVD devices and allows you to change the boot sequence of these devices.

1st Drive/2nd Drive

When the system boots up, it searches for all CDROM and DVD drives and displays the description of each drive it has detected.

If you have more than one ATAPI CDROM drive, you may change the order in which the system will attempt to boot the available drives by changing these line items. The number of options displayed for each line item depends on the number of CDROM and DVD devices in your system.

Disabled is also available as an option if you do not want a particular drive to be included in the boot sequence.

The Setup screen displays the system option:

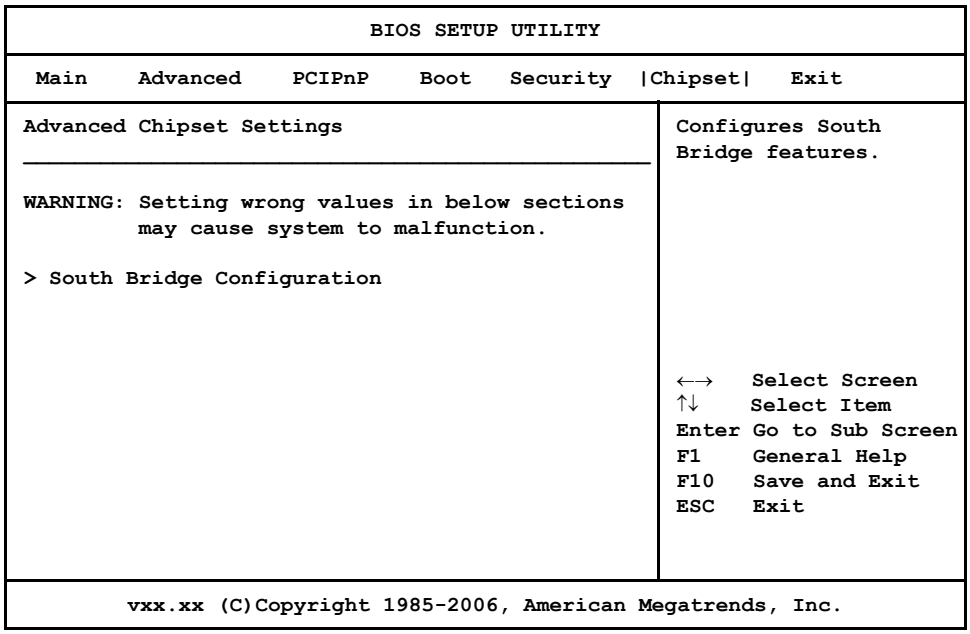
Drive [xxxxxxxxx]

where ### is the boot order and xxxxxxxxx is the description of the CDROM or DVD drive.

Chapter 7 Chipset Setup

CHIPSET SETUP

When you select **Chipset** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Chipset Setup Screen

When you display the Chipset Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Chipset Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: The values on the Chipset Setup subscreens do not necessarily reflect the values appropriate for your SHB. Refer to the explanations following the screens for specific instructions about entering correct information.

CHIPSET SETUP OPTIONS

NOTE: Do *not* change the values for any Chipset Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

South Bridge Configuration

The options on the **South Bridge Configuration** subscreen allow you to set up or modify parameters to configure the Intel® South Bridge chip. The following options may be modified:

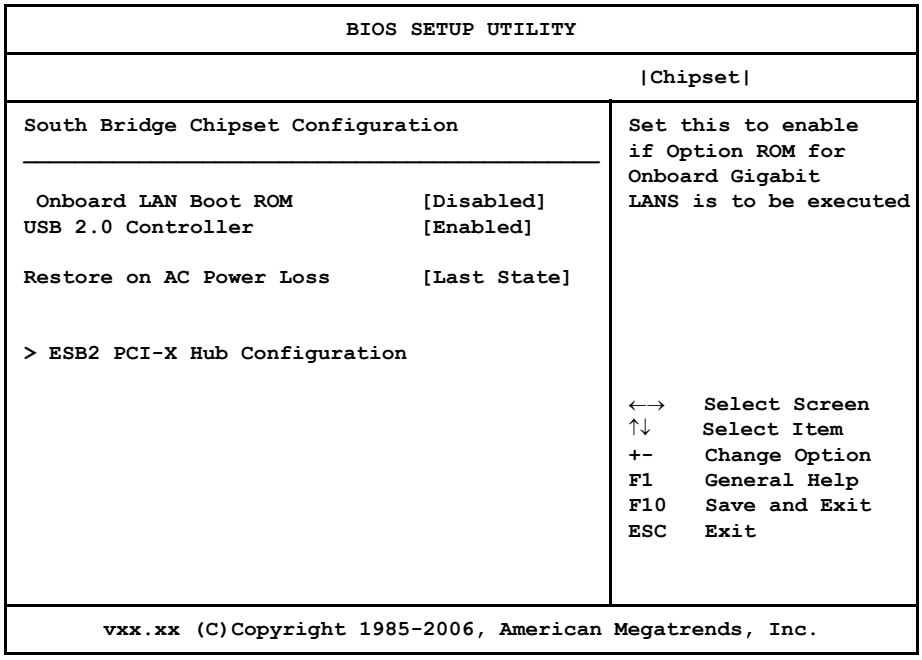
- Onboard LAN Boot ROM
- USB 2.0 Controller
- Restore on AC Power Loss
- ESB2 PCI-X Hub Configuration
    - PCI Bus Frequency
    - I/O Port Decode
    - RAS Sticky Error Handling
    - VGA 16-Bit Decode

Saving and Exiting

When you have made all desired changes to **Chipset** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

SOUTH BRIDGE CONFIGURATION

When you select **South Bridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:



South Bridge Configuration Screen

When you display the South Bridge Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

SOUTH BRIDGE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

Onboard LAN Boot ROM

When this option is enabled, the system will have the ability to boot from either one of the SHB's on-board Ethernet ports.

The Setup screen displays the system option:

Onboard LAN Boot ROM [Disabled]

Available options are:

Disabled
Enabled

USB 2.0 Controller

Enable the SHB's USB 2.0 controller to make the USB ports available for use by the system.

The Setup screen displays the system option:

USB 2.0 Controller [Enabled]

Available options are:

Enabled
Disabled

Restore on AC Power Loss

This option specifies the state the system should return to when power is restored after AC power is lost.

The Setup screen displays the system option:

Restore on AC Power Loss [Last State]

Three options are available:

- Select **Power Off** to have the system remain off until it is powered back on via a soft power-on, i.e., by pressing and releasing the power button.
- Select **Power On** to have the system turn the power back on automatically if AC power becomes active again.
- Select **Last State** to return the system to the state it was in (power on or off) when AC power was lost.

ESB2 PCI-X HUB CONFIGURATION

When you select **ESB2 PCI-X Hub Configuration** from the South Bridge Chipset Setup Screen, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
                                                          |Chipset|
Configure advanced settings for ESB2 PCI-X Hub  | This question will
________________________________________________| allow the selection of
                                                | the maximum PCI bus
PCI Bus Frequency              [Auto]           | speed to be
I/O Port Decode                [4K Decode]      | programmed. Default
RAS Sticky Error Handling      [Clear Errors]   | will always be set to
VGA 16-bit Decode              [Enabled]        | AUTO, where bus speed
                                                | will be decided based
                                                | on the capabilities of
                                                | the device on that
                                                | bus.
                                                |
                                                |
                                                | ←→   Select Screen
                                                | ↑↓   Select Item
                                                | +-   Change Option
                                                | F1   General Help
                                                | F10  Save and Exit
                                                | ESC  Exit
      vxx.xx (C)Copyright 1985-2006, American Megatrends, Inc.
```

ESB2 PCI-X Hub Configuration Screen

When you display the ESB2 PCI-X Hub Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

ESB2 PCI-X HUB CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear on the sample screen shown above.

PCI Bus Frequency

This option defines how the SHB's BIOS programs the maximum PCI bus speed. The **Auto** option enables the SHB's BIOS to determine the maximum PCI bus speed based of the device connected on the bus and program the bus speed accordingly. Trenton recommends using the **Auto** setting option for **PCI Bus Frequency**.

The Setup screen displays the system option:

PCI Bus Frequency [Auto]

Available options are:

Auto
33MHz PCI
66MHz PCI
66 MHz PCI-X M1
100 MHz PCI-X M1
133 MHz PCI-X M1
66 MHz PCI-X M2
100 MHz PCI-X M2
133 MHz PCI-X M2

I/O Port Decode

An I/O port decode range of either 4K or 1K is available for selection.

The Setup screen displays the system option:

I/O Port Decode [4K Decode]

Available options are:

4K Decode
1K Decode

RAS Sticky Error Handling

The BIOS checks for RAS sticky errors by periodically testing the SHB's system memory. The BIOS can either leave the errors for future analysis or clear the errors upon detection.

The Setup screen displays the system option:

RAS Sticky Error Handling [Clear Errors]

Available options are:

Clear Errors
Leave Errors

VGA 16-Bit Decode

This option enables the decoding of VGA devices that may exist on an option card in a card slot located behind a backplane's bridge chip.

The Setup screen displays the system option:

VGA 16-Bit Decode [Enabled]

Available options are:
Enabled
Disabled

Appendix A BIOS Messages

BIOS BEEP CODES

Errors may occur during the POST (Power-On Self Test) routines which are performed each time the system is powered on.

Non-fatal errors are those which, in most cases, allow the system to continue the bootup process. The error message normally appears on the screen. See *BIOS Error Messages* later in this section for descriptions of these messages.

Fatal errors are those which will not allow the system to continue the bootup procedure.

These fatal errors are usually communicated through a series of audible beeps. Each error message has its own specific beep code, defined by the number of beeps following the error detection. The following table lists the errors which are communicated audibly.

Beep Count	Description
1	Memory refresh timer error
2	Parity Error
3	Main memory read/write test error
4	Timer not operational
5	Processor error
6	Keyboard controller BAT test error
7	General exception error
8	Display memory error
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

BIOS BEEP CODE TROUBLESHOOTING

Beep Count	Troubleshooting Action
1, 2 or 3	Reseat the memory or replace with known good modules.
4-7, 9-11	Fatal error. Perform the following steps before calling Technical Support.
	Remove all expansion cards and try to reboot. If the beep code is still generated, call Technical Support. If the beep code is not generated, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem recurs. This will indicate the malfunctioning card.
8	The board may be faulty. Call Technical Support.

BIOS ERROR MESSAGES

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press F1 to Resume

Note the error message and press the **<F1>** key to continue with the bootup procedure.

NOTE: If the **Wait for 'F1' If Any Error** option in the Advanced Setup portion of the BIOS Setup Program has been set to **Disabled**, the "Press F1 to Resume" prompt will not appear on the last line. The bootup procedure will continue without waiting for operator response.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing an ERROR Message Line 2, the text will be "RUN SETUP UTILITY." Pressing the **<F1>** key will invoke the BIOS Setup Utility.

A description of each error message appears below.

MEMORY ERRORS

Message	Description
Gate20 Error	The BIOS is unable to properly control the SBC's Gate A20 function, which controls access to memory over 1MB. This may indicate a problem with the board.
Multi-Bit ECC Error	This message only occurs on systems using ECC enabled memory modules. ECC memory has the ability to correct single-bit errors that may occur from faulty memory modules. A multiple bit corruption of memory has occurred, and the ECC memory algorithm cannot correct it. This may indicate a defective memory module.
Parity Error	Fatal memory parity error. System halts after displaying this message.

BOOT ERRORS

Message	Description
Boot Failure ...	This is a generic message indicating the BIOS could not boot from a particular device. This message is usually followed by other information concerning the device.
Invalid Boot Diskette	A diskette was found in the drive, but it is not configured as a bootable diskette.
Drive Not Ready	The BIOS was unable to access the drive because it indicated it was not ready for data transfer. This is often reported by drives when no media is present.

BIOS ERROR MESSAGES (CONTINUED)

BOOT ERRORS (continued)

Message	Description
A: Drive Error	The BIOS attempted to configure the A: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive.
B: Drive Error	The BIOS attempted to configure the B: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive.
Insert BOOT diskette in A:	The BIOS attempted to boot from the A: drive, but could not find a proper boot diskette.
Reboot and Select proper Boot device or Insert Boot Media in selected Boot device	BIOS could not find a bootable device in the system and/or removable media drive does not contain media.
NO ROM BASIC	This message occurs on some systems when no bootable device can be detected.

STORAGE DEVICE ERRORS

Message	Description
The following errors are typically displayed when the BIOS is trying to detect and configure IDE/ ATAPI devices in POST.	
XXXXXX Hard Disk Error XXXXXX - ATAPI Incompatible	Messages in this format indicate that the specified device could not be properly initialized by the BIOS. Possible message are: Primary Master Hard Disk Error Primary Slave Hard Disk Error Secondary Master Hard Disk Error Secondary Slave Hard Disk Error Primary Master Drive - ATAPI Incompatible Primary Slave Drive - ATAPI Incompatible Secondary Master Drive - ATAPI Incompatible Secondary Slave Drive - ATAPI Incompatible
The following messages can be reported by an ATAPI device using the S.M.A.R.T. error reporting standard. The S.M.A.R.T. failure message may indicate the need to replace the hard disk.	
S.M.A.R.T. Capable but Command Failed	The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed.
S.M.A.R.T. Command Failed	The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed.
S.M.A.R.T. Status BAD, Backup and Replace	A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure.
S.M.A.R.T. Capable and Status BAD	A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure.

BIOS ERROR MESSAGES (CONTINUED)

VIRUS RELATED ERRORS

Message	Description
The following messages only display if Virus Detection is enabled in the BIOS Setup Utility.	
BootSector Write !!	The BIOS has detected software attempting to write to a drive's boot sector. This is flagged as possible virus activity.
VIRUS: Continue (Y/N)?	The BIOS has detected possible virus activity.

SYSTEM CONFIGURATION ERRORS

Message	Description
DMA-2 Error	Error initializing secondary DMA controller. This is a fatal error, often indicating a problem with system hardware.
DMA Controller Error	POST error while trying to initialize the DMA controller. This is a fatal error, often indicating a problem with system hardware.
Checking NVRAM..Update Failed	BIOS could not write to the NVRAM block. This message appears when the FLASH part is write-protected or if there is no FLASH part (system uses a PROM or EPROM).
Microcode Error	BIOS could not find or load the CPU Microcode Update to the processor. This message only applies to Intel processors. The message is most likely to appear when a brand new processor is installed in an SBC with an outdated BIOS. In this case, the BIOS must be updated to include the Microcode Update for the new processor.
NVRAM Checksum Bad, NVRAM Cleared	There was an error while validating the NVRAM data. This causes POST to clear the NVRAM data.
Resource Conflict	More than one system device is trying to use the same non-shareable resources (memory or I/O).
NVRAM Ignored	The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST.
NVRAM Bad	The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST due to a data error.
Static Resource Conflict	Two or more static devices are trying to use the same resource space (usually memory or I/O).
PCI I/O Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI ROM Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI IRQ Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI IRQ Routing Table Error	BIOS POST (DIM code) found a PCI device in the system but was unable to figure out how to route an IRQ to the device. Usually this error is caused by an incomplete description of the PCI Interrupt Routine of the system.

BIOS ERROR MESSAGES (CONTINUED)

SYSTEM CONFIGURATION ERRORS (continued)

Message	Description
Timer Error	Indicates an error while programming the count register of channel 2 of the 8254 timer. This may indicate a problem with system hardware.
Interrupt Controller-1 Error	BIOS POST could not initialize the Master Interrupt Controller. This may indicate a problem with system hardware.
Interrupt Controller-2 Error	BIOS POST could not initialize the Slave Interrupt Controller. This may indicate a problem with system hardware.

CMOS ERRORS

Message	Description
CMOS Date/Time Not Set	The CMOS Date and/or Time are invalid. This error can be resolved by readjusting the system time in the BIOS Setup Utility.
CMOS Battery Low	CMOS Battery is low. This message usually indicates that the CMOS battery needs to be replaced. It could also appear when the user intentionally discharges the CMOS battery.
CMOS Settings Wrong	CMOS settings are invalid. This error can be resolved by using the BIOS Setup Utility.
CMOS Checksum Bad	CMOS contents failed the Checksum check. Indicates that the CMOS data has been changed by a program other than the BIOS or that the CMOS is not retaining its data due to malfunction. This error can typically be resolved by using the BIOS Setup Utility.

MISCELLANEOUS ERRORS

Message	Description
Keyboard Error	Keyboard is not present or the hardware is not responding when the keyboard controller is initialized.
Keyboard/Interface Error	Keyboard Controller failure. This may indicate a problem with system hardware.
System Halted	The system has been halted. A reset or power cycle is required to reboot the machine. This message appears after a fatal error has been detected.

BOOTBLOCK INITIALIZATION CODE CHECKPOINTS

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the Bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable cache before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Reenable cache. Verify that flat mode is enabled.
D4	Test base 512K memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See the *Bootblock Recovery Code Checkpoints* section of this appendix for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copy Main BIOS into memory. Leave all RAM below 1MB Read/Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (Execute POSTKernel). See the *POST Code Checkpoints* section of this appendix for more information.

BOOTBLOCK RECOVERY CODE CHECKPOINTS

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Check-point	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
E9 or EA	Determine information about root directory of recovery media.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

POST CODE LEDS The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the MCX-series SHB. The LEDs are located below the memory banks and are numbered from right (0) to left (7). Refer to the board layouts in the *Specifications* chapter for the exact location of the POST code LEDs.

Upper Nibble (UN)				
Hex. Value	LED 7	LED 6	LED 5	LED 4
0	Off	Off	Off	Off
1	Off	Off	Off	**On**
2	Off	Off	**On**	Off
3	Off	Off	**On**	**On**
4	Off	**On**	Off	Off
5	Off	**On**	Off	**On**
6	Off	**On**	**On**	Off
7	Off	**On**	**On**	**On**
8	**On**	Off	Off	Off
9	**On**	Off	Off	**On**
A	**On**	Off	**On**	Off
B	**On**	Off	**On**	**On**
C	**On**	**On**	Off	Off
D	**On**	**On**	Off	**On**
E	**On**	**On**	**On**	Off
F	**On**	**On**	**On**	**On**

Lower Nibble (LN)				
Hex. Value	LED 3	LED 2	LED 1	LED 0
0	Off	Off	Off	Off
1	Off	Off	Off	**On**
2	Off	Off	**On**	Off
3	Off	Off	**On**	**On**
4	Off	**On**	Off	Off
5	Off	**On**	Off	**On**
6	Off	**On**	**On**	Off
7	Off	**On**	**On**	**On**
8	**On**	Off	Off	Off
9	**On**	Off	Off	**On**
A	**On**	Off	**On**	Off
B	**On**	Off	**On**	**On**
C	**On**	**On**	Off	Off
D	**On**	**On**	Off	**On**
E	**On**	**On**	**On**	Off
F	**On**	**On**	**On**	**On**

POST CODE CHECKPOINTS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The table below describes the type of checkpoints that may occur during the POST portion of the BIOS. Refer to the chart in the previous section to interpret the hexadecimal values of POST code LEDs 0 through 7.

Check-point	Description
03	Disable NMI, parity, video for EGA and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialize CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables that are based on CMOS setup questions. Initialize both the 8259 compatible PICs in the system.
05	Initialize the interrupt controlling hardware (generally OPIC) and interrupt vector table.
06	Do read/write test to CH-2 count register. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initialize the processor. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after auto detection of keyboard/mouse using AMI KB-5.
0A	Initialize the 8042 compatible keyboard controller.
0B	Detect the presence of PS/2 mouse.
0C	Detect the presence of keyboard in KBC port.
0E	Testing and initialization of different input devices. Also, update the Kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo and silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initialize different devices through DIM. See *DIM Code Checkpoints* section of this appendix for more information.
2C	Initialize different devices. Detects and initializes the video adapter installed in the system.
2E	Initialize all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initialize the silent boot module. Set the window for displaying text information.
37	Display sign-on message, processor information, setup key message and any OEM specific information.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
38	Initialize different devices through DIM. See *DIM Code Checkpoints* section of this appendix for more information.
39	Initialize DMAC-1 and DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (parallel ports, serial ports and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDA, etc.
50	Program the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initialize NUM-LOCK status and program the keyboard Typematic rate.
75	Initialize INT13 and prepare for IPL detection.
78	Initialize IPL devices controlled by BIOS and option ROMs.
7A	Initialize remaining option ROMs.
7C	Generate and write contents of ESCD in NVRAM.
84	Log errors encountered during POST.
85	Display errors to the user and get the user response for error.
87	Execute BIOS setup if needed/requested.
8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/disable NMI as selected.
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh.
	Initialize the Microsoft IRQ Routing Table. Prepare the runtime language module. Disable the system configuration display if needed.
A4	Initialize runtime language module.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
A7	Display system configuration screen if enabled. Initialize the processor before boot, which includes the programming of the MTRRs.
A8	Prepare processor for OS boot, including final MTRR values.
A9	Wait for user input at configuration display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitialize the ADM module.
AB	Prepare BBS for INT19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Pass control to OS Loader (typically INT19h)

DIM CODE CHECKPOINTS

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different buses. The following table describes the main checkpoints where the DIM module is accessed:

Check-point	Description
2A	Initialize different buses and perform the following functions: Reset, Detect and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices and PnP ISA cards. It also assigns PCI Bus numbers. Function 1 initializes all static devices, which include manually configured on-board peripherals, memory and I/O decode windows in PCI-to-PCI bridges and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI or AGP video drivers.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all on-board peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

ADDITIONAL CHECKPOINTS

While control is in the different functions, additional checkpoints are output to Port 80H as word values to identify the routines being executed.

The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two sets of information. The details of the high byte of these checkpoints are detailed in the following table:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0	Function 0. Disable all devices on the bus.
1	Function 1. Initialize static devices on the bus.
2	Function 2. Initialize output devices on the bus.
3	Function 3. Initialize input devices on the bus.
4	Function 4. Initialize IPL devices on the bus.
5	Function 5. Initialize general devices on the bus.
6	Function 6. Error reporting for the bus.
7	Function 7. Initialize add-on ROMs for all buses.
8	Function 8. Initialize BBS ROMs for all buses.

The lower nibble 'Y' indicates the bus on which the different routines are being executed. 'Y' can be from 0 to 5.

0	Generic DIM (Device Initialization Manager)
1	On-board system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

Appendix B Power Connection

INTRODUCTION

The combination of new power supply technologies and the system capabilities defined in the SHB Express™ (PICMG® 1.3) specification requires a different approach to connecting system power to a PICMG 1.3 backplane and/or SHB hardware.

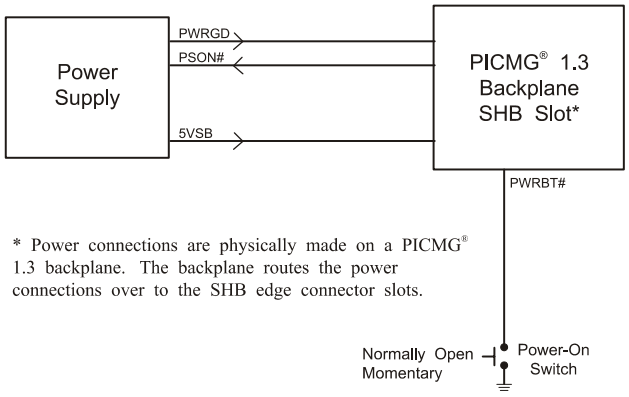
To improve system MTTR (Mean Time To Repair), the PICMG 1.3 specification defines enough power connections to the SHB's edge connectors to eliminate the need to connect auxiliary power to the SHB. All power connections in a PICMG 1.3 system can be made to the PICMG 1.3 backplane. This is true for SHBs that use high-performance processors. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive these high-performance SHBs. Trenton's PICMG 1.3 backplanes define ATX/EPS and +12V connectors that are compatible with ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in this manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

POWER SUPPLY AND SHB INTERACTION

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.



Power Supply and SHB Interaction

PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

ELECTRICAL CONNECTION CONFIGURATIONS

There are a number of different connector types, such as EPS, ATX or terminal blocks, which can be utilized in wiring power supply and control functions to a PICMG 1.3 backplane. However, there are only two basic electrical connection configurations.

ACPI Connection

The diagram on the previous page shows how to connect an ACPI compliant power supply to an ACPI enabled PICMG 1.3 system. The following table shows the required connections which must be made for soft power control to work.

Signal	Description	Source
+ 12V	DC voltage for those systems that require it	Power Supply
+ 5V	DC voltage for those systems that require it	Power Supply
+ 3.3V	DC voltage for those systems that require it	Power Supply
+ 5VSB	5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up.	Power Supply
PWRGD	Power Good. This signal indicates that the power supply's voltages are stable and within tolerance.	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply.	SHB/Backplane
PWRBT#	Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state. If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs.	Power Button

Legacy Non-ACPI Connection

For system integrators that either do not have or do not require an ACPI compliant power supply as described in the section above, an alternative electrical configuration is described in the table on the following page.

Signal	Description	Source
+ 12V	DC voltage for those systems that require it	Power Supply
+ 5V	DC voltage for those systems that require it	Power Supply
+ 3.3V	DC voltage for those systems that require it	Power Supply
+ 5VSB	Not required	Power Supply
PWRGD	Not required	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply. If an ATX or EPS power supply is used in this legacy configuration, a shunt must be installed on the backplane from PSON# to signal Ground. This forces the power supply DC outputs on whenever AC to the power supply is active.	Backplane
PWRBT#	Not used	

In addition to these connections, there is usually a switch controlling AC power input to the power supply.

When using the legacy electrical configuration, the SHB BIOS **Power Supply Shutoff** setting should be set to **Manual shutdown**. In addition to this BIOS setting; if you are using an older style AT power supply in the system, this will require you to install a shunt across the 2-pin jumper JU-13. JU-13 is located on the back of the SHB. Refer to the *General ACPI Configuration* section of the *Advanced Setup* chapter in this manual for details.

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Appendix C PCI Express™ Backplane Usage

INTRODUCTION

PCI Express™ is a scalable, full-duplex serial interface which consists of multiple communication lanes grouped into links. PCI Express scalability is achieved by grouping these links into multiple configurations. A x1 ("by 1") PCI Express link is made up of one full-duplex link that consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. A x4 configuration is made up of four PCI Express links. The most commonly used PCIe link sizes are x1, x4, x8 and x16.

PCI Express devices with different PCI Express link configurations establish communication with each other using a process called auto-negotiation or link training. For example, a PCI Express device or option card that has a x16 PCI Express interface and is placed into a x16 mechanical/x8 electrical slot on a backplane establishes communication with a PICMG® 1.3 SHB using auto-negotiation. The option card's PCI Express interface will "train down" to establish communication with the SHB via the x8 PCI Express link between the SHB and the backplane option card slot.

SHB EDGE CONNECTORS

The PICMG 1.3 specification enables SHB vendors to provide multiple PCI Express configuration options for the edge connectors A and B of a particular SHB. These edge connectors carry the PCI Express links and reference clocks down to the SHB slot on the PICMG 1.3 backplane. The potential PCI Express link configurations of an SHB fall into two main classifications: server-class and graphics-class. The specific class and PCI Express link configuration of an SHB is determined by the chipset components used on the SHB.

In a server-class configuration, the main goal of the SHB is to route as many high-bandwidth PCI Express links as possible down to the backplane. Typically, these links are a combination of x4 and x8 PCI Express links.

A graphics-class configuration should provide a x16 PCI Express link down to the backplane in order to support high-end PCI Express graphics and video cards. Graphics-class SHB configurations also provide as many lower bandwidth (x1 or x4) links as possible.

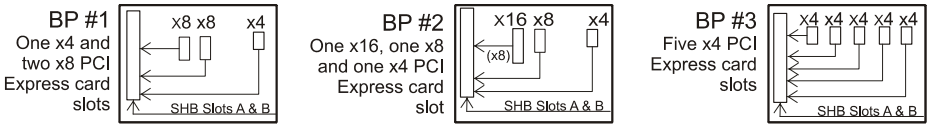
Trenton's MCX-series SHBs are server-class SHBs and have two x8 PCI Express links, one x4 PCI Express link and eight PCI Express reference clocks routed down to the backplane via edge connectors A and B. The PICMG 1.3 specification states that the SHB must provide as many reference clocks as there are potential PCI Express links on the PICMG 1.3 backplane. Each of the x8 links on an MCX-series SHB can be bifurcated into two x4 PCIe links; the single x4 PCIe link can be divided into four x1 PCIe links. The SHB also provides a x4 link to the controlled impedance connector for use with PCI Express plug-in option cards.

Server-class SHBs should be used with server-class PICMG 1.3 backplanes. Server-class SHBs are not recommended for use with graphics-class backplanes because some of the PCI Express option card slots and/or devices may not function. There may not be enough available PCI Express links and reference clocks to establish communication between all of the backplane's PCIe option card slots and the SHB. Precautions have been engineered into the PICMG 1.3 specification to prevent either SHB or backplane damage if this functionality mismatch occurs.

The figures below show some typical SHB and backplane combinations that would result in all of the PCI Express slots successfully establishing communication with the SHB host device. The first figure shows a server-class SHB; the second shows a generic graphics-class SHB.

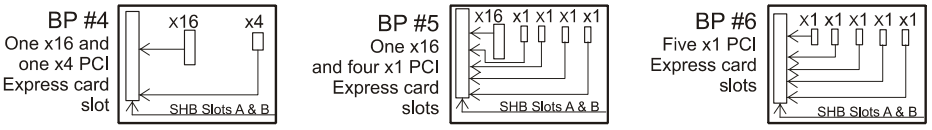
Server-Class SHB:

PCI Express™ Edge Connectors A & B: One x4 and two x8 PCI Express™ Links with five reference clocks



Graphics-Class SHB:

PCI Express™ Edge Connectors A & B: One x16 and one x4 PCI Express™ Link with five reference clocks



PCI Express link configuration straps for each PCI Express option card slot on a PICMG 1.3 backplane are required as part of the PICMG 1.3 SHB Express™ specification. These configuration straps alert the SHB as to the specific link configuration expected on each PCI Express option card slot. PCI Express communication between the SHB and option card slots is successful only when there are enough available PCI Express links established between the PICMG 1.3 SHB and each PCI Express slot or device on the backplane.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

Appendix D I/O Expansion Boards

INTRODUCTION

The IOB30MC and IOB31 are I/O expansion boards (IOBs) for legacy I/O support for PCI Express™ system host boards (SHBs).

These I/O boards connect to the impedance connector (P20) on Trenton Technology's MCX series of SHBs and provide two serial ports, mouse and keyboard ports, parallel port and floppy drive connector. The IOB31 also provides a PS/2 mouse/keyboard mini DIN connector.

In addition, the IOB31 provides a x4 PCI Express edge connector which connects to an expansion slot on a PCI Express compatible backplane.

MODELS

Model #	Model Name	Description
6391-001	IOB30MC	MC I/O Plate
6474-000	IOB31	Standard

FEATURES

- IOB30MC (6391-001):
  - I/O plate is optimized for use on an MCX-series SHB
  - Two serial ports and PS/2 mouse/keyboard mini DIN on the I/O bracket
  - PS/2 mouse, keyboard, parallel port and floppy drive connectors
- IOB31 (6474-000):
  - Two serial ports
  - PS/2 mouse, keyboard, parallel port and floppy drive connectors
  - PCI Express expansion capability for use with PCI Express backplanes
  - Compatible with PCI Industrial Computer Manufacturers Group (PICMG®) PCI Express Specification

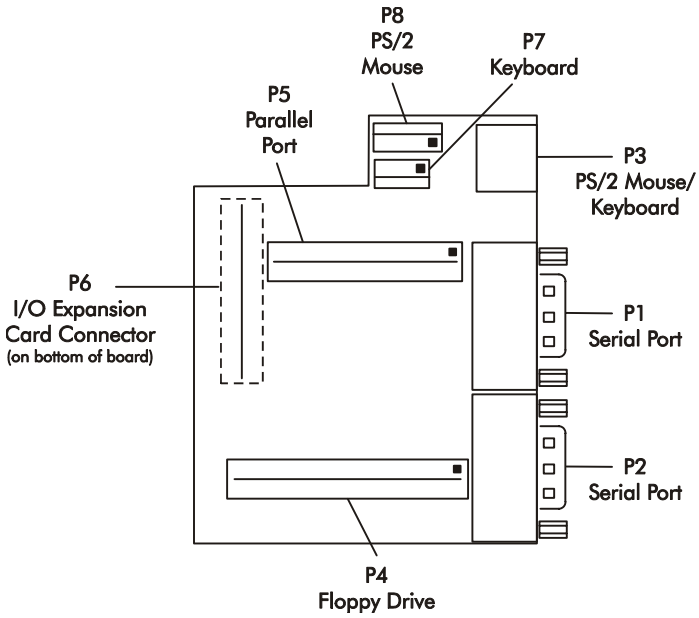
TEMPERATURE/ ENVIRONMENT

Operating Temperature: 0° C. to 60° C.

Storage Temperature: - 20° C. to 70° C.

Humidity: 5% to 90% non-condensing

IOB30MC (6391-001) I/O BOARD LAYOUT



IOB30MC CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Serial Port Connector
9 position "D" right angle, Spectrum #56-402-001

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-O	8	Clear to Send-I
4	Data Terminal Ready-O	9	Ring Indicator-I
5	Signal Gnd		

P2 - Serial Port Connector
9 position "D" right angle, Spectrum #56-402-001

Pin	Signal	Pin	Signal
1	Carrier Detect	6	Data Set Ready-I
2	Receive Data-I	7	Request to Send-O
3	Transmit Data-O	8	Clear to Send-I
4	Data Terminal Ready-O	9	Ring Indicator-I
5	Signal Gnd		

IOB30MC
CONNECTORS (CONTINUED)

P3 - PS/2 Mouse and Keyboard Connector
6 pin mini DIN, Kycon #KMDG-6S-B4T

Pin	Signal
1	Ms Data
2	Kbd Data
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P4 - Floppy Drive Connector
34 pin dual row header, Amp #103308-7

Pin	Signal	Pin	Signal
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

P5 - Parallel Port Connector
26 pin dual row header, Amp #103308-6

Pin	Signal	Pin	Signal
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

IOB30MC
CONNECTORS (CONTINUED)

P6 - Impedance Connector
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12V	2	+5V_STANDBY
3	NC	4	+5V_STANDBY
5	NC	6	+5V_DUAL
7	NC	8	+5V_DUAL
9	NC	10	NC
11	NC	12	NC
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SMBCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP4	48	C_PE_RXP4
49	C_PE_TXN4	50	C_PE_RXN4
51	Gnd	52	Gnd
53	C_PE_TXP3	54	C_PE_RXP3
55	C_PE_TXN3	56	C_PE_RXN3
57	Gnd	58	Gnd
59	C_PE_TXP2	60	C_PE_RXP2
61	C_PE_TXN2	62	C_PE_RXN2
63	Gnd	64	Gnd
65	C_PE_TXP1	66	C_PE_RXP1
67	C_PE_TXN1	68	C_PE_RXN1
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5V

IOB30MC
CONNECTORS (CONTINUED)

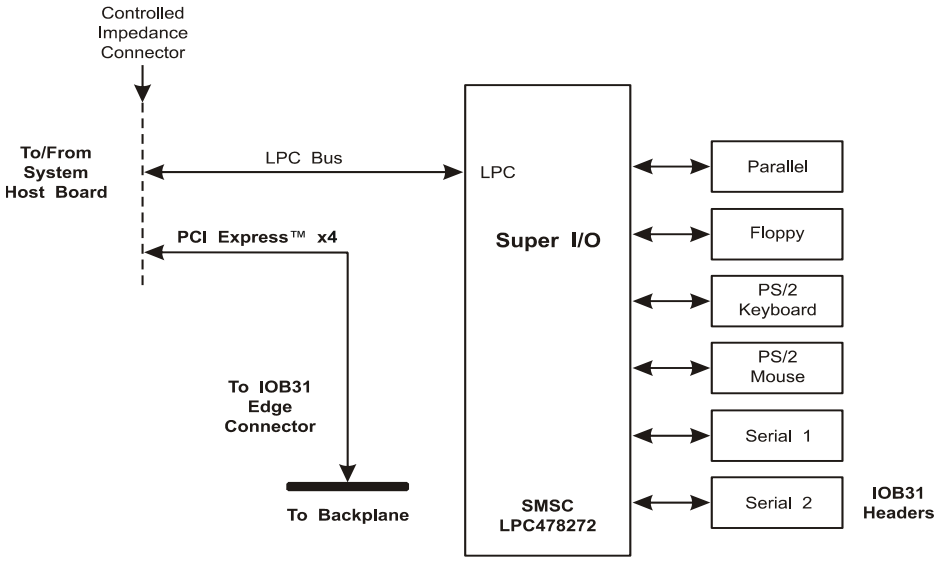
P7 - Keyboard Header
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

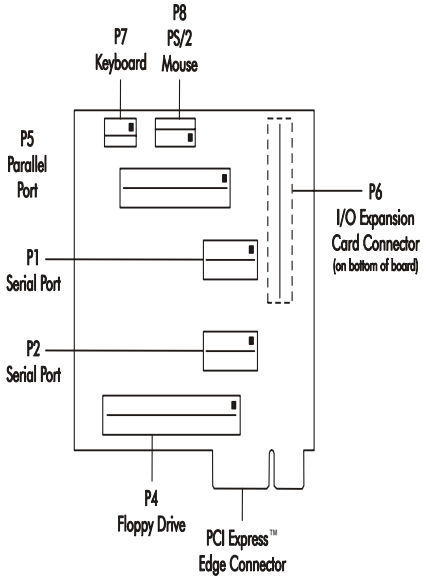
P8 - PS/2 Mouse Header
6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	Reserved
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

IOB31 (6474-000)
BLOCK DIAGRAM



IOB31 (6474-000)
I/O BOARD
LAYOUT



IOB31 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - Serial Port 1 Connector
10 pin dual row header, Amp #103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P2 - Serial Port 2 Connector
10 pin dual row header, Amp #103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P4 - Floppy Drive Connector
34 pin dual row header, Amp #103308-7

Pin	Signal	Pin	Signal
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

IOB31
CONNECTORS (CONTINUED)

P5 - Parallel Port Connector
26 pin dual row header, Amp #103308-6

Pin	Signal	Pin	Signal
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

P6 - Impedance Connector
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

Pin	Signal	Pin	Signal
1	+12V	2	+5V_STANDBY
3	NC	4	+5V_STANDBY
5	NC	6	+5V_DUAL
7	NC	8	+5V_DUAL
9	NC	10	NC
11	NC	12	NC
13	ICH_SMI#	14	ICH_RCIN#
15	ICH_SIOPME#	16	ICH_A20GATE
17	Gnd	18	Gnd
19	L_FRAME#	20	L_AD3
21	L_DRQ1#	22	L_AD2
23	L_DRQ0#	24	L_AD1
25	SERIRQ	26	L_AD0
27	Gnd	28	Gnd
29	PCLK14SIO	30	PCLK33LPC
31	Gnd	32	Gnd
33	SMBDATA_RESUME	34	IPMB_DAT
35	SMBCLK_RESUME	36	IPMB_CLK
37	SALRT#_RESUME	38	IPMB_ALRT#
39	Gnd	40	Gnd
41	EXP_CLK100	42	EXP_RESET#
43	EXP_CLK100#	44	ICH_WAKE#
45	Gnd	46	Gnd
47	C_PE_TXP4	48	C_PE_RXP4
49	C_PE_TXN4	50	C_PE_RXN4
51	Gnd	52	Gnd

IOB31

CONNECTORS (CONTINUED)

P6 - Impedance Connector (continued)

Pin	Signal	Pin	Signal
53	C_PE_TXP3	54	C_PE_RXP3
55	C_PE_TXN3	56	C_PE_RXN3
57	Gnd	58	Gnd
59	C_PE_TXP2	60	C_PE_RXP2
61	C_PE_TXN2	62	C_PE_RXN2
63	Gnd	64	Gnd
65	C_PE_TXP1	66	C_PE_RXP1
67	C_PE_TXN1	68	C_PE_RXN1
69	Gnd	70	Gnd
71	+3.3V	72	+5V
73	+3.3V	74	+5V
75	+3.3V	76	+5V

P7 - Keyboard Header

5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

P8 - PS/2 Mouse Header

6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	Reserved
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

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DECLARATION OF CE CONFORMITY

APLICATION OF COUNCIL DIRECTIVE 89/336/EEC

Standard(s) to which conformity is declared:
Emissions Test Methods per
EN55022: 2006 Class B, EN61000-3-2 :2006, EN61000-3-3 :2005
Immunity Test Methods per
EN61000-4-2:2001, EN61000-4-3 :2005, EN61000-4-4 :2006, EN61000-4-5 :2006, EN61000-4-6 :2006, EN61000-4-8 :2001, EN61000-4-11 :2004

Manufacture:	Trenton Technology, Inc 2350 Centennial Drive Gainesville, Georgia 30504-5700 USA Telephone: (770) 287-3100 Fax: (770) 287-3150
Type of Equipment:	MCX / MCG System Host Board
Model Name:	MCX 92-XX6633-XXX, 92-XX6338-XXX, 92-XX6685-XXX, 92-XX6700-XXX MCG 92-XX6680-XXX, 92-XX6675-XXX 92-XX6690-XXX, 92-XX6695-XXX
Tested By:	International Technology Company 9959 Calaveras Road, P.O. Box 543 Sunol, California 94586-0543 USA Telephone: (925) 862-2944 Fax: (952) 862-9013
Director:	Mr. Michael Gbadebo, PE

I, the undersigned, hereby declare that the specified equipment conforms to the Directive(s) and Standard(s) listed above:

Signature:	*Charles B. Hinson*
Name (printed):	Charles B. Hinson
Title:	Development Quality Assurance Manager
Date:	June 1, 2007

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