# TQ9

## 6731-xxx

**No. 87-006734-000 Revision D**

## TECHNICAL REFERENCE

**Intel® Pentium® Dual Core**

**or**

**Intel® Core™ 2 Duo**

**or**

**Intel® Core™ 2 Quad**

**or**

**Intel® Celeron®**

**PROCESSOR-BASED**

## SHB

## WARRANTY

The following is an abbreviated version of Trenton Technology's warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonTechnology.com.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Technology Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Technology's discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Technology Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Technology Inc. Trenton Technology Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

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To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

TRENTON Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

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## HANDLING PRECAUTIONS

**WARNING:** This product has components which may be damaged by electrostatic discharge.

To protect your system host board (SHB) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SHB in its static-shielded bag until you are ready to perform your installation.
- Handle the SHB by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the SHB.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

### RECOMMENDED BOARD HANDLING PRECAUTIONS

This SHB has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

# *Before You Begin*

### INTRODUCTION

It is important to be aware of the system considerations listed below before installing your TQ9 (6731-xxx) SHB. Overall system performance may be affected by incorrect usage of these features.

### PS/2 REQUIREMENTS DURING BOOT-UP

Certain operating systems require a PS/2 keyboard during boot-up. Since the SHB itself does not have a PS/2 keyboard connector, you may need Trenton's IOB30MC (6391-001) or IOB31 (6474-000) I/O board in your system to provide this functionality. Trenton has determined that an IOB30MC or IOB31 is required when using a Sun® Solaris™ 10.0 or SCO ODT 5.07 operating system. An IOB30MC or IOB31 is *not* required when using Red Hat Enterprise Linux 5.0, Fedora 7.0, SUSE Enterprise 10.0, Microsoft® Windows® Vista Business and Ultimate, Windows® XP Professional, Microsoft® Windows® 2000 Professional, and Windows® 2003 Enterprise Server operating systems. If your operating system is not included here, contact Trenton for the latest information regarding IOB30MC/IOB31 requirements.

### MOUSE/KEYBOARD "Y" CABLE

If you have an IOB30MC I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation.

### DDR2 MEMORY

The DDR2 memory modules used in the TQ9 must be non-ECC (64-bit) DDR2, unbuffered DIMMs and must be PC2-6400 compliant.

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**NOTES:**

- To maximize system performance and reliability, Trenton recommends using DIMMs that support the Serial Presence Detect (SPD) data structure.
- All memory modules must have gold contacts.
- To minimize memory channel errors regardless of the type of memory module used; Trenton recommends memory DIMMs with a memory clock cycle specification of ten (10).

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A memory module can be installed in only one DIMM socket. If only one DIMM module is used, it must be populated in either DIMM socket BKA1 or BKB1. The TQ9's memory interface operates at maximum bandwidth with two DIMMs of the same size installed in DIMM socket BKA1 and BKB1, but the DIMMs may differ in technology (i.e. component density) and/or device width. Populating identical DIMMs in all four DIMM sockets will also achieve maximum memory bandwidth operation.

### SATA RAID OPERATION

The ICH9DO I/O Controller Hub used in the TQ9 features Intel® Matrix Storage Technology, which allows the ICH9DO's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. To configure the SATA ports as RAID drives or to use advanced features of the ICH9DO, you must install the Intel® Matrix Storage Manager. A link to the software may be found on Trenton's website by accessing the RAID Drivers section of the Technical Support page.

### UNIVERSAL SERIAL BUS (USB)

The USB 2.0 specification defines two types of devices connected to a USB port: low-power and high-power devices. Low-power devices draw one unit load of 5V power and high-power devices can draw up to five unit loads. A unit load is defined as 100mA; therefore, five unit loads is equal to 500mA or .5A of 5V power for a high power USB device connected to a USB port. A USB routing hub can be considered a high-power USB device.

The 5V power circuitry on the SHB derives the USB interface power from the 5V standby voltage delivered to the SHB by the system's power supply. Many industry standard power supplies provide a maximum of around 3A of 5V standby power. If a power supply capable of delivering more than 3A of 5V standby voltage can be found, then caution must be used when using a large number of high-power USB devices. The TQ9 can provide a maximum of 3.5A of 5V power to the SHB's USB interfaces; therefore, you must limit the number of USB devices connected to the TQ9 such that total 5V standby power drain never exceeds 3.5A. Failure to observe the 3.5A limit of 5V standby power will result in board damage.

### POWER CONNECTION

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). The TQ9 supports these signals, controlled by the ACPI and are used to implement various sleep modes. When control signals are implemented, the type of ATX or EPS power supply used and the operating system software will dictate how system power should connect to the SHB. It is critical that the correct method be used. Refer to - *Power Connection* in the TQ9 manual to determine the method that will work with your specific system design. The *Advanced Setup* chapter in the manual contains the ACPI BIOS settings.

### PCI EXPRESS LINKS AND PICMG® 1.3 BACKPLANES

The PCI Express™ links on the TQ9 SHB utilizes what Trenton calls a graphics-configuration. To ensure maximum PCI Express option card slot usability on 1.3 backplanes, a graphics-class SHB should be used with a graphics-class backplane. Refer to the *PCI Express™ Reference* chapter and to *Appendix C - Backplane* the TQ9 manual for more information.

### PICMG 1.3 BACKPLANE I/O

The TQ9 enables the following PICMG 1.3 backplane I/O connectivity via the SBC's edge connector C:

- Two eSATA/300 interfaces
- Four USB 2.0 interfaces
- One 10/100Base-T Ethernet interface

### PICMG 1.3 BACKPLANE CLASSIFICATION

The TQ9 system host board is a Graphics-Class PICMG 1.3 SHB. Trenton recommends using a Graphics-Class PICMG 1.3 backplane with the TQ9 in order to ensure the use of all available backplane option card slots. The BPG6741, BPG6714, BPG6615, BPG6600, BPG6544, BPG4 and BPG2/2 are examples of Graphic-Class PICMG 1.3 backplanes available from Trenton Technology. See *Appendix C, PCI Express Backplane Usage* for more details.

### FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections *TQ9 Technical Reference Manual* (#87-006731-000). The latest revision of may be found on Trenton's website - www.TrentonTechnology.com.

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# *Chapter 1 Specifications*

## INTRODUCTION

The TQ9 is a graphics-class, PICMG® 1.3 system host board that supports a wide variety of Intel Core™ 2 processors and I/O interface capabilities. New I/O features on the TQ9 include an audio codec interface, two eSATA connections to the backplane and a dozen USB interfaces. The Intel Q35 MCH and Intel ICH9D0 ICH deliver advanced features like SATA RAID. Plugging the TQ9 into a PICMG 1.3 graphics-class backplane enhances system design flexibility. A system designed with the TQ9 supports option cards from x16 PCI Express to legacy 32-bit/33MHz PCI cards.

## MODELS

| Model # | Model Name | Speed | Intel CPU Number |
|---|---|---|---|
| **Intel Pentium Dual Core Processor – Dual Core, 800MHz FSB, 1MB cache** | | | |
| 6731-001 | TQ9/1.6D1 | 1.6GHz | E2140 |
| 6731-002 | TQ9/1.8D1 | 1.8GHz | E2160 |
| 6731-003 | TQ9/2.0D1 | 2.0GHz | E2180 |
| 6731-005 | TQ9/2.2D2 | 2.2GHz | E2200 |
| 6731-006 | TQ9/2.4D2 | 2.2GHz | E2220 |
| **Intel Core 2 Duo – Dual Core, 800MHz FSB, 2MB cache with Vllv** | | | |
| 6731-012 | TQ9/1.8DV2 | 1.8GHz | E4300 |
| 6731-013 | TQ9/2.0DV2 | 2.0GHz | E4400 |
| 6731-015 | TQ9/2.2DV2 | 2.2GHz | E4500 |
| 6731-016 | TQ9/2.4DV2 | 2.4GHz | E4600 |
| 6731-018 | TQ9/2.6DV2 | 2.6GHz | E4700 |
| **Intel Core 2 Duo – Dual Core, 1066MHz FSB, 2MB cache withVllv, Vpro** | | | |
| 6731-022 | TQ9/2.13DP2 | 2.13GHz | E6400 |
| **Intel Core 2 Duo – Dual core, 1333MHz FSB, 4MB cache with Vllv, Vpro** | | | |
| 6731-043 | TQ9/2.33DPK4 | 2.33GHz | E6550 |
| 6731-045 | TQ9/2.66DPK4 | 2.66GHz | E6750 |
| 6736-047 | TQ9/3.0DPK4 | 3.0GHz | E6850 |
| **Intel Core 2 – Dual Core, 1333MHz FSB, 6MB cache with Vllv, Vpro** | | | |
| 6731-125 | TQ9/2.66DP6 | 2.66GHz | E8200 |
| 6731-126 | TQ9/2.83DP6 | 2.83GHz | E8300 |
| 6731-129 | TQ9/3.0DP6 | 3.0GHz | E8400 |
| 6731-130 | TQ9/3.16DP6 | 3.16GHz | E8500 |
| **Intel Core 2 – Quad Core, 1066MHz FSB, 8MB cache with Vllv** | | | |
| 6731-303 | TQ9/2.4QV8 | 2.66GHz | Q6600 |
| 6731-305 | TQ9/2.66QV8 | 2.83GHz | Q6700 |
| **Intel Core 2 – Quad Core, 1333MHz FSB, 6MB cache with Vllv, Vpro** | | | |
| 6731-404 | TQ9/2.5QP6 | 2.5GHz | Q9300 |
| **Intel Core 2 – Quad Core, 1333MHz FSB, 12MB cache with Vllv, Vpro** | | | |
| 6731-425 | TQ9/2.66QP12 | 2.66GHz | Q9550 |
| 6731-426 | TQ9/2.83QP12 | 2.83GHz | Q9550 |

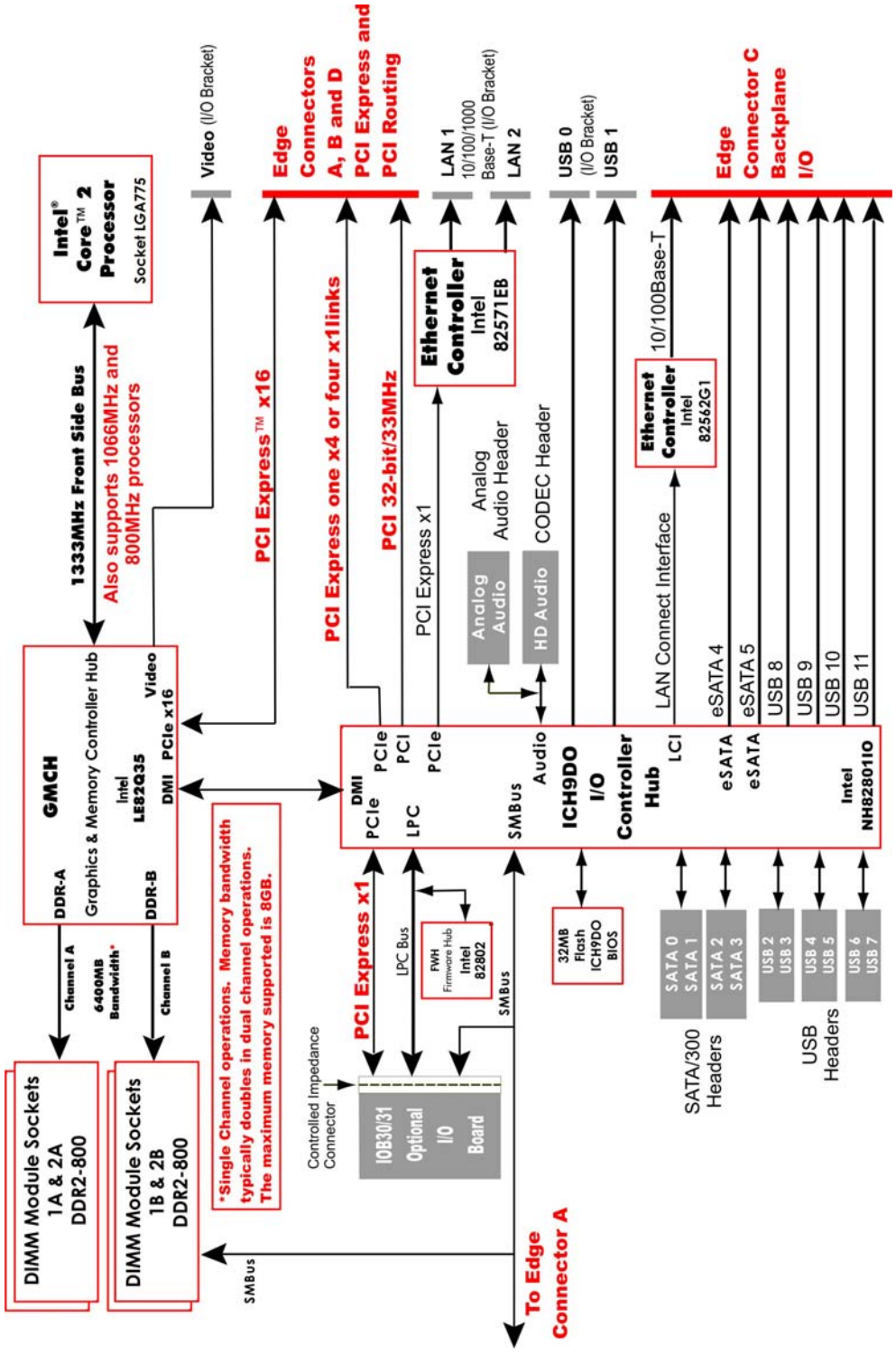
**Intel Celeron – Single Core, 800MHz FSB, 512KB cache**

| | | | |
|---|---|---|---|
| 6731-501 | TQ9/1.6SC | 1.6GHz | 420 |
| 6731-502 | TQ9/1.8SC | 1.8GHz | 430 |
| 6731-503 | TQ9/2.0SC | 2.0GHz | 440 |

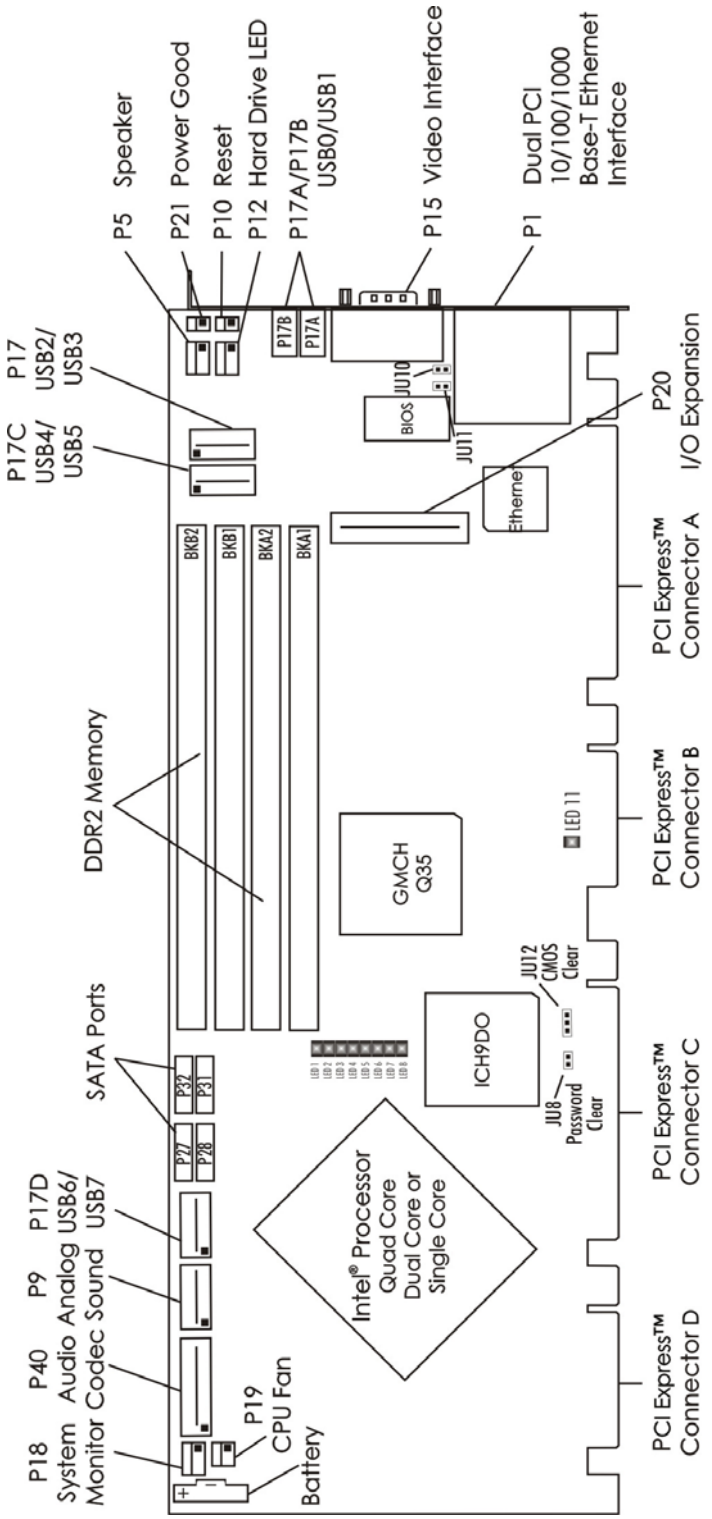
## FEATURES

- Intel Core 2, Pentium Dual Core and Celeron Processors
- Intel Q35 chipset with 800MHz, 1066MHz or 1333MHz FSB (FSB)
- PCI Local Bus operating in 32-bit/33MHz mode and PCI Express™ Bus operating in x16, x4 and x1 modes
- Video interface utilizing Intel® Graphics Media Accelerator 3100
- Dual 10/100/1000Base-T Ethernet interfaces
- Four Serial on-board ATA/300 ports support four independent SATA storage devices
    - SATA/300 ports may be configured to support RAID 0, 1, 5 or 10 implementations
- A Graphics-class SHB that is compatible with PCI Industrial Computer Manufacturers Group (PICMG) 1.3 Specifiction
- Supports up to 8GB of Double Data Rate (DDR2) on-board memory
- Universal Serial Bus (USB 2.0) interfaces
- Automatic or manual peripheral configuration
- HD audio support via CODEC header
- Analog audio support via the analog audio header
- Off-board I/O support provided for one 10/100Base-T Ethernet interface, two eSATA/300 and four USB 2.0 port connections on a PICMG 1.3 backplane
- Legacy I/O and dual serial port support via Trenton IOB30MC or IOB31 expansion boards
- An additional x1 PCI Express link to a Trenton PICMG 1.3 backplane via the IOB31 expansion board
- Full PC compatibility

## TQ9 (6713-XXX) – SHB BLOCK DIAGRAM



## TQ9 (6731-XXX) - SHB BOARD LAYOUT



#### PROCESSOR

- Intel® Core™ 2, Intel® Pentium® Dual Core or Intel® Celeron® Processor microprocessor
- Processor uses the FC-LGA4 packaging and plugs into an LGA775 socket

#### BUS INTERFACE

PCI Local Bus and PCI Express™ compatible

#### DATA PATH

DDR2 Memory - 64-bit (per channel)
PCI Bus - 32-bit

#### BUS SPEEDS

PCI - 33MHz
PCI Express - 2.5GHz per lane

#### BUS SPEED SYSTEM

1333MHz, 1066MHz or 800MHz Front Side Bus

#### MEMORY INTERFACE

Dual Double Data Rate (DDR2) memory channels; theoretical memory interface bandwidth is up to 6.4GB/s for asymmetric operation and up to 12.8GB/s for interleave mode (dual-channel) operation.

#### SYSTEM BUS

Intel® Q35 Express chipset supports the system bus at 1333MHz, 1066MHz or 800MHz, which provides a higher bandwidth path for transferring data between main memory/chipset and the processors.

#### DMA CHANNELS

The SHB is fully PC compatible with seven DMA channels, each supporting type F transfers.

#### INTERRUPTS

The SHB is fully PC compatible with interrupt steering for PCI plug and play compatibility.

#### BIOS (FLASH)

The BIOS is an AMIBIOS with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. The Flash BIOS resides in the Intel® 82802AC Firmware Hub (FWH). The BIOS may be upgraded from floppy disk by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the floppy disk in drive A:. Custom BIOSs are available.

#### CACHE MEMORY

The processor includes integrated on-die, 8-way set associative level two (L2) cache, which implements the Advanced Transfer Cache architecture and runs at the full speed of the processor core. **Intel® Pentium® Dual Core** processors are dual core and have 1Mof L2 cache. **Intel® Core™ 2 Duo** processors are dual core and have 2M, 3M, 4M and 6M of L2 cache memory. **Intel® Core 2 - Quad Core** processors are quad core and have 6M and 12M of L2 cache. **Intel® Celeron® 4xx series** processors are single core and have 512 K of L2 cache. All processors have a 16K level 1 (L1) data cache.

### DDR2 MEMORY

The Double Data Rate (DDR2) memory interface is a dual-channel interface that supports up to 8GB of memory and supports memory transfer rates of 800MHz. Each of the channels (A and B) terminates at a dual in-line memory module (DIMM) socket. The System BIOS automatically detects memory type, size and speed.

The SHB uses industry standard gold finger memory modules, which must be PC2-6400 compliant and have the following features:

- Gold-plated contacts
- Non-ECC (64-bit) DDR2 memory
- Unbuffered configuration

The following DIMM sizes are supported:

| FSB | DIMM Type | Width | Component Density |
|---|---|---|---|
| 1333 | PC2-6400 | x8, x16 | 256MB, 512MB, 1GB, 2GB |
| 1066 | PC2-6400 | x8, x16 | 256MB, 512MB, 1GB, 2GB |
| 800 | PC2-6400 | x8, x16 | 256MB, 512MB, 1GB, 2GB |
| 667 | PC2-6400 | x8, x16 | 256MB, 512MB, 1GB, 2GB |

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NOTE 1: To maximize system performance and reliability, Trenton recommends using DIMMs that support the Serial Presence Detect (SPD) data structure. All memory modules must have gold contacts.

NOTE 2: Double-sided DIMMS with a x16 organization are not supported.

NOTE 3: To minimize memory channel errors regardless of the type of memory module used; Trenton recommends memory DIMMs with a memory clock cycle specification of ten (10).

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Trenton's TQ9 supports Interleaved and Asymmetric memory operations. The mode of memory operation is determined by how the DIMMs are populated. Listed below are descriptions of the Interleaved and Asymmetric memory operations.

Interleaved Mode - This is the mode of operation that enables the highest memory interface speed and bandwidth throughput capability. Often times this mode of operation is referred to as "dual-channel mode". Interleaved mode occurs when using two or four DIMM modules with equal memory capacities. The DIMM technology and device width can vary but the installed memory capacity for each channel must be equal. If different speed DIMMs are used in each channel then the slowest DIMM will determine the memory interface speed.

Asymmetric Mode - A memory module can be installed in only one DIMM socket. If only one DIMM module is used, it must be populated in either DIMM socket BKA1 or BKB1. From a system operational standpoint, asymmetric mode functions as a "single-channel" memory interface. Asymmetric mode occurs when using either a single DIMM module or multiple DIMMs with unequal memory capacities. The DIMM technology and device width can vary in each channel and if different speed DIMMs are used in each channel then the slowest DIMM will determine the memory interface speed.

The TQ9's memory interface operates at maximum bandwidth with two DIMMs of the same size installed in DIMM socket BKA1 and BKB1, but the DIMMs may differ in technology (i.e. component density) and/or device width. Populating identical DIMMs in all four DIMM sockets will also achieve maximum memory bandwidth operation. For example, when using a single PC2-6400 DIMM, the peak memory interface bandwidth is 6.4GB/s, but placing a PC2-6400 DIMM in all four sockets or one socket in each of the two memory channels (e.g. socket BKA1 and BKB1) produces a TQ9 theoretical peak memory bandwidth of 12.8GB/s.

### BUS INTERFACES

The SHB provides a x16 PCI Express link on edge connectors A and B. This PCIe link is designed to support a wide variety of PCI Express cards on an SHB Express™ (PICMG 1.3) backplane. A x4 PCI Express link and five PCI Express reference clocks are also included on edge connectors A and B. In addition, the SHB provides a x1 link to the controlled impedance connector for use with PCI Express plug-in option cards. This additional x1 PCI Express link is routed down to a Trenton PICMG 1.3 backplane via a Trenton IOB31 module connected to the TQ9's controlled impedance connector. The x1 PCI Express link from the IOB31 can be-used to support PCI Express option cards and devices on a PICMG 1.3 backplane. Refer to the *PCI Express Reference* chapter of this manual for more information, including edge connector pin assignments. A PCI Local Bus interface is provided on edge connector D. The interface is 32 bits wide and runs at 33MHz.

### UNIVERSAL SERIAL BUS (USB)

The SHB has eight on-board high-speed USB 2.0 ports. Connectors for two of the USB ports (0 and 1) are on the I/O bracket; six ports (2, 3, 4, 5, 6 and 7) are available via headers on the SHB. USB ports 8, 9, 10 and 11 are routed directly to edge connector C of the SHB for use on a PICMG 1.3 backplane.

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**NOTE –** The USB 2.0 specification defines two types of devices connected to a USB port: low-power and high-power devices. Low-power devices draw one unit load of 5V power and high-power devices can draw up to five unit loads. A unit load is defined as 100mA; therefore, five unit loads is equal to 500mA or .5A of 5V power for a high power USB device connected to a USB port. A USB routing hub can be considered a high-power USB device.

The 5V power circuitry on the SHB derives the USB interface power from the 5V standby voltage delivered to the SHB by the system's power supply. Many industry standard power supplies provide a maximum of around 3A of 5V standby power. If a power supply capable of delivering more than 3A of 5V standby voltage can be found, then caution must be used when using a large number of high-power USB devices. The TQ9 can provide a maximum of 3.5A of 5V power to the SHB's USB interfaces; therefore, you must limit the number of USB devices connected to the TQ9 such that total 5V standby power drain never exceeds 3.5A. Failure to observe the 3.5A limit of 5V standby power will result in board damage.

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### VIDEO INTERFACE

The SHB supports three video options. The first is a direct connection via the chipset's Intel Graphics Media Accelerator 3100, which provides faster graphics and 3D performance. The second is the x16 PCI Express port that provides 3.5 times more bandwidth than an AGP 8X interface. The third option is ADD2 video and graphics cards. Software drivers are available for most popular operating systems.

### ETHERNET INTERFACES

The SHB provides two on-board Ethernet interfaces. The two 10/100/1000Base-T Ethernet interfaces located on the TQ9's I/O bracket are implemented using an Intel® 82571EB Ethernet controller with two channels. These I/O bracket interfaces support Gigabit, 10Base-T and 100Base-TX Fast Ethernet modes and are compliant with the IEEE 802.3 Specification.

The main components of the I/O bracket Ethernet interfaces are:

- Intel® 82571EB for 10/100/1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCIe interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connectors on the SHB's I/O bracket for direct connection to the network. The connectors require category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cables for a 100-Mb/s network connection or category3 (CAT3) or higher UTP 2-pair cables for a 10-Mb/s network connection. Category 5e (CAT5e) or higher UTP 2-pair cables are recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

The third LAN is supported by the ICH9DO's internal LAN Interconnect Interface (LCI). This 10/100Base-T Ethernet interface is routed to the PICMG 1.3 backplane via edge connector C of the SHB.

Software drivers are supplied for most popular operating systems.

### DMI INTERFACE

The Intel® Q35 chipset utilizes a Direct Media Interface (DMI) connection between the graphics memory controller hub (GMCH) and the I/O controller hub (ICH9DO). The purpose of the DMI interface is to provide efficient, high-speed communication between chipset components in order to support high-speed I/O applications. It is a parity-protected, 2GB/s point-to-point interface.

### SERIAL ATA/300 PORTS

The four Serial ATA (SATA) ports on the SHB comply with the SATA 1.0 specification and support four independent SATA storage devices such as hard disks and CD-RW devices. SATA produces higher performance interfacing by providing data transfer rates up to 300MB per second on each port. The ICH9DO I/O Controller Hub features Intel® Matrix Storage Technology, which allows the ICH9DO's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5 and 10 implementations. Two additional eSATA/300 interfaces are provided and are routed to the SHB's edge connector C for use on a PICMG 1.3 backplane.

### POWER FAIL DETECTION

A hardware reset is issued when any of the monitored voltages drops below its specified nominal low voltage limit. The monitored voltages and their nominal low limits are listed below.

| Monitored Voltage | Nominal Low Limit | Voltage Source |
|---|---|---|
| +12V | 9.3 volts | System Power Supply |
| +5V | 4.5 volts | System Power Supply |
| +3.3V | 2.97 volts | System Power Supply |
| vcc_ddr(+1.8V) | 1.08 volts | On-Board Regulator |
| +1.5V | 1.35 volt | On-Board Regulator |
| vtt_cpu(1.1V or 1.2V) | 75% of CPU voltage | On-Board Regulator |

### BATTERY

A built-in lithium battery is provided, for ten years of data retention for CMOS memory.

**CAUTION:** There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

### POWER REQUIREMENTS

The following are typical values:

| Processor Type | Processor Speed | +5V | +12V | +3.3V |
|---|---|---|---|---|
| **CPU Idle State:** | | | | |
| Core 2 Quad (Q9550) | 2.83GHz | 1.10A | 1.75A | 2.30A |
| Core 2 Dual ((E8400) | 3.00GHz | 1.10A | 1.25A | 2.30A |
| Core 2 Duo (E6400) | 2.13GHz | 1.10A | 1.10A | 2.30A |
| Core 2 Duo (E4300) | 1.80GHz | 1.10A | 1.00A | 2.30A |
| Celeron 440 | 2.00Ghz | 1.00A | 0.90A | 2.30A |
| **100% CPU Stress State:** | | | | |
| Core 2 Quad (Q9550) | 2.83GHz | 1.20A | 4.50A | 2.40A |
| Core 2 Dual ((E8400) | 3.00GHz | 1.20A | 3.75A | 2.40A |
| Core 2 Duo (E6400) | 2.13GHz | 1.20A | 2.10A | 2.40A |
| Core 2 Duo (E4300) | 1.80GHz | 1.20A | 2.00A | 2.40A |
| Celeron 440 | 2.00Ghz | 1.20A | 1.90A | 2.40A |

Tolerance for all voltages is +/- 5%

**CAUTION**: Trenton recommends an EPS type of power supply for systems using high-performance processors. The power needs of backplane option cards, high-performance processors and other system components may result in drawing 20A of current from the +12V power supply line. If this occurs, hazardous energy (240VA) could exist inside the system chassis. Final system/equipment suppliers must provide protection to service personnel from these potentially hazardous energy levels.

Stand-by voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

### TEMPERATURE/ENVIRONMENT

**Operating Temperature:** 0º C. to 60º C. (Celeron processors/std. cooling solution)
**Operating Temperature:** 0º C. to 50º C. (all other processors/std. cooling solution)
**Operating Temperature:** 0º C. to 55º C. (Celeron processors/low profile cooling solution)
**Operating Temperature:** 0º C. to 45º C. (all dual-core processors /low profile cooling solution)
**Operating Temperature:** 0º C. to 40º C. (all quad-core processors /low profile cooling solution)

**Storage Temperature:** - 40º C. to 70º C.

**Humidity:** 5% to 90% non-condensing

### MECHANICAL

The standard cooling solution used on the TQ9 SHBs enables placement of option cards approximately 2.48" (62.99mm) away from the top component side of the SHB. An optional lower profile cooling solution is available that allows the placement of option cards approximately 2.20" (55.88mm) away from the top component side of the SHB. The TQ9's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

### UL RECOGNITION

This SHB is a UL recognized product listed in file #E208896. This board was investigated and determined to be in compliance under the Bi-National Standard for Information Technology Equipment. This included the Electrical Business Equipment, UL 1950, Third Edition, and CAN/CSA C22.22 No. 950-95.

### CONFIGURATION JUMPERS

The setup of the configuration jumpers on the SHB is described below. * indicates the default value of each jumper.

**NOTE:** For two-position jumpers (3-post), "RIGHT" is toward the bracket end of the board; "LEFT" is toward the processor.

| Jumper | Description |
|---|---|
| **JU8** | **Password Clear**<br>Install for one power-up cycle to reset the password to the default (null password).<br>Remove for normal operation. * |
| **JU10/JU11** | **System Flash ROM Operational Modes**<br>The Flash ROM has two programmable sections: the Boot Block for "flashing" in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system. |

| | JU10 | JU11 |
|---|---|---|
| All Blocks Write Enabled | Remove * | Remove * |
| Boot Block Write Protected | Install | Remove |
| Block 2-16 Write Protected | Remove | Install |

| | |
|---|---|
| **JU12** | **CMOS Clear**<br>Install on the RIGHT to clear.<br>Install on the LEFT to operate. * |

**NOTE**: To clear the CMOS, power down the system and install the jumper on the RIGHT. Wait for at least two seconds, move the jumper back to the LEFT and turn the power on. When AMIBIOS displays the "CMOS Settings Wrong" message, press F1 to go into the BIOS Setup Utility, where you may reenter your desired BIOS settings, load optimal defaults or load failsafe defaults.

### ETHERNET LEDS AND CONNECTORS

Each Ethernet interface has two LEDs for status indication and an RJ-45 network connector.

| LED/Connector | Description |
|---|---|
| Activity LED | Green LED which indicates network activity. This is the upper LED on the LAN connector (i.e., toward the memory sockets). |
| Off | Indicates there is no current network transmit or receive activity. |
| On (flashing) | Indicates network transmit or receive activity. |
| Speed LED | Green LED which identifies the connection speed. This is the lower LED on the LAN connector (i.e., toward the edge connectors). |
| Off | Indicates a valid link at 1000-Mb/s. |
| Green | Indicates a valid link at 100-Mb/s. |
| RJ-45 Network Connector | The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection |

### STATUS LEDS

**Post Code LEDs**

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 1 through 8, which are located in the center of the board to the right of the processor and are numbered from top (1) to bottom (8). Refer to the board layout earlier in this chapter for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. Specific error codes are listed in *Appendix A - BIOS Messages*, along with a chart to interpret the LEDs into hexadecimal format.

**CPU Throttling LED**

The CPU throttling LED (LED9), which is located in the upper left corner of the TQ9, indicates the status of CPU thermal shutdown, as shown below:

| LED Status | Description |
|---|---|
| Off | Indicates the CPU is operating within acceptable thermal levels |
| On (flashing) | Indicates the CPU is throttling down to a lower operating speed due to rising CPU temperature |
| On (solid) | Indicates the CPU has reached the thermal shutdown threshold limit. The SHB is still operating, but a thermal shutdown may soon occur. |

**NOTE:** When a thermal shutdown occurs, the LED will stay on in systems using non- ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the SHB. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all SHB LEDs will turn off; however, stand-by power will still be present.

**Backplane LAN LED**

The backplane LAN LED (LED11), which is located at the center bottom of the SHB, indicates the status of communication between the SHB and the backplane, as shown below:

| LED Status | Description |
|---|---|
| Off | Indicates the LAN is inactive and link communications have not been established. |
| On (flashing) | Indicates that data is being transferred between the SHB and the backplane. |
| On (solid) | Indicates the LAN has a valid link and is ready for data transfers. |

## SYSTEM BIOS SETUP UTILITY

The System BIOS is an AMIBIOS with a ROM-resident setup utility. The BIOS Setup Utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- PCIPnP Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual.

## CONNECTORS

**NOTE:** Pin 1 on the connectors is indicated by the square pad on the PCB.

**P1 - 10/100/1000Base-T Ethernet Connectors - LAN1/LAN2**
Dual RJ-45 connector, Pulse #JG0-0024NL
Each individual RJ-45 connector is defined as follows:

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1A | L2_MDI0n | 1B | L1_MDI0n |
| 2A | L2_MDI0p | 2B | L1_MDI0p |
| 3A | L2_MDI1n | 3B | L1_MDI1n |
| 4A | L2_MDI1p | 4B | L1_MDI1p |
| 5A | L2_MDI2n | 5B | L1_MDI2n |
| 6A | L2_MDI2p | 6B | L1_MDI2p |
| 7A | L2_MDI3n | 7B | L1_MDI3n |
| 8A | L2_MDI3p | 8B | L1_MDI3p |
| 9A | VCC_1.8V | 9B | VCC_1.8V |
| 10A | GND_A | 10B | GND_b |

**P5 - Speaker Port Connector**
4 pin single row header, Amp #640456-4

| Pin | Signal |
|---|---|
| 1 | Speaker Data |
| 2 | Key |
| 3 | Gnd |
| 4 | +5V |

**P9 - Audio Connector**
10 pin dual row header, Amp #1761610-3

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Line_IN_L | 2 | Line_IN_R |
| 3 | Gnd | 4 | Gnd |
| 5 | Mic-L | 6 | Mic_R |
| 7 | Gnd | 8 | Gnd |
| 9 | HP_OUT_L | 10 | HP_OUT_R |

**P10 - External Reset Connector**
2 pin single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | Reset In |

**P12 - Hard Drive LED Connector**
4 pin single row header, Amp #640456-4

| Pin | Signal |
|---|---|
| 1 | LED+ |
| 2 | LED- |
| 3 | LED- |
| 4 | LED+ |

**P15 - Video Interface Connector**
15 pin connector, Kycon K31X-E15S-N

| Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|
| | | 6 | Gnd | | |
| 1 | Red | | | 11 | NC |
| | | 7 | Gnd | | |
| 2 | Green | | | 12 | EEDI |
| | | 8 | Gnd | | |
| 3 | Blue | | | 13 | HSYNC |
| | | 9 | +5 | | |
| 4 | NC | | | 14 | VSYNC |
| | | 10 | Gnd | | |
| 5 | Gnd | | | 15 | EECS |

**P17 - Universal Serial Bus (USB) Connector**
8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB2 | 2 | +5V-USB3 |
| 3 | USB2- | 4 | USB3- |
| 5 | USB2+ | 6 | USB3+ |
| 7 | Gnd-USB2 | 8 | Gnd-USB3 |

**P17A - Universal Serial Bus (USB) Connector**
USB vertical connector, Molex #47500-0001
(+5V fused with self-resetting fuse)

| Pin | Signal |
|---|---|
| 1 | +5V-USB0 |
| 2 | USB0- |
| 3 | USB0+ |
| 4 | Gnd-USB0 |

**P17B - Universal Serial Bus (USB) Connector**
USB vertical connector, Molex #47500-0001
(+5V fused with self-resetting fuse)

| Pin | Signal |
|---|---|
| 1 | +5V-USB1 |
| 2 | USB1- |
| 3 | USB1+ |
| 4 | Gnd-USB1 |

**P17C - Universal Serial Bus (USB) Connector**
8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB4 | 2 | +5V-USB5 |
| 3 | USB4- | 4 | USB5- |
| 5 | USB4+ | 6 | USB5+ |
| 7 | Gnd-USB4 | 8 | Gnd-USB5 |

**P17D - Universal Serial Bus (USB) Connector**
8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB6 | 2 | +5V-USB7 |
| 3 | USB6- | 4 | USB7- |
| 5 | USB6+ | 6 | USB7+ |
| 7 | Gnd-USB6 | 8 | Gnd-USB7 |

**P18 - System Hardware Monitor Connector**
4 pin single row header, Amp #640456-4

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | GPO (General Purpose Output) |
| 3 | CI (Chassis Intrusion Input) |
| 4 | OVT (Over Temperature) |

**P19 - CPU Fan**
3 pin single row header, Molex #22-23-2031

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | +12V |
| 3 | FanTach |

**P20 - I/O Expansion Mezzanine Card Connector**

76 pin controlled impedance connector, Samtec #MIS-038-01-FD-K

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +12 | 2 | +5V_STANDBY |
| 3 | NC | 4 | +5V_STANDBY |
| 5 | NC | 6 | +5V_DUAL |
| 7 | NC | 8 | +5V_DUAL |
| 9 | NC | 10 | NC |
| 11 | NC | 12 | NC |
| 13 | ICH_SMI# | 14 | ICH_RCIN# |
| 15 | ICH_SIOPME# | 16 | ICH_A20GATE |
| 17 | Gnd | 18 | Gnd |
| 19 | L_FRAME# | 20 | L_AD3 |
| 21 | L_DRQ1# | 22 | L_AD2 |
| 23 | L_DRQ0# | 24 | L_AD1 |
| 25 | SERIRQ | 26 | L_AD0 |
| 27 | Gnd | 28 | Gnd |
| 29 | PCLK14SIO | 30 | PCLK33LPC |
| 31 | Gnd | 32 | Gnd |
| 33 | SMBDATA_RESUME | 34 | IPMB_DAT |
| 35 | SBMCLK_RESUME | 36 | IPMB_CLK |
| 37 | SALRT#_RESUME | 38 | IPMB_ALRT# |
| 39 | Gnd | 40 | Gnd |
| 41 | EXP_CLK100 | 42 | EXP_RESET# |
| 43 | EXP_CLK100# | 44 | ICH_WAKE# |
| 45 | Gnd | 46 | Gnd |
| 47 | C_PE_TXP5 | 48 | C_PE_RXP5 |
| 49 | C_PE_TXN5 | 50 | C_PE_RXN5 |
| 51 | Gnd | 52 | Gnd |
| 53 | NC | 54 | NC |
| 55 | NC | 56 | NC |
| 57 | Gnd | 58 | Gnd |
| 59 | NC | 60 | NC |
| 61 | NC | 62 | NC |
| 63 | Gnd | 64 | Gnd |
| 65 | NC | 66 | NC |
| 67 | NC | 68 | NC |
| 69 | Gnd | 70 | Gnd |
| 71 | +3.3V | 72 | +5V |
| 73 | +3.3V | 74 | +5V |
| 75 | +3.3V | 76 | +5V |

**P21 - Power Good LED**

2 pin single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | LED- |
| 2 | LED+ |

**P27 - SATA Port 1**
7 pin vertical connector, Molex #67491-0031

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | TX+ |
| 3 | TX- |
| 4 | Gnd |
| 5 | RX- |
| 6 | RX+ |
| 7 | Gnd |

**P28 - SATA Port 2**
7 pin vertical connector, Molex #67491-0031

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | TX+ |
| 3 | TX- |
| 4 | Gnd |
| 5 | RX- |
| 6 | RX+ |
| 7 | Gnd |

**P31 - SATA Port 3**
7 pin vertical connector, Molex #67491-0031

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | TX+ |
| 3 | TX- |
| 4 | Gnd |
| 5 | RX- |
| 6 | RX+ |
| 7 | Gnd |

**P32 - SATA Port 4**
7 pin vertical connector, Molex #67491-0031

| Pin | Signal |
|---|---|
| 1 | Gnd |
| 2 | TX+ |
| 3 | TX- |
| 4 | Gnd |
| 5 | RX- |
| 6 | RX+ |
| 7 | Gnd |

**P40 - Audio Codec**
16-pin , 3M #N2516-6002RB

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | HDA0_BCLK | 2 | Gnd |
| 3 | HDA0_RST# | 4 | 3.3V |
| 5 | HDA0_SYNC | 6 | Gnd |
| 7 | HDA0_SDOUT | 8 | 3.3V |
| 9 | HDA0_SDIN0 | 10 | 12V |
| 11 | NC | 12 | NC |
| 13 | NC | 14 | 3.3V |
| 15 | NC | 16 | Gnd |

# *Chapter 2 PCI Express™ Reference*

### INTRODUCTION

PCI Express™ is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

### PCI EXPRESS LINKS

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion. A link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. In PCI Express Gen 1 the bandwidths for the PCIe links are deter-mined by the link width multiplied by 250MB/s and 500MB/s, as follows:

| Slot Size | Bandwidth | Full-Duplex Bandwidth |
|---|---|---|
| x1 | 250MB/s | 500MB/s |
| x4 | 1GB/s | 2GB/s |
| x8 | 2GB/s | 4GB/s |
| x16 | 4GB/s | 8GB/s |

Scalability is a core feature of PCI Express. Some chipsets allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. In addition, although a board with a higher number of lanes will not function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) because the connectors are mechanically and electrically incompatible, the reverse configuration will function. A board with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot). The link auto-negotiates between the PCI Express devices to establish communication. The mechanical option card slots on a PICMG 1.3 backplane must have PCI Express configuration straps that alert the SHB to the PCI

Express electrical configuration expected. The SHB can then reconfigure the PCIe links for optimum system performance.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

### SHB CONFIGURATIONS

There are two classes of PCI Express SHB configurations: server-class and graphics-class. Server applications require multiple, high-bandwidth PCIe links, and therefore the server-class SHB configuration is identified by multiple x8 and x4 links to the SHB edge connectors.

SHBs which require high-end video or graphics cards generally use a x16 PCI Express link. The graphics-class SHB configuration is identified by one x16 PCIe link and one x4 or four x1 links to the edge connectors. As PCI Express chipsets continue to evolve, it is possible that more x4 and/or x1 links could be supported in graphics-class SHBs. Currently, most video or graphics cards communicate to the SHB at an effective x1, x4 or x8 PCI Express data rate and do not actually make use of all of the signal lanes in a x16 connector.

**NOTE:** Server-class SHBs should always be used with server-class PICMG 1.3 backplanes and graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes. Combining incompatible SHBs and backplanes will not cause damage to the option cards or SHB, but one or more of the slots may not function and may result in one or more PCI Express option cards on the backplane being non-functional. This is due to the fact that there will not be enough available links to properly connect all of the PCI Express option card slots to the SHB.

### PCI EXPRESS EDGE CONNECTOR PIN ASSIGNMENTS

Trenton's TQ9 SHB uses edge connectors A, B, C and D. Optional I/O signals are defined in the PICMG 1.3 specification and if implemented must be located on edge connector C of the SHB. The TQ9 makes the Intelligent Platform Management Bus (IPMB) signals available to the user. The TQ9 supports four USB ports (USB 8, 9, 10 and 11), one 10/100Base-T Ethernet interface and two eSATA/300 interfaces for use on PICMG 1.3 compatible backplanes via the SHB's edge connector C.

The following table shows pin assignments for the PCI Express edge connectors on the TQ9 SHB.

* Pins 3 and 4 of Side B of Connector A (TDI and TDO) are jumpered together.

| Connector A | | | Connector B | | | Connector C | | | Connector D | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Side B | Side A | | Side B | Side A | | Side B | Side A | | Side B | Side A |
| 1 | SMCLK | SMBDAT | 1 | +5VSBY | +5VSBY | 1 | USBP0+ | GND | 1 | INTB# | INTA# |
| 2 | GND | GND | 2 | GND | ISA_NOGO | 2 | USBP0- | GND | 2 | INTD# | INTC# |
| 3 | TDI TDO* | NC | 3 | A_PE_TXP8 | GND | 3 | GND | USBP1+ | 3 | GND | NC |
| 4 | TDI TDO* | NC | 4 | A_PE_TXN8 | GND | 4 | GND | USBP1- | 4 | REQ3# | GNT3# |
| 5 | NC | ICH WAKE# | 5 | GND | A_PE_RXP8 | 5 | USBP2+ | GND | 5 | REQ2# | GNT2# |
| 6 | PWRBTN# | ICH PCIPME# | 6 | GND | A_PE_RXN8 | 6 | USBP2- | GND | 6 | PCIRST# | GNT1# |
| 7 | PWROK | PSON# | 7 | A_PE_TXP9 | GND | 7 | GND | USBP3+ | 7 | REQ1# | GNT0# |
| 8 | SHBRST# | EXP RESET# | 8 | A_PE_TXN9 | GND | 8 | GND | USBP3- | 8 | REQ0# | SERR# |
| 9 | CFG0 | CFG1 | 9 | GND | A_PE_RXP9 | 9 | USBOC0 | GND | 9 | NC | 3.3V |
| 10 | CFG2 | CFG3 | 10 | GND | A_PE_RXN9 | 10 | GND | USBOC1 | 10 | GND | CLKFI |
| 11 | | GND | 11 | RSVD | GND | 11 | USBOC2 | GND | 11 | CLKFO | GND |
| Mechanical Connector | | | Mechanical Connector | | | Mechanical Connector | | | Mechanical Connector | | |
| 12 | GND | RSVD | 12 | GND | RSVD | 12 | GND | USBOC3 | 12 | CLKC | CLKD |
| 13 | B_PE_TXPO | GND | 13 | A_PE_TXP10 | GND | 13 | S5_TXP | GND | 13 | GND | 3.3V |
| 14 | B_PE_TXN0 | GND | 14 | A_PE_TXN10 | GND | 14 | S5_TXN | GND | 14 | CLKA | CLKB |
| 15 | GND | B_PE_RXP0 | 15 | GND | A_PE_RXP10 | 15 | GND | S5_RXP | 15 | 3.3V | GND |
| 16 | GND | B_PE_RXN0 | 16 | GND | A_PE_RXN10 | 16 | GND | S5_RXN | 16 | AD31 | PME# |
| 17 | B_PE_TXP1 | GND | 17 | A_PE_TXP11 | GND | 17 | S4_TXP | GND | 17 | AD29 | 3.3V |
| 18 | B_PE_TXN1 | GND | 18 | A_PE_TXN11 | GND | 18 | S4_TXN | GND | 18 | M6_6_EN | AD30 |
| 19 | GND | B_PE_RXP1 | 19 | GND | A_PE_RXP11 | 19 | GND | S4_RXP | 19 | AD27 | AD28 |
| 20 | GND | B_PE_RXN1 | 20 | GND | A_PE_RXN11 | 20 | GND | S4_RXN | 20 | AD25 | GND |
| 21 | B_PE_TXP2 | GND | 21 | A_PE_TXP12 | GND | 21 | A_MDI0P | GND | 21 | GND | AD26 |
| 22 | B_PE_TXN2 | GND | 22 | A_PE_TXN12 | GND | 22 | A_MDI0N | GND | 22 | CBE3# | AD24 |
| 23 | GND | B_PE_RXP2 | 23 | GND | A_PE_RXP12 | 23 | GND | A_MDI1P | 23 | AD23 | 3.3V |
| 24 | GND | B_PE_RXN2 | 24 | GND | A_PE_RXN12 | 24 | GND | A_MDI1N | 24 | GND | AD22 |
| 25 | B_PE_TXP3 | GND | 25 | A_PE_TXP13 | GND | 25 | NC | GND | 25 | AD21 | AD20 |
| 26 | B_PE_TXN3 | GND | 26 | A_PE_TXN13 | GND | 26 | NC | GND | 26 | AD19 | PCIXCAP |
| 27 | GND | B_PE_RXP3 | 27 | GND | A_PE_RXP13 | 27 | GND | NC | 27 | +5V | AD18 |
| 28 | GND | B_PE_RXN3 | 28 | GND | A_PE_RXN13 | 28 | NC | NC | 28 | AD17 | AD16 |
| 29 | REFCLK0 | GND | 29 | A_PE_TXP14 | GND | 29 | IPMB_CLK | GND | 29 | CBE2# | GND |
| 30 | REFCLK0# | GND | 30 | A_PE_TXN14 | GND | 30 | IPMB_DAT | GND | 30 | GND | FRAME# |
| 31 | GND | REFCLK1# | 31 | GND | A_PE_RXP1 | 31 | NC | NC | 31 | IRDY# | TRDY# |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 32 | RSVD-G | REFCLK1 | 32 | GND | 4<br>A_PE_RXN1<br>4 | 32 | NC | NC | 32 | DEVSEL# | +5V |

| Connector A | | |
|---|---|---|
| | Side B | Side A |
| 33 | REFCLK2# | GND |
| 34 | REFCLK2 | GND |
| 35 | GND | REFCLK3# |
| 36 | RSVD-G | REFCLK3 |
| 37 | REFCLK4# | GND |
| 38 | REFCLK4 | GND |
| 39 | GND | REFCLK5# PU |
| 40 | RSVD-G | REFCLK PU |
| 41 | REFCLK6# PU | GND |
| 42 | REFCLK6 PU | GND |
| 43 | GND | REFCLK7# PU |
| 44 | GND | REFCLK7 PU |
| 45 | A_PE_TXP0 | GND |
| 46 | A_PE_TXN0 | GND |
| 47 | GND | A_PE_RXP0 |
| 48 | GND | A_PE_RXN0 |
| 49 | A_PE_TXP1 | GND |
| 50 | A_PE_TXN1 | GND |
| 51 | GND | A_PE_RXP1 |
| 52 | GND | A_PE_RXN1 |
| 53 | A_PE_TXP2 | GND |
| 54 | A_PE_TXN2 | GND |
| 55 | GND | A_PE_RXP2 |
| 56 | GND | A_PE_RXN2 |
| 57 | A_PE_TXP3 | GND |
| 58 | A_PE_TXN3 | GND |
| 59 | GND | A_PE_RXP3 |
| 60 | GND | A_PE_RXN3 |
| 61 | A_PE_TXP4 | GND |
| 62 | A_PE_TXN4 | GND |
| 63 | GND | A_PE_RXP4 |
| 64 | GND | A_PE_RXN4 |
| 65 | A_PE_TXP5 | GND |
| 66 | A_PE_TXN5 | GND |
| 67 | GND | A_PE_RXP5 |
| 68 | GND | A_PE_RXN5 |
| 69 | A_PE_TXP6 | GND |
| 70 | A_PE_TXN6 | GND |
| 71 | GND | A_PE_RXP6 |
| 72 | GND | A_PE_RXN6 |
| 73 | A_PE_TXP7 | GND |
| 74 | A_PE_TXN7 | GND |
| 75 | GND | A_PE_RXP7 |
| 76 | GND | A_PE_RXN7 |
| 77 | SERIRQ | GND |
| 78 | 3.3V | 3.3V |
| 79 | 3.3V | 3.3V |
| 80 | 3.3V | 3.3V |
| 81 | 3.3V | 3.3V |
| 82 | NC | NC |

| Connector B | | |
|---|---|---|
| | Side B | Side A |
| 33 | A_PE_TXP15 | GND |
| 34 | A_PE_TXN15 | GND |
| 35 | GND | A_PE_RXP15 |
| 36 | GND | A_PE_RXN15 |
| 37 | CRTLDA | GND |
| 38 | CRTLCK | EXPEN |
| 39 | GND | GND |
| 40 | GND | GND |
| 41 | GND | GND |
| 42 | GND | GND |
| 43 | GND | GND |
| 44 | +12V | +12V |
| 45 | +12V | +12V |
| 46 | +12V | +12V |
| 47 | +12V | +12V |
| 48 | +12V | +12V |
| 49 | +12V | +12V |

| Connector C | | |
|---|---|---|
| | Side B | Side A |
| 33 | NC | NC |
| 34 | NC | GND |
| 35 | NC | GND |
| 36 | GND | NC |
| 37 | GND | NC |
| 38 | NC | GND |
| 39 | NC | GND |
| 40 | GND | NC |
| 41 | GND | NC |
| 42 | 3.3V | 3.3V |
| 43 | 3.3V | 3.3V |
| 44 | 3.3V | 3.3V |
| 45 | 3.3V | 3.3V |
| 46 | 3.3V | 3.3V |
| 47 | 3.3V | 3.3V |
| 48 | 3.3V | 3.3V |
| 49 | 3.3V | 3.3V |
| 50 | 3.3V | 3.3V |
| 51 | GND | GND |
| 52 | GND | GND |
| 53 | GND | GND |
| 54 | GND | GND |
| 55 | GND | GND |
| 56 | GND | GND |
| 57 | GND | GND |
| 58 | GND | GND |
| 59 | +5V | +5V |
| 60 | +5V | +5V |
| 61 | +5V | +5V |
| 62 | +5V | +5V |
| 63 | GND | GND |
| 64 | GND | GND |
| 65 | GND | GND |
| 66 | GND | GND |
| 67 | GND | GND |
| 68 | GND | GND |
| 69 | GND | GND |
| 70 | GND | GND |
| 71 | GND | GND |
| 72 | GND | GND |
| 73 | +12V_VRM | +12V_VRM |
| 74 | +12V_VRM | +12V_VRM |
| 75 | +12V_VRM | +12V_VRM |
| 76 | +12V_VRM | +12V_VRM |
| 77 | +12V_VRM | +12V_VRM |
| 78 | +12V_VRM | +12V_VRM |
| 79 | +12V_VRM | +12V_VRM |
| 80 | +12V_VRM | +12V_VRM |
| 81 | +12V_VRM | +12V_VRM |
| 82 | +12V_VRM | +12V_VRM |

| Connector D | | |
|---|---|---|
| | Side B | Side A |
| 33 | PLOCK# | STOP# |
| 34 | PERR# | GND |
| 35 | GND | CBE1# |
| 36 | PAR | AD14 |
| 37 | NC | GND |
| 38 | GND | AD12 |
| 39 | AD15 | AD10 |
| 40 | AD13 | GND |
| 41 | GND | AD9 |
| 42 | AD11 | CBE0# |
| 43 | AD8 | GND |
| 44 | GND | AD6 |
| 45 | AD7 | AD5 |
| 46 | AD4 | GND |
| 47 | GND | AD2 |
| 48 | AD3 | AD1 |
| 49 | AD0 | GND |

### PCI EXPRESS SIGNALS OVERVIEW

The following table provides a description of the SHB slot signal groups on the PCI Express connectors.

| Type | Signals | Description | Connector | Source |
|---|---|---|---|---|
| Global | GND, +5V, +3.3V, +12V | Power | | Backplane |
| | PSON# | Optional ATX support | A | SHB |
| | PWRGD, PWRBT#, 5Vaux | Optional ATX support | A and B | Backplane |
| | TDI | Optional JTAG support | A | Backplane |
| | TDO | Optional JTAG support | A | SHB |
| | SMCLK, SMDAT | Optional SMBus support | A | SHB & Backplane |
| | IPMB_CL, IPMB_DA | Optional IPMB support | C | SHB & Backplane |
| | CFG[0:3] | PCIe configuration straps | A | Backplane |
| | SHB_RST# | Optional reset line | A | SHB |
| | RSVD | Reserved | A and B | |
| | RSVD-G | Reserved ground | A | Backplane |
| | WAKE# | Signal for link reactivation | A | Backplane |
| PCIe | a_PETp[0:15]<br>a_PETn[0:15]<br>a_PERp[0:15]<br>a_PERn[0:15] | Point-to-point from SHB slot through the x16 PCIe connector (A) to the target device(s) | A and B | SHB & Backplane |
| | b_PETp[0:3]<br>b_PETn[0:3]<br>b_PERp[0:3]<br>b_PERn[0:3] | Point-to-point from SHB slot through the x8 PCIe connector (B) to the target device(s) | A | SHB & Backplane |
| | REFCLK[0:7]+, REFCLK[0:7]- | | A | SHB |
| | PERST# | Clock synchronization of PCIe expansion slots<br><br>PCIe fundamental reset | A | SHB & Backplane |
| PCI(-X) | AD[0:31], FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, C/BE[0:3], SDONE, SBO#, PAR | Bussed on SHB slot and expansion slots | D | SHB & Backplane |
| | GNT[0:3], REQ[0:3], CLKA, CLKB, CLKC, CLKD, CLKFO, CLKFI | Point-to-point from SHB slot to each expansion slot | D | SHB & Backplane |
| | INTA#, INTB#, INTC#, INTD# | Bussed (rotating) on SHB slot and expansion slots | D | Backplane |
| | M66EN, PCIXCAP | Bussed on SHB slot and expansion slots | D | Backplane |
| | PCI_PRST# | PCI(-X) present on backplane detect | A | Backplane |
| | PME# | Optional PCI wake-up event bussed on SHB and backplane expansion slots | | |
| Misc. I/O | USB[0:3]P, USB[0:3]N, USBOC[0:3]# | Optional point-to-point from SHB Connector C to a destination USB device | C | SHB & Backplane |
| SATA | ESATATX(4:5)P,<br>ESATATX(4:5)N,<br>ESATARX(4:5)P,<br>ESATARX(4:5)N, | Optional point-to-point from SHB Connector C to a destination SATA device | C | SHB & Backplane |
| Ethernet | a_MDI(0:1)p,<br>a_MDI(0:1)n | Optional point-to-point from SHB Connector C to a destination Ethernet device | C | SHB & Backplane |

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# *Chapter 3 System BIOS*

## BIOS OPERATION

Chapters 3 through 7 of this manual describe the operation of the American Megatrends AMIBIOS and the BIOS Setup Utility. Refer to *Running AMIBIOS Setup* later in this chapter for standard Setup screens, options and defaults. The available Setup screens, options and defaults may vary if you have a custom BIOS.

When the system is powered on, AMIBIOS performs the Power-On Self Test (POST) routines. These routines are divided into two phases:

1) **System Test and Initialization**. Test and initialize system boards for normal operations.

2) **System Configuration Verification**. Compare defined configuration with hardware actually installed.

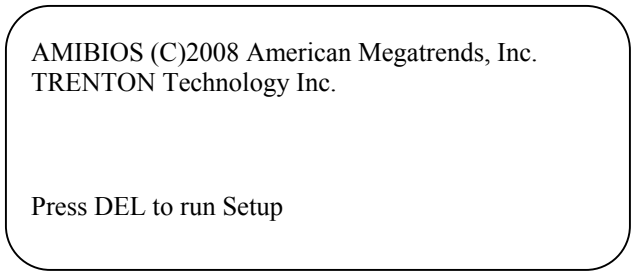
If an error is encountered during the diagnostic tests, the error is reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps is transmitted. If the error occurs after the display device is initialized, the error message is displayed on the screen. See *BIOS Errors* later in this section for more information on error handling.

The following are some of the Power-On Self Tests (POSTs) which are performed when the system is powered on:

- CMOS Checksum Calculation
- Keyboard Controller Test
- CMOS Shutdown Register Test
- 8254 Timer Test
- Memory Refresh Test
- Display Memory Read/Write Test
- Display Type Verification
- Entering Protected Mode
- Memory Size Calculation
- Conventional and Extended Memory Test
- DMA Controller Tests
- Keyboard Test
- System Configuration Verification and Setup

AMIBIOS checks system memory and reports it on both the initial AMIBIOS screen and the AMIBIOS System Configuration screen which appears after POST is completed. AMIBIOS attempts to initialize the peripheral devices and if it detects a fault, the screen displays the error condition(s) which has/have been detected. If no errors are detected, AMIBIOS attempts to load the system from a bootable device, such as a floppy disk or hard disk. Boot order may be specified by the **Boot Device Priority** option on the Boot Setup Menu as described in the *Boot Setup* chapter later in this manual.

Normally, the only POST routine visible on the screen is the memory test. The following screen displays when the system is powered on:




**Initial Power-On Screen**

You have two options:

- Press **<Del>** to access the BIOS Setup Utility.

  This option allows you to change various system parameters such as date and time, disk drives, etc. The *Running AMIBIOS Setup* section of this manual describes the options available.

  You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* later in this section.)

  If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays. (See *Running AMIBIOS Setup* later in this section.)

- Allow the bootup process to continue without invoking the BIOS Setup Utility.

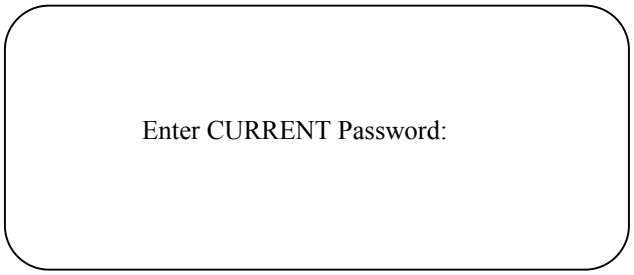
  In this case, after AMIBIOS loads the system, you may be requested to enter a password. (See *Password Entry* later in this section.)

Once the POST routines complete successfully, a screen displays showing the current configuration of your system, including processor type, base and extended memory amounts, floppy and hard drive types, display type and peripheral ports.

**Password Entry**
The system may be configured so that the user is required to enter a password each time the system boots or whenever an attempt is made to enter the BIOS Setup Utility. The password function may also be disabled so that the password prompt does not appear under any circumstances.

The **Password Check** option in the Security Menu allows you to specify when the password prompt displays: **Always** or only when **Setup** is attempted. This option is available only if the supervisor and/or user password(s) have been established. The supervisor and user passwords may be changed using the **Change Supervisor Password** and **Change User Password** options on the Security Menu. If the passwords are null, the password prompt does not display at any time. See the *Security Setup* section of this chapter for details on setting up passwords.

When password checking is enabled, the following password prompt displays:



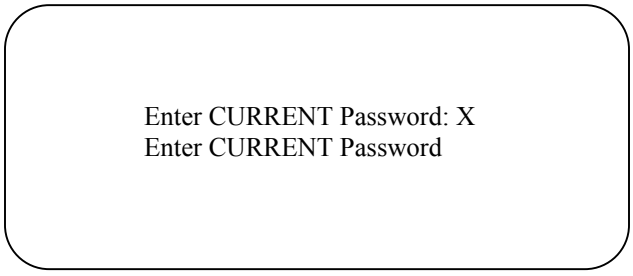

Type the password and press **<Enter>**.

---

**NOTE:** The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the password prompt does not display. To set up passwords, you may use the **Change Supervisor Password** and **Change User Password** options on the Security Menu of the BIOS Setup Utility. (See the *Security Setup* section later in this chapter.)

---

If an incorrect password is entered, the following screen displays:




You may try again to enter the correct password. If you enter the password incorrectly three times, the system responds in one of two different ways, depending on the value specified in the **Password Check** option on the *Security* Menu:

1) If the **Password Check** option is set to **Setup**, the system does not let you enter Setup, but does continue the booting process. You must reboot the system manually to retry entering the password.

2) If the **Password Check** option is set to **Always**, the system locks and you must reboot.

After rebooting, you will be requested to enter the password. Once the password has been entered correctly, you are allowed to continue.

### BIOS ERRORS

If an error is encountered during the diagnostic checks performed when the system is powered on, the error is reported in one of two different ways:

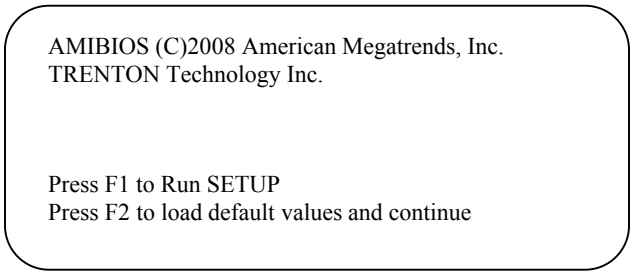
1) If the error occurs before the display device is initialized, a series of beeps is transmitted.

2) If the error occurs after the display device is initialized, the screen displays the error message. In the case of a non-fatal error, a prompt to press the **<F1>** key may also appear on the screen.

Explanations of the beep codes and BIOS error messages may be found in *Appendix A - BIOS Messages*.

As the POST routines are performed, test codes are presented on Port 80H. These codes may be helpful as a diagnostic tool and are listed in *Appendix A - BIOS Messages*.

If certain non-fatal error conditions occur, you are requested to run the BIOS Setup Utility. The error messages are followed by this screen:




### RUNNING AMIBIOS SETUP

AMIBIOS Setup keeps a record of system parameters, such as date and time, disk drives and other user-defined parameters. The Setup parameters reside in the Read Only Memory Basic Input/Output System (ROM BIOS) so that they are available each time the system is turned on. The BIOS Setup Utility stores the information in the complementary metal oxide semiconductor (CMOS) memory. When the system is turned off, a backup battery retains system parameters in the CMOS memory.

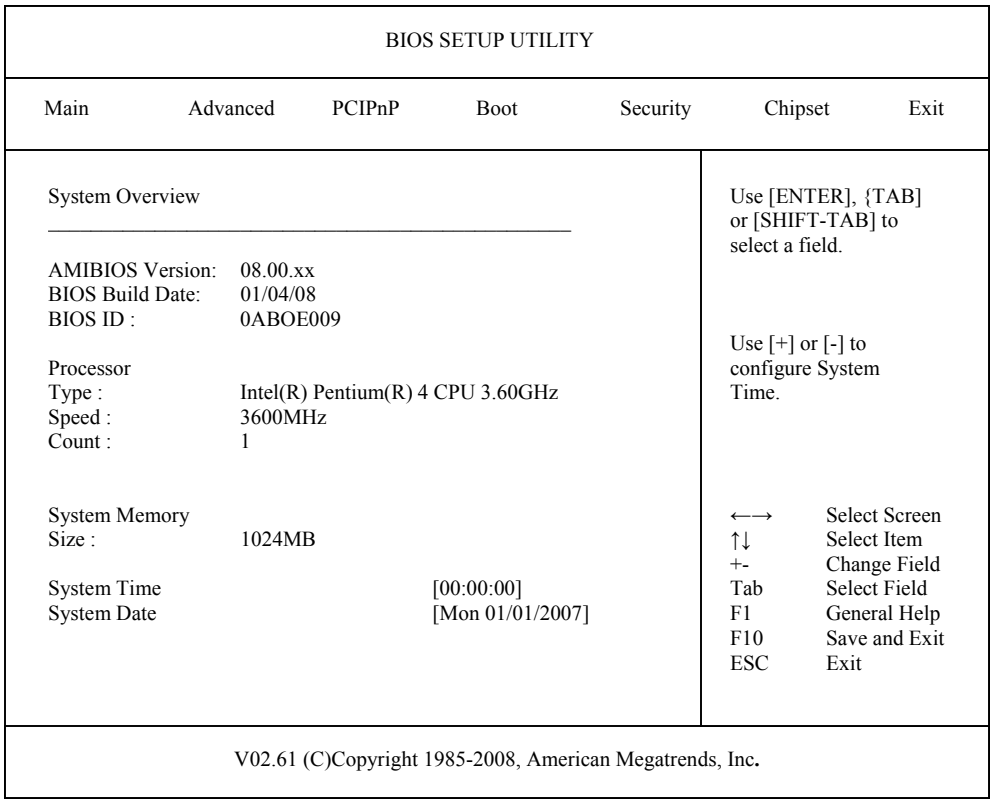
Each time the system is powered on, it is configured with these values, unless the CMOS has been corrupted or is faulty. The BIOS Setup Utility is resident in the ROM BIOS so that it is available each time the computer is turned on. If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file.

As soon as the system is turned on, the power-on diagnostic routines check memory, attempt to prepare peripheral devices for action, and offer you the option of pressing **<Del>** to run the BIOS Setup Utility.

If certain non-fatal errors occur during the Power-On Self Test (POST) routines which are run when the system is turned on, you may be prompted to run the BIOS Setup Utility by pressing **<F1>**.

### BIOS SETUP UTILITY MAIN MENU

When you press **<F1>** in response to an error message received during the POST routines or when you press the **<Del>** key to enter the BIOS Setup Utility, the following screen displays:




**BIOS Setup Utility Main Menu**

When you display the BIOS Setup Utility Main Menu, the format is similar to the sample shown above. The data displayed on the top portion of the screen details parameters detected by AMIBIOS for your processor board and may not be modified. The system time and date displayed on the bottom portion of the screen may be modified.

### BIOS SETUP UTILITY MAIN MENU OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**System Time/System Date**

These options allow you to set the correct system time and date. If you do not set these parameters the first time you enter the BIOS Setup Utility, you will receive a "Run SETUP" error message when you boot the system until you set the correct parameters.

The Setup screen displays the system options:

| | |
|---|---|
| **System Time** | **[00:00:00]** |
| **System Date** | **[Mon 01/01/2001]** |

There are three fields for entering the time or date. Use the **<Tab>** key or the **<Enter>** key to move from one field to another and type in the correct value for the field.

If you enter an invalid value in any field, the screen will revert to the previous value when you move to the next field. When you change the value for the month, day or year field, the day of the week changes automatically when you move to the next field.

### BIOS SETUP UTILITY OPTIONS

The BIOS Setup Utility allows you to change system parameters to tailor your system to your requirements. Various options which may be changed are listed below. Further explanations of these options and available values may be found in later chapters of this manual, as noted below.

NOTE: Do *not* change the values for any option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

**NOTE:** Menu items listed below in *italics* are only available when and IOB module is installed.

Use the **Right Arrow** key to display the desired menu. The following menus are available:

- Select **Advanced** to make changes to Advanced Setup parameters as described in the *Advanced Setup* chapter of this manual. The following options may be modified:
    - CPU Configuration
        - Ratio CMOS setting
        - Hardware Prefetcher
        - Max CPUID Value Limit
        - PECI
        - Intel (R) SpeedStep(tm) tech
    - IDE Configuration
        - SATA#1 Configuration
            - Configure SATA#1 as
            - Max Ports on SATA#1
        - SATA#2 Configuration
        - Primary IDE Master/Primary IDE Slave
          Secondary IDE Master/Secondary IDE Slave
          Third IDE Master
          Fourth IDE Master
            - Type
            - LBA/Large Mode
            - Block (Multi-Sector Transfer)
            - PIO Mode
            - DMA Mode
            - S.M.A.R.T.
            - 32Bit Data Transfer

- Hot Plug
- Hard Disk Write Protect
- IDE Detect Time Out (Sec)
- ATA(PI) 80Pin Cable Detection

- *Floppy Configuration*
  - *Floppy A/Floppy B*
- *SuperIO Configuration*
  - *OnBoard Floppy Controller*
  - *Serial Port1 Address/Serial Port2 Address*
  - *Parallel Port Address*
    - *Parallel Port Mode*
    - *Parallel Port IRQ*
- ACPI Configuration
  - General ACPI Configuration
    - Suspend Mode
    - Repost Video on S3 Resume
    - Power Supply Shutoff
  - Advanced ACPI Configuration
    - ACPI Version Features
    - ACPI APIC Support
    - AMI OEMB Table
    - Headless Mode
  - Chipset ACPI Configuration
    - APIC ACPI SCI IRQ
    - USB Device Wakeup From S3/S4
- AHCI
  - AHCI CD/DVD Boot Time out
  - AHCI Port 0
    AHCI Port 1
    AHCI Port 2
    AHCI Port 3
    AHCI Port 4
    AHCI Port 5
    - SATA Port(x)
    - S.M.A.R.T.

- MPS Configuration
    - MPS Revision
- *Remote Access Configuration*
    - *Remote Access*
    - *Serial Port Number*
    - *Serial Port Mode*
    - *Flow Control*
    - *Redirection After BIOS POST*
    - *Terminal*
    - *Type*
    - *VT-UTF8 Combo Key Support*
    - *Sredir Memory Display Mode*
- USB Configuration
    - Legacy USB Support
    - Port 64/60 Emulation
    - USB 2.0 Controller Mode
    - BIOS EHCI Hand-Off

- Select **PCIPnP** to make changes to PCI Plug and Play Setup parameters as described in the *PCI Plug and Play Setup* chapter of this manual. The following options may be modified:
    - Clear NVRAM •
    - Plug & Play O/S
    - PCI Latency Timer
    - Allocate IRQ to PCI VGA
    - Palette Snooping
    - PCI IDE BusMaster
    - OffBoard PCI/ISA IDE Card
    - Onboard LAN Controllers
        - Onboard LAN Boot ROM
    - Backplane ISA Bridge Support
    - Backplane IRQ routing
    - IRQs 3, 4, 5, 7, 9, 10, 11, 14 and 15
    - DMA Channels 0, 1, 3 5, 6 and 7
    - Reserved Memory Size
    - Reserved Memory Address

- Select **Boot** to make changes to Boot Setup parameters as described in the *Boot Setup* chapter of this manual. The following options may be modified:
    - Boot Settings Configuration
        - Quick Boot
        - Quiet Boot
        - AddOn ROM Display Mode
        - Bootup Num-Lock
        - PS/2 Mouse Support
        - Wait For 'F1' If Error
        - Hit 'DEL' Message Display
        - Interrupt 19 Capture
    - Boot Device Priority
    - Hard Disk Drives
    - Removable Drives
    - CD/DVD Drives

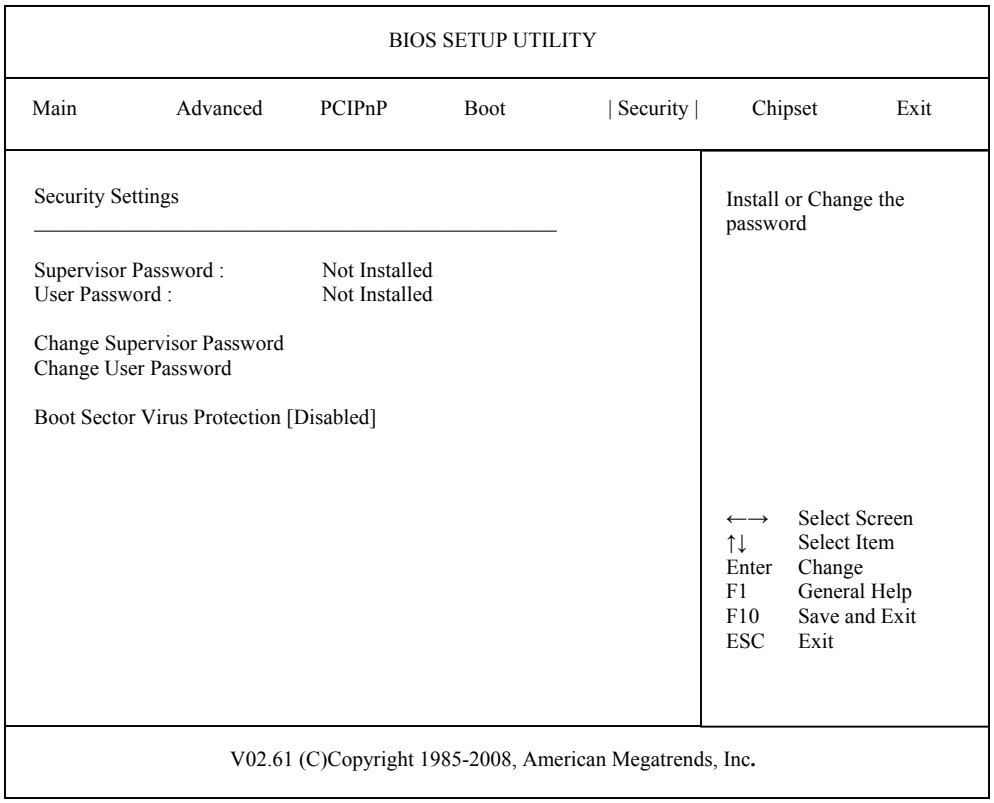
- Select **Security** to establish or change the supervisor or user password or to enable boot sector virus protection. These functions are described later in this chapter. The following options may be modified:
    - Change Supervisor Password
        - User Access Level
        - Password Check
    - Change User Password
        - Password Check
    - Clear User Password
    - Boot Sector Virus Protection

- Select **Chipset** to make changes to Chipset Setup parameters as described in the *Chipset Setup* chapter of this manual. The following options may be modified:
    - North Bridge Chipset Configuration
        - Memory Remap Feature
        - Initiate Graphics Adapter
        - Internal Graphics Mode Select
    - South Bridge Configuration
        - USB Functions
        - USB Port Configure
        - USB 2.0 Controller
        - HAD Controller
        - SMBUS Controller
        - Restore on AC Power Loss

- Select **Exit** to save or discard changes you have made to AMIBIOS parameters or to load the Optimal or Failsafe default settings. These functions are described later in this chapter. The following options are available:
    - Save Changes and Exit
    - Discard Changes and Exit
    - Discard Changes
    - Load Optimal Defaults
    - Load Failsafe Defaults

### SECURITY SETUP

When you select **Security** from the BIOS Setup Utility Main Menu, the following Setup screen displays:




**Security Setup Screen**

When you display the Security Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>**.

---

**NOTE:** The values on this screen do not necessarily reflect the values appropriate for your SHB. Refer to the explanations below for specific instructions about entering correct information.

---

### SECURITY SETUP OPTIONS

The Security Setup options allow you to establish, change or clear the supervisor or user password and to enable boot sector virus protection.

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

### CHANGE SUPERVISOR PASSWORD

This option allows you to establish a supervisor password, change the current password or disable the password prompt by entering a null password. The password is stored in CMOS RAM.

If you have signed on under the user password, this option is *not* available.

The **Change Supervisor Password** feature can be configured so that a password must be entered each time the system boots or just when a user attempts to enter the BIOS Setup Utility.

**NOTE:** The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the "Enter CURRENT Password" prompt is bypassed when you boot the system, and you must establish a new password.

If you select the **Change Supervisor Password** option, the following window displays:

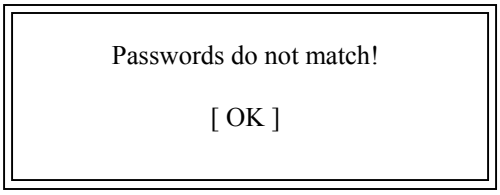

This is the message which displays before you have established a password, or if the last password entered was the null password. If a password has already been established, you are asked to enter the *current* password before being prompted to enter the *new* password.

Type the new password and press **<Enter>**. The password cannot exceed six (6) characters in length. The screen displays an asterisk (*****) for each character you type.

After you have entered the new password, the following window displays:

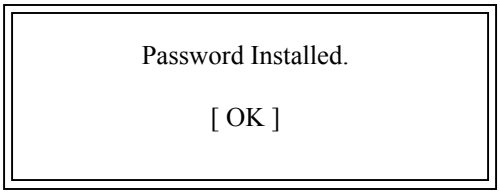

Re-key the new password as described above.

If the password confirmation is miskeyed, AMIBIOS Setup displays the following message:




No retries are permitted; you must restart the procedure.

If the password confirmation is entered correctly, the following message displays:



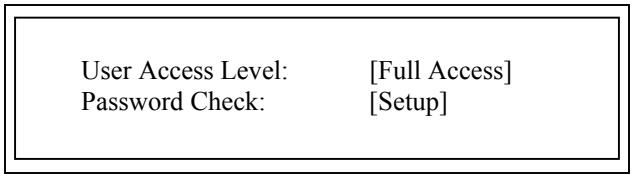
Press the **<Enter>** key to return to the Security screen. **Installed** displays on the screen next to the **Supervisor Password** option, indicating the password has been accepted. This setting will remain in effect until the supervisor password is either disabled or discarded upon exiting the BIOS Setup Utility. If you have created a new password, be sure to select **Exit**, then **Save Changes and Exit** to save the password. The password is then stored in CMOS RAM. The next time the system boots, you are prompted for the password.

---

**NOTE:** Be sure to keep a record of the new password each time it is changed. If you forget it, use the Password Clear jumper to reset it to the default (null password). See the *Specifications* chapter of this manual for details.

---

If a password has been established, the following options and their default values are added to the screen:




**User Access Level**

This option allows you to define the level of access the user will have to the system.

The Setup screen displays the system option:

**User Access Level [Full Access]**

Four options are available:

- Select **No Access** to prevent user access to the BIOS Setup Utility.
- Select **View Only** to allow access to the BIOS Setup Utility for viewing, but to prevent the user from changing any of the fields.
- Select **Limited** to allow the user to change only a limited number of options, such as Date and Time.
- Select **Full Access** to allow the user full access to change any option in the BIOS Setup Utility.

**Password Check**

This option determines when a password is required for access to the system.

The Setup screen displays the system option:

**Password Check [Setup]**

Two options are available:

- Select **Setup** to have the password prompt appear only when an attempt is made to enter the BIOS Setup Utility program.
- Select **Always** to have the password prompt appear each time the system is powered on.

#### DISABLING THE SUPERVISOR PASSWORD

To *disable* password checking so that the password prompt does not appear, you may create a null password by selecting the **Change Supervisor Password** function and pressing **<Enter>** without typing in a new password. You will be asked to enter the current password before being allowed to enter the null password. After you press **<Enter>** at the **Enter New Password** prompt, the following message displays:


#### CHANGE USER PASSWORD

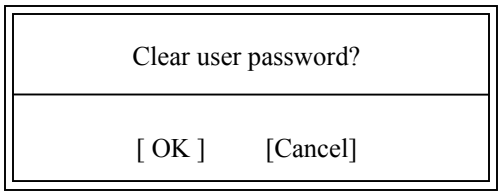
The **Change User Password** option is similar in functionality to the **Change Supervisor Password** and displays the same messages. If you have signed on under the user password, the **Change Supervisor Password** function is not available for modification.

If a user password has been established, the **Password Check** option and its default value is added to the screen. This option determines when a user password is required for access to the system. For details, refer to the description for **Password Check** under the **Change Supervisor Password** heading earlier in this section.

#### CLEAR USER PASSWORD

This option allows you to clear the user password. It disables the user password by entering a null password.

If you select the **Clear User Password** option, the following window displays:




You have two options:

- Select **Ok** to clear the user password.
- Select **Cancel** to leave the current user password in effect.

#### BOOT SECTOR VIRUS PROTECTION

This option allows you to request AMIBIOS to issue a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

The Setup screen displays the system option:

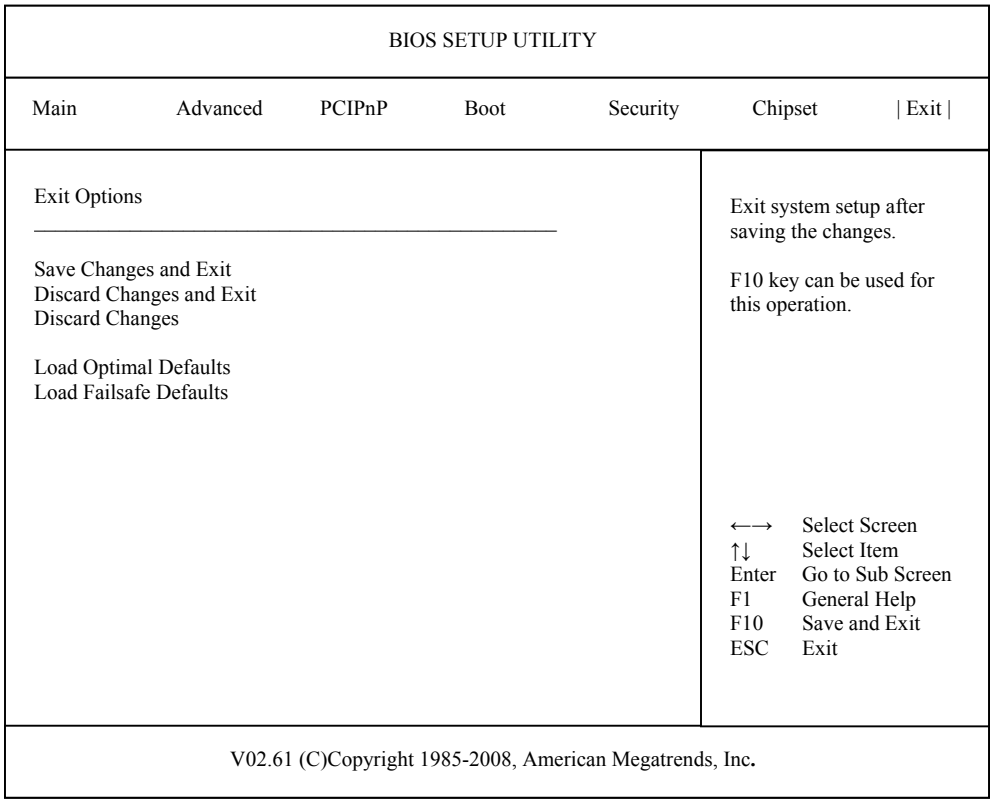
**Boot Sector Virus Protection [Disabled]**

Available options are:

Disabled
Enabled

**NOTE:** You should *not* enable boot sector virus protection when formatting a hard drive.

Exit Menu
When you select Exit from the BIOS Setup Utility Main Menu, the following screen displays:




**Exit Menu Screen**

When you display the Exit Menu screen, the format is similar to the sample shown above. Highlight the option you wish to select and press **<Enter>**.

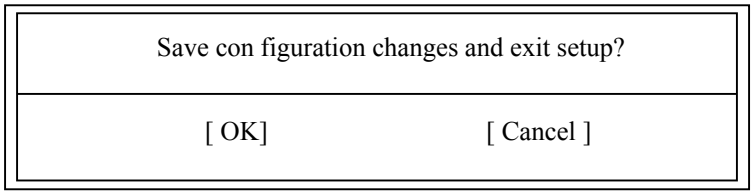
## EXIT MENU OPTIONS

When you are running the BIOS Setup Utility program, you may either save or discard changes you have made to AMIBIOS parameters, or you may load the Optimal or Failsafe default settings.

### Save Changes and Exit

The features selected and configured in the Setup screens are stored in the CMOS when this option is selected. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the AMIBIOS and the booting process continues, using the new CMOS values.

If you select the **Save Changes and Exit** option, the following window displays:

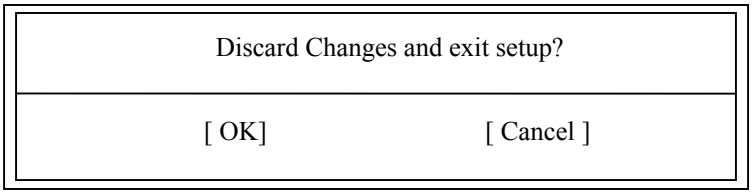


You have two options:

- Select **Ok** to save the system parameters and continue with the booting process.
- Select **Cancel** to return to the BIOS Setup Utility screen.

**Discard Changes and Exit**
When the **Discard Changes and Exit** option is selected, the BIOS Setup Utility exits *without* saving the changes in the CMOS. Control is then passed back to AMIBIOS and the booting process continues, using the previous CMOS values.

If you select the **Discard Changes and Exit** option, the following window displays:

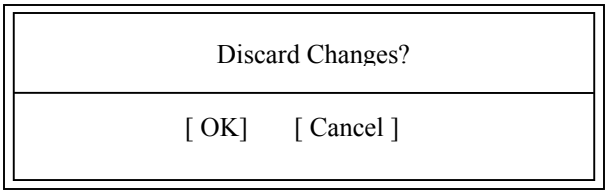



You have two options:

- Select **Ok** to continue the booting process *without* writing any changes to the CMOS.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes
When the Discard Changes option is selected, the BIOS Setup Utility resets any parameters you have changed back to the values at which they were set when you entered the Setup Utility. Control is then passed back to the BIOS Setup Utility screen.

If you select the Discard Changes option, the following window displays:




You have two options:

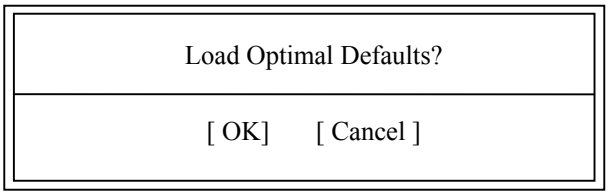
- Select Ok to reset any parameters you have changed back to the values at which they were set when you entered the BIOS Setup Utility. This option then returns you to the BIOS Setup Utility screen.
- Select Cancel to return to the BIOS Setup Utility screen without discarding any changes you have made.

**Load Optimal or Failsafe Defaults**
Each AMIBIOS Setup option has two default settings (Optimal and Failsafe). These settings can be applied to all AMIBIOS Setup options when you select the appropriate configuration option from the BIOS Setup Utility Main Menu.

You can use these configuration options to quickly set the system configuration parameters which should provide the best performance characteristics, or you can select a group of settings which have a better chance of working when the system is having configuration-related problems.

**Load Optimal Defaults**
This option allows you to load the Optimal default settings. These settings are best-case values which should provide the best performance characteristics. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

If you select the **Load Optimal Defaults** option, the following window displays:

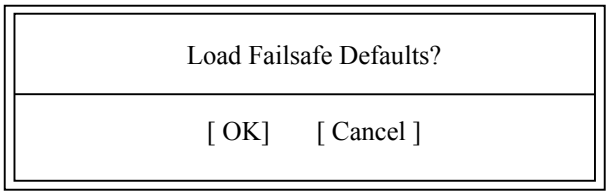



You have two options:

- Select Ok to load the Optimal default settings.
- Select Cancel to leave the current values in effect.

**Load Failsafe Defaults** This option allows you to load the Failsafe default settings when you cannot boot your computer successfully. These settings are more likely to configure a workable computer. They may not provide optimal performance, but are the most stable settings. You may use this option as a diagnostic aid if your system is behaving erratically. Select the Failsafe settings and then try to diagnose the problem after the computer boots.

If you select the **Load Failsafe Defaults** option, the following window displays:



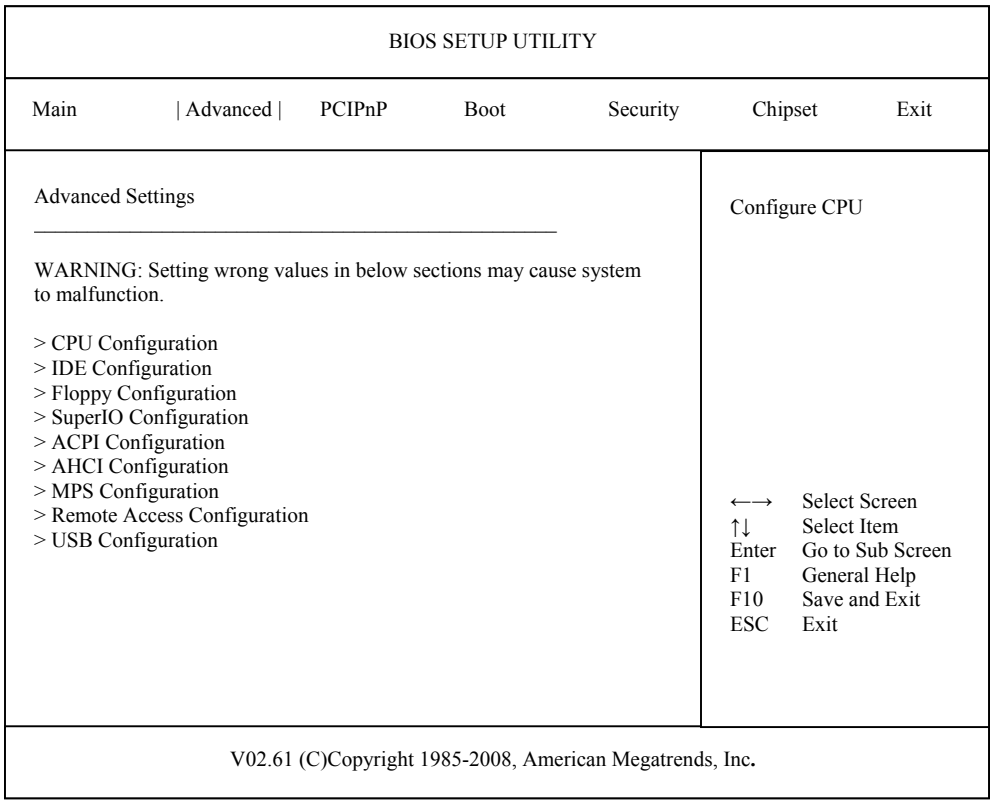

You have two options:

- Select **Ok** to load the Failsafe default settings.
- Select **Cancel** to leave the current values in effect.

# *Chapter 4 Advanced Setup*

### ADVANCED SETUP

When you select **Advanced** from the BIOS Setup Utility Main Menu, the following Setup screen displays:




When you display the Advanced Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Advanced Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

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**NOTE**: The **Floppy Configuration, SuperIO Configuration** & **Remote Access** menu options appear only if an I/O board such as the IOB30MC (6391-000) or IOB31 (6474-000) is connected to the SHB. Otherwise, these line items are not available. The values on the Advanced Setup subscreens do not necessarily reflect the values appropriate for your SHB. Refer to the explanations following each screen for specific instructions about entering correct information.

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### ADVANCED SETUP OPTIONS

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**NOTE**: Do *not* change the values for any Advanced Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

---

**CPU Configuration**
The **CPU Configuration** subscreen provides you with information about the processor in your system. The following options may be modified:

- CPU Configuration
    - Ratio CMOS setting
    - Hardware Prefetcher
    - Max CPUID Value Limit
    - PECI
    - Intel(R) SpeedStep(tm) tech

**IDE Configuration**
The options on the **IDE Configuration** subscreens allow you to set up or modify parameters for your IDE controller and hard disk drive(s). The following options may be modified:

- IDE Configuration
    - SATA#1 Configuration
        - Configure SATA#1 as
        - Max Ports on SATA#1
    - SATA#2 Configuration
    - Primary IDE Master/Primary IDE Slave
      Secondary IDE Master/Secondary IDE Slave
      Third IDE Master
      Fourth IDE Master
        - Type
        - LBA/Large Mode
        - Block (Multi-Sector Transfer)
        - PIO Mode
        - DMA Mode
        - S.M.A.R.T.
        - 32Bit Data Transfer
    - Hot Plug
    - Hard Disk Write Protect
    - IDE Detect Time Out (Sec)
    - ATA(PI) 80Pin Cable Detection

**Floppy Configuration**
The options on the **Floppy Configuration** subscreen allow you to set up or modify parameters for your floppy disk drive(s). The following options may be modified:

- Floppy A/Floppy B

**SuperIO Configuration**
The options on the **SuperIO Configuration** subscreen allow you to set up or modify parameters for your on-board peripherals. The following options may be modified:

- OnBoard Floppy Controller
- Serial Port1 Address/Serial Port2 Address
- Parallel Port Address
    - Parallel Port Mode
    - Parallel Port IRQ

**ACPI Configuration**
The **ACPI Configuration** subscreen allows you to set up or modify the following options:

- ACPI Configuration
    - General ACPI Configuration
        - Suspend Mode
        - Repost Video on S3 Resume
        - Power Supply Shutoff
    - Advanced ACPI Configuration
        - ACPI Version Features
        - ACPI APIC Support
        - AMI OEMB Table
        - Headless Mode
    - Chipset ACPI Configuration
        - APIC ACPI SCI IRQ
        - USB Device Wakeup From S3/S4

**AHCI Configuration**
The **ACPI Configuration** subscreen allows you to set up or modify the following options:

- AHCI
    - AHCI CD/DVD Boot Time out
    - AHCI Port 0
      AHCI Port 1
      AHCI Port 2
      AHCI Port 3
      AHCI Port 4
      AHCI Port 5

- SATA Port(x)
- S.M.A.R.T.

**MPS Configuration**
The **MPS Configuration** subscreen allows you to modify the following option:

- MPS Revision

**Remote Access Configuration**
The options on the **Remote Access Configuration** subscreen allow you to set up or modify parameters for configuring remote access type and parameters. The following options may be modified:

- Remote Access
- Serial Port Number
- Serial Port Mode
- Flow Control
- Redirection After BIOS POST
- Terminal Type
- VT-UTF8 Combo Key Support
- Sredir Memory Display Mode

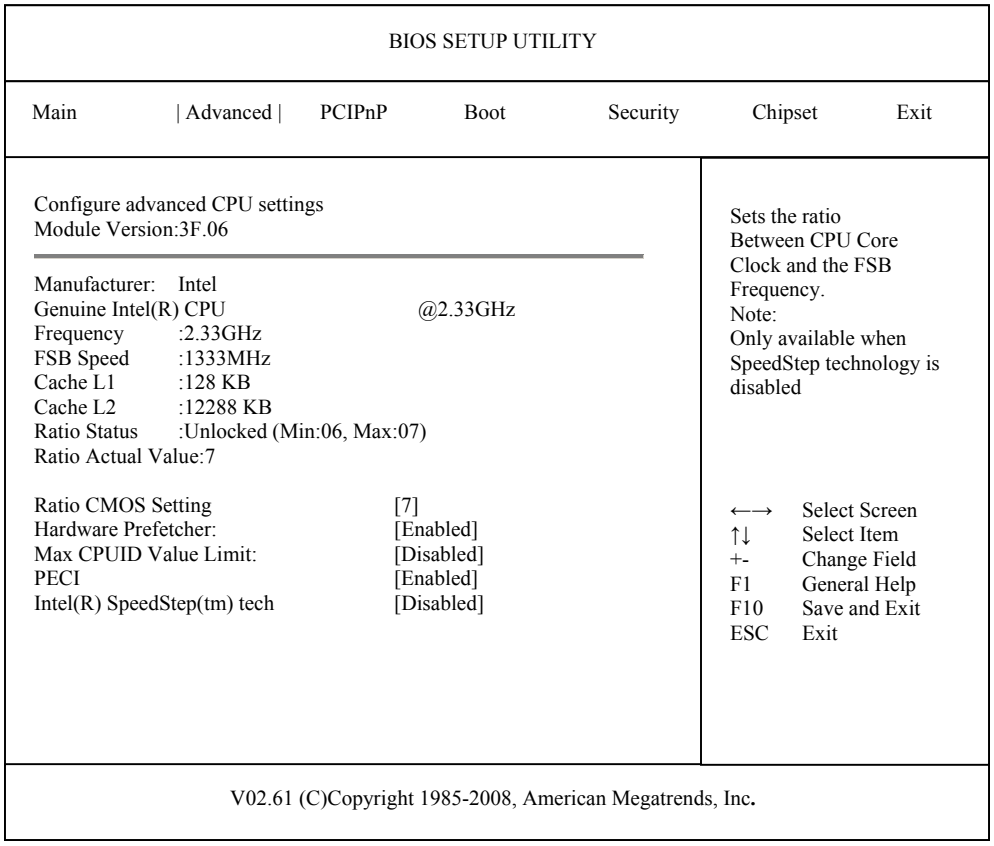
**USB Configuration**
The options on the **USB Configuration** subscreen allow you to set up or modify parameters for your on-board USB ports. The following options may be modified:

- Legacy USB Support
- Port 64/60 Emulation
- USB 2.0 Controller Mode
- BIOS EHCI Hand-Off

**Saving and Exiting**
When you have made all desired changes to **Advanced** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

### CPU CONFIGURATION SETUP

When you select **CPU Configuration** from the Advanced Setup Screen, the following Setup screen displays:




**CPU Configuration Screen**

When you display the CPU Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### CPU CONFIGURATION SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Advanced Setup. Once you change the settings, the new settings display each time Advanced Setup is run.

**Ratio CMOS Setting**

This option sets the ratio between the CPU Core Clock and the FSB Frequency. This is only available for modification when SpeedStep technology is disabled.

The Setup screen displays the system option:

**Ratio CMOS Setting: [x]**

**Hardware Prefetcher**

The Setup screen displays the system option:

**Hardware Prefetcher: [Enabled]**

Available options are:
Disabled
Enabled

**Max CPUID Value Limit**

The Setup screen displays the system option:

**Max CPUID Value Limit: [Disabled**]

Available options are:
Disabled
Enabled

**PECI**

The Setup screen displays the system option:

**PECI: [Enabled**]

Available options are:
Disabled
Enabled

**Intel(R) SpeedStep(tm) tech**

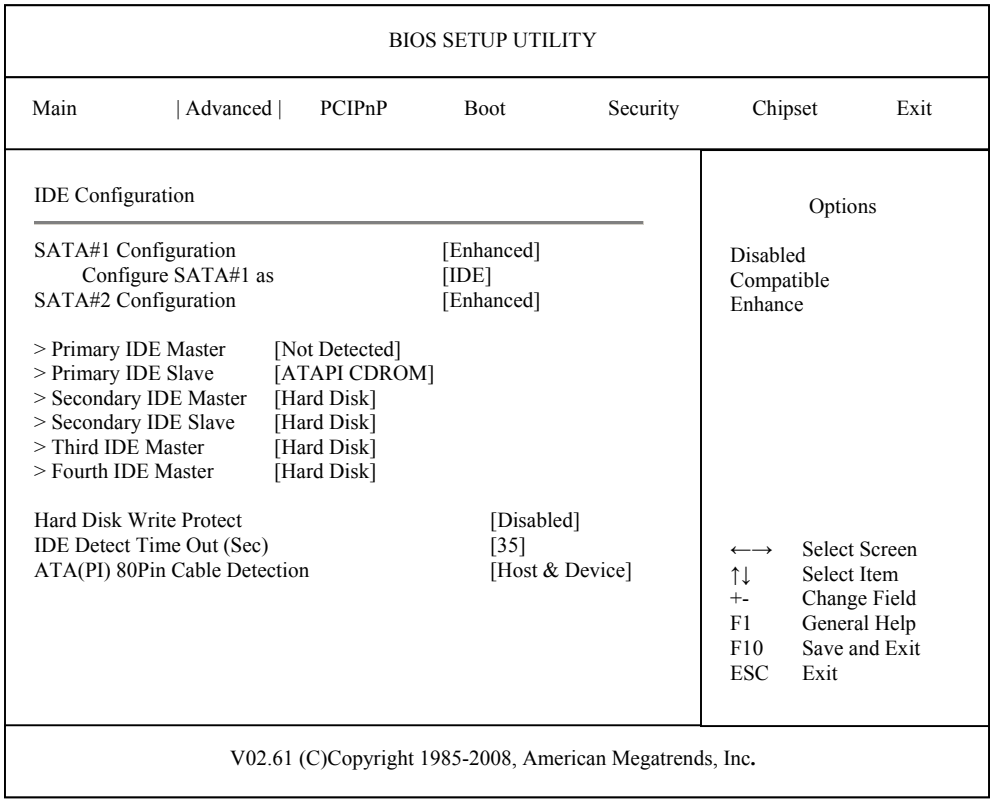
The Setup screen displays the system option:

**Intel(R) SpeedStep(tm) tech [Disabled]**

Available options are:
Disabled
Enabled

### IDE CONFIGURATION

When you select **IDE Configuration** from the Advanced Setup Menu, a Setup screen similar to the following displays:




**IDE Configuration Screen**

When you display the IDE Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

Some of the options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

### IDE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

#### SATA#1 Configuration

The Setup screen displays the system option:

**SATA#1 Configuration [Enhanced]**

Three options are available:

- Select **Disabled** to disable all ports. No drives are displayed on the screen..
- Select **Compatible** to allow up to four serial devices
- Select **Enhanced** to allow up to six serial devices, four onboard and two from links down to the backplane.

### Configure SATA As

This option allows you specify how to configure the available SATA devices. It is only available if the SATA#1 Configuration option is set to Compatible or Enhanced.

The Setup screen displays the system option:

**Configure SATA as [IDE]**

Three options are available:

- Select IDE to enable the SATA devices as IDE devices.
- Select RAID to enable the SATA devices as a RAID device. When RAID is selected:
    - The SATA#1 Configuration and SATA#2 Configuration screens disappear.
    - The Max Ports on Sata#1 appears with a default value of 6 ports. If this option is changed to 4 Ports the SATA#2 Configuration Screen reappears.
    - The Hot Plug Menu Displays below the Fourth IDE Master displays with a default value of Disabled.
- Select AHCI to enable Native Command Queuing (NCQ) and SATA hot plug capability. When AHCI is selected:
    - The SATA#1 Configuration and SATA#2 Configuration screens disappear.
    - The Max Ports on Sata#1 appears with a default value of 6 ports. If this option is changed to 4 Ports the SATA#2 Configuration Screen reappears.
    - The Hot Plug Menu Displays below the Fourth IDE Master displays with a default value of Disabled.

### SATA#2 Configuration

The Setup screen displays the system option:

**SATA#2 Configuration [Enhanced]**

Two options are available:

- Select **Disabled** to disable all ports. No drives are displayed on the screen.
- Select **Enhanced** to allow up to two from links down to the backplane.

**Primary IDE Master/Primary IDE Slave**
**Secondary IDE Master/Secondary IDE Slave**
**Third IDE Master**
**Fourth IDE Master**

The line items which display are determined by the settings of the **ATA/IDE Configuration**, **Configure SATA as**, **Configure SATA Channels** and **Legacy IDE Channels** options described above. The values for the line items depend on the devices detected by AMIBIOS.

The Setup screen displays the system options:

**Primary IDE Master [ATAPI CDROM]**
**Primary IDE Slave [Not Detected]**
**Third IDE Master [Not Detected]**
**Third IDE Slave [Not Detected]**
**Fourth IDE Master [Not Detected]**
**Fourth IDE Slave [Not Detected]**

This is an example of the screen. To view and/or change parameters for any of the devices, press **<Enter>** to proceed to the IDE Device Setup screen, which is described later in this section.

**Hard Disk Write Protect**
This option allows you to disable or enable device write protection. Write protection will be effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

**Hard Disk Write Protect [Disabled]**

Available options are:

Disabled
Enabled

**IDE Detect Time Out (Sec)**

This option allows you to select the time-out value (in seconds) for detecting an ATA/ ATAPI device.

The Setup screen displays the system option:

**IDE Detect Time Out (Sec) [35]**

Available options are:
0
5
10
15
20
25
30
35

**ATA(PI) 80Pin Cable Detection**

This option allows you to select the mechanism for detecting an 80-pin ATA(PI) cable.

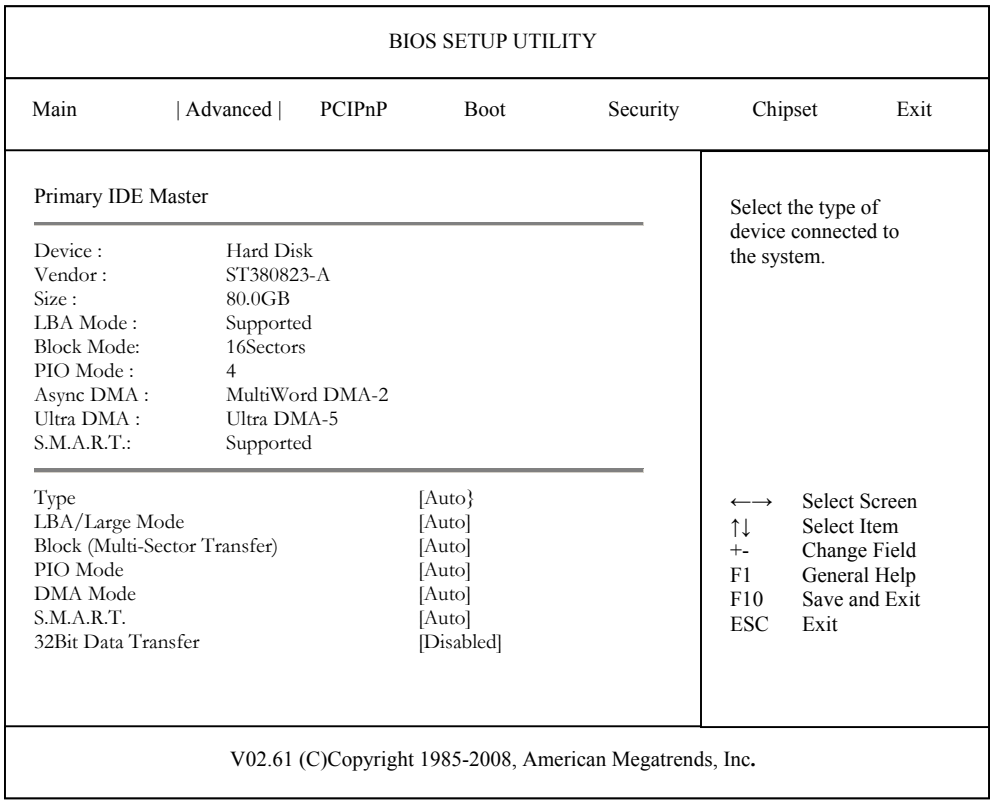
The Setup screen displays the system option:

**ATA(PI) 80Pin Cable Detection [Host & Device]**

Available options are:
Host & Device
Host
Device

### IDE DEVICE SETUP

When you select one of the IDE devices from the **IDE Configuration** screen, a Setup screen similar to the following displays:




**IDE Device Screen**

When you display the IDE Device subscreen, the format is similar to the sample shown above. The data displayed on the top portion of the screen details the parameters detected by AMIBIOS for the specified device and may not be modified. The data displayed on the bottom portion of the screen may be modified.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which AMIBIOS detected upon initial bootup.

### IDE DEVICE SETUP OPTIONS

The following options are available for each of the IDE devices on the primary and secondary IDE controllers:

**Type**

This option allows you to specify what type of device is on the IDE controller.

The Setup screen displays the system option:

**Type [Auto]**

Available options are:

Not Installed
Auto
CDROM
ARMD

If **Not Installed** is selected, the other options on the bottom portion of this screen do not display.

### LBA/Large Mode

This option allows you to enable IDE LBA (Logical Block Addressing) Mode for the specified IDE drive. Data is accessed by block addresses rather than by the traditional cylinder-head-sector format. This allows you to use drives larger than 528MB.

The Setup screen displays the system option:

**LBA/Large Mode [Auto]**

Two options are available:

- Select **Disabled** to have AMIBIOS use the physical parameters of the hard disk and do no translation to logical parameters. The operating system which uses the parameter table will then see only 528MB of hard disk space even if the drive contains more than 528MB.
- Select **Auto** to enable LBA mode and translate the physical parameters of the drive to logical parameters. LBA Mode must be supported by the drive and the drive must have been formatted with LBA Mode enabled.

### Block (Multi-Sector Transfer) Mode

This option supports transfer of multiple sectors to and from the specified IDE drive. Block mode boosts IDE drive performance by increasing the amount of data transferred during an interrupt.

If **Block Mode** is set to **Disabled**, data transfers to and from the device occur one sector at a time.

The Setup screen displays the system option:

**Block (Multi-Sector Transfer) [Auto]**

Available options are:
Disabled
Auto

**PIO Mode**

IDE Programmed I/O (PIO) Mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Set the **PIO Mode** option to **Auto** to have AMIBIOS select the PIO mode used by the IDE drive being configured. If you select a specific value for the PIO mode, you must make *absolutely* certain that you are selecting the PIO mode supported by the IDE drive being configured.

The Setup screen displays the system option:

**PIO Mode [Auto]**

Available options are:

Auto
0
1
2
3
4

**DMA Mode**

This option allows you to select DMA Mode for the device.

The Setup screen displays the system option:

**DMA Mode [Auto]**

Available options are:

Auto
SWDMA0 (SingleWord DMA 0 - 2)
SWDMA1
SWDMA2
MWDMA0 (MultiWord DMA 0 - 2)
MWDMA1
MWDMA2
UDMA0 (UltraDMA 0 - 6)
UDMA1
UDMA2
UDMA3
UDMA4
UDMA5
UDMA6

**S.M.A.R.T.**

This option allows AMIBIOS to use the SMART (Self-Monitoring Analysis and Reporting Technology) protocol for reporting server system information over a network.

The Setup screen displays the system option:

**S.M.A.R.T. [Auto]**

Available options are:

Auto
Disabled
Enabled

**32Bit Data Transfer**
If the **32Bit Data Transfer** parameter is set to **Enabled**, AMIBIOS enables 32-bit data transfers. If the host controller does not support 32-bit transfer, this feature *must* be set to **Disabled**.

The Setup screen displays the system option:

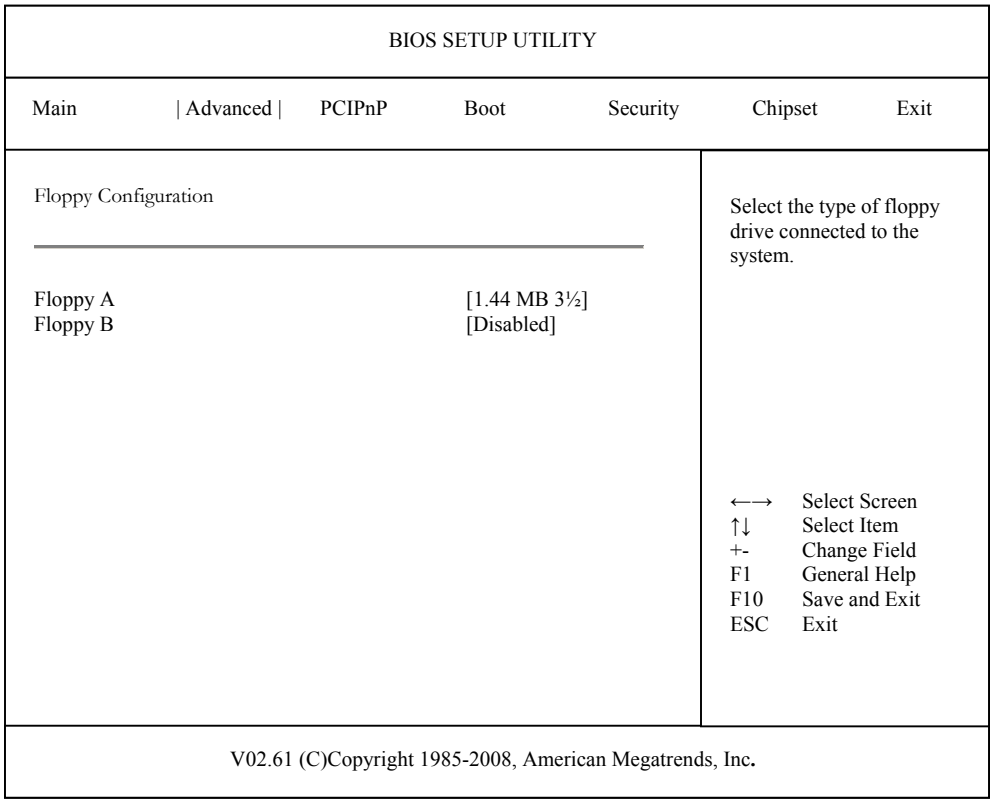
**32Bit Data Transfer [Disabled]**

Available options are:

Disabled
Enabled

### FLOPPY CONFIGURATION

When you select **Floppy Configuration** from the Advanced Setup Menu, the following Setup screen displays. This menu is only available if an IOB module is installed.




**Floppy Configuration Screen**

When you display the Floppy Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

---

**NOTE**: The **Floppy Configuration** subscreen is available only if an I/O board such as the IOB30MC (6391-000) or IOB31 (6474-000) is connected to the SHB.

---

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which AMIBIOS detected upon initial bootup.

### FLOPPY CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**Floppy A/Floppy B**

The floppy drive(s) in your system can be configured using these options. The **Disabled** option can be used for diskless workstations.

The Setup screen displays the system options:

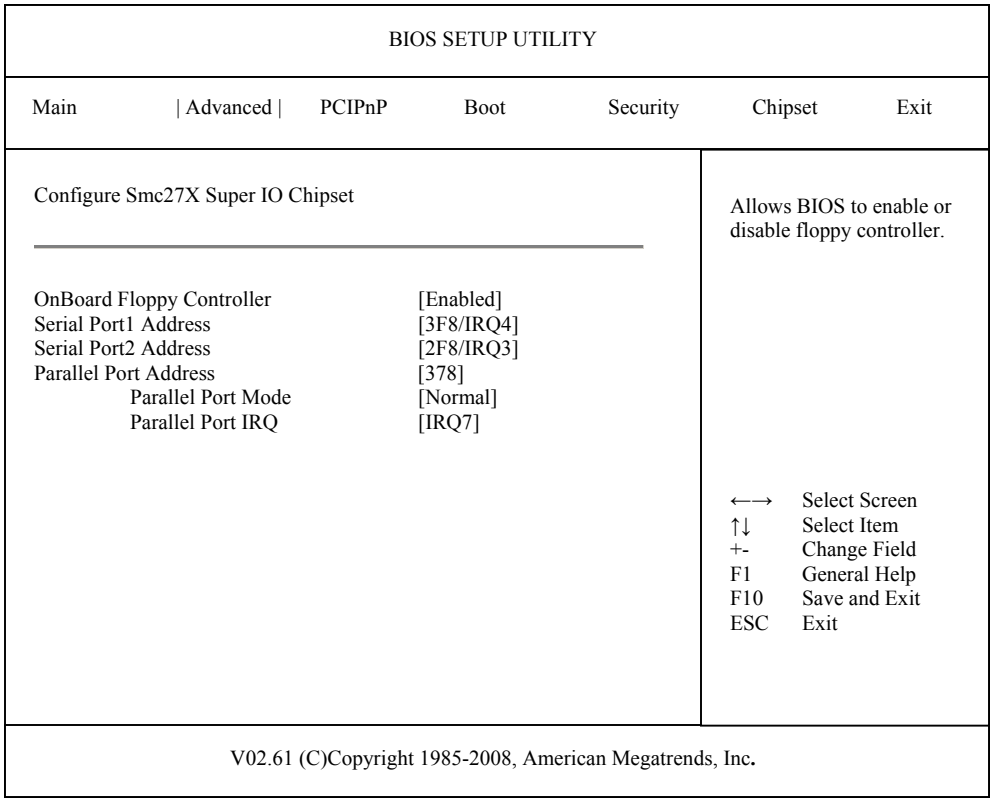
**Floppy A [1.44 MB 3½"]**
**Floppy B [Disabled]**

Available options are:

Disabled
360 KB 5¼"
1.2 MB 5¼"
720 KB 3½"
1.44MB 3½"
2.88MB 3½"

### SUPERIO CONFIGURATION

When you select **SuperIO Configuration** from the Advanced Setup Menu, the following Setup screen displays. This menu is only available if an IOB module is installed.




**SuperIO Configuration Screen**

When you display the SuperIO Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

**NOTE**: The **SuperIO Configuration** subscreen is available only if an I/O board such as the IOB30MC (6391-000) or IOB31 (6474-000) is connected to the SHB.

### SUPERIO CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**OnBoard Floppy Controller**

The on-board floppy drive controller may be enabled or disabled using this option.

The Setup screen displays the system option:

**OnBoard Floppy Controller [Enabled]**

Available options are:

Disabled
Enabled

**Serial Port1 Address/Serial Port2 Address**

Each of these options enables the specified serial port on the SBC and establishes the base I/O address and the number of the interrupt request for the port.

The Setup screen displays the system option:

**Serial Port1 Address [3F8/IRQ4]**
**Serial Port2 Address [2F8/IRQ3]**

Available options are:

Disabled
3F8/IRQ4
3E8/IRQ4
2F8/IRQ3
2E8/IRQ3

---

**NOTE:** The values available for each on-board serial port may vary, depending on the setting previously selected for the other on-board serial port and any off-board serial ports. If an I/O address is assigned to another serial port, AMIBIOS automatically omits that address from the values available.

---

If the system has off-board serial ports which are configured to specific starting I/O ports via jumper settings, AMIBIOS configures the on-board serial ports to avoid conflicts.

When AMIBIOS checks serial ports, any off-board serial ports found are left at their assigned addresses. Serial Port1, the first on-board serial port, is configured with the first available address and Serial Port2, the second on-board serial port, is configured with the next available address. The default address assignment order is 3F8H, 2F8H, 3E8H, 2E8H. Note that this same assignment order is used by AMIBIOS to place the active serial port addresses in lower memory (BIOS data area) for configuration as logical COM devices.

For example, if there is one off-board serial port and its address is set to 2F8H, Serial Port1 is assigned address 3F8H and Serial Port2 is assigned address 3E8H. Configuration is then as follows:

COM1 - Serial Port1 (at 3F8H)
COM2 - off-board serial port (at 2F8H)
COM3 - Serial Port2 (at 3E8H)

**Parallel Port Address**

This option enables the parallel port on the SBC and establishes the base I/O address for the port.

The Setup screen displays the system option:

**Parallel Port Address [378]**

Available options are:

Disabled
378
278
3BC

When AMIBIOS checks for parallel ports, any off-board parallel ports found are left at their assigned addresses. The on-board Parallel Port is automatically configured with the first available address not used by an off-board parallel port.

If this option is set to **Disabled**, the **Parallel Port Mode** and **Parallel Port IRQ** options are not available.

**Parallel Port Mode**

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes which adhere to the IEEE P1284 specifications. If the **Parallel Port Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

**Parallel Port Mode [Normal]**

Four options are available:

- Select **Normal** to use normal parallel port mode.
- Select **Bi-Directional** to use bi-directional parallel port mode.
- Select **EPP** to allow the parallel port to be used with devices which adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
- Select **ECP** to allow the parallel port to be used with devices which adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5MB/second. ECP provides symmetric bidirectional communication.

When you select **ECP** mode, the **ECP Mode DMA Channel** line item displays. Valid DMA channel options are DMA1 and DMA3; the default is DMA3.

### Parallel Port IRQ

This option specifies the interrupt request (IRQ) which is used by the parallel port. If the **Parallel Port Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

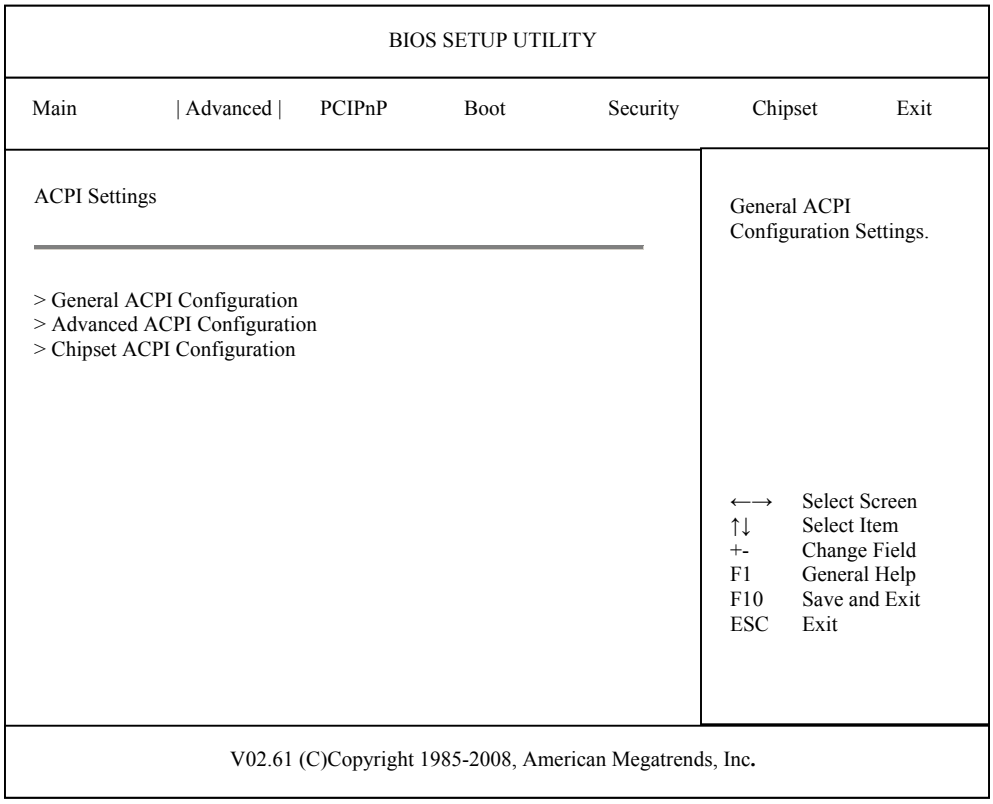
**Parallel Port IRQ [IRQ7]**

Available options are:

IRQ5
IRQ7

### ACPI CONFIGURATION

When you select **ACPI Configuration** from the Advanced Setup Menu, the following Setup screen displays:




**ACPI Configuration Screen**

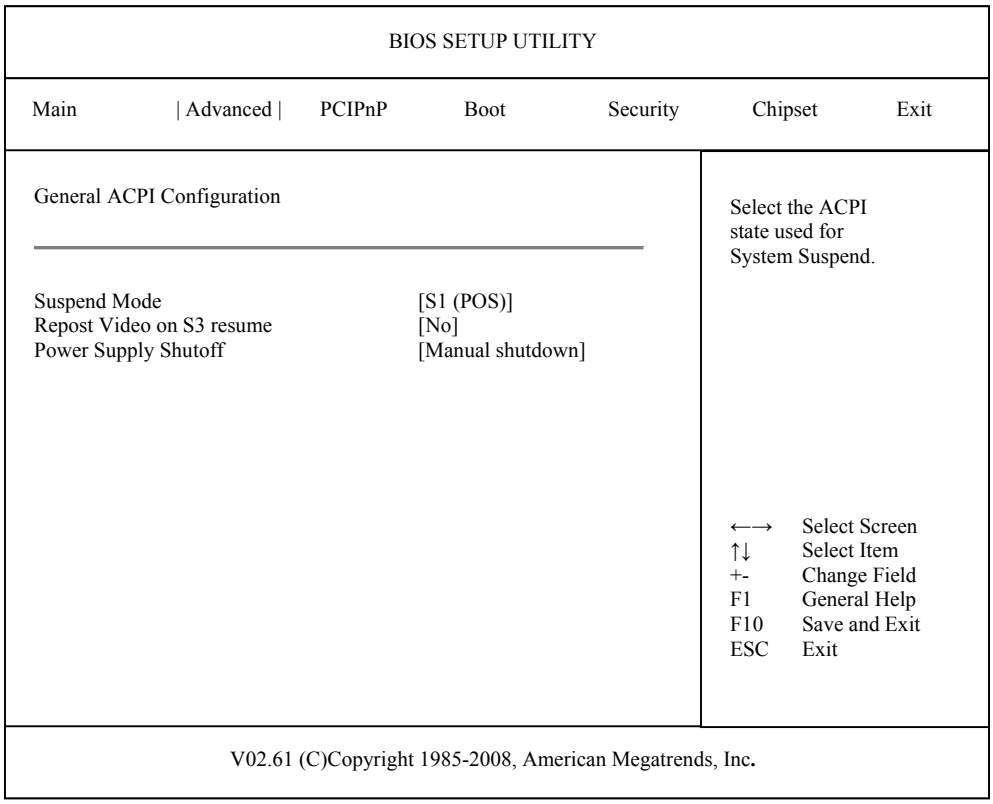
When you display the ACPI Configuration screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the ACPI Configuration options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

The subscreens allow you to set up or modify the following options:

- General ACPI Configuration
  - Suspend Mode
  - Repost Video on S3 Resume
  - Power Supply Shutoff
- Advanced ACPI Configuration
  - ACPI 2.0 Features
  - ACPI APIC Support
  - AMI OEMB Table
  - Headless Mode
- Chipset ACPI Configuration
  - APIC ACPI SCI IRQ
  - USB Device Wakeup From S3/S4

### GENERAL ACPI CONFIGURATION

When you select **General ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:




**General ACPI Configuration Screen**

When you display the General ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### GENERAL ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**Suspend Mode**

The Setup screen displays the system option:

**Suspend Mode [S1 (POS)]**

Available options are:

S1 (POS)
S3 (STR)
Auto

If you select any value other than **S1 (POS)**, the following option is added to the screen.

**Repost Video on S3 Resume**

If the **Suspend Mode** option is set to **S1(POS)**, this option is not available.

The Setup screen displays the system options:

**Repost Video on S3 Resume [No]**

Available options are:

No
Yes

**Power Supply Shutoff**

This option should be set to **Auto** if the power supply can turn off automatically on Windows shutdown.

The Setup screen displays the system option:

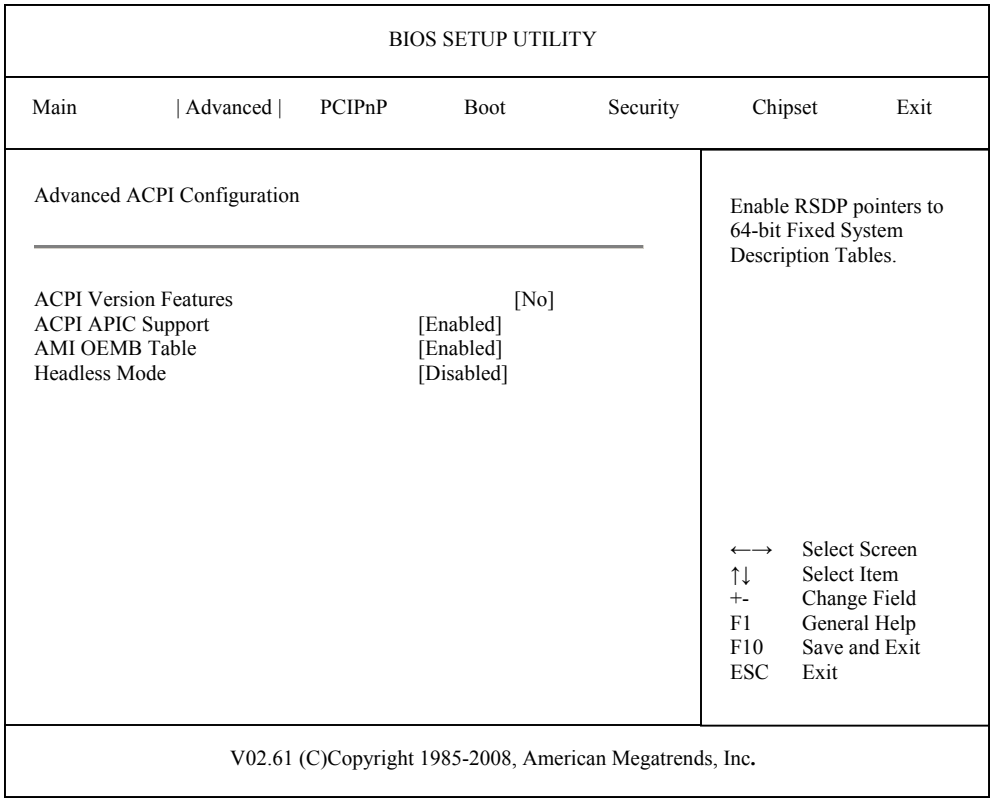
**Power Supply Shutoff [Manual shutdown]**

Two options are available:

- Select **Auto** to have the system automatically shut down when commanded by the operating system.
- Select **Manual shutdown** to require that the user manually shut down the system. After successful shutdown, the system displays the message "It is now safe to turn off your computer." The power supply may then be turned off manually.

### ADVANCED ACPI CONFIGURATION

When you select **Advanced ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:




**Advanced ACPI Configuration Screen**

When you display the Advanced ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### ADVANCED ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**ACPI Version Features**

The Setup screen displays the system option:

**ACPI Version Features [ACPI v1.0]**

Available options are:

ACPI v1.0
ACPI v2.0
ACPI v3.0

**ACPI APIC Support**

The Setup screen displays the system option:

**ACPI APIC Support [Enabled]**

Available options are:
Disabled
Enabled

**AMI OEMB Table**

The Setup screen displays the system option:

**AMI OEMB Table [Enabled]**

Available options are:
Disabled
Enabled

**Headless Mode**

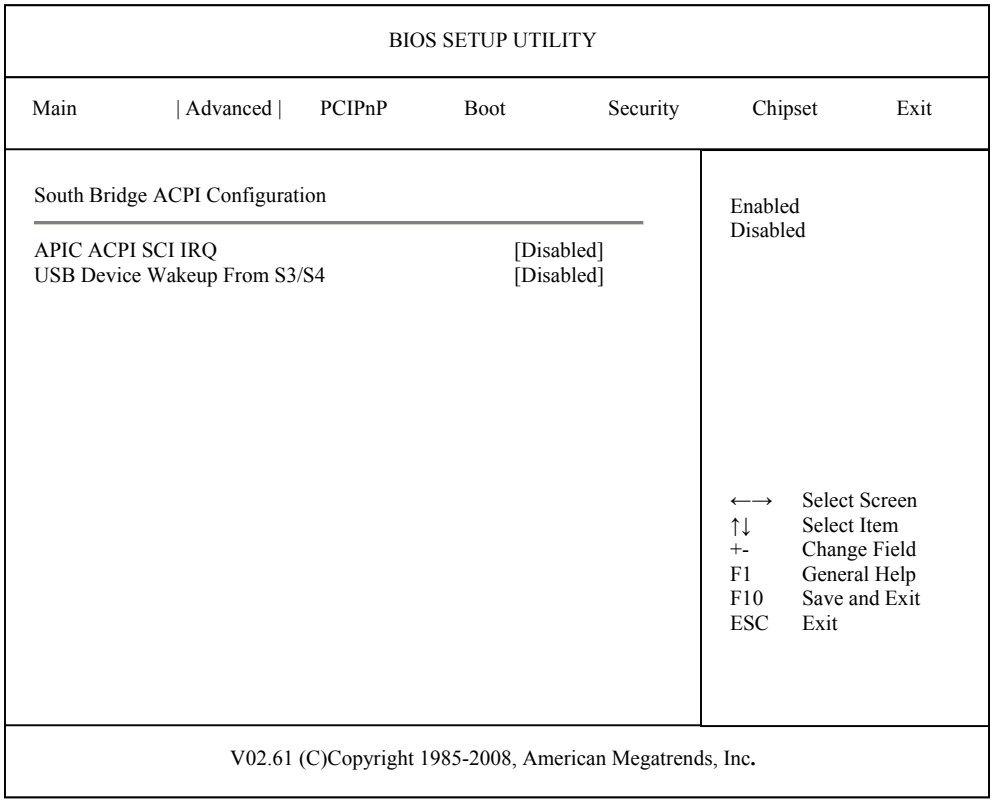
The Setup screen displays the system option:

**Headless Mode [Disabled]**

Available options are:
Disabled
Enabled

### CHIPSET ACPI CONFIGURATION

When you select **Chipset ACPI Configuration** from the ACPI Configuration Menu, the following Setup screen displays:




**Chipset ACPI Configuration Screen**

When you display the Chipset ACPI Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### CHIPSET ACPI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**APIC ACPI SCI IRQ**

The Setup screen displays the system option:

**APIC ACPI SCI IRQ [Disabled]**

Available options are:

Disabled
Enabled

**USB Device Wakeup From S3/S4**

The Setup screen displays the system option:

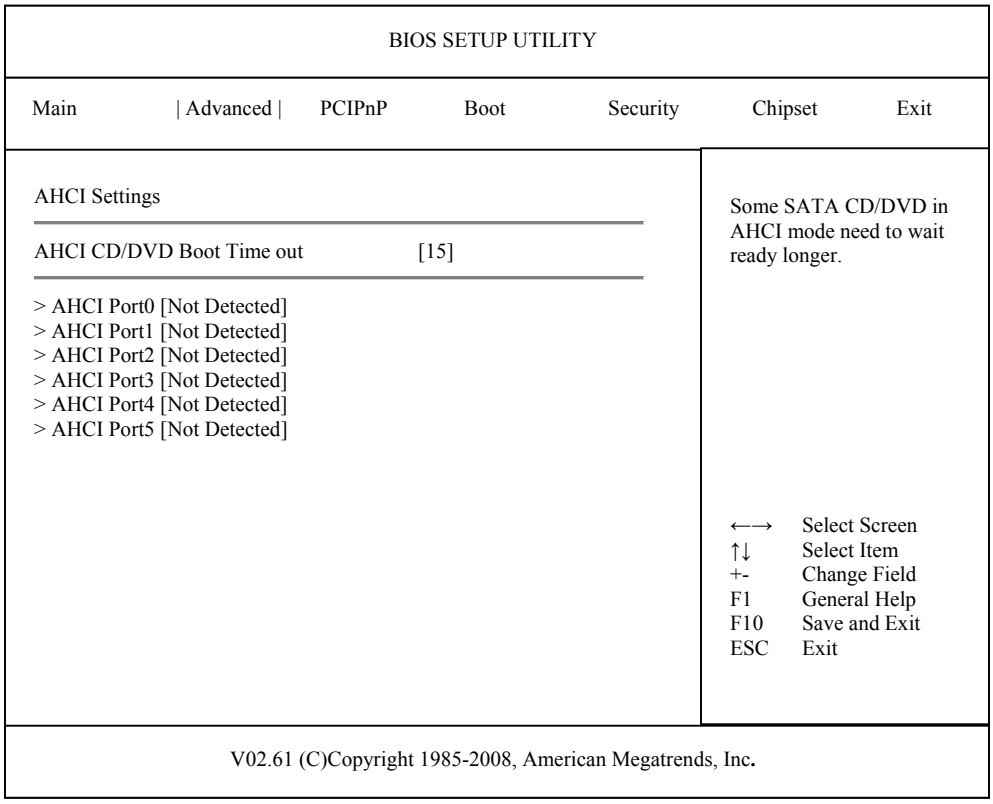
**USB Device Wakeup From S3/S4 [Disabled]**

Available options are:

Disabled
Enabled

### AHCI CONFIGURATION

When you select **AHCI Configuration** from the Advanced Setup Menu, the following Setup screen displays:




**AHCI Configuration Screen**

When you display the AHCI Configuration screen, the format is similar to the sample shown above. You may highlight the option you wish to change, press enter to display the available options and then press **<Enter>** again to accept the highlighted value you chose.

Other options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

### AHCI CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**AHCI CD/DVD Boot Time out**

The Setup screen displays the system option:

**AHCI CD/DVD Boot Time out [15]**

Available Options are:

0
5
10
15
20
25
30
35

**AHCI PORT 0, 1, 2, 3, 4, 5, 6**

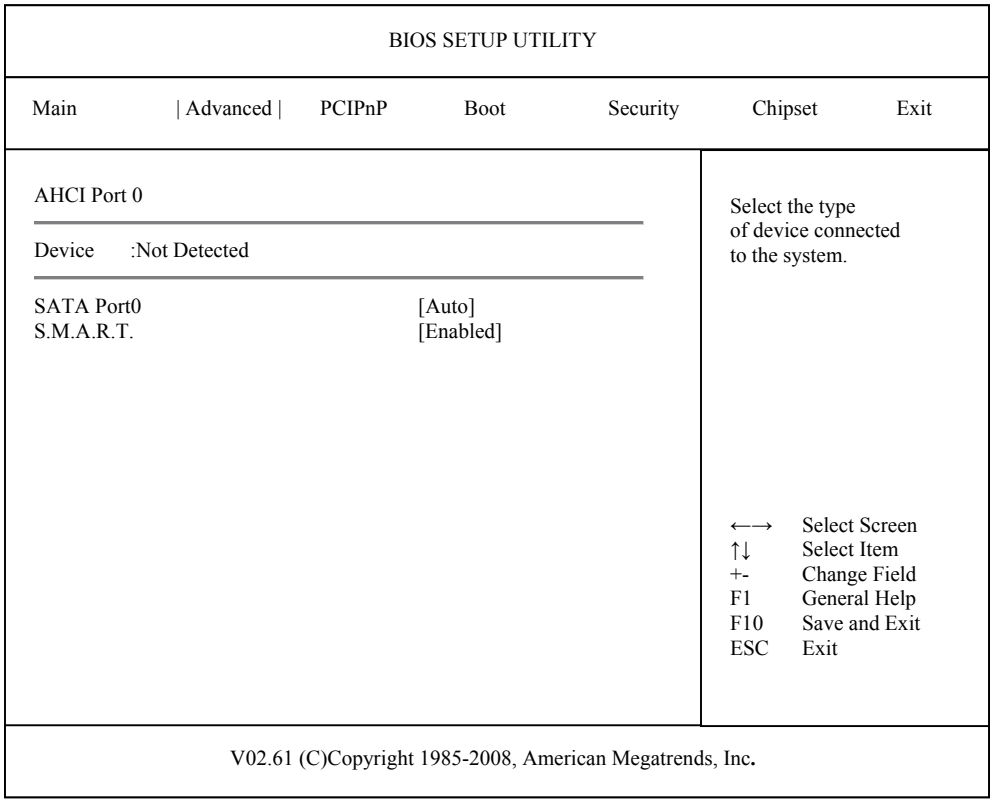
The Setup screen displays the system options:

**AHCI Port 0 [Not Detected]**
**AHCI Port 1 [Not Detected]**
**AHCI Port 2 [Not Detected]**
**AHCI Port 3 [Not Detected]**
**AHCI Port 4 [Not Detected]**
**AHCI Port 5 [Not Detected]**

This is an example of the screen. To view and/or change parameters for any of the devices, press <ENTER> to proceed to the IDE Device Setup screen.

### AHCI PORT CONFIGURATION

When you select an **AHCI Port x** option from the **AHCI Configuration Menu**, the following Setup screen will display for each **AHCI Port x** option:




**AHCI Port Configuration Screen**

When you display the AHCI Port Configuration screen **for any of the 6 AHCI Ports listed on the AHCI Configuration screen**, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### AHCI PORT CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run. The AHCI Port screen is the same for all 6 AHCI Ports listed on the AHCI Configuration screen.

**SATA Port0**

The Setup screen displays the system option:

**SATA Port0 [Disabled]**

Available options are:

Auto
Not Installed

**S.M.A.R.T.**

The Setup screen displays the system option:

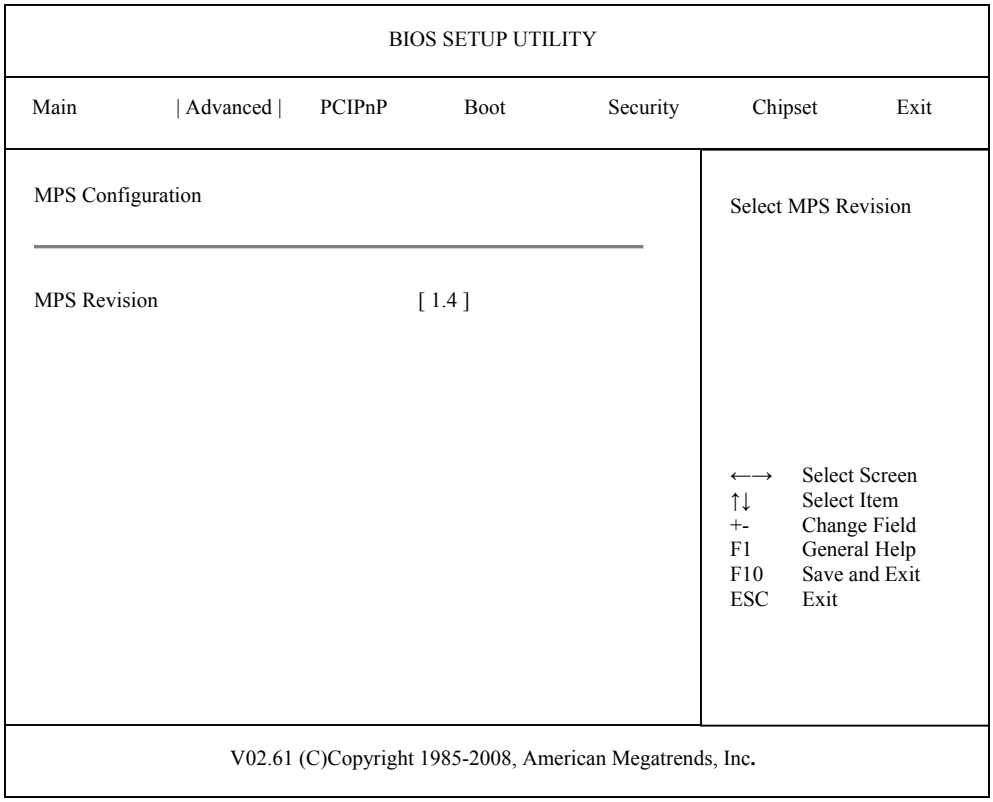
**S.M.A.R.T. [Enabled]**

Available options are:

Disabled
Enabled

### MPS CONFIGURATION

When you select **MPS Configuration** from the Advanced Setup Screen, the following Setup screen displays:




**MPS Configuration Screen**

When you display the MPS Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### MPS CONFIGURATION SETUP OPTIONS

The description for the system option listed below shows the value as it appears if you have not yet run Advanced Setup. Once you change the setting, the new setting displays each time Advanced Setup is run.

**MPS Revision**

The Setup screen displays the system option:

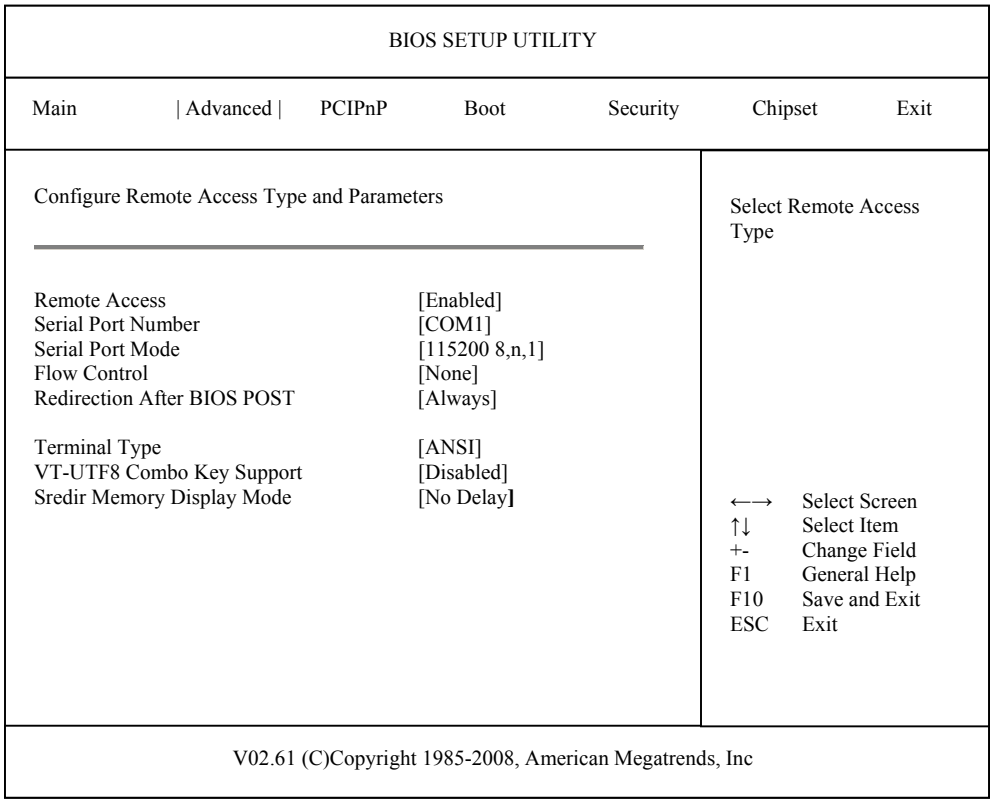
**MPS Revision [1.4**]

Available options are:

1.1
1.4

### REMOTE ACCESS CONFIGURATION

When you select **Remote Access Configuration** from the Advanced Setup Menu, the following Setup screen displays. This menu is only available if an IOB module has been installed.




**Remote Access Configuration Screen**

When you display the Remote Access Configuration screen, the format is similar to the sample shown above if you have enabled **Remote Access**. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

---

**NOTE**: The **Remote Access** options on this subscreen are only accessible if an I/O board such as the IOB30MC (6391-000) or IOB31 (6474-000) is connected to the SHB.

---

### REMOTE ACCESS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Advanced Setup. Once values have been defined, they display each time Advanced Setup is run.

**Remote Access**

This option allows you to use a terminal connected to a serial port on an I/O expansion board to control changes to the BIOS settings.

The sample above shows the appearance of the screen if **Remote Access** is set to **Enabled**. If this option is set to **Disabled**, which is the default, the other options on this screen do not display.

The Setup screen displays the system option:

**Remote Access [Enabled]**

Available options are:

Disabled
Enabled

**Serial Port Number**

This option specifies the serial port on which remote access is to be enabled. If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Serial Port Number [COM1]**

Available options are:
COM1
COM2

**Serial Port Mode**

This option specifies settings for the serial port on which remote access is enabled. The settings indicate baud rate, eight bits per character, no parity and one stop bit. If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Serial Port Mode [115200 8,n,1]**

Available options are:
115200 8,n,1
57600 8,n,1
38400 8,n,1
19200 8,n,1
09600 8,n,1

**Flow Control**

This option allows you to select flow control for console redirection.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Flow Control [None]**

Available options are:

None
Hardware
Software

**Redirection After BIOS POST**

This option specifies when redirection should be active.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Redirection After BIOS POST [Always]**

Three options are available:

- Select **Disabled** to turn off the redirection after POST.
- Select **Boot Loader** to keep redirection active during POST and during Boot Loader.
- Select **Always** to always keep redirection active. Note that some operating systems may not work properly if this option is set to **Always**.

**Terminal Type**

This option allows you to select the target terminal type.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Terminal Type [ANSI]**

Available options are:

ANSI
VT100
VT-UTF8

**VT-UTF8 Combo Key Support**

This option allows you to enable VT-UTF8 combination key support for ANSI or VT100 terminals.

If the **Remote Access** option is set to **Disabled** or the **Terminal Type** option is set to **VT-UTF8**, this option is not available.

The Setup screen displays the system option:

**VT-UTF8 Combo Key Support [Enabled]**

Available options are:
Disabled
Enabled

**Sredir Memory Display Mode**

This option indicates the delay in seconds to display memory information.

The Setup screen displays the system option:

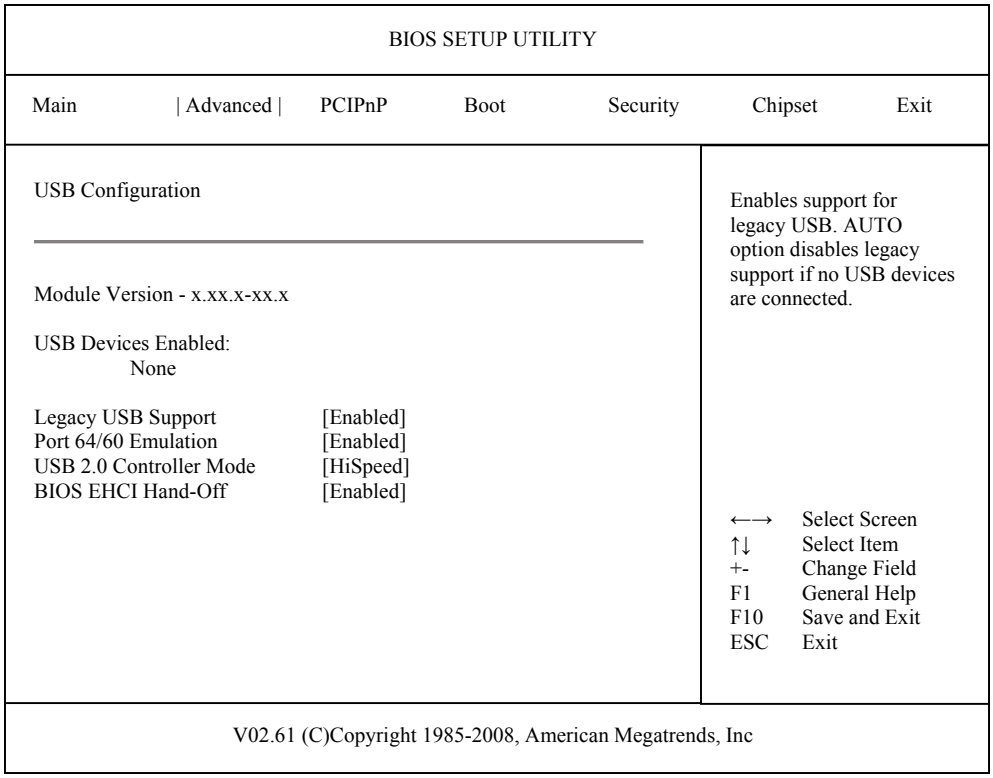
**Sredir Memory Display Mode [No Delay]**

Available options are:

No Delay
Delay 1 Sec
Delay 2 Sec
Delay 4 Sec

### USB CONFIGURATION

When you select **USB Configuration** from the Advanced Setup Menu, the following Setup screen displays:




**USB Configuration Screen**

When you display the USB Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### USB CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

**Legacy USB Support**

This option allows you to enable support for older USB devices. The **Auto** option disables legacy support if no USB devices are connected. If this option is set to **Disabled**, the remaining three options are not available.

The Setup screen displays the system option:

**Legacy USB Support [Enabled]**

Available options are:

Disabled
Enabled
Auto

**Port 64/60 Emulation**

This option allows you to enable or disable I/O port 60h/64h emulation support. This option should be set to **Enabled** for complete USB keyboard legacy support for operating systems which are not USB-aware. If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Port 64/60 Emulation [Enabled]**

Available options are:

Disabled
Enabled

**USB 2.0 Controller Mode**

This option configures the USB 2.0 controller to high-speed (480Mbps) or full-speed (12Mbps) mode. If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:
**USB 2.0 Controller Mode [HiSpeed]**

Available options are:

FullSpeed
HiSpeed

**BIOS EHCI Hand-Off**
This option is a work-around for operating systems without EHCI hand-off support. If the **Legacy USB Support** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**BIOS EHCI Hand-Off [Enabled]**

Available options are:
Disabled
Enabled

# *Chapter 5 Plug and Play Setup*

### PLUG AND PLAY SETUP

When you select **PCIPnP** from the BIOS Setup Utility Main Menu, the following Setup screen displays:

BIOS SETUP UTILITY

Main | Advanced | PCIPnP | Boot | Security | Chipset | Exit

Advanced PCI/PNP Setup

WARNING: Setting wrong values in below sections may cause system to malfunction.

| | |
|---|---|
| Clear NVRAM | [No] |
| Plug & Play O/S | [No] |
| PCI Latency Timer | [64] |
| Allocate IRQ to PCI VGA | [Yes] |
| Palette Snooping | [Disabled] |
| PCI IDE BusMaster | [Enabled] |
| OffBoard PCI/ISA IDE Card | [Auto] |
| OffBoard PCI IDE Primary IRQ | [Disabled] |
| OffBoard PCI IDE Secondary | [Disabled] |
| Onboard LAN Controllers | [Both LAN0 & LAN1 E] |
| Onboard LAN Boot ROM | [Disabled] |
| Backplane ISA Bridge Support | [Disabled] |
| Backplane IRQ routing as | [Secondary] |
| IRQ3 | [Available] |
| IRQ4 | [Available] |
| IRQ5 | [Available] |
| IRQ7 | [Available] |
| IRQ9 | [Available] |
| IRQ10 | [Available] |
| IRQ11 | [Available] |
| IRQ14 | [Available] |
| IRQ15 | [Available] |
| DMA Channel 0 | [Available] |
| DMA Channel 1 | [Available] |
| DMA Channel 3 | [Available] |
| DMA Channel 5 | [Available] |
| DMA Channel 6 | [Available] |
| DMA Channel 7 | [Available] |
| Reserved Memory Size | [Disabled] |
| Reserved Memory Address | [C8000] |

Clear NVRAM during System Boot

| | |
|---|---|
| ←→ | Select Screen |
| ↑↓ | Select Item |
| +- | Change Field |
| F1 | General Help |
| F10 | Save and Exit |
| ESC | Exit |

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**PCIPnP Setup Screen**

When you display the PCIPnP Setup screen, the format is similar to the sample shown above, except the screen does not display all of the options at one time. If you need to change other options, use the down arrow key to locate the appropriate option. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

---

**NOTE:** The values on the PCIPnP Setup screen do not necessarily reflect the values appropriate for your SHB. Refer to the explanations below for specific instructions about entering correct information.

---

### PCIPnP Setup Options

The descriptions for the system options listed below show the values as they appear if you have not yet run PCIPnP Setup. Once values have been defined, they display each time PCIPnP Setup is run.

---

**NOTE**: Do not change the values for any PCIPnP Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

---

**Clear NVRAM**

This option allows you to clear NVRAM during system boot.

The Setup screen displays the system option:

**Clear NVRAM [No]**

Available options are:
No
Yes

**Plug & Play O/S**

This option indicates whether or not the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP adapter cards which are required for system boot. An operating system which is PnP-aware detects and enables all other PnP-aware adapter cards. Set this option to **No** if the operating system (such as DOS or OS/2) does *not* use PnP.

---

**NOTE:** You *must* set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

---

The Setup screen displays the system option:

**Plug & Play O/S [No]**

Two options are available:

- Select **No** to allow AMIBIOS to configure the devices in the system.

- Select **Yes** if your system has a Plug and Play operating system and you want to allow the operating system to configure all Plug and Play (PnP) devices which are not required for bootup.

### PCI Latency Timer

This option specifies the latency of all PCI devices on the PCI Local Bus. The settings are in units equal to PCI clocks.

The Setup screen displays the system option:

**PCI Latency Timer [64]**

Available options are:

| | |
|---|---|
| 32 | 160 |
| 64 | 192 |
| 96 | 224 |
| 128 | 248 |

### Allocate IRQ to PCI VGA

This option allows you to assign an IRQ to a PCI VGA card if the card requests an IRQ.

The Setup screen displays the system option:

**Allocate IRQ to PCI VGA [Yes]**

Available options are:

Yes
No

### Palette Snooping

This option, when set to **Enabled**, indicates to the PCI devices that a graphics device is installed in the system so the card will function correctly.

The Setup screen displays the system option:

**Palette Snooping [Disabled]**

Available options are:

Disabled
Enabled

### PCI IDE BusMaster

This option specifies whether the IDE controller on the PCI Local Bus has bus mastering capability for reading and writing to IDE drives. The IDE drive(s) must support PCI bus mastering.

The Setup screen displays the system option:

**PCI IDE BusMaster [Disabled]**

Available options are:

Disabled
Enabled

**OffBoard PCI/ISA IDE Card**

This option specifies the PCI expansion slot on the SHB where the off-board PCI IDE controller is installed, if any.

The Setup screen displays the system option:

**OffBoard PCI/ISA IDE Card [Auto]**

Available options are:

Auto
PCI Slot1
PCI Slot2
PCI Slot3
PCI Slot4
PCI Slot5
PCI Slot6

If you select any value other than **Auto**, the following options and their default values are added to the screen:

**OffBoard PCI IDE Primary IRQ/OffBoard PCI IDE Secondary**

These options specify the PCI interrupts used by the primary and secondary IDE channels on the off-board PCI IDE controller. You may use the **INTA**, **INTB**, **INTC** and **INTD** options to assign IRQs to the Int Pin used by the specified channel. If the **OffBoard PCI/ISA IDE Card** option is set to **Auto**, these options are not available.

The Setup screen displays the system options:

**OffBoard PCI IDE Primary IRQ [Disabled]**
**OffBoard PCI IDE Secondary [Disabled]**

Available options are:

Disabled
INTA
INTB
INTC
INTD
Hardwired

### Onboard LAN Controllers

This option indicates which LAN devices are to be enabled.

---

**NOTE:** When the setting for this option has been changed and saved, the system should be powered down and powered up in order for the new setting to take effect.

---

The Setup screen displays the system option:

**Onboard LAN Controllers [Both LAN0 & LAN1 E]**

Available options are:

Both LAN0 & LAN1 Enabled (default)
Both LAN0 & LAN1 Disabled

### Onboard LAN Boot ROM

This option, when set to **Enabled**, indicates that the option ROM for the on-board Gigabit LANs is to be executed. This option should remain **Disabled** if you are not booting from a LAN device.

The Setup screen displays the system option:

**Onboard LAN Boot ROM [Disabled]**

Available options are:

Disabled
Enabled

### Backplane ISA Bridge Support

The Setup screen displays the system option:

**Backplane ISA Bridge Support [Disabled]**

Available options are:

Disabled
Enabled

### Backplane IRQ routing as

The Setup screen displays the system option:

**Backplane IRQ routing as [Secondary]**

Available options are:

Primary
Secondary

**IRQ3/IRQ4/IRQ5/IRQ7/IRQ9/IRQ10/IRQ11/IRQ14/IRQ15**

These options indicate whether the specified interrupt request (IRQ) is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices. This allows you to specify IRQs for use by legacy adapter cards.

The IRQ setup options indicate whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices.

The Setup screen displays the system option:

**IRQ# [Available]**

where # is the number of the interrupt request (IRQ)

Two options are available:

- Select **Available** to make the specified IRQ available for use by PCI/PnP devices. •
- Select **Reserved** to reserve the specified IRQ for use by legacy devices.

**DMA Channels 0, 1, 3, 5, 6 and 7**

These options indicate whether the specified DMA channel is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices.

The Setup screen displays the system option:

**DMA Channel # [Available]**

where # is the DMA Channel number

Two options are available:

- **Available** indicates that the specified DMA channel is available for use by PCI/PnP devices.
- **Reserved** indicates the specified DMA channel is reserved for use by legacy devices.

**Reserved Memory Size**

This option specifies the size of the memory area reserved for legacy devices. If this option is set to **Disabled**, the **Reserved Memory Address** option is not available.

The Setup screen displays the system option:

**Reserved Memory Size [Disabled]**

Available options are:

Disabled
16k
32k
64k

**Reserved Memory Address**

This option specifies the beginning address (in hexadecimal) of the ROM memory area reserved for use by legacy devices. If the **Reserved Memory Size** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

**Reserved Memory Address [C8000]**

Available options are:

| | |
|---|---|
| C0000 | D0000 |
| C4000 | D4000 |
| C8000 | D8000 |
| CC000 | DC000 |

**Saving and Exiting**
When you have made all desired changes to **PCIPnP** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

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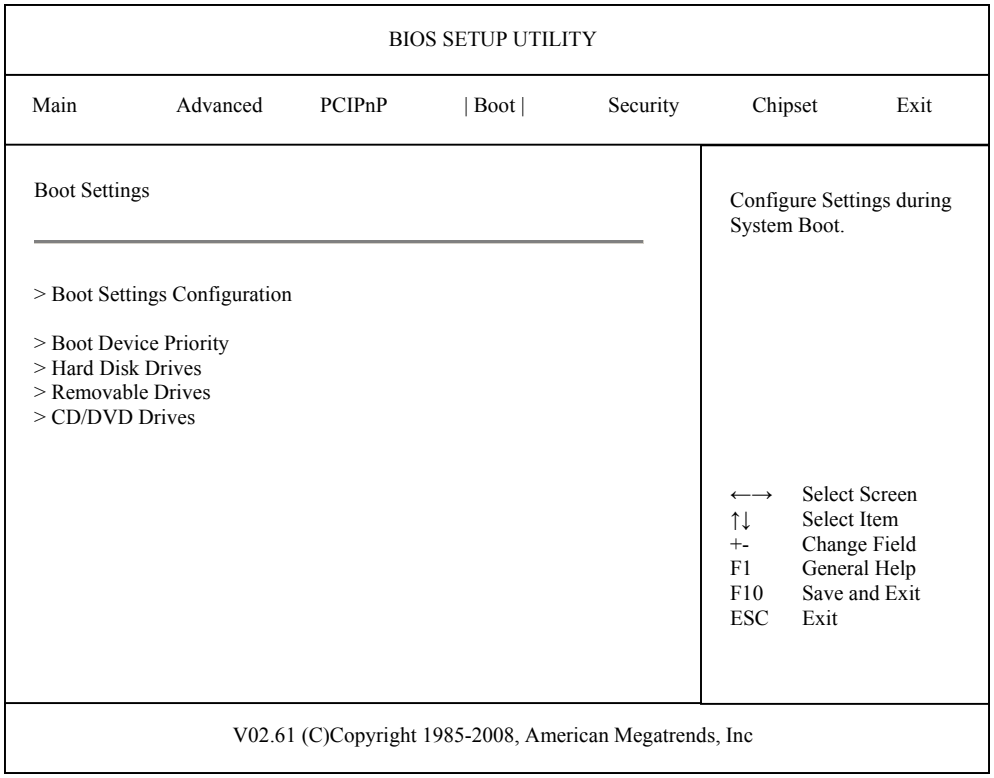
# *Chapter 6 Boot Setup*

## BOOT SETUP




**Boot Setup Screen**

When you display the Boot Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Boot Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

---

**NOTE:** If no device is found for one of the device types, the line item for that device type does not display.

---

### BOOT SETUP OPTIONS

The descriptions for the system option listed below show the values as they appear if you have not yet run Boot Setup. Once values have been changed, they display each time Boot Setup is run. You may also continue to subscreens to specify boot parameters and the boot sequence of bootable devices in your system.

### Boot Settings Configuration

The options on the **Boot Settings Configuration** subscreen allow you to set up or modify parameters for boot procedures.

The following options may be modified:

- Quick Boot
- Quiet Boot
- AddOn ROM Display Mode
- Bootup Num-Lock
- PS/2 Mouse Support
- Wait For 'F1' If Error
- Hit 'DEL' Message Display
- Interrupt 19 Capture

### Boot Device Priority

The options on the **Boot Device Priority** subscreen specify the order in which AMIBIOS attempts to boot devices available in the system. It allows you to select the drive which will be booted first, second, third, etc.

### Hard Disk Drives

The **Hard Disk Drives** subscreen specifies the boot sequence of the hard drives available in the system.

### Removable Drives

The **Removable Drives** subscreen specifies the boot sequence of the removable devices available in the system.

### CD/DVD Drives

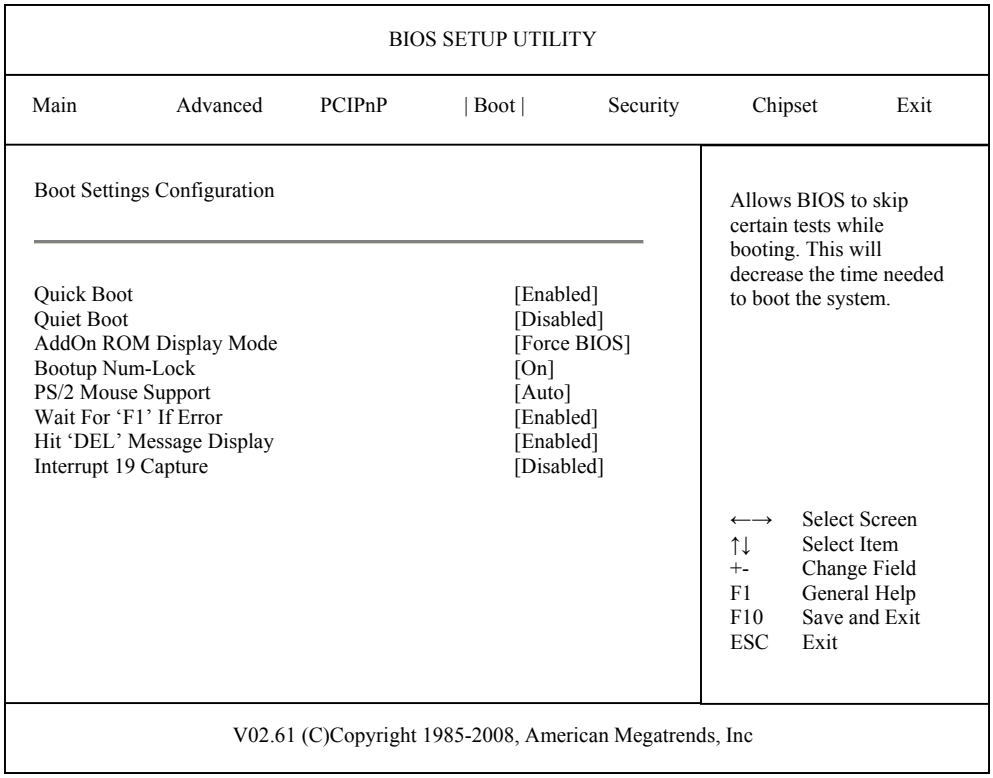
The **CD/DVD Drives** subscreen specifies the boot sequence of the CDROM and DVD devices available in the system.

### Saving and Exiting

When you have made all desired changes to **Boot** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

### BOOT SETTING CONFIGURATION

When you select **Boot Settings Configuration** from the Boot Setup Menu, the following Setup screen displays:




**Boot Settings Configuration Screen**

When you display the Boot Settings Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### BOOT SETTINGS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

#### Quick Boot

This option allows you to have the AMIBIOS boot quickly when the computer is powered on or go through more complete testing. If you set the **Quick Boot** option to **Enabled**, the BIOS skips certain tests while booting and decreases the time needed to boot the system.

The Setup screen displays the system option:

**Quick Boot [Disabled]**

Available options are:

Disabled
Enabled

**Quiet Boot**

This option specifies what will be displayed on the screen while the system is performing the POST routines when the computer is powered on or a soft reboot is performed.

The Setup screen displays the system option:

**Quiet Boot [Disabled]**

Two options are available:

- Select **Disabled** to display normal POST messages.
- Select **Enabled** to display the OEM logo instead of the POST messages.

**AddOn ROM Display Mode**

This option specifies the system display mode which is set at the time the AMIBIOS post routines initialize an optional option ROM.

The Setup screen displays the system option:

**AddOn ROM Display Mode [Force BIOS]**

Two options are available:

Select **Force BIOS** to use the display mode currently being used by AMIBIOS.
Select **Keep Current** to use the current display mode.

**BootUp Num-Lock**

This option enables you to turn off the Num-Lock option on the enhanced keyboard when the system is powered on. If Num-Lock is turned off, the arrow keys on the numeric keypad can be used, as well as the other set of arrow keys on the enhanced keyboard.

The Setup screen displays the system option:

**BootUp Num-Lock [On]**

Available options are:

Off
On

**PS/2 Mouse Support**

This option indicates whether or not a PS/2-type mouse is supported.

The Setup screen displays the system option:

**PS/2 Mouse Support [Auto]**

Available options are:

Auto
Disabled
Enabled

**Wait For 'F1' If Error**

Before the system boots up, the AMIBIOS executes the Power-On Self Test (POST) routines, a series of system diagnostic routines. If any of these tests fail but the system can still function, a non-fatal error has occurred. The AMIBIOS responds with an appropriate error message followed by:

**Press F1 to RESUME**

If this option is set to **Disabled**, a non-fatal error does not generate the "Press F1 to RESUME" message. The AMIBIOS still displays the appropriate message, but continues the booting process without waiting for the **<F1>** key to be pressed. This eliminates the need for any user response to a non-fatal error condition message. Non-fatal error messages are listed in *Appendix A - BIOS Messages*.

The Setup screen displays the system option:

**Wait For 'F1' If Error [Enabled]**

Available options are:
Disabled
Enabled

**Hit 'DEL' Message Display**

The "Hit DEL to run Setup" message displays when the system boots up. Disabling this option prevents the message from displaying.

The Setup screen displays the system option:

**Hit 'DEL' Message Display [Enabled]**

Available options are:
Disabled
Enabled

**Interrupt 19 Capture**

This option allows option ROMs to trap Interrupt 19.

The Setup screen displays the system option:

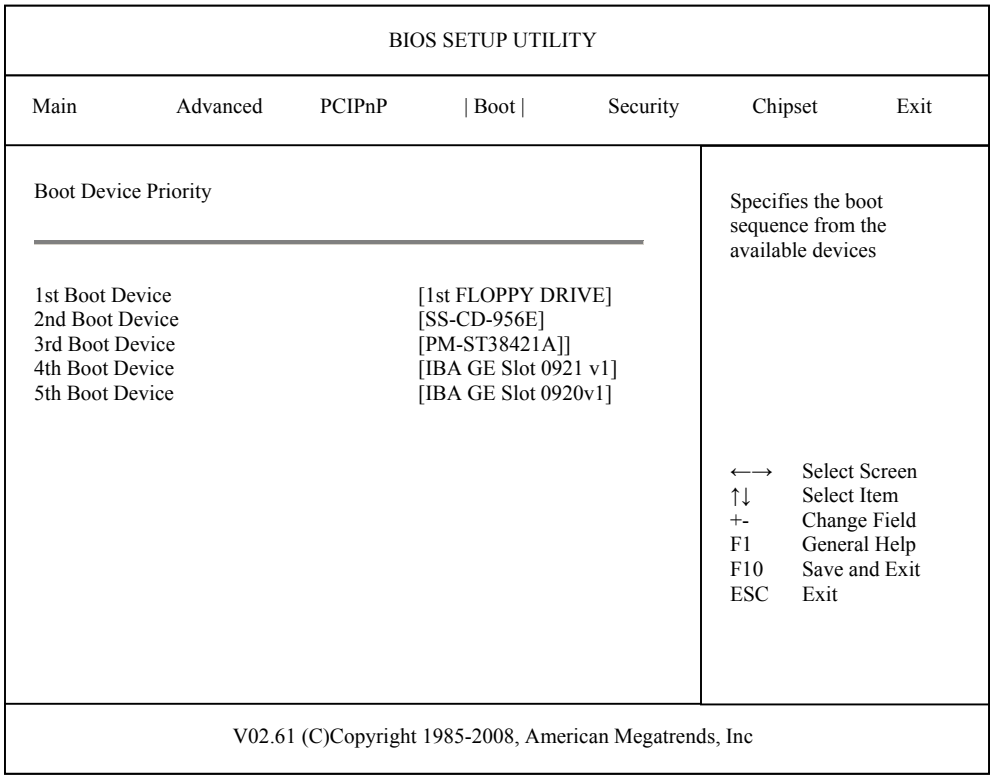
**Interrupt 19 Capture [Disabled]**

Available options are:

Disabled
Enabled

### BOOT DEVICE PRIORITY

When you select **Boot Device Priority** from the Boot Setup Menu, a Setup screen similar to the following displays:




**Boot Device Priority Screen**

When you display the Boot Device Priority screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

**NOTE:** The number of line items on this screen may vary depending on the number of bootable devices available on your system.

### BOOT DEVICE PRIORITY OPTIONS

**1st Boot Device through 5th Boot Device**

These options specify the order in which AMIBIOS attempts to boot the devices after the POST routines complete. The setting for each boot device line item is the description of the bootable device. The number of line items on this screen is dynamic. If new system devices are added, the new devices are displayed at the end of the list as additional line items.

The SHB supports bootup from a LAN device. In the sample screen above, the 4th Boot Device and 5th Boot Device line items are boot from LAN options.

The Setup screen displays the system option(s):

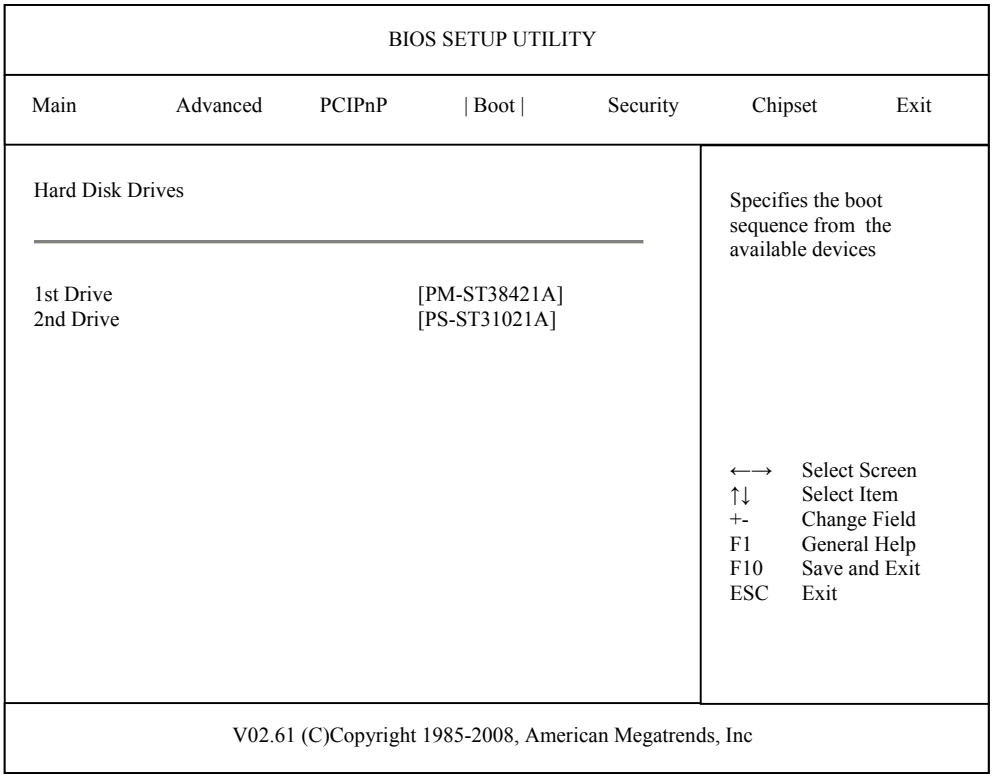
**### Boot Device [xxxxxxxxx]**

where ### is the boot order and xxxxxxxxx is the description of the device.

**NOTE: Disabled** is also available as an option if you do not want a particular device to be included in the boot sequence. Setting a device to **Disabled** will eliminate unnecessary delays during the bootup process.

### HARD DISK DRIVES

When you select **Hard Disk Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:




**Hard Disk Drives Screen**

When you display the Hard Disk Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

**NOTE:** The number of line items on this screen is determined by the number of hard disk drives available.

### HARD DISK DRIVES OPTIONS

The SHB supports up to four hard disk drives through a primary and secondary controller in a master/slave configuration.

#### 1st Drive/2nd Drive

When the system boots up, it searches for all hard drives and displays the description of each disk drive it has detected.

If you have more than one hard disk drive, you may change the order in which the system will attempt to boot the available hard drives by changing these line items. The number of options displayed for each line item depends on the number of hard disk drives in your system.

**Disabled** is also available as an option if you do not want a particular drive to be included in the boot sequence.

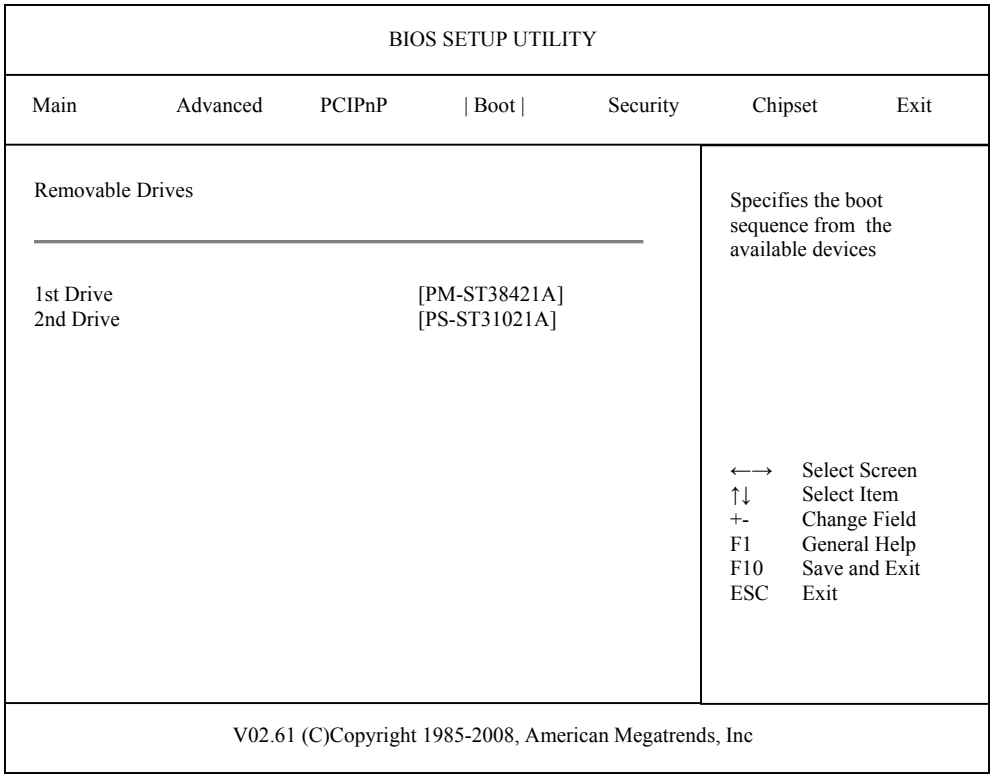
The Setup screen displays the system option(s):

**### Drive [xxxxxxxxx]**

where ### is the boot order and xxxxxxxxx is the description of the hard disk drive.

### REMOVABLE DRIVES

When you select **Removable Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:




**Removable Drives Screen**

When you display the Removable Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

---

**NOTE:** The number of line items on this screen is determined by the number of removable devices available.

---

### REMOVABLE DRIVE OPTIONS

The SHB supports multiple removable drives and allows you to change the boot sequence of these devices.

**1st Drive/2nd Drive**

When the system boots up, it searches for all removable devices and displays the description of each device it has detected.

If you have more than one removable device, you may change the order in which the system will attempt to boot the available devices by changing these line items. The number of options displayed for each line item depends on the number of removable devices in your system.

**Disabled** is also available as an option if you do not want a particular device to be included in the boot sequence.

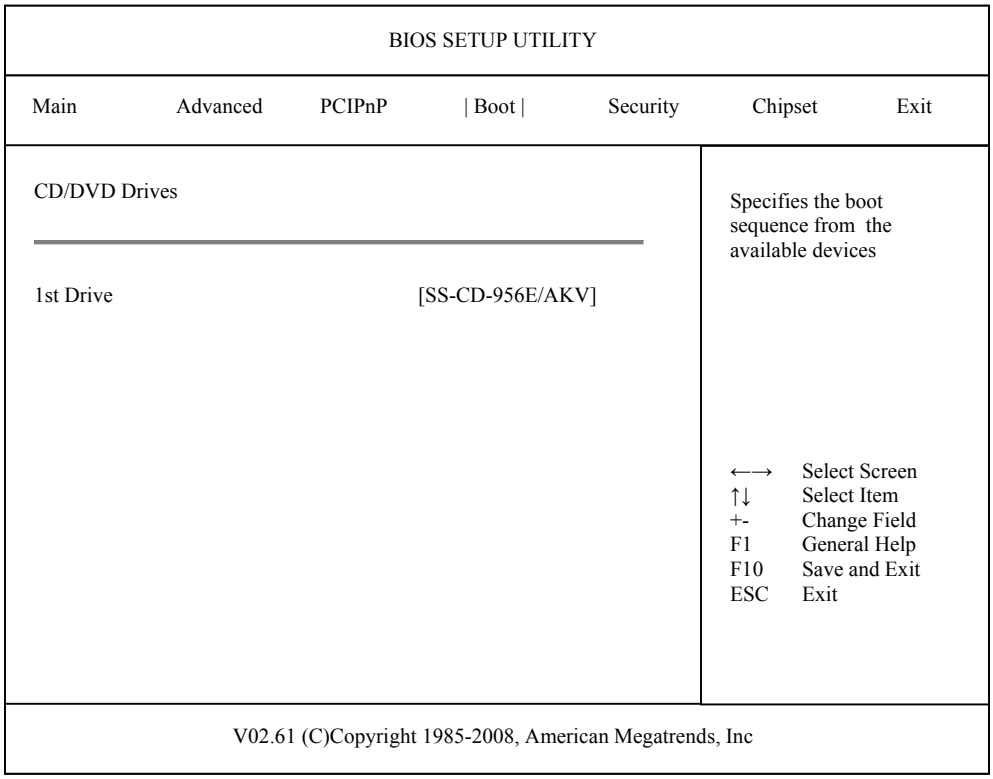
The Setup screen displays the system option(s):

**### Drive [xxxxxxxxx]**

where ### is the boot order and xxxxxxxxx is the description of the removable drive.

### CD/DVD DRIVES

When you select **CD/DVD Drives** from the Boot Setup Menu, a Setup screen similar to the following displays:




**CD/DVD Drives Screen**

When you display the CD/DVD Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

**NOTE:** The number of line items on this screen is determined by the number of CDROM and DVD drives available.

### CD/DVD DRIVE OPTIONS

The SHB supports multiple CDROM and DVD devices and allows you to change the boot sequence of these devices.

**1st Drive/2nd Drive**

When the system boots up, it searches for all CDROM and DVD drives and displays the description of each drive it has detected.

If you have more than one ATAPI CDROM drive, you may change the order in which the system will attempt to boot the available drives by changing these line items. The number of options displayed for each line item depends on the number of CDROM and DVD devices in your system.

**Disabled** is also available as an option if you do not want a particular drive to be included in the boot sequence.

The Setup screen displays the system option:

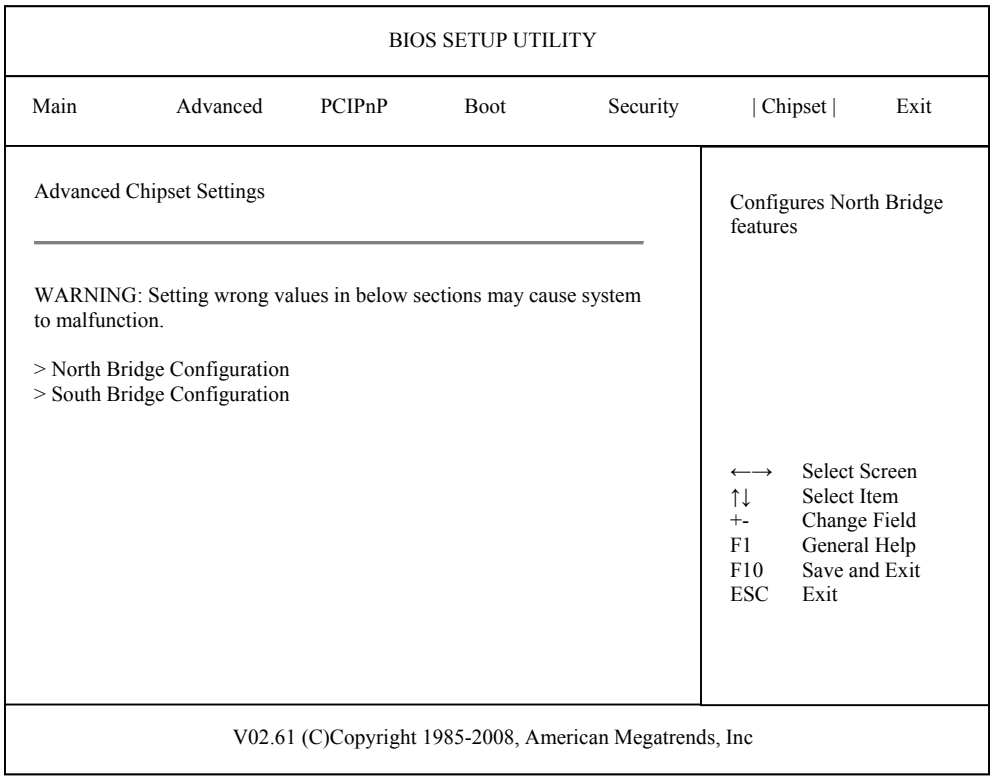
**### Drive [xxxxxxxxx]**

where ### is the boot order and xxxxxxxxx is the description of the CDROM or DVD drive.

# *Chapter 7 Chipset Setup*

## CHIPSET SETUP

When you select **Chipset** from the BIOS Setup Utility Main Menu, the following Setup screen displays:




**Chipset Setup Screen**

When you display the Chipset Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Chipset Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

---

**NOTE**: The values on the Chipset Setup subscreens do not necessarily reflect the values appropriate for your SHB. Refer to the explanations following the screens for specific instructions about entering correct information.

---

## CHIPSET SETUP OPTIONS

---

**NOTE**: Do *not* change the values for any Chipset Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

---

### North Bridge Configuration

The options on the **North Bridge Configuration** subscreen allow you to set up or modify parameters to configure the Intel® North Bridge chip.

The following options may be modified:

- Memory Remap Feature
- Initiate Graphic Adapter
- Internal Graphics Mode Select

### South Bridge Configuration

The options on the **South Bridge Configuration** subscreen allow you to set up or modify parameters to configure the Intel® South Bridge chip.

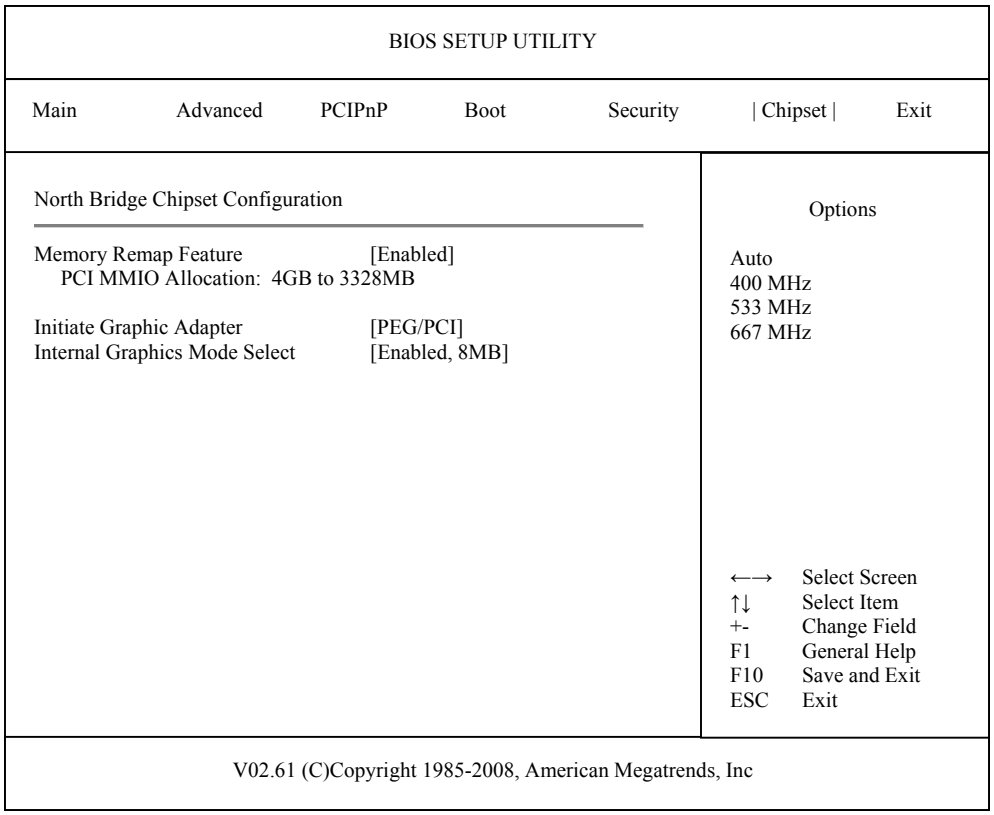
The following options may be modified:

- USB Functions
- USB Port Configure
- USB 2.0 Controller
- SMBUS Controller
- Restore on AC Power Loss

**Saving and Exiting** When you have made all desired changes to **Chipset** Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

### NORTH BRIDGE CONFIGURATION

When you select **North Bridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:




**North Bridge Configuration Screen**

When you display the North Bridge Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### NORTH BRIDGE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

#### Memory Remap Feature

The Setup screen displays the system option:

**Memory Remap Feature [ Enabled]**

Available options are:

Disabled
Enabled

**Initiate Graphic Adapter**

The Setup screen displays the system option:

**Initiate Graphic Adapter [PEG/PCI]**

Available options are:

IGD
PCI/IGD
PCI/PEG
PEG/IGD
PEG/PCI

**Internal Graphic Mode Select**

The Setup screen displays the system option:

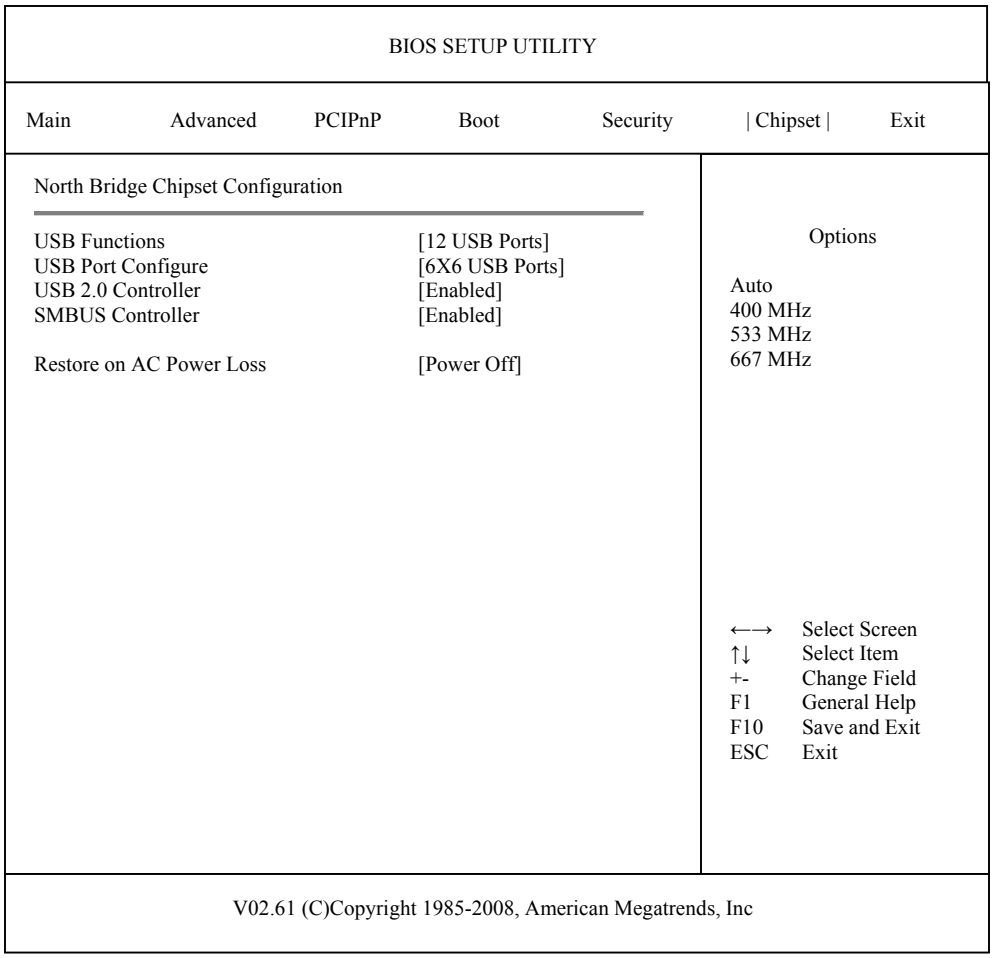
**Internal Graphic Mode Select [Enabled, 8MB]**

Available options are:

Enabled, 1MB
Enabled, 8MB

### SOUTH BRIDGE CONFIGURATION

When you select **South Bridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:




**South Bridge Configuration Screen**

When you display the South Bridge Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

### SOUTH BRIDGE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

**USB Functions**

This option specifies the number of Universal Serial Bus (USB) ports to be used.

The Setup screen displays the system option:

**USB Functions [12 USB Ports]**

Available options are:

Disabled
2 USB Ports
4 USB Ports
6 USB Ports
8 USB Ports
10 USB Ports
12 USB Ports

**USB Port Configure**

This Option is not visible if USB Functions is set to Disabled.

The Setup screen displays the system option:

**USB Port Configure [6X6 USB Ports]**

Available options are:
6X6 USB Ports
8X4 USB Ports

**USB 2.0 Controller**

This Option can only be changed from its default if USB Functions is set to Disabled.
The Setup screen displays the system option:

**USB 2.0 Controller [Enabled]**

Available options are:
Disabled
Enabled

**SMBUS Controller**

The Setup screen displays the system option:

**SMBUS Controller [Enabled]**

Available options are:

Disabled
Enabled

### Restore on AC Power Loss

This option specifies the state the system should return to when power is restored after AC power is lost.

The Setup screen displays the system option:

**Restore on AC Power Loss [Last State]**

Three options are available:

- Select **Power Off** to have the system remain off until it is powered back on via a soft power-on, i.e., by pressing and releasing the power button.
- Select **Power On** to have the system turn the power back on automatically if AC power becomes active again.
- Select **Last State** to return the system to the state it was in (power on or off) when AC power was lost.

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# *Appendix A BIOS Messages*

### BIOS BEEP CODES

Errors may occur during the POST (Power-On Self Test) routines which are performed each time the system is powered on.

**Non-fatal errors** are those which, in most cases, allow the system to continue the bootup process. The error message normally appears on the screen. See *BIOS Error Messages* later in this section for descriptions of these messages.

**Fatal errors** are those which will not allow the system to continue the bootup procedure.

These fatal errors are usually communicated through a series of audible beeps. Each error message has its own specific beep code, defined by the number of beeps following the error detection. The following table lists the errors which are communicated audibly.

| Beep Codes | Description |
|---|---|
| 1 | Memory refresh timer error |
| 2 | Parity Error |
| 3 | Main memory read/write test error |
| 4 | Timer not operational |
| 5 | Processor error |
| 6 | Keyboard controller BAT test error |
| 7 | General exception error |
| 8 | Display memory error |
| 9 | ROM checksum error |
| 10 | CMOS shutdown register read/write error |
| 11 | Cache memory bad |

### BIOS BEEP CODE TROUBLESHOOTING

| Beep Counts | Description |
|---|---|
| 1, 2 or 3 | Reseat the memory or replace with known good modules. |
| 4-7, 9-11 | Fatal error. Perform the following steps before calling Technical Support.<br><br>Remove all expansion cards and try to reboot. If the beep code is still generated, call Technical Support. If the beep code is not generated, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem recurs. This will indicate the malfunctioning card. |
| 8 | The board may be faulty. Call Technical Support. |

## BIOS ERROR MESSAGES

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press F1 to Resume

Note the error message and press the **<F1>** key to continue with the bootup procedure.

---

**NOTE:** If the **Wait for 'F1' If Any Error** option in the Advanced Setup portion of the BIOS Setup Program has been set to **Disabled**, the "Press F1 to Resume" prompt will not appear on the last line. The bootup procedure will continue without waiting for operator response.

---

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing an ERROR Message Line 2, the text will be "RUN SETUP UTILITY." Pressing the **<F1>** key will invoke the BIOS Setup Utility.

A description of each error message appears below.

**Memory Errors**

| Message | Description |
|---|---|
| Gate20 Error | The BIOS is unable to properly control the SBC's Gate A20 function, which controls access to memory over 1MB. This may indicate a problem with the board. |
| Multi-Bit ECC Error | This message only occurs on systems using ECC enabled memory modules. ECC memory has the ability to correct singlebit errors that may occur from faulty memory modules. A multiple bit corruption of memory has occurred, and the ECC memory algorithm cannot correct it. This may indicate a defective memory module. |
| Parity Error | Fatal memory parity error. System halts after displaying this message. |

**Boot Errors**

| Message | Description |
|---|---|
| Boot Failure | This is a generic message indicating the BIOS could not boot from a particular device. This message is usually followed by other information concerning the device. |
| Invalid Boot Diskette | A diskette was found in the drive, but it is not configured as a bootable diskette. |
| Drive Not Ready | The BIOS was unable to access the drive because it indicated it was not ready for data transfer. This is often reported by drives when no media is present. |

## BIOS ERROR MESSAGES (CONTINUED)

**Boot Errors (Continued)**

| Message | Description |
|---|---|
| A: Drive Error | The BIOS attempted to configure the A: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive. |
| B: Drive Error | The BIOS attempted to configure the B: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive. |
| Insert BOOT diskette in A: | The BIOS attempted to boot from the A: drive, but could not find a proper boot diskette. |
| Reboot and Select proper Boot device or Insert Boot Media in selected Boot device | BIOS could not find a bootable device in the system and/or removable media drive does not contain media. |
| NO ROM BASIC | This message occurs on some systems when no bootable device can be detected. |

**Storage Device Errors**

| Message | Description |
|---|---|
| The following errors are typically displayed when the BIOS is trying to detect and configure IDE/ ATAPI devices in POST. | |
| XXXXXX Hard Disk Error<br>XXXXXX - ATAPI Incompatible | Messages in this format indicate that the specified device could not be properly initialized by the BIOS. Possible message are:<br>Primary Master Hard Disk Error<br>Primary Slave Hard Disk Error<br>Secondary Master Hard Disk Error<br>Secondary Slave Hard Disk Error<br>Primary Master Drive - ATAPI Incompatible<br>Primary Slave Drive - ATAPI Incompatible<br>Secondary Master Drive - ATAPI Incompatible<br>Secondary Slave Drive - ATAPI Incompatible |
| The following messages can be reported by an ATAPI device using the S.M.A.R.T. error reporting standard. The S.M.A.R.T. failure message may indicate the need to replace the hard disk. | |
| S.M.A.R.T. Capable but Command Failed | The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed. |
| S.M.A.R.T. Command Failed | The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed. |
| S.M.A.R.T. Status BAD, Backup and Replace | A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure. |
| S.M.A.R.T. Capable and Status BAD | A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure. |

## BIOS ERROR MESSAGES (CONTINUED)

### Virus Related Errors

| Message | Description |
|---|---|
| The following messages only display if Virus Detection is enabled in the BIOS Setup Utility. | |
| BootSector Write !! | The BIOS has detected software attempting to write to a drive's boot sector. This is flagged as possible virus activity. |
| VIRUS: Continue (Y/N)? | The BIOS has detected possible virus activity. |

### System Configuration Errors

| Message | Description |
|---|---|
| DMA-2 Error | Error initializing secondary DMA controller. This is a fatal error, often indicating a problem with system hardware. |
| DMA Controller Error | POST error while trying to initialize the DMA controller. This is a fatal error, often indicating a problem with system hardware. |
| Checking NVRAM..Update Failed | BIOS could not write to the NVRAM block. This message appears when the FLASH part is write-protected or if there is no FLASH part (system uses a PROM or EPROM). |
| Microcode Error | BIOS could not find or load the CPU Microcode Update to the processor. This message only applies to Intel processors. The message is most likely to appear when a brand new processor is installed in an SBC with an outdated BIOS. In this case, the BIOS must be updated to include the Microcode Update for the new processor. |
| NVRAM Checksum Bad, NVRAM Cleared | There was an error while validating the NVRAM data. This causes POST to clear the NVRAM data.. |
| Resource Conflict | More than one system device is trying to use the same non-shareable resources (memory or I/O). |
| NVRAM Ignored | The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST. |
| NVRAM Bad | The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST due to a data error. |
| Static Resource Conflict | Two or more static devices are trying to use the same resource space (usually memory or I/O). |
| PCI I/O Conflict | A PCI adapter generated an I/O resource conflict when configured by BIOS POST. |
| PCI ROM Conflict | A PCI adapter generated an I/O resource conflict when configured by BIOS POST. |
| PCI IRQ Conflict | A PCI adapter generated an I/O resource conflict when configured by BIOS POST. |
| PCI IRQ Routing Table Error | BIOS POST (DIM code) found a PCI device in the system but was unable to figure out how to route an IRQ to the device. Usually this error is caused by an incomplete description of the PCI Interrupt Routine of the system. |

## BIOS ERROR MESSAGES (CONTINUED)

### System Configuration Errors

| Message | Description |
|---|---|
| Timer Error | Indicates an error while programming the count register of channel 2 of the 8254 timer. This may indicate a problem with system hardware. |
| Interrupt Controller-1 Error | BIOS POST could not initialize the Master Interrupt Controller. This may indicate a problem with system hardware. |
| Interrupt Controller-2 Error | BIOS POST could not initialize the Slave Interrupt Controller. This may indicate a problem with system hardware. |

### CMOS Errors

| Message | Description |
|---|---|
| CMOS Date/Time Not Set | The CMOS Date and/or Time are invalid. This error can be resolved by readjusting the system time in the BIOS Setup Utility. |
| CMOS Battery Low | CMOS Battery is low. This message usually indicates that the CMOS battery needs to be replaced. It could also appear when the user intentionally discharges the CMOS battery. |
| CMOS Settings Wrong | CMOS settings are invalid. This error can be resolved by using the BIOS Setup Utility. |
| CMOS Checksum Bad | CMOS contents failed the Checksum check. Indicates that the CMOS data has been changed by a program other than the BIOS or that the CMOS is not retaining its data due to malfunction. This error can typically be resolved by using the BIOS Setup Utility. |

### Miscellaneous Errors

| Message | Description |
|---|---|
| Keyboard Error | Keyboard is not present or the hardware is not responding when the keyboard controller is initialized. |
| Keyboard/Interface Error | Keyboard Controller failure. This may indicate a problem with system hardware. |
| System Halted | The system has been halted. A reset or power cycle is required to reboot the machine. This message appears after a fatal error has been detected. |

### BOOTBLOCK INITIALIZATION CODE CHECKPOINTS

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the Bootblock initialization portion of the BIOS:

| Checkpoint | Description |
|---|---|
| Before D1 | Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled. |
| D1 | Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS. |
| D0 | Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum. |
| D2 | Disable cache before memory detection. Execute full memory sizing module. Verify that flat mode is enabled. |
| D3 | If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Reenable cache. Verify that flat mode is enabled. |
| D4 | Test base 512K memory. Adjust policies and cache first 8MB. Set stack. |
| D5 | Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. |
| D6 | Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See the Bootblock Recovery Code Checkpoints section of this appendix for more information. |
| D7 | Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash. |
| D8 | The Runtime module is uncompressed into memory. CPUID information is stored in memory. |
| D9 | Store the Uncompressed pointer for future use in PMM. Copy Main BIOS into memory. Leave all RAM below 1MB Read/Write including E000 and F000 shadow areas but closing SMRAM. |
| DA | Restore CPUID value back into register. Give control to BIOS POST (Execute POSTKernel). See the POST Code Checkpoints section of this appendix for more information. |

### BOOTBLOCK RECOVERY CODE CHECKPOINTS

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

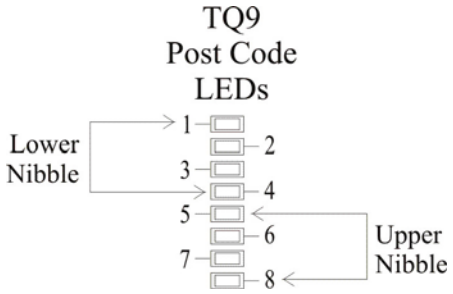
| Checkpoint | Description |
|---|---|
| E0 | Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled. |
| E9 | Set up floppy controller and data. Attempt to read from floppy. |
| EA | Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM. |
| EB | Disable ATAPI hardware. Jump back to checkpoint E9. |
| EF | Read error occurred on media. Jump back to checkpoint EB. |
| E9 or Ea | Determine information about root directory of recovery media. |
| F0 | Search for pre-defined recovery file name in root directory. |
| F1 | Recovery file not found. |
| F2 | Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file. |
| F3 | Start reading the recovery file cluster by cluster. |
| F5 | Disable L1 cache. |
| FA | Check the validity of the recovery file configuration to the current configuration of the flash part. |
| FB | Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size. |
| F4 | The recovery file size does not equal the found flash part size. |
| FC | Erase the flash part. |
| FD | Program the flash part. |
| FF | The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h. |

### POST CODE LEDS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 1 through 8 on the TQ9 SHB. The LEDs are located in the center of the board to the right of the processor and are numbered from top (1) to bottom (8). Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

| Upper Nibble (UN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED8 | LED7 | LED6 | LED5 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |

| Lower Nibble (LN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED4 | LED3 | LED2 | LED1 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |



### POST CODE CHECKPOINTS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The table below describes the type of checkpoints that may occur during the POST portion of the BIOS. Refer to the chart in the previous section to interpret the hexadecimal values of POST code LEDs 1 through 8.

| Checkpoint | Description |
|---|---|
| 03 | Disable NMI, parity, video for EGA and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialize CMOS as mentioned in the Kernel Variable “wCMOSFlags.” |
| 04 | Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables that are based on CMOS setup questions. Initialize both the 8259 compatible PICs in the system. |
| 05 | Initialize the interrupt controlling hardware (generally OPIC) and interrupt vector table. |
| 06 | Do read/write test to CH-2 count register. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock.” |
| 08 | Initialize the processor. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after auto detection of keyboard/mouse using AMI KB-5. |
| 0A | Initialize the 8042 compatible keyboard controller. |
| 0B | Detect the presence of PS/2 mouse. |
| 0C | Detect the presence of keyboard in KBC port. |
| 0E | Testing and initialization of different input devices. Also, update the Kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo and silent logo modules. |
| 13 | Early POST initialization of chipset registers |
| 24 | Uncompress and initialize any platform specific BIOS modules. |
| 30 | Initialize System Management Interrupt. |
| 2A | Initialize different devices through DIM. See *DIM Code Checkpoints* section of this appendix for more information. |
| 2C | Initialize different devices. Detects and initializes the video adapter installed in the system. |
| 2E | Initialize all the output devices. |
| 31 | Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module. |
| 33 | Initialize the silent boot module. Set the window for displaying text information. |
| 37 | Display sign-on message, processor information, setup key message and any OEM specific information. |

**POST CODE CHECKPOINTS (CONTINUED)**

| Checkpoint | Description |
|---|---|
| 38 | Initialize different devices through DIM. See DIM Code Checkpoints section of this appendix for more information. |
| 39 | Initialize DMAC-1 and DMAC-2. |
| 3A | Initialize RTC date/time. |
| 3B | Test for total memory installed in the system. Also, check for DEL or ESC keys to limit memory test. Display total memory in the system. |
| 3C | Mid POST initialization of chipset registers. |
| 40 | Detect different devices (parallel ports, serial ports and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDA, etc. |
| 50 | Program the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed. |
| 52 | Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. |
| 60 | Initialize NUM-LOCK status and program the keyboard Typematic rate. |
| 75 | Initialize INT13 and prepare for IPL detection. |
| 78 | Initialize IPL devices controlled by BIOS and option ROMs. |
| 7A | Initialize remaining option ROMs. |
| 7C | Generate and write contents of ESCD in NVRAM. |
| 84 | Log errors encountered during POST. |
| 85 | Display errors to the user and get the user response for error. |
| 87 | Execute BIOS setup if needed/requested. |
| 8C | Late POST initialization of chipset registers. |
| 8E | Program the peripheral parameters. Enable/disable NMI as selected. |
| 90 | Late POST initialization of system management interrupt. |
| A0 | Check boot password if installed. |
| A1 | Clean-up work needed before booting to OS. |
| A2 | Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh.<br><br>Initialize the Microsoft IRQ Routing Table. Prepare the runtime language module. Disable the system configuration display if needed. |
| A4 | Initialize runtime language module. |

### POST CODE CHECKPOINTS (CONTINUED)

| Checkpoint | Description |
|---|---|
| A7 | Display system configuration screen if enabled. Initialize the processor before boot, which includes the programming of the MTRRs. |
| A8 | Prepare processor for OS boot, including final MTRR values. |
| A9 | Wait for user input at configuration display if needed. |
| AA | Uninstall POST INT1Ch vector and INT09h vector. Deinitialize the ADM module. |
| AB | Prepare BBS for INT19 boot. |
| AC | End of POST initialization of chipset registers. |
| B1 | Save system context for ACPI. |
| 00 | Pass control to OS Loader (typically INT19h) |

### DIM CODE CHECKPOINTS

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different buses. The following table describes the main checkpoints where the DIM module is accessed:

| Checkpoint | Description |
|---|---|
| 2A | Initialize different buses and perform the following functions: Reset, Detect and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices and PnP ISA cards. It also assigns PCI Bus numbers. Function 1 initializes all static devices, which include manually configured on-board peripherals, memory and I/O decode windows in PCI-to-PCI bridges and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI or AGP video drivers. |
| 38 | Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all on-board peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices. |

### ADDITIONAL CHECKPOINTS

While control is in the different functions, additional checkpoints are output to Port 80H as word values to identify the routines being executed.

The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two sets of information. The details of the high byte of these checkpoints are detailed in the following table:

**High Byte XY**

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 8.

| | |
|---|---|
| 0 | Function 0. Disable all devices on the bus. |
| 1 | Function 1. Initialize static devices on the bus. |
| 2 | Function 2. Initialize output devices on the bus. |
| 3 | Function 3. Initialize input devices on the bus. |
| 4 | Function 4. Initialize IPL devices on the bus. |
| 5 | Function 5. Initialize general devices on the bus. |
| 6 | Function 6. Error reporting for the bus. |
| 7 | Function 7. Initialize add-on ROMs for all buses. |
| 8 | Function 8. Initialize BBS ROMs for all buses. |

The lower nibble 'Y' indicates the bus on which the different routines are being executed. 'Y' can be from 0 to 5.

| | |
|---|---|
| 0 | Generic DIM (Device Initialization Manager) |
| 1 | On-board system devices |
| 2 | ISA devices |
| 3 | EISA devices |
| 4 | ISA PnP devices |
| 5 | PCI devices |

# *Appendix B Power Connection*

## INTRODUCTION

The combination of new power supply technologies and the system capabilities defined in the SHB Express™ (PICMG® 1.3) specification requires a different approach to connecting system power to a PICMG 1.3 backplane and/or SHB hardware.

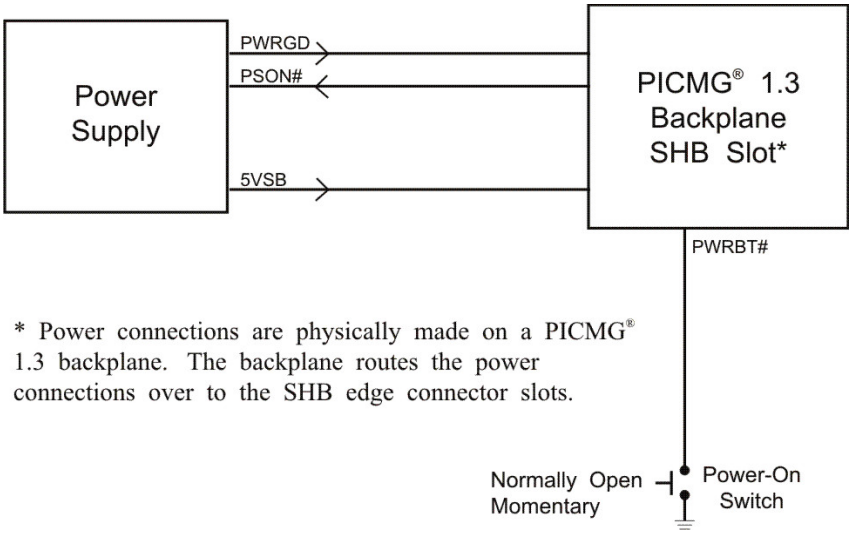
To improve system MTTR (Mean Time To Repair), the PICMG 1.3 specification defines enough power connections to the SHB's edge connectors to eliminate the need to connect auxiliary power to the SHB. All power connections in a PICMG 1.3 system can be made to the PICMG 1.3 backplane. This is true for SHBs that use high-performance processors. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive these high-performance SHBs. Trenton's PICMG 1.3 backplanes define ATX/EPS and +12V connectors that are compatible with ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The PICMG® 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in this manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

## POWER SUPPLY AND SHB INTERACTION

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.




**Power Supply and SHB Interaction**

PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

**CAUTION:** In some ATX/EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

### ELECTRICAL CONNECTION CONFIGURATIONS

There are a number of different connector types, such as EPS, ATX or terminal blocks, which can be utilized in wiring power supply and control functions to a PICMG 1.3 backplane. However, there are only two basic electrical connection configurations: **ACPI Connection** and **Legacy Non-ACPI Connection.**

**ACPI Connection**

The diagram on the previous page shows how to connect an ACPI compliant power supply to an ACPI enabled PICMG 1.3 system. The following table shows the required connections which must be made for soft power control to work.

| Signal | Description | Source |
|---|---|---|
| +12 | DC voltage for those systems that require it | Power Supply |
| +5V | DC voltage for those systems that require it | Power Supply |
| +3.3V | DC voltage for those systems that require it | Power Supply |
| +5VSB | 5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up. | Power Supply |
| PWRGD | Power Good. This signal indicates that the power supply's voltages are stable and within tolerance. | Power Supply |
| PSON# | Power Supply On. This signal is used to turn on an ATX or EPS type power supply. | SHB/Backplane |
| PWRBT# | Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state.<br><br>If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs. | Power Button |

### Legacy Non-ACPI Connection

For system integrators that either do not have or do not require an ACPI compliant power supply as described in the section above, an alternative electrical configuration is described in the table on the following page.

| Signal | Description | Source |
|---|---|---|
| +12 | DC voltage for those systems that require it | Power Supply |
| +5V | DC voltage for those systems that require it | Power Supply |
| +3.3V | DC voltage for those systems that require it | Power Supply |
| +5VSB | Not Required | Power Supply |
| PWRGD | Not Required | Power Supply |
| PSON# | Power Supply On. This signal is used to turn on an ATX or EPS type power supply. If an ATX or EPS power supply is used in this legacy configuration, a shunt must be installed on the backplane from PSON# to signal Ground. This forces the power supply DC outputs on whenever AC to the power supply is active. | Backplane |
| PWRBT# | Not Used | |

In addition to these connections, there is usually a switch controlling AC power input to the power supply.

When using the legacy electrical configuration, the SHB BIOS **Power Supply Shutoff** setting should be set to **Manual shutdown**. Refer to the *General ACPI Configuration* section of the *Advanced Setup* chapter in this manual for details.

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# *Appendix C PCI Express Backplane Usage*

## INTRODUCTION

PCI Express™ is a scalable, full-duplex serial interface which consists of multiple communication lanes grouped into links. PCI Express scalability is achieved by grouping these links into multiple configurations. A x1 ("by 1") PCI Express link is made up of one full-duplex link that consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. A x4 configuration is made up of four PCI Express links. The most commonly used PCIe link sizes are x1, x4, x8 and x16.

PCI Express devices with different PCI Express link configurations establish communication with each other using a process called auto-negotiation or link training. For example, a PCI Express device or option card that has a x16 PCI Express interface and is placed into a x16 mechanical/x8 electrical slot on a backplane establishes communication with a PICMG® 1.3 SHB using auto-negotiation. The option card's PCI Express interface will "train down" to establish communication with the SHB via the x8 PCI Express link between the SHB and the backplane option card slot.

## SHB EDGE CONNECTORS

The PICMG 1.3 specification enables SHB vendors to provide multiple PCI Express configuration options for edge connectors A and B of a particular SHB. These edge connectors carry the PCI Express links and reference clocks down to the SHB slot on the PICMG 1.3 backplane. The potential PCI Express link configurations of an SHB fall into two main classifications: server-class and graphics-class. The specific class and PCI Express link configuration of an SHB is determined by the chipset components used on the SHB.

In a server-class configuration, the main goal of the SHB is to route as many high-bandwidth PCI Express links as possible down to the backplane. Typically, these links are a combination of x4 and x8 PCI Express links.

A graphics-class configuration should provide a x16 PCI Express link down to the backplane in order to support high-end PCI Express graphics and video cards. Graphics-class SHB configurations also provide as many lower bandwidth (x1 or x4) links as possible.

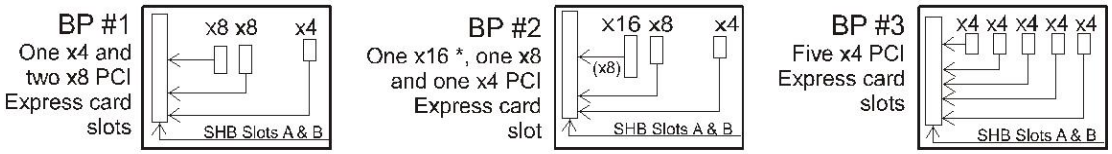
Trenton's TQ9 is a graphics-class system host board which provides one x16 PCI Express link on the SHB's edge connectors A and B. This x16 PCIe link is designed to support PCI Express video/graphics cards on an SHB Express™ (PICMG 1.3) backplane. A x4 PCI Express link and five PCIe reference clocks are also included on edge connectors A and B. The PICMG 1.3 specification states that the SHB must provide as many reference clocks as there are potential PCI Express links on the PICMG 1.3 backplane.

In addition, the SHB provides a x1 link to the controlled impedance connector for use with PCI Express plug-in option cards. The x4 and x1 PCI Express links are used on SHB Express backplanes to support PCI Express option cards and the bridge chips that provide PCI/PCI-X option card support. Refer to the *PCI Express Reference* chapter of this manual for more information, including edge connector pin assignments.

The figures below show some typical SHB and backplane combinations that would result in all of the PCI Express slots successfully establishing communication with the SHB host device. The first figure shows a server-class SHB; the second shows a graphics-class SHB.

### Server-Class SHB:

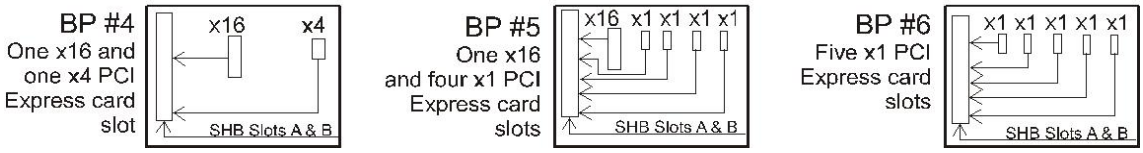
PCI Express™ Edge Connectors A & B: One x4 and two x8 PCI Express™ Links with five reference clocks




* x16 slot is x16 mech./x8 elec.

### Graphics-Class SHB:

PCI Express™ Edge Connectors A & B: One x16 and one x4 PCI Express™ Link with five reference clocks




PCI Express link configuration straps for each PCI Express option card slot on a PICMG 1.3 backplane are required as part of the PICMG 1.3 SHB Express™ specification. These configuration straps alert the SHB as to the specific link configuration expected on each PCI Express option card slot. PCI Express communication between the SHB and option card slots is successful only when there are enough available PCI Express links established between the PICMG 1.3 SHB and each PCI Express slot or device on the backplane.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

# *Appendix D I/O Expansion Boards*

## INTRODUCTION

The IOB30MC and IOB31 are I/O expansion boards (IOBs) for legacy I/O support for PCI Express™ system host boards (SHBs).

These I/O boards connect to the impedance connector (P20) on Trenton Technology's TQ9 SHBs and provide two serial ports, mouse and keyboard ports, parallel port and floppy drive connector. The IOB31 also provides a PS/2 mouse/keyboard mini DIN connector.

In addition, the IOB31 provides a x4 PCI Express edge connector which connects to an expansion slot on a PCI Express compatible backplane.

## MODELS

| Model # | Model Name | Description |
|---|---|---|
| 6391-001 | IOB30MC | MC I/O Plate |
| 6474-000 | IOB31 | Standard |

## FEATURES

IOB30MC(6391-001)

- I/O plate is optimized for use on a TQ9 system host board
- Two serial ports and PS/2 mouse/keyboard mini DIN on the I/O bracket
- PS/2 mouse, keyboard, parallel port and floppy drive connectors

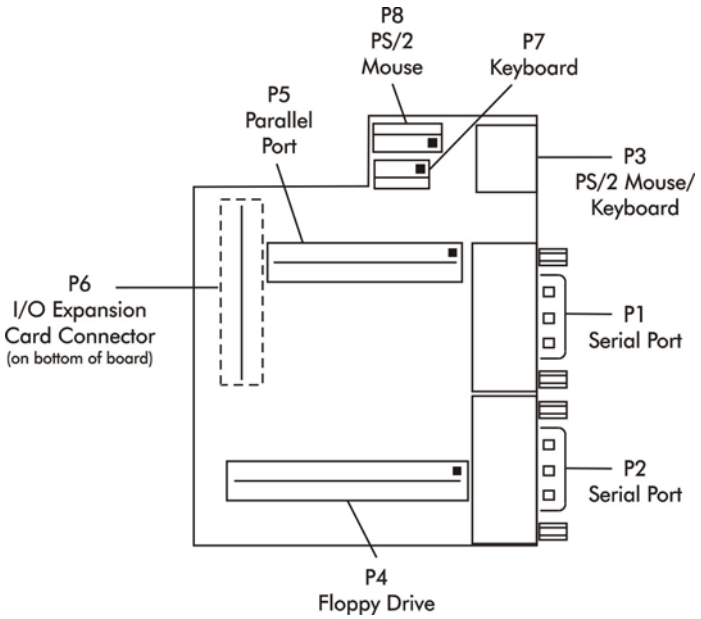
IOB31(6474-000)

- Two serial ports
- PS/2 mouse, keyboard, parallel port and floppy drive connectors
- PCI Express expansion capability for use with PCI Express backplanes
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG®) PCI Express Specification

## TEMPERATURE/ENVIRONMENT

- **Operating Temperature:** 0º C. to 60º C.
- **Storage Temperature:** - 20º C. to 70º C.
- **Humidity:** 5% to 90% non-condensing

## IOB30MC (6391-001) I/O BOARD LAYOUT




## IOB30MC CONNECTORS

**NOTE:** Pin 1 on the connectors is indicated by the square pad on the PCB.

**P1** - **Serial Port Connector**
9 position "D" right angle, Spectrum #56-402-001

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier Detect | 6 | Data Set Ready-I |
| 2 | Receive Data-I | 7 | Request to Send-O |
| 3 | Transmit Data-O | 8 | Clear to Send- |
| 4 | Data Terminal Ready-O | 9 | Ring Indicator-I |
| 5 | Signal Gnd | | |

**P2** - **Serial Port Connector**
9 position "D" right angle, Spectrum #56-402-001

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier Detect | 6 | Data Set Ready-I |
| 2 | Receive Data-I | 7 | Request to Send-O |
| 3 | Transmit Data-O | 8 | Clear to Send- |
| 4 | Data Terminal Ready-O | 9 | Ring Indicator-I |
| 5 | Signal Gnd | | |

## IOB30MC CONNECTORS (CONTINUED)

**P3 - PS/2 Mouse and Keyboard Connector**
6 pin mini DIN, Kycon #KMDG-6S-B4T

| Pin | Signal |
|---|---|
| 1 | Ms Data |
| 2 | Kbd Data |
| 3 | Gnd |
| 4 | Power (+5V fused) with self-resetting fuse |
| 5 | Ms Clock |
| 6 | Kbd Clock |

**P4 - Floppy Drive Connector**
34 pin dual row header, Amp #103308-7

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Gnd | 2 | N-RPM |
| 3 | Gnd | 4 | NC |
| 5 | Gnd | 6 | D-Rate0 |
| 7 | Gnd | 8 | P-Index |
| 9 | Gnd | 10 | N-Motoron 1 |
| 11 | Gnd | 12 | N-Drive Sel2 |
| 13 | Gnd | 14 | N-Drive Sel1 |
| 15 | Gnd | 16 | N-Motoron 2 |
| 17 | Gnd | 18 | N-Dir |
| 19 | Gnd | 20 | N-Stop Step |
| 21 | Gnd | 22 | N-Write Data |
| 23 | Gnd | 24 | N-Write Gate |
| 25 | Gnd | 26 | P-Track 0 |
| 27 | Gnd | 28 | P-Write Protect |
| 29 | Gnd | 30 | N-Read Data |
| 31 | Gnd | 32 | N-Side Select |
| 33 | Gnd | 34 | Disk Change |

**P5 - Parallel Port Connector**
26 pin dual row header, Amp #103308-6

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Strobe | 2 | Auto Feed XT |
| 3 | Data Bit 0 | 4 | Error |
| 5 | Data Bit 1 | 6 | Init |
| 7 | Data Bit 2 | 8 | Slct In |
| 9 | Data Bit 3 | 10 | Gnd |
| 11 | Data Bit 4 | 12 | Gnd |
| 13 | Data Bit 5 | 14 | Gnd |
| 15 | Data Bit 6 | 16 | Gnd |
| 17 | Data Bit 7 | 18 | Gnd |
| 19 | ACK | 20 | Gnd |
| 21 | Busy | 22 | Gnd |
| 23 | Paper End | 24 | Gnd |
| 25 | Slct | 26 | NC |

## IOB30MC CONNECTORS (CONTINUED)

**P6 - Impedance Connector**
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +12 | 2 | +5V_STANDBY |
| 3 | NC | 4 | +5V_STANDBY |
| 5 | NC | 6 | +5V_DUAL |
| 7 | NC | 8 | +5V_DUAL |
| 9 | NC | 10 | NC |
| 11 | NC | 12 | NC |
| 13 | ICH_SMI# | 14 | ICH_RCIN# |
| 15 | ICH_SIOPME# | 16 | ICH_A20GATE |
| 17 | Gnd | 18 | Gnd |
| 19 | L_FRAME# | 20 | L_AD3 |
| 21 | L_DRQ1# | 22 | L_AD2 |
| 23 | L_DRQ0# | 24 | L_AD1 |
| 25 | SERIRQ | 26 | L_AD0 |
| 27 | Gnd | 28 | Gnd |
| 29 | PCLK14SIO | 30 | PCLK33LPC |
| 31 | Gnd | 32 | Gnd |
| 33 | SMBDATA_RESUME | 34 | IPMB_DAT |
| 35 | SBMCLK_RESUME | 36 | IPMB_CLK |
| 37 | SALRT#_RESUME | 38 | IPMB_ALRT# |
| 39 | Gnd | 40 | Gnd |
| 41 | EXP_CLK100 | 42 | EXP_RESET# |
| 43 | EXP_CLK100# | 44 | ICH_WAKE# |
| 45 | Gnd | 46 | Gnd |
| 47 | C_PE_TXP4 | 48 | C_PE_RXP4 |
| 49 | C_PE_TXN4 | 50 | C_PE_RXN4 |
| 51 | Gnd | 52 | Gnd |
| 53 | C_PE_TXP3 | 54 | C_PE_RXP3 |
| 55 | C_PE_TXN3 | 56 | C_PE_RXN3 |
| 57 | Gnd | 58 | Gnd |
| 59 | C_PE_TXP2 | 60 | C_PE_RXP2 |
| 61 | C_PE_TXN2 | 62 | C_PE_RXN2 |
| 63 | Gnd | 64 | Gnd |
| 65 | C_PE_TXP1 | 66 | C_PE_RXP1 |
| 67 | C_PE_TXN1 | 68 | C_PE_RXN1 |
| 69 | Gnd | 70 | Gnd |
| 71 | +3.3V | 72 | +5V |
| 73 | +3.3V | 74 | +5V |
| 75 | +3.3V | 76 | +5v |

## IOB30MC CONNECTORS CONTINUED

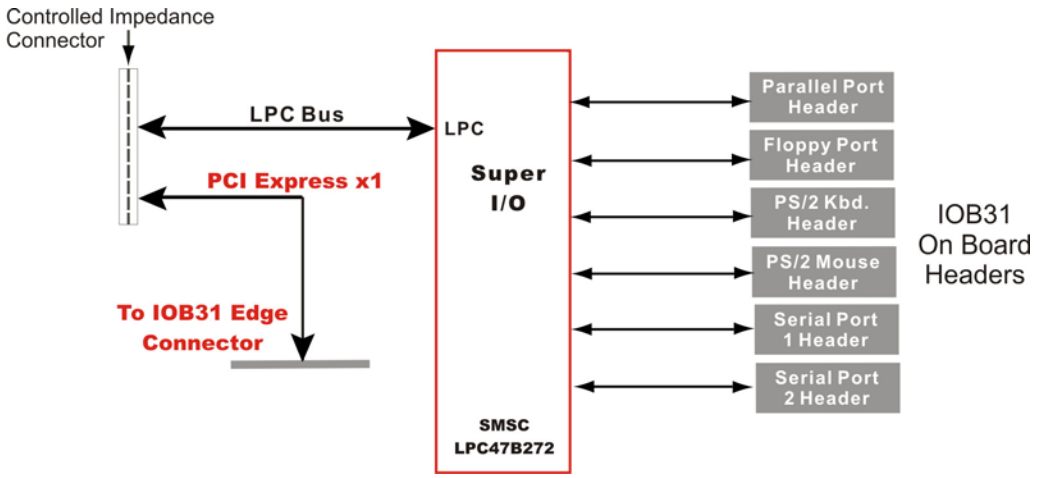
**P7 - Keyboard Header**
5 pin single row header, Amp #640456-5

| Pin | Signal |
|---|---|
| 1 | Kbd Clock |
| 2 | Kbd Data |
| 3 | Key |
| 4 | Kbd Gnd |
| 5 | Kbd Power (+5V fused) with self resetting fuse |

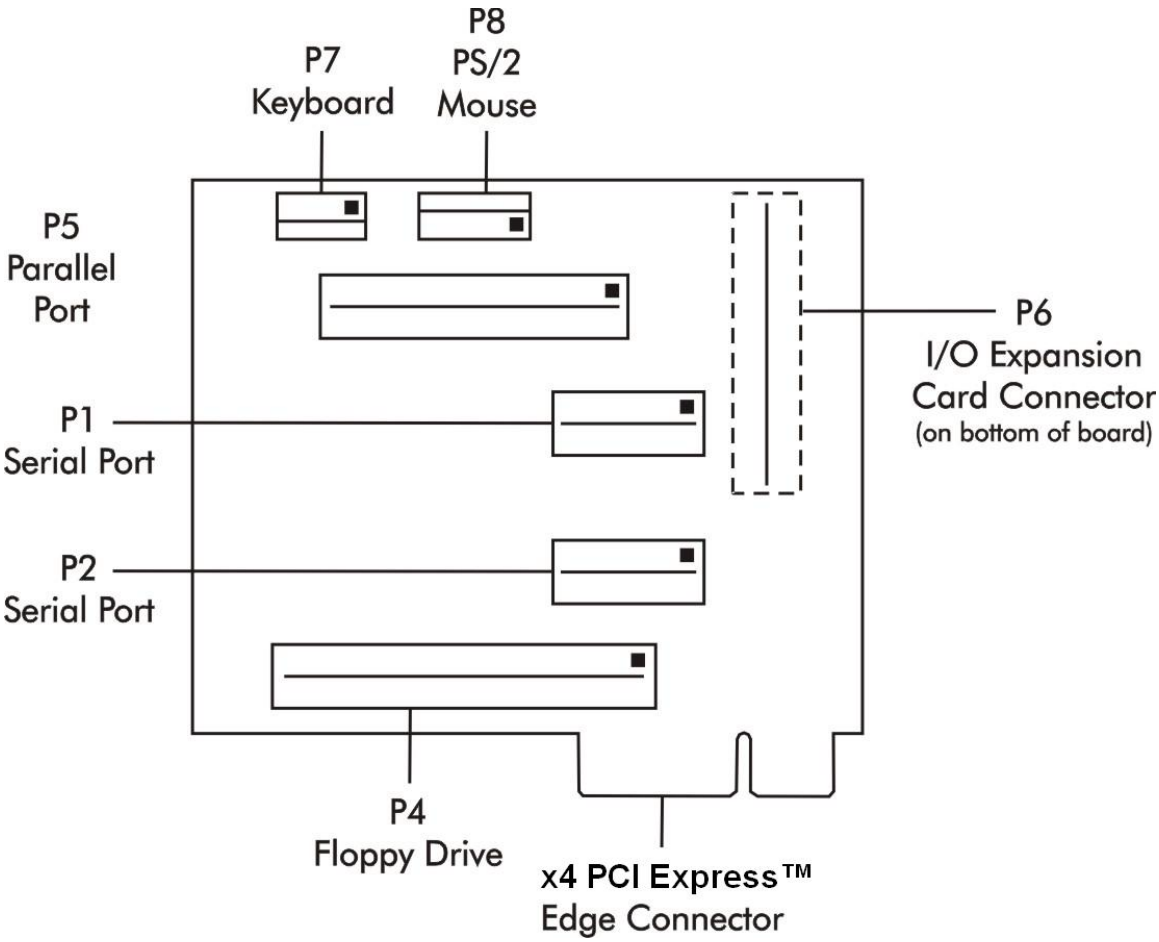
**P7 - PS/2 Mouse Header**
6 pin single row header, Amp #640456-6

| Pin | Signal |
|---|---|
| 1 | Ms Data |
| 2 | Reserved |
| 3 | Gnd |
| 4 | Power (+5V fused) with self-resetting fuse |
| 5 | Ms Clock |
| 6 | Reserved |

### IOB31 (6474-000) BLOCK DIAGRAM




### IOB31 (6474-000) I/O BOARD LAYOUT



## IOB31 CONNECTORS

**NOTE:** Pin 1 on the connectors is indicated by the square pad on the PCB.

**P1 - Serial Port Connector**
10 pin dual row header, Amp #103308-1

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier Detect | 2 | Data Set Ready-I |
| 3 | Receive Data-I | 4 | Request to Send-O |
| 5 | Transmit Data-O | 6 | Clear to Send-I |
| 7 | Data Terminal Ready-O | 8 | Ring Indicator-I |
| 9 | Signal Gnd | 10 | NC |

**P2 - Serial Port Connector**
10 pin dual row header, Amp #103308-1

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier Detect | 2 | Data Set Ready-I |
| 3 | Receive Data-I | 4 | Request to Send-O |
| 5 | Transmit Data-O | 6 | Clear to Send-I |
| 7 | Data Terminal Ready-O | 8 | Ring Indicator-I |
| 9 | Signal Gnd | 10 | NC |

**P4 - Floppy Drive Connector**
34 pin dual row header, Amp #103308-7

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Gnd | 2 | N-RPM |
| 3 | Gnd | 4 | NC |
| 5 | Gnd | 6 | D-Rate0 |
| 7 | Gnd | 8 | P-Index |
| 9 | Gnd | 10 | N-Motoron 1 |
| 11 | Gnd | 12 | N-Drive Sel2 |
| 13 | Gnd | 14 | N-Drive Sel1 |
| 15 | Gnd | 16 | N-Motoron 2 |
| 17 | Gnd | 18 | N-Dir |
| 19 | Gnd | 20 | N-Stop Step |
| 21 | Gnd | 22 | N-Write Data |
| 23 | Gnd | 24 | N-Write Gate |
| 25 | Gnd | 26 | P-Track 0 |
| 27 | Gnd | 28 | P-Write Protect |
| 29 | Gnd | 30 | N-Read Data |
| 31 | Gnd | 32 | N-Side Select |
| 33 | Gnd | 34 | Disk Change |

### IOB31 CONNECTORS (CONTINUED)

**P5 - Parallel Port Connector**
26 pin dual row header, Amp #103308-6

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Strobe | 2 | Auto Feed XT |
| 3 | Data Bit 0 | 4 | Error |
| 5 | Data Bit 1 | 6 | Init |
| 7 | Data Bit 2 | 8 | Slct In |
| 9 | Data Bit 3 | 10 | Gnd |
| 11 | Data Bit 4 | 12 | Gnd |
| 13 | Data Bit 5 | 14 | Gnd |
| 15 | Data Bit 6 | 16 | Gnd |
| 17 | Data Bit 7 | 18 | Gnd |
| 19 | ACK | 20 | Gnd |
| 21 | Busy | 22 | Gnd |
| 23 | Paper End | 24 | Gnd |
| 25 | Slct | 26 | NC |

**P6 - Impedance Connector**
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +12 | 2 | +5V_STANDBY |
| 3 | NC | 4 | +5V_STANDBY |
| 5 | NC | 6 | +5V_DUAL |
| 7 | NC | 8 | +5V_DUAL |
| 9 | NC | 10 | NC |
| 11 | NC | 12 | NC |
| 13 | ICH_SMI# | 14 | ICH_RCIN# |
| 15 | ICH_SIOPME# | 16 | ICH_A20GATE |
| 17 | Gnd | 18 | Gnd |
| 19 | L_FRAME# | 20 | L_AD3 |
| 21 | L_DRQ1# | 22 | L_AD2 |
| 23 | L_DRQ0# | 24 | L_AD1 |
| 25 | SERIRQ | 26 | L_AD0 |
| 27 | Gnd | 28 | Gnd |
| 29 | PCLK14SIO | 30 | PCLK33LPC |
| 31 | Gnd | 32 | Gnd |
| 33 | SMBDATA_RESUME | 34 | IPMB_DAT |
| 35 | SBMCLK_RESUME | 36 | IPMB_CLK |
| 37 | SALRT#_RESUME | 38 | IPMB_ALRT# |
| 39 | Gnd | 40 | Gnd |
| 41 | EXP_CLK100 | 42 | EXP_RESET# |
| 43 | EXP_CLK100# | 44 | ICH_WAKE# |
| 45 | Gnd | 46 | Gnd |
| 47 | C_PE_TXP4 | 48 | C_PE_RXP4 |
| 49 | C_PE_TXN4 | 50 | C_PE_RXN4 |
| 51 | Gnd | 52 | Gnd |
| 53 | C_PE_TXP3 | 54 | C_PE_RXP3 |
| 55 | C_PE_TXN3 | 56 | C_PE_RXN3 |
| 57 | Gnd | 58 | Gnd |
| 59 | C_PE_TXP2 | 60 | C_PE_RXP2 |

## IOB31 CONNECTORS (CONTINUED)

**P6 - Impedance Connector (continued)**
76 pin controlled impedance connector,
Samtec #MIS-038-01-FD-K

| | | | |
|---|---|---|---|
| 61 | C_PE_TXN2 | 62 | C_PE_RXN2 |
| 63 | Gnd | 64 | Gnd |
| 65 | C_PE_TXP1 | 66 | C_PE_RXP1 |
| 67 | C_PE_TXN1 | 68 | C_PE_RXN1 |
| 69 | Gnd | 70 | Gnd |
| 71 | +3.3V | 72 | +5V |
| 73 | +3.3V | 74 | +5V |
| 75 | +3.3V | 76 | +5v |

**P7 - Keyboard Header**
5 pin single row header, Amp #640456-5

| Pin | Signal |
|---|---|
| 1 | Kbd Clock |
| 2 | Kbd Data |
| 3 | Key |
| 4 | Kbd Gnd |
| 5 | Kbd Power (+5V fused) with self resetting fuse |

**P7 - PS/2 Mouse Header**
6 pin single row header, Amp #640456-6

| Pin | Signal |
|---|---|
| 1 | Ms Data |
| 2 | Reserved |
| 3 | Gnd |
| 4 | Power (+5V fused) with self-resetting fuse |
| 5 | Ms Clock |
| 6 | Reserved |

# *Appendix E Declaration of Conformity*

# DECLARATION OF CE CONFORMITY

APLICATION OF COUNCIL DIRECTIVE 89/336/EEC

Standard(s) to which conformity is declared:
Emissions Test Methods per
**EN55022: 2006 Class B, EN61000-3-2 :2006, EN61000-3-3 :2005**
Immunity Test Methods per
**EN61000-4-2:2001, EN61000-4-3 :2005, EN61000-4-4 :2006, EN61000-4-5 :2006, EN61000-4-6 :2006, EN61000-4-8 :2001, EN61000-4-11 :2004**

| | |
|---|---|
| Manufacture: | Trenton Technology, Inc<br>2350 Centennial Drive<br>Gainesville, Georgia 30504-5700<br>USA<br>Telephone: (770) 287-3100<br>Fax: (770) 287-3150 |
| Type of Equipment: | TQ9 System Host Board |
| Model Name: | TQ9 92-XX6731-XXX |
| Tested By: | International Technology Company<br>9959 Calaveras Road, P.O. Box 543<br>Sunol, California 94586-0543<br>USA<br>Telephone: (925) 862-2944<br>Fax: (952) 862-9013 |
| Director: | Mr. Michael Gbadebo, PE |

I, the undersigned, hereby declare that the specified equipment conforms to the Directive(s) and Standard(s) listed above:

| | |
|---|---|
| Signature: | *Charles B. Hinson* |
| Name (printed): | Charles B. Hinson |
| Title: | Development Quality Assurance Manager |
| Date: | June 1 2007 |