An Implementation Guide for High Density Embedded Computing (HDEC) Hardware

A Trenton Systems White Paper

Contents

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Introduction

High Density Embedded Computing or HDEC comprises an innovative set of system host board, backplane and rackmount computer system technologies designed exclusively to solve the data throughput needs of high density embedded computing applications. HDEC applications also require robust computing performance. HDEC board and system-level technologies take full advantage of the ever increasing number of processor cores and native PCI Express 3.0 links available on a CPU die to deliver a 5x increase in aggregate system bandwidth with lower SHB-to-PCIe plug-in card data latencies.

Maximizing system compute density has become an important factor in reducing overall program costs while increasing the operating efficiency of military systems. We'll explore some HDEC performance data to illustrate how the HDEC system host boards and backplanes compare to other hardware options. We'll also discuss how the HDEC hardware works with the latest embedded processors and backplane form factors to make the HDEC promise of added bandwidth with lower data latencies an application reality in a wide variety of high-density embedded computing systems.

Section 1 - Why HDEC and What Is It?

The PCI Industrial Computer Manufactures Group (PICMG®) was established in 1994 with the publication of the PICMG 1.0 PCI-ISA standard for single board computers. This single board computer/system host board edge-card computing form factor has served industry well by providing faster MTTR times, hardware platform stability and expanded support for industry standard plug-in cards. Initially the SBC form factor defined in the PICMG 1.0 standard had a shared SBC-to-option card parallel bus comprised of an 8-bit ISA and a 32-bit/33MHz PCI interface.

As embedded computing applications evolved and branched into other industry segments the ISA bus was quickly replaced by the 32-bit/33MHz PCI parallel bus and its later 64-bit/66MHz and PCI-X iterations. Additional PICMG standards such as PICMG 2.0 and 3.0 focused on pin-and-socket SBC form factors with PCI parallel buses and fabric interfaces as the key card-to-card backplane interconnect methodologies. These buses served us well for about a decade, but applications were demanding faster card-to-card interconnect speeds with lower data latencies. Figure 1 illustrates various PICMG standards as a function of card-to-card interconnects.

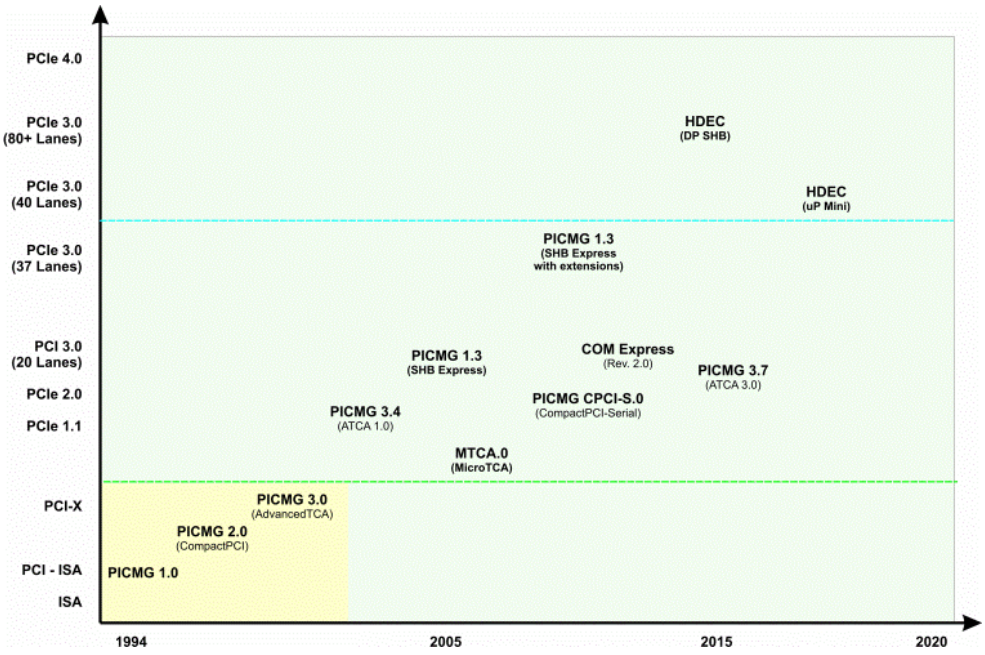


Figure 1 – Board Interconnect Architecture

PCI Express® stepped into the industrial computer arena with the adoption of several PICMG industry standards in the mid-2000s. For example, PICMG 1.3 or SHB Express™ replaced the parallel buses of PICMG 1.0 with the PCIe serial interconnect. The base PICMG 1.3 standard maintained an optional PCI bus for those applications that needed it, but the primary interface connectivity in a PICMG 1.3 system is the twenty (20) PCIe base links from the system host board's edge connectors A and B to a PICMG 1.3 backplane. With a mezzanine card approach it was possible to expand the number of PCIe links to 37 links in some cases depending on the number of SHB processors, chipset type, mezzanine card design and backplane type.

PCI Express switching technology enabled system designers to expand the number of PCIe option card slots on a backplane well beyond the number of base links available from the system host board. This approached worked great while PCIe switch technology was relatively inexpensive and PCIe 1.1 and 2.0 plug-in cards were not resource intensive. PCIe switch technology did a good job of limiting latency through the switch and provided reasonable bandwidth for most PCI Express option cards. Unfortunately, the implementation cost of PCI Express switches skyrocketed a few years ago and continues to escalate. The introduction of high-performance PCIe 3.0 option cards has placed greater bandwidth and latency demands on today's industrial computer architecture. It became apparent back in 2014 that we needed a better way to support more direct or native PCI Express links in today's high-density embedded computing systems.

That's where the High Density Embedded Computer or HDEC® standard comes into play. The HDEC standard defines the pin-outs of five, double-density/high-speed edge card connectors on a dual-processor HDEC Series system host board. The standard also calls out the industry standard SHB mating connectors that an HDEC backplane would use to connect the HDEC SHB into a high density embedded computing system. The standard defines more than enough signal pins to meet the demands of today's high performance server processors with enough head room for next generation processors, and optional edge card interfaces to the backplane such as Ethernet.

HDEC System Host Board – Processors Provide 80 Lanes of PCI Express 3.0

Long-life processors are at the core of all embedded computing systems. What makes an HDEC system host board (SHB) different is that the SHB supports two, high-performance Intel® processors of the type commonly found in high-end servers. Dual Intel® Xeon® Processors E5-2600 v3/v4 Series are supported on HDEC SHBs such as Trenton's HEP8225.

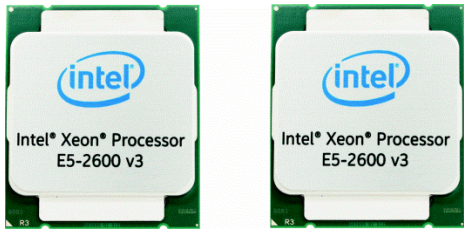


Figure 2 – HDEC SHB Processors

There were number of compelling reasons to choose this processor family for the HDEC system host boards, but the most critical reason is that each processor supports forty (40) native links of PCI Express 3.0. Put two of these on a plug-in SHB and you have eighty (80) lanes of PCI Express 3.0 to work with in a long-life high-performance rackmount server design. Bring these 80 links down to a backplane and you could support a fair number of direct option card slots without expensive PCIe switches. If you want to support a greater number of option card slots; say with x16 electrical links, HDEC SHBs makes this possible, but with far fewer PCIe switches on an HDEC backplane. Sounds great, but how do we get 80 lanes of PCIe 3.0 off an SHB using card edge fingers as opposed to the more expensive and more brittle pin-and-socket connectors?

HDEC System Host Board – Double Density Card Edge Fingers Deliver 80 Lanes of PCIe Plus Added System I/O

New advancements in edge card connector technology now make it possible to double the number of connector contacts without an appreciable impact on circuit board area utilization. The HEP8225 HDEC Series SHB supports two processors and has five sets of card edge fingers, with each set of fingers having two rows of card edge contacts.

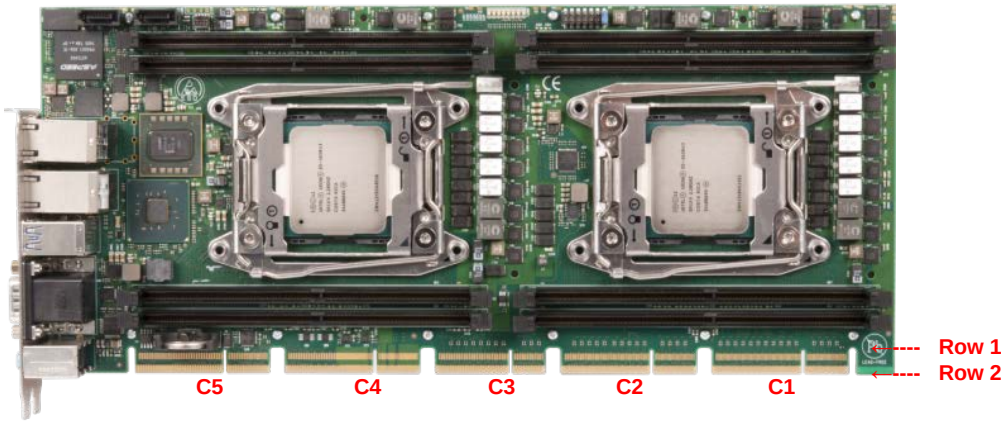


Figure 3 – Double-Density Card Edge Connectors

The top-side view of the HDEC SHB shown in Figure 3 illustrates the SHB's high-density edge card connectors. Notice the double row of card edge contacts. As a side note, the contacts that are merged together in this particular SHB design are for power and ground connections.

Using five sets of double-density PCI Express card edge contacts provides a total of 960 unique connection points between the SHB and the corresponding backplane connectors. HDEC represents an increase of 125% in available PCI Express and device I/O interconnects compared to the previous PICMG 1.3 PCI Express only implementation standard. This makes it possible to route more PCIe links, device I/O and communication interfaces down to the backplane. The HDEC design approach streamlines system cabling and improves system airflow by having these connect points on the backplane rather than the system host board. The additional connection points also enable more advanced system diagnostic signals to be passed between the system host board and the other devices contained within the system.

The 960 available connector contacts in the dual-processor HDEC SHB standard have the capability of supporting today's 80 lanes of PCIe 3.0 from current processors. The HDEC standard also has built-in head room for an additional eight lanes of PCIe Gen3. This additional head room will come in handy for future high-performance embedded processor designs currently on the drawing board.

The industry standard backplane mating connectors; Samtec model BEC5 or equivalent, used with an HDEC system host board securely engage with the SHB card edge contacts in adverse application environments commonly found in military computing, industrial automation, energy production and field exploration.

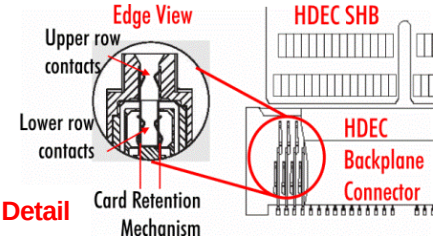


Figure 4 – SHB Connector Detail

Figure 4 illustrates the SHB mating connector detail for the backplane connectors used on an HDEC Series backplane. These are high density, high speed connectors and are ideal for PCI Express 3.0 interconnects. Notice the card retention mechanism in the edge view of the SHB connector for securing the HDEC SHB. This helps to secure the SHB's electrical connections to the backplane regardless of the system's application environment.

The two appendices contain several useful illustrations that will be of a great help in implementing either an HDEC Series board design, or applying HDEC system host boards and backplanes in an embedded computing system design. Appendix A, Table 1 defines all of the I/O pin assignments for the HDEC system host board standard covering dual processor SHB designs. This information answers the basic questions regarding specific signal placements as well as power and ground locations. As in the PICMG 1.3 standard, some interfaces through the card edge connectors such as Ethernet are optional. For example, the designers of the HEP8225 HDEC Series SHB cited in this paper elected to route two 10G and two 1G Ethernet LANs to the board's I/O bracket rather than down to the edge connectors. The HDEC standard honors the precedent established with the PICMG 1.0 and 1.3 standards by building in the board design flexibility necessary to meet unique system requirements.

Appendix B, Figure 1 will be of the most use to the majority of the project managers, project engineers and system design engineers reading this paper. This illustration provides a typical I/O map for an HDEC SHB (HEP8225) and backplane system implementation. You can use this information as a guide to what's possible in embedded computing systems based on example HDEC board hardware.

Section 2 – Processor Capabilities and Thermal Considerations

Intel® technology is the foundation of the HDEC Series, offering a wide range of options for high density embedded computing applications. The 12-core processor options are well-suited to high-performance applications, while the lower core count processors have distinct advantages in certain applications. As always, processor performance needs have to be balanced against a system's thermal and power consumption requirements.

Name	Cores	Base Core Speed	Max Turbo Speed	Cache	Max DDR4 Supported	QPI (2)	Max TDP	T_{CASE}
Intel Xeon E5-2680 v3	12	2.5GHz	3.3GHz	30MB	DDR4-2133	9.6GT/s	120W	84.5°C
Intel Xeon E5-2658 v3	12	2.2GHz	2.9GHz	30MB	DDR4-2133	9.6GT/s	105W	86.9°C
Intel Xeon E5-2648L v3	12	1.8GHz	2.5GHz	30MB	DDR4-2133	9.6GT/s	75W	87.0°C
Intel Xeon E5-2628L v3	10	2.0GHz	2.5GHz	25MB	DDR4-1866	8.0GT/s	75W	87.0°C
Intel Xeon E5-2618L v3	8	2.3GHz	3.4GHz	20MB	DDR4-1866	8.0GT/s	75W	87.0°C
Intel Xeon E5-2608L v3	6	2.0GHz	n/a	15MB	DDR4-1600	6.4GT/s	50W	88.8°C

Table 1 – HDEC Long-Life Processor Options

The chart in Table 1 summarizes the base specifications for the Intel® Xeon® E5-2600 v3 Series of processors currently supported on the HEP8225 HDEC Series system host board. In addition to these base specs, the processors support a variety of Intel® Advanced Technologies including:

- Intel® Hyper-Threading
- Intel® Virtualization Technology (VT-x)
- Enhanced Intel SpeedStep® Technology
- Thermal Monitoring Technologies
- Intel® Data Protection Technology
- Intel® Platform Protection Technology

What's interesting about the thermal properties of these high-performance, long-life processors is that for number of cores supported, the maximum thermal design power (MaxTDP) is actually pretty good. This is particularly true when you look at some of the T_{CASE} ratings. Not too long ago T_{CASE} ratings were down below 70°C for some previous high-performance processor generations. This made it a nightmare to efficiently cool a system, and in some cases required a de-rating of a system's operating temperature.

The improved thermal profiles of these processors are excellent matches for space-constrained chassis applications. For most of these Intel® Xeon® E5-2600 v3 Series processors, a dual HDEC Series system host board will typically have a 0°C to 50°C operating temperature range specification. System operating temperature ranges can vary significantly depending on the enclosure design and the system cooling mechanisms employed. A typical rackmount computer deployed in the usual server rack installation and using a dual HDEC SHB may carry the most common 0°C to 35°C system operating temperature rating with a system airflow requirement in the neighborhood of 350LFM. However, special purpose enclosures designed for military or outside applications may carry significantly expanded operating temperature ratings enabled by a combination of advanced enclosure warmers and cold-plate enclosure cooling technology.

HDEC System Host Board – Power Requirements for Dual Intel® Xeon® E5-2600 v3 Processors

Power consumption is always a concern in high performance computing, and high density embedded computing applications based on a dual-processor HDEC Series system host board is no exception. Intel® Xeon® E5-2600 v3 Series processor features like Intel® Turbo Boost and Enhanced Intel® SpeedStep technologies help mitigate power consumption by varying the processor cores speeds. Slowing down the processors while the computational demands are low saves power and reduces unnecessary heat generation. Peak power demands of the system host board and the system's plug-in option cards need to be accounted for when choosing the system power supply. The tables below provide a general guide to the power requirements for a system power supply's +3.3V. +5V and +12V rails when using a dual processor HDEC Series SHB such as Trenton's HEP8225.

Processor	Base Core Speed	Cores	+3.3V	+5V	+12V
Intel Xeon E5-2608L v3	2.0GHz	6	2.61A	3.80A	3.52A
Intel Xeon E5-2618L v3	2.3GHz	8	3.06A	4.36A	4.56A
Intel Xeon E5-2628L v3	2.0GHz	10	2.30A	4.23A	5.18A
Intel Xeon E5-2648L v3	1.8GHz	12	2.29A	4.24A	5.24A
Intel Xeon E5-2658 v3	2.2GHz	12	2.28A	4.24A	5.41A
Intel Xeon E5-2680 v3	2.5GHz	12	2.28A	4.30A	5.62A

Table 2 – HEP8225 Power Requirements – Static Desktop/Idle State

Processor	Base Core Speed	Cores	+3.3V	+5V	+12V
Intel Xeon E5-2608L v3	2.0GHz	6	2.93A	4.10A	12.51A
Intel Xeon E5-2618L v3	2.3GHz	8	3.21A	4.79A	14.10A
Intel Xeon E5-2628L v3	2.0GHz	10	2.60A	4.73A	18.16A
Intel Xeon E5-2648L v3	1.8GHz	12	2.59A	4.88A	18.20A
Intel Xeon E5-2658 v3	2.2GHz	12	2.77A	5.08A	24.81A
Intel Xeon E5-2680 v3	2.5GHz	12	2.79A	5.28A	27.67A

Table 3 – HEP8225 Power Requirements – 100% Stressed/Fully Loaded State

The power numbers in tables two and three are pretty good guidelines, but your actual power numbers will vary by a number of system application factors including the amount of system memory installed on the SHB. For these power requirement tests we used 64GB of DDR4-2400 memory.

Section 3 – System Host Board Performance Benchmark Considerations

Processor benchmarks can serve as a useful guide in selecting the specific CPU to meet the unique application requirements. Analyzing the benchmark results below will help you assess the relative processing capabilities of long-life embedded Intel® Xeon® E5-2600 v3 Series of processors currently supported on the HEP8225 HDEC Series system host board. Table 4 lists the processors tested, the type of benchmark tests we ran on the HEP8225 SHB, and the numerical results of each benchmark test.

Note1: All Haswell-EP processors listed here support Intel Hyper-Threading Note2: Processors have slightly different maximum memory interface speeds Benchmark Test	Units	Dual, Intel Xeon E5-2608L v3 Core Speed: 2.0GHz, no turbo, DMI2: 6.4GT/s CPU Cores: Six (6), Cache: 15MB, TDP: 52W Max. Memory Interface Speed: DDR4-1600	Dual, Intel Xeon E5-2618L v3 Core Speed: 2.3GHz base/3.4GHz turbo, DMI2: 8.0GT/s CPU Cores: Eight (8), Cache: 20MB, TDP: 75W Max. Memory Interface Speed: DDR4-1866	Dual, Intel Xeon E5-2628L v3 Core Speed: 2.0GHz base/2.5GHz turbo, DMI2: 8.0GT/s CPU Cores: Ten (10), Cache: 25MB, TDP: 75W Max. Memory Interface Speed: DDR4-1866	Dual, Intel Xeon E5-2648L v3 Core Speed: 1.8GHz base/2.5GHz turbo, DMI2: 9.6GT/s CPU Cores: Twelve (12), Cache: 30MB, TDP: 75W Max. Memory Interface Speed: DDR4-2133	Dual, Intel Xeon E5-2658 v3 Core Speed: 2.2GHz base/2.9GHz turbo, DMI2: 9.6GT/s CPU Cores: Twelve (12), Cache: 30MB, TDP: 105W Max. Memory Interface Speed: DDR4-2133	Dual, Intel Xeon E5-2680 v3 Core Speed: 2.5GHz base/3.3GHz turbo, DMI2: 9.6GT/s CPU Cores: Twelve (12), Cache: 30MB, TDP: 120W Max. Memory Interface Speed: DDR4-2133
Processor Arithmetic							
Aggregate Native Performance	(GOPs)	177.81	296.54	320.14	350.23	433.89	501.50
Dhrystone Integer Native AVX2	(GIPs)	239.45	397.55	438.76	461.33	580.86	672.76
Whetstone Single-float Native AVX	(GFLOPs)	157.48	263.11	281.28	317.59	383.00	444.88
WhetstoneDouble-float AVX	(GFLOPs)	110.70	186.00	194.43	222.60	274.29	314.15
Whetstone Aggregated-float Native	(GFLOPs)	132.10	221.19	233.86	265.89	324.11	373.84
Processor MultiMedia							
Aggregate MultiMedia Native Performance	(Mpixel/s)	249.69	347.67	431.79	466.26	536.24	589.24
MultiMedia Integer Native x32 AVX2	(Mpixel/s)	275.90	371.00	468.44	511.36	565.00	633.57
MultiMedia Long-int Native x1 ALU	(Mpixel/s)	97.45	163.44	178.55	204.40	244.00	279.78
MultiMedia Quad-int Native x1 ALU	(Mpixel/s)	3.00	5.10	5.55	6.16	7.58	8.82
MultiMedia Single-float Native x16 FMA	(Mpixel/s)	268.17	375.36	465.41	502.75	582.57	626.45
MultiMedia Double-float Native x8 FMA	(Mpixel/s)	210.40	301.74	369.26	394.28	468.51	515.47
MultiMedia Quad-float Native x2 FMA	(Mpixel/s)	11.56	19.36	21.32	23.23	27.85	32.45
MultiCore Efficiency							
InterCore Bandwidth	(GB/s)	56.38	86.65	88.00	88.50	114.29	123.00
InterCore Latency***	(ns)	161.40	125.20	140.10	154.70	131.30	126.60
Memory Bandwidth							
Aggregate Memory Performance	(GB/s)	52.90	79.00	87.00	90.80	97.28	98.30
Integer Memory Bandwidth B/F AVX2/256	(GB/s)	53.09	79.00	86.00	88.79	96.28	97.13
Float Memory Bandwidth B/F FMA/256	(GB/s)	52.72	79.00	88.00	92.84	98.19	99.50
Memory Latency							
Memory Latency***	(ns)	42.90	31.00	37.70	36.60	33.60	32.70
Speed Factor***	-	21.50	26.30	23.00	22.30	24.30	26.80

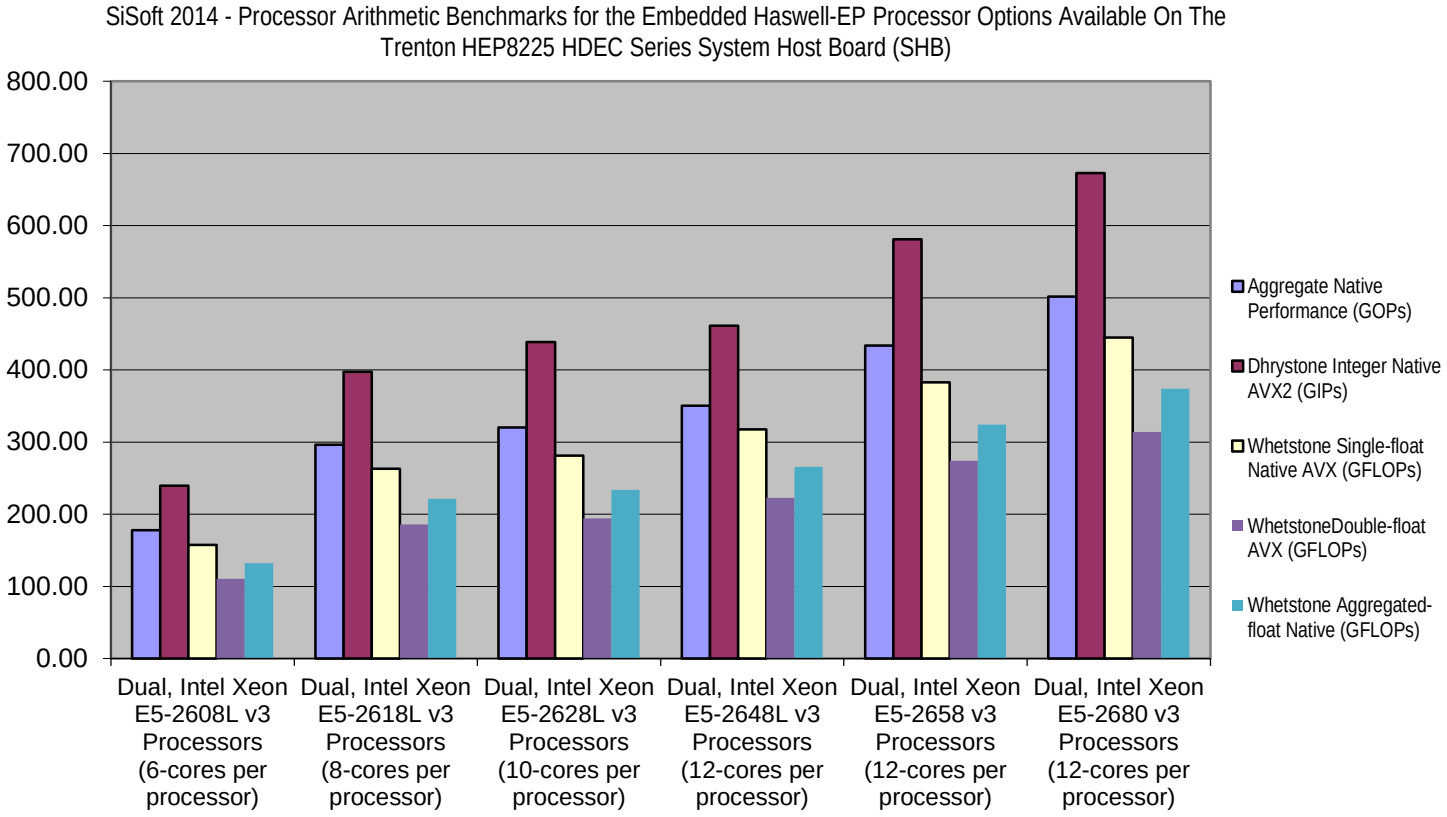
*** lower value indicates a better score

Table 4 - SiSoft 2014.06.20.35 Benchmark Comparisons for long-life Intel Xeon E5-2600 v3 Series Processors

The HEP8225 benchmark testing setup was the same for each set of dual processors and included:

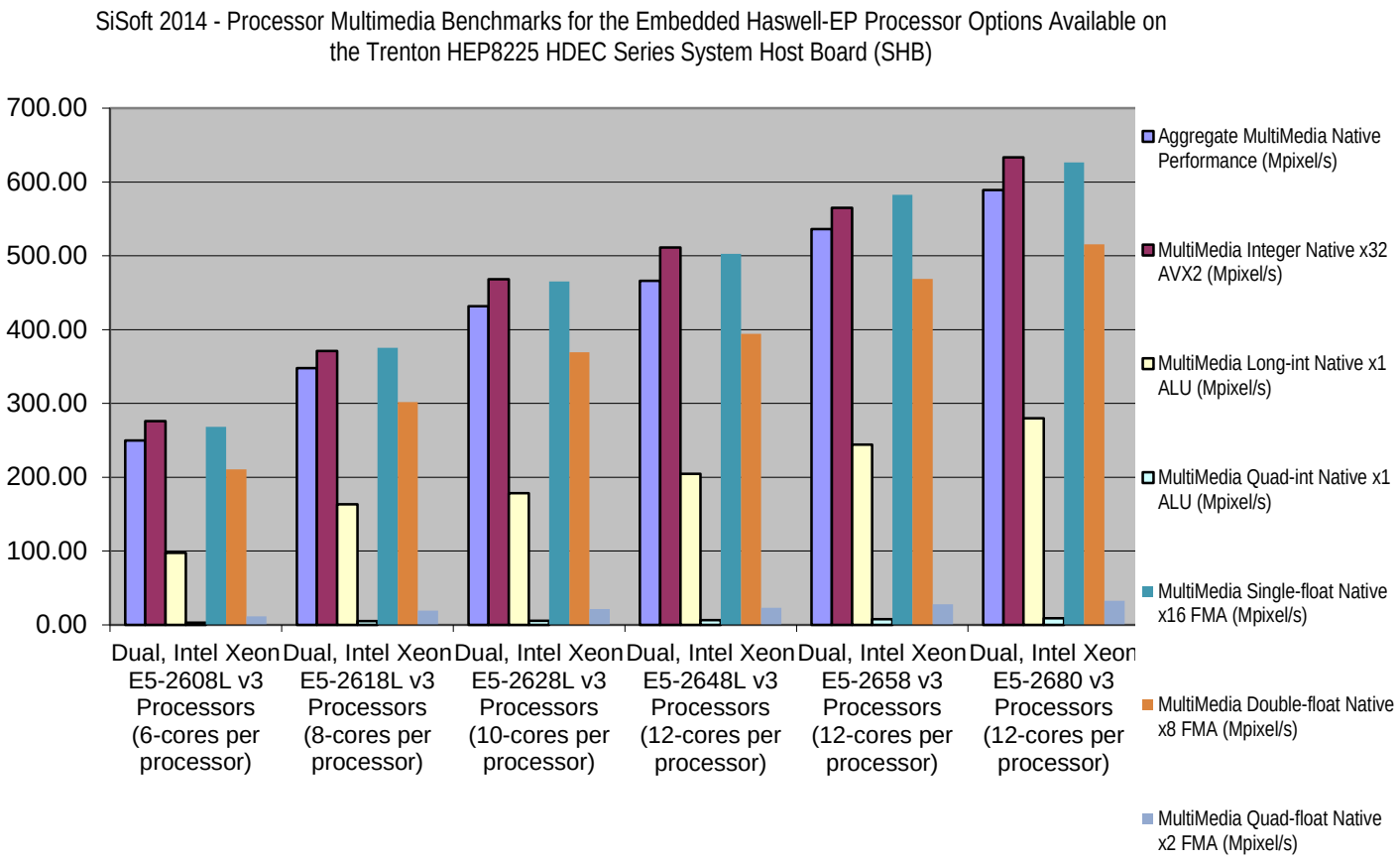
- Benchmark test software version: SiSoft 2014.06.20.35
- System memory: eight (8), 8GB, DDR4-2133, Registered, ECC, 288P DIMMs
- Total memory: 64GB
- Operating System: Windows 8.1

HDEC System Host Board – Processor Arithmetic Benchmark Results



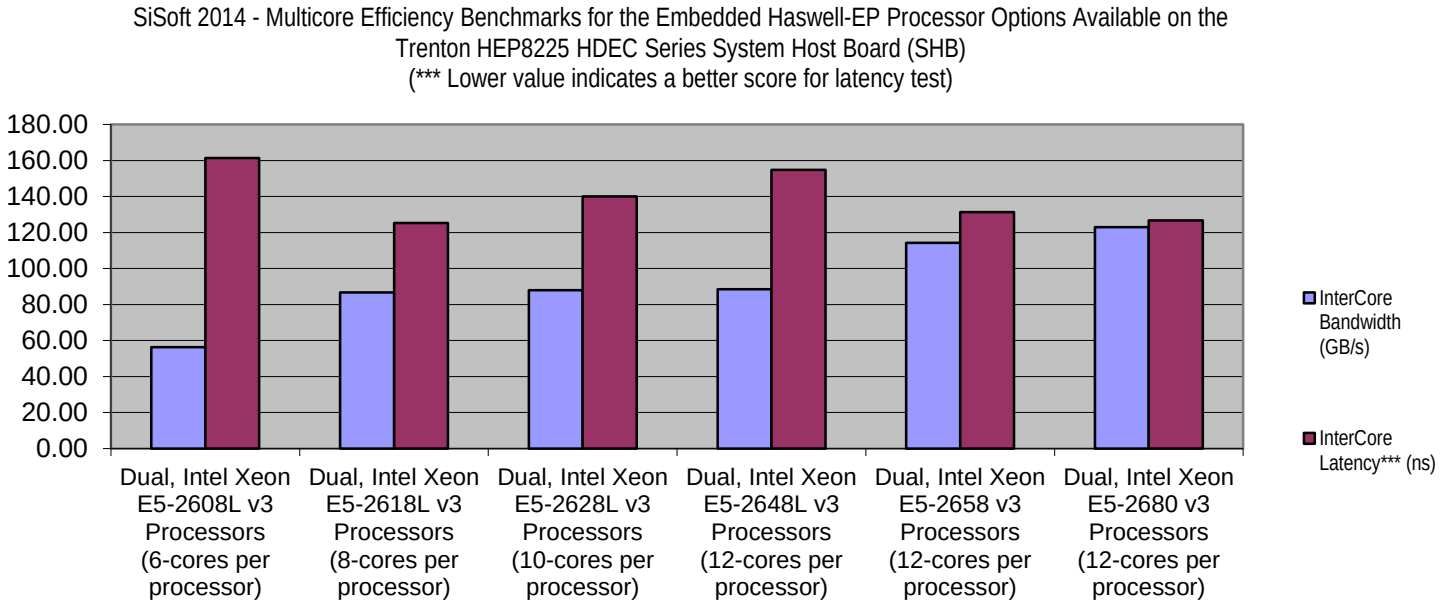
This is probably the most important benchmark measure for processors used in high-density/high-performance embedded computing applications since it measures how fast the processor performs the basic computational tasks common in all computing applications. What's interesting about these results are that both increasing the number of cores *and* increasing the core speed is critical to improved performance. For example, compare the test results returned by the E5-2618L v3, E5-2628L v3 and E5-2648L v3. The 8-core E5-2618L v3 delivers similar performance to the 12-core E5-2648L v3 for about half the processor cost. This is something to consider for cost-constrained applications. As expected the E5-2680 v3 delivered the best overall performance due to both the processor's 12 cores and the base and turbo boost frequencies of this particular CPU. As with all of the processors, increasing the number of cores provides the most system performance benefit for highly multi-threaded software applications.

HDEC System Host Board – Processor Multimedia Benchmark Results



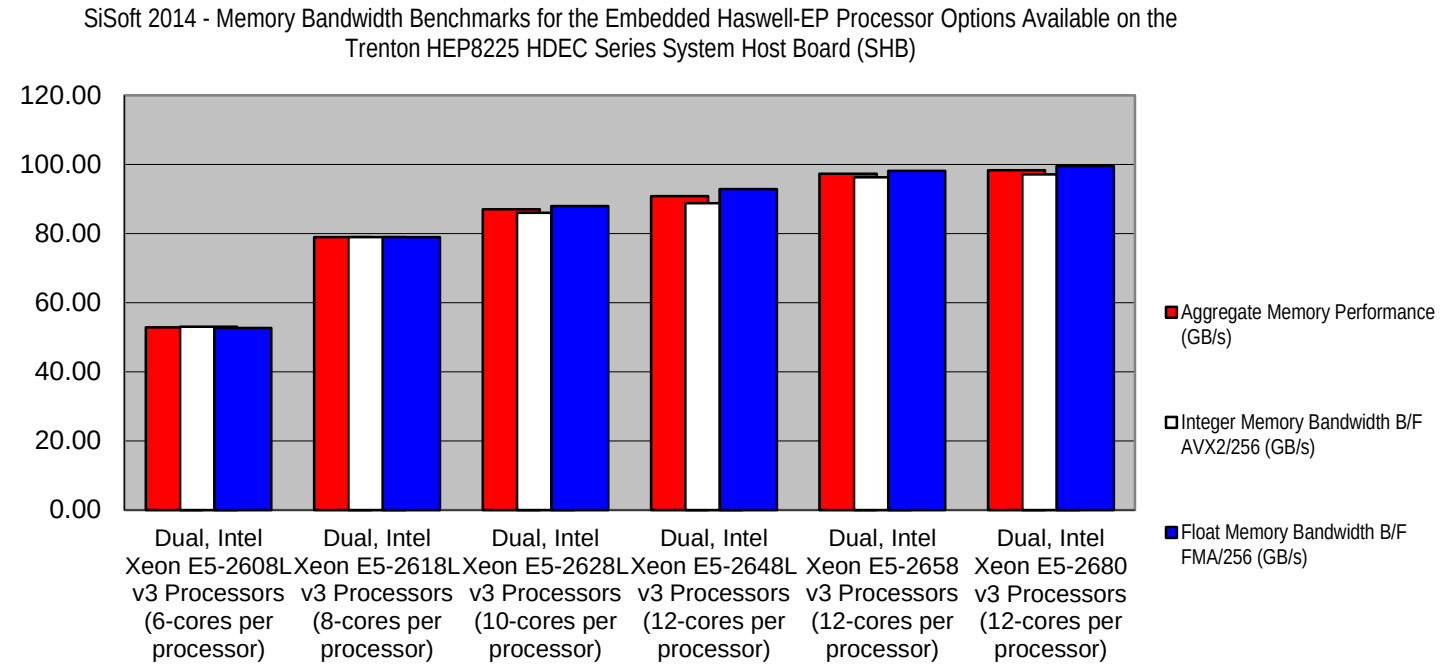
If handling multimedia operations is of prime consideration in the application, then it might make sense to consider a 12-core processor.

HDEC System Host Board – Processor Multicore Efficiency Benchmark Results



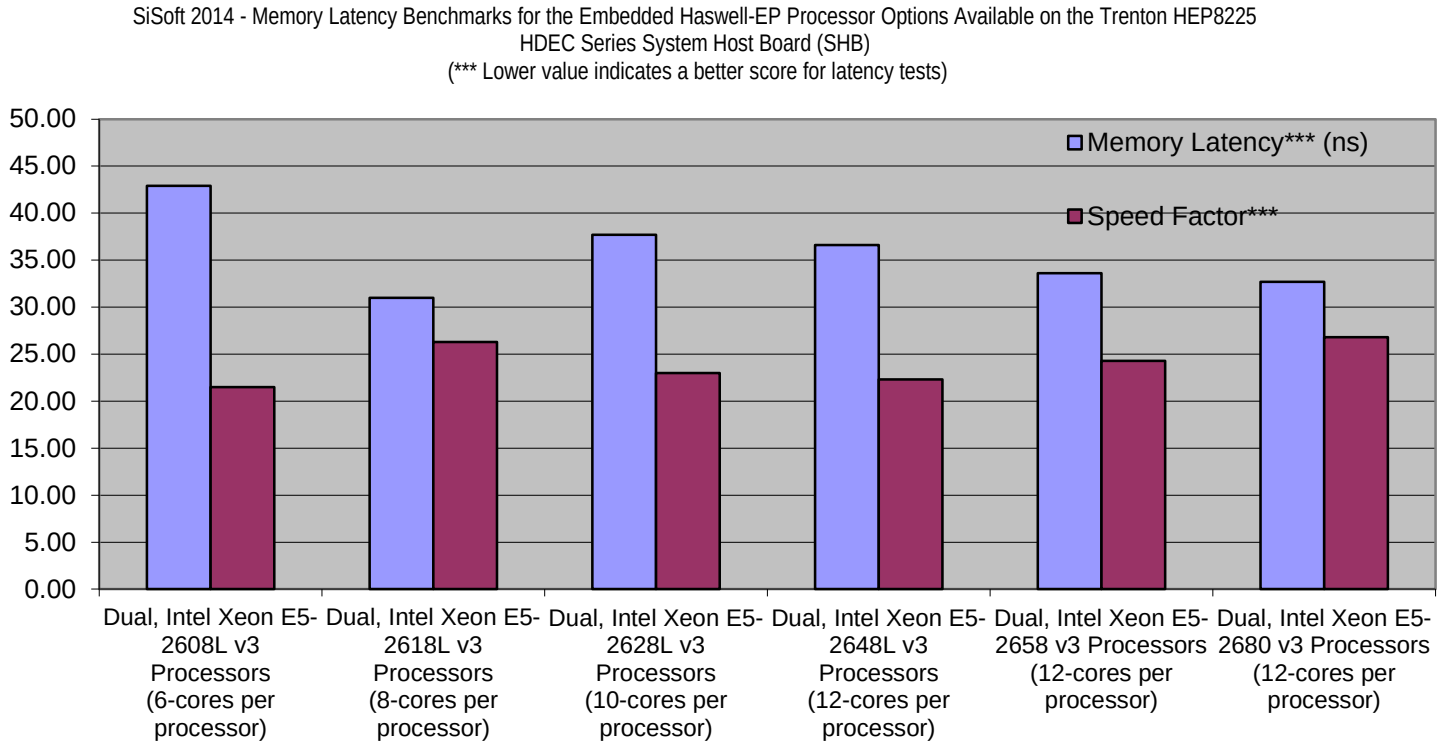
The lower the number when measuring inter-core latency indicates a better multi-core efficiency. Notice that again the L processor versions do not perform as well on both the inter-core bandwidth and latency benchmark measures.

HDEC System Host Board – Processor Memory Bandwidth Benchmark Results



Remember that the three processors on the right side of the memory bandwidth chart are capable of running at the DDR4-2133 memory interface speed. You can see this performance advantage in the chart, and it's something to consider in intensive system memory applications.

HDEC System Host Board – Processor Memory Latency Benchmark Results



Like the multicore efficiency measures, lower numbers indicate better performance for the processor memory latency benchmarks.

Section 4 – HDEC Backplane Considerations

The advantage of having eighty lanes of PCI Express 3.0 to work with in an HDEC backplane design results in backplane designs that deliver more bandwidth with lower data latencies between an HDEC Series system host board and industry standard, commercial-off-the-shelf (COTS), PCIe plug-in cards. In some cases, an HDEC backplane design can eliminate expensive PCI Express switches entirely.

Routing PCIe Gen3 links directly to a backplane's option card slots eliminates PCIe switch hops between the SHB and any of the system plug-in cards. Eliminating switch hops can provide a 15.3% average bandwidth gain per option card slot compared to previous generation PICMG 1.3 backplane designs. For example, compared to the 32GB/s aggregate slot bandwidth of a similar PICMG 1.3 backplane design, a switchless design HDEC Series midsize backplane delivers a 5x bandwidth increase for an amazing 160GB/s of aggregate slot bandwidth. Figure 6 shows the slot layout of roughly equivalent PICMG 1.3 and a compatible HDEC backplane to illustrate this point.

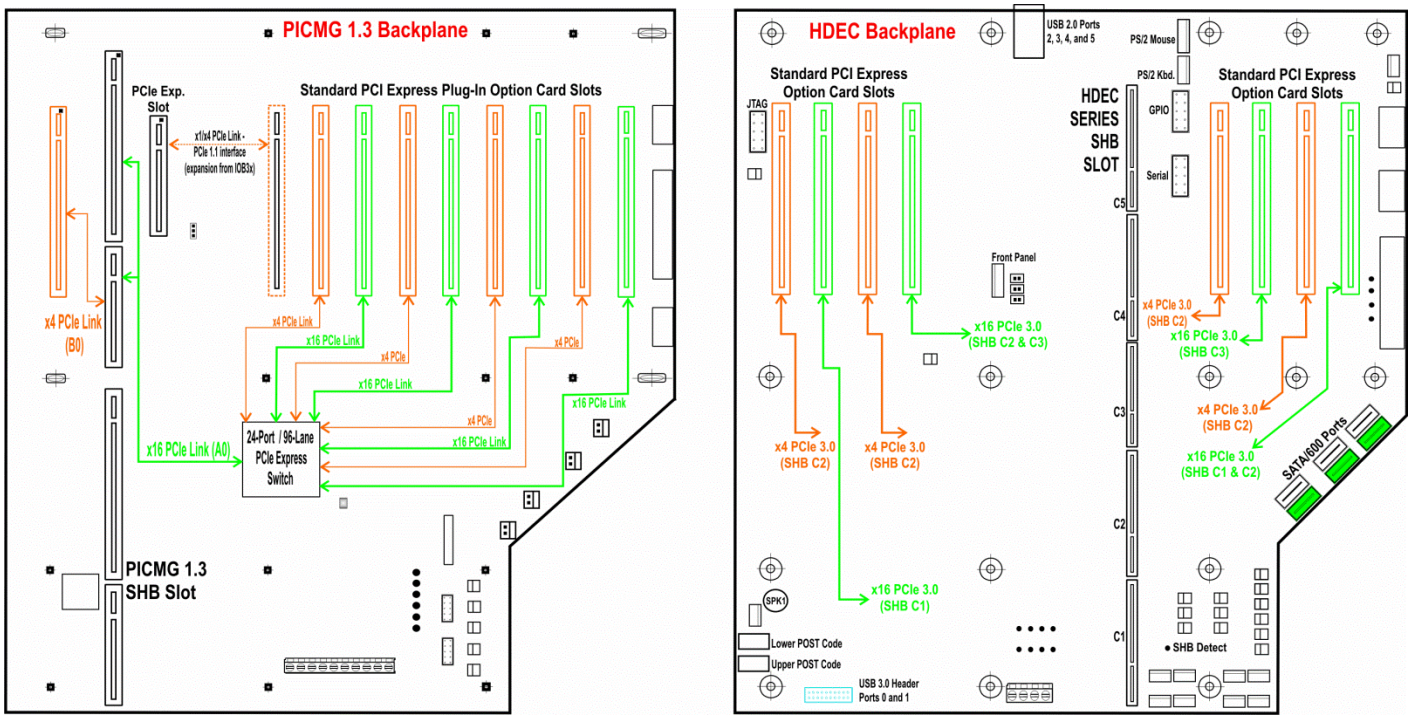


Figure 6 – HDEC and PICMG 1.3 Backplane Layout Comparisons

Notice that there are significantly more system diagnostics and device level I/O connectors on the HDEC backplane located on the right side of Figure 6. This was mentioned earlier and is a direct result of using high-density/hi-speed connectors for the system host board to backplane interface. The additional contacts available to the HDEC SHB and backplane designer enables these I/O connections to be located on the backplane thereby providing a more streamlined system cable harness design. Moving the I/O connections off the system host board improves an HDEC system's airflow, and this design approach results in greater long-term system reliability and operational efficiency.

PCI Express 3.0 Link Design Considerations for HDEC Backplanes

As we've seen, HDEC backplanes are driven by PCI Express Gen3 link technology. Here is a short list of some important considerations when designing PCI Express 3.0 backplanes:

- Need to maximize signal integrity across the entire single trace length
- Must maintain a consistently open PCIe signal transmission "eye"
- Effectively managing the following PCIe Gen3 parameters will lead to successful HDEC backplane designs
    - Jitter Control
    - Impedance discontinuities
    - High frequency losses

At PCIe 3.0 speeds, maintaining signal integrity and achieving target performance levels present a number of backplane design challenges. At 8GT/s bit rates the signal loss increases, both capacitive and signal/noise ratio loss. PCIe Gen3 clock-jitter specifications also have been tightened. In addition, the change to 128b/130b encoding means DC wander becomes a more significant issue that must be tightly controlled in the hardware rather than compensated for by the encoding scheme (as was the case with 8b/10b encoding).

In the past, links could use "dumb" redrivers but now the Gen3 links need more end-to-end integrity and can't simply be broken up with passive redrivers. PCIe 3.0 link re-timers are going to need to be incorporated into any HDEC backplane design to ensure optimum automatic link negotiation between the HDEC SHB's root link complex at the board's processors and the downstream PCIe target devices or plug-in option cards.

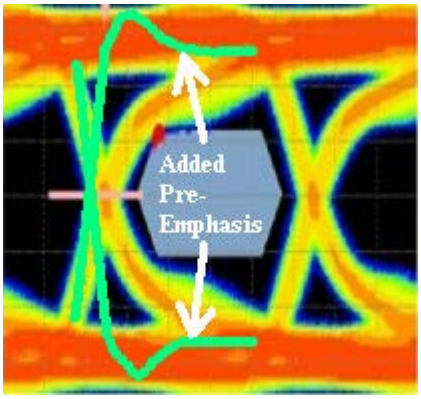


Figure 7 – PCIe 3.0 Link Pre-Emphasis Added to Maintain an Open Signal Eye

The backplane material itself, component placements and the length of the traces that connect them together all factor into a backplane design. The max overall length of a PCIe trace depends on several factors including the dielectric loss due to the roughness of the copper traces, weave of board material used, trace width, rotation of the panel weave during PCB fabrication, and the successful application of the automatic 8Gb/s equalization training. For example, with previous generations of PCI Express it was best practice to keep traces well below 16 inches to insure optimum operability. The PCIe Gen3 specification makes the length requirement even more restrictive.

The Gen3 specification also requires a pre-validation of the link before data transfer. If the automatic equalization training cannot establish a reliable link, it will not allow the transfer of data at 8Gb/s speeds, which significantly compromises the target performance goals. For more backplane design details see the paper entitled, "Optimizing PCIe 3.0 Backplane Designs for Performance and Reliability".

Available HDEC Backplane Form Factors

HDEC backplanes come in a wide variety of shapes and sizes. Backplane size selection is primarily driven by the number of option card slots needed and the system chassis design. Other application factors come into play such as the need to support multiple system host boards in one common chassis enclosure. Table 5 below summarizes some of the available HDEC backplane form factors as a function of system chassis type.

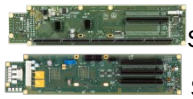
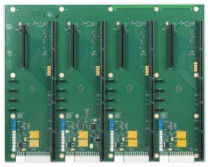
Backplane Type	Image	Chassis Type	Electrical Card Slot Interfaces Supported (all slots use x16 PCIe mechanical connectors)	HDEC SHB Slots
2U Butterfly Format	 Side A Side B (Trenton HDB8227)	2U Rackmount	4 - x16 PCIe 3.0/2.0/1.1	1
Shoebox Format	 (Trenton HDB8236)	Custom or dual 4U or 5U Rackmount	4 - x16 PCIe 3.0/2.0/1.1 1 – x8 PCIe 3.0/2.0/1.1	1
Midsize Format	 (Trenton HDB8228)	4U Rackmount (short depth)	4 - x16 PCIe 3.0/2.0/1.1 4 – x8 PCIe 3.0/2.0/1.1	1
Multi-Segment, Large Format	 (Trenton HDB8237)	5U Rackmount	4 - x16 PCIe 3.0/2.0/1.1 (one per SHB segment)	4

Table 5 – HDEC Backplane Form Factors

Section 5 – HDEC System Considerations

High density embedded computing (HDEC) systems provide superior processing performance, expanded PCI Express I/O card support, rugged dependability and system configuration stability over the life of your application. The HDEC system host board and backplane technology can be easily integrated into industry standard 2U, 4U and 5U rackmount computer enclosures as well as custom-built enclosure form factors.

HDEC embedded computing systems deliver wider system bandwidths and lower data latencies when integrating large numbers of today's standard, off-the-shelf PCI Express plug-in cards. The HDEC system designs are flexible, general purpose solutions for high-end data gathering, data storage, and video processing applications. The HDEC system configuration flexibility and rugged computer design enables deployment across a wide spectrum of industries such as government and defense, big data, industrial automation, and test & measurement that all demand longevity and robust computing performance.

HDEC System Considerations – Rear I/O Fence

The rear I/O bracket of an HDEC system host board takes up two I/O slot positions. Most I/O positions at the rear of a standard 4U or 5U, 19" rackmount computer enclosure have a single slot I/O dimension of approximately 0.55"/13.97mm. You will need to remove the center I/O slot divider on your chassis' rear I/O fence at the HDEC SHB's backplane slot location as illustrated in Figure 8.

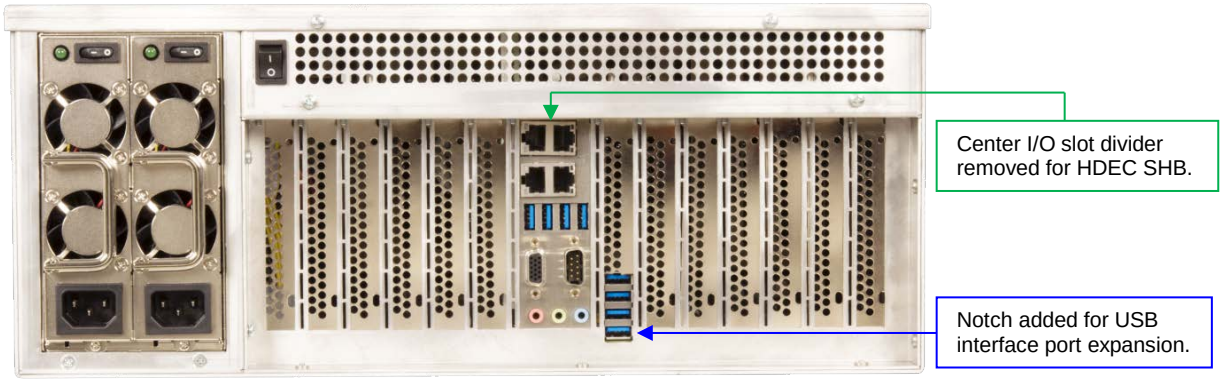


Figure 8 – HDEC Chassis Rear I/O

As discussed previously, you may design an HDEC backplane that takes advantage of the SHB-to-Backplane routings of various USB device interfaces. Some chassis; like the example shown in Figure 8, may not have backplane mounting plate that serves to raise up the HDEC backplane to, among other things align the top surface of the backplane with the lower surface of the rear I/O slots. If this is the case, you may need to notch out the rear fence to accommodate any required rear USB I/O expansion.

HDEC System Considerations – Hot Swap Storage Drives and System Fans

The HDEC system I/O map in Appendix B lists the various system monitoring and control signals available to the system designer. For example the PWM signal lines are ideal for controlling system fan speed, while the fan and drive status can be monitored via other available signal lines such as the Intelligent Platform Management Bus (IPMB). Figure 9 shows an example of an HDEC system that supports front access, hot swap system fans and storage drives in order to minimize Mean Time to Repair (MTTR) durations while maximizing system up time.

Figure 9 – Hot Swap Fans and Storage Drives

HDEC System Considerations – Maximizing Airflow and Cooling Efficiency

The interior shots of the HDEC Systems in Figure 10 illustrate how moving as many I/O interconnects off the system host board and onto the backplane enable a more streamlined interconnect cable design. The idea is to get the interconnect cables out of the way of all of the plug-in boards so as to not impede the flow of air through the HDEC system chassis.

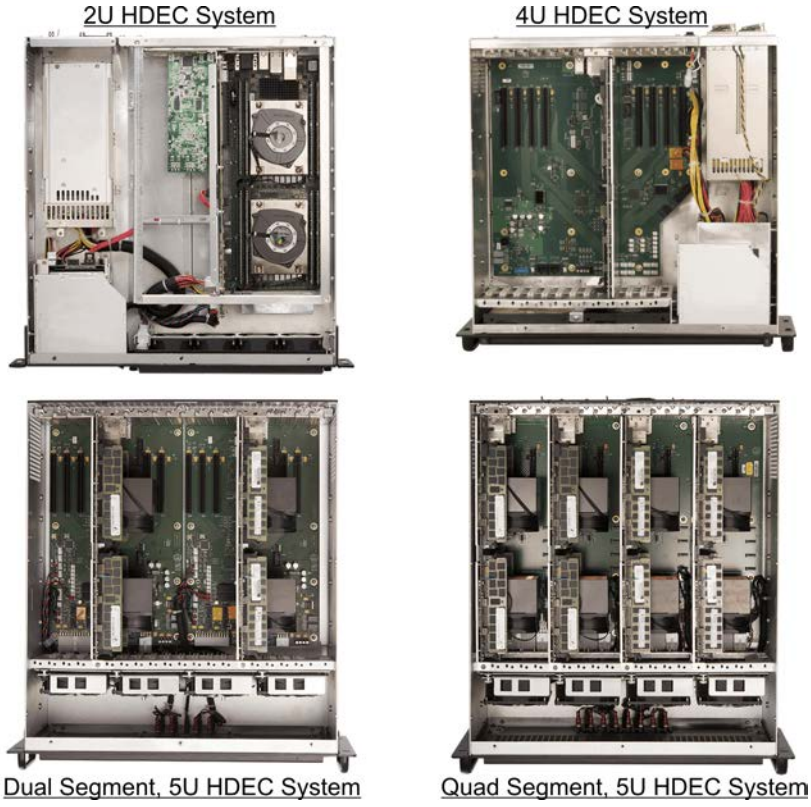


Figure 10 – HDEC System Cabling vs. System Airflow Efficiency

Section 6 – HDEC Summary and Conclusions

As you can now see the high density/high speed edge connectors utilizes by HDEC system host boards and backplanes enables expanded system I/O and 80 or more lanes of PCIe 3.0 lanes to be routed down to the system backplane. This embedded system design approach provides some significant advantages to system designers. Supporting 80 lanes of native PCI Express 3.0 links delivers a 5x increase in aggregate system bandwidth with lower SHB-to-PCIe plug-in card data latencies compared to previous system board and backplane technologies.

The processors utilized in the latest dual-processor HDEC system host boards deliver impressive performance. The power budget and thermal dissipations for these processors are reasonable given the high-performance computing levels obtained. HDEC backplane designs are as varied as the universe of high-performance embedded computing system applications. Best backplane design practices were discussed for PCI Express 3.0 link technology. Finally, HDEC systems are the glue that pulls all the new high density embedded computing technology advancements of the SHBs and backplanes together to deliver on the promise of added bandwidth with lower data latencies in a wide variety of embedded computing applications.

About Trenton Systems & For Additional Information

Contact us for more information about Trenton's HDEC Series of system host boards, backplanes, and complete system offerings or any of our other embedded computing products or integrated computer systems. Trenton team members welcome the opportunity to work with you.

Trenton Systems is a designer and manufacturer of military and industrial computing systems, PCI Express expansion systems, rackmount computers, video capture and display wall controllers, GPU computing systems, custom systems, embedded motherboards, single board computers, system host boards, and backplanes for critical embedded computing applications.

Trenton products are designed and built in the U.S. and are well suited to deliver long-life performance, precision and reliability in military, DoD, medical instrumentation, industrial control, and video capture and display wall systems.

Trenton industry partnerships with Intel and other leading technology companies play an important role in the design, manufacture, integration and deployment of our high-performance system solutions. For example, Trenton Systems is an Affiliate member of the Intel® Internet of Things Solutions Alliance**.** From modular components to market-ready systems, Intel and the 250+ global member companies of the Intel® Internet of Things Solutions Alliance provide scalable, interoperable solutions that accelerate deployment of intelligent devices and end-to-end analytics. For example, Trenton Systems' board level products and integrated computer systems are used to create a variety of mission critical solutions, from Government and Defense to Industrial Automation, Virtualization, Video Processing, Medical, Communications, Energy, GPU Computing, Test & Measurement and Video Display Walls.

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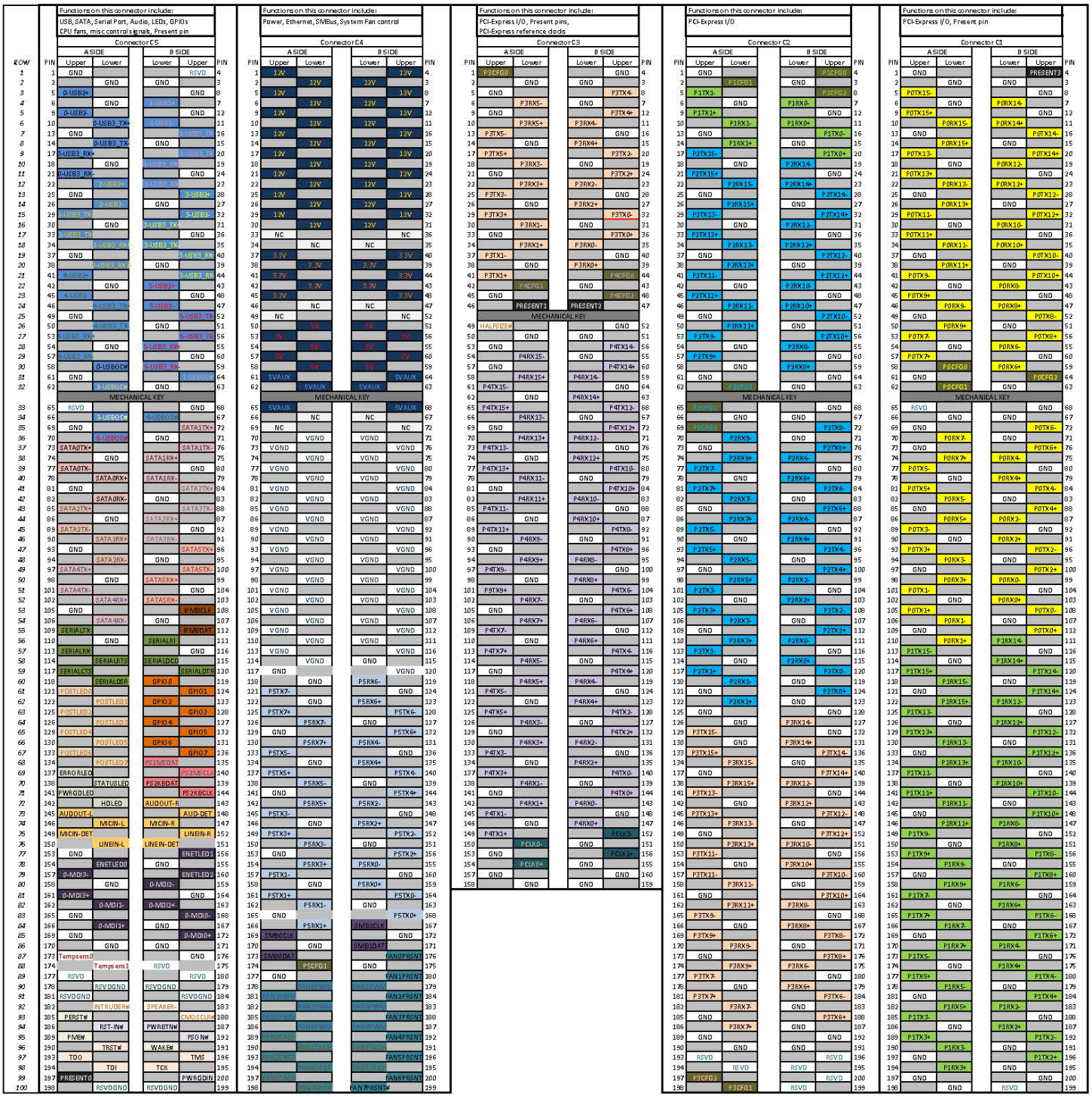
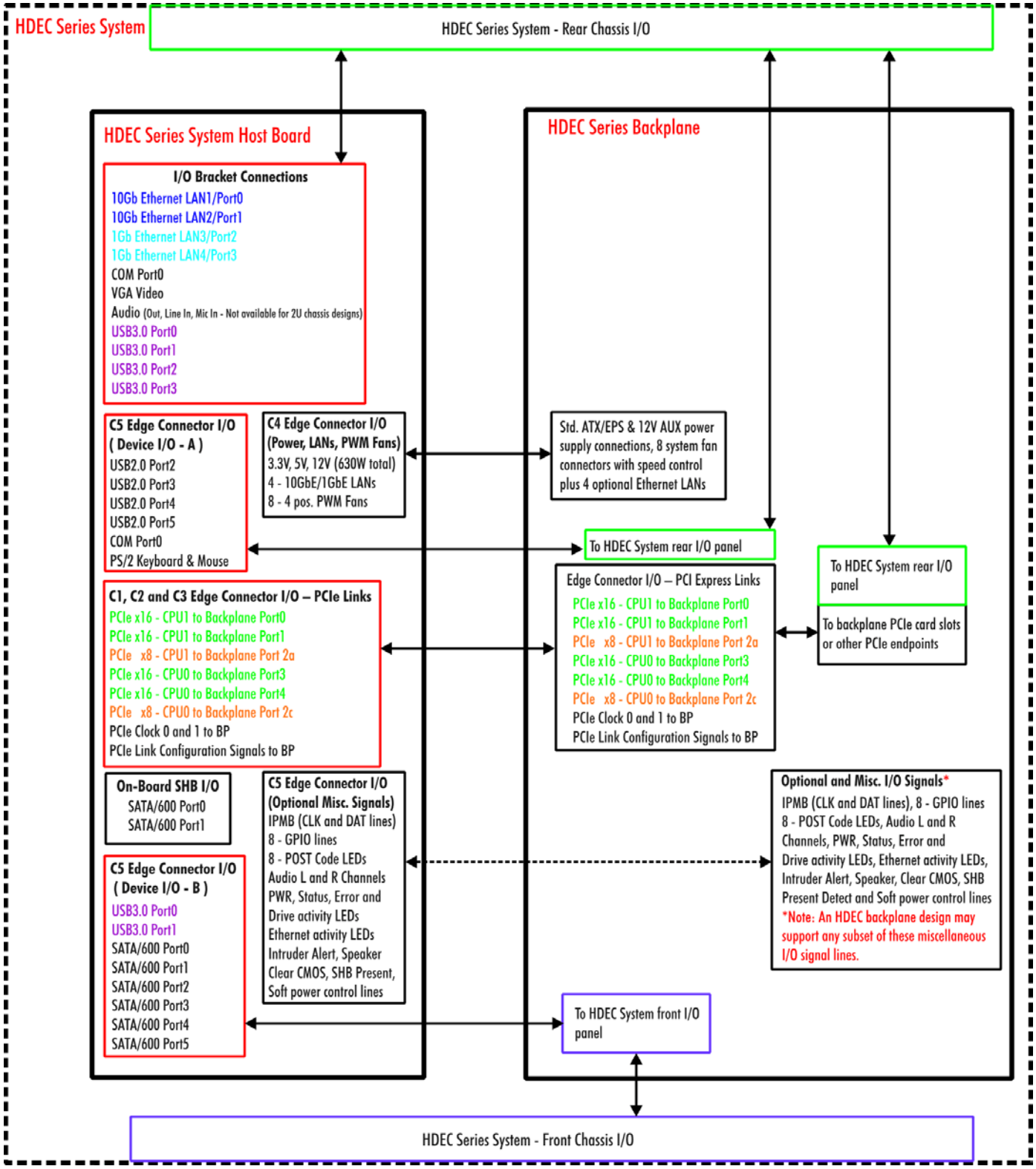
Appendix A – HDEC Pin Assignmments



Appendix A, Table 1 – HDEC SHB Pin Assignments

Appendix B – HDEC I/O System Map



Appendix B, Figure 1 – HDEC System I/O Map