TECHNICAL PAPER

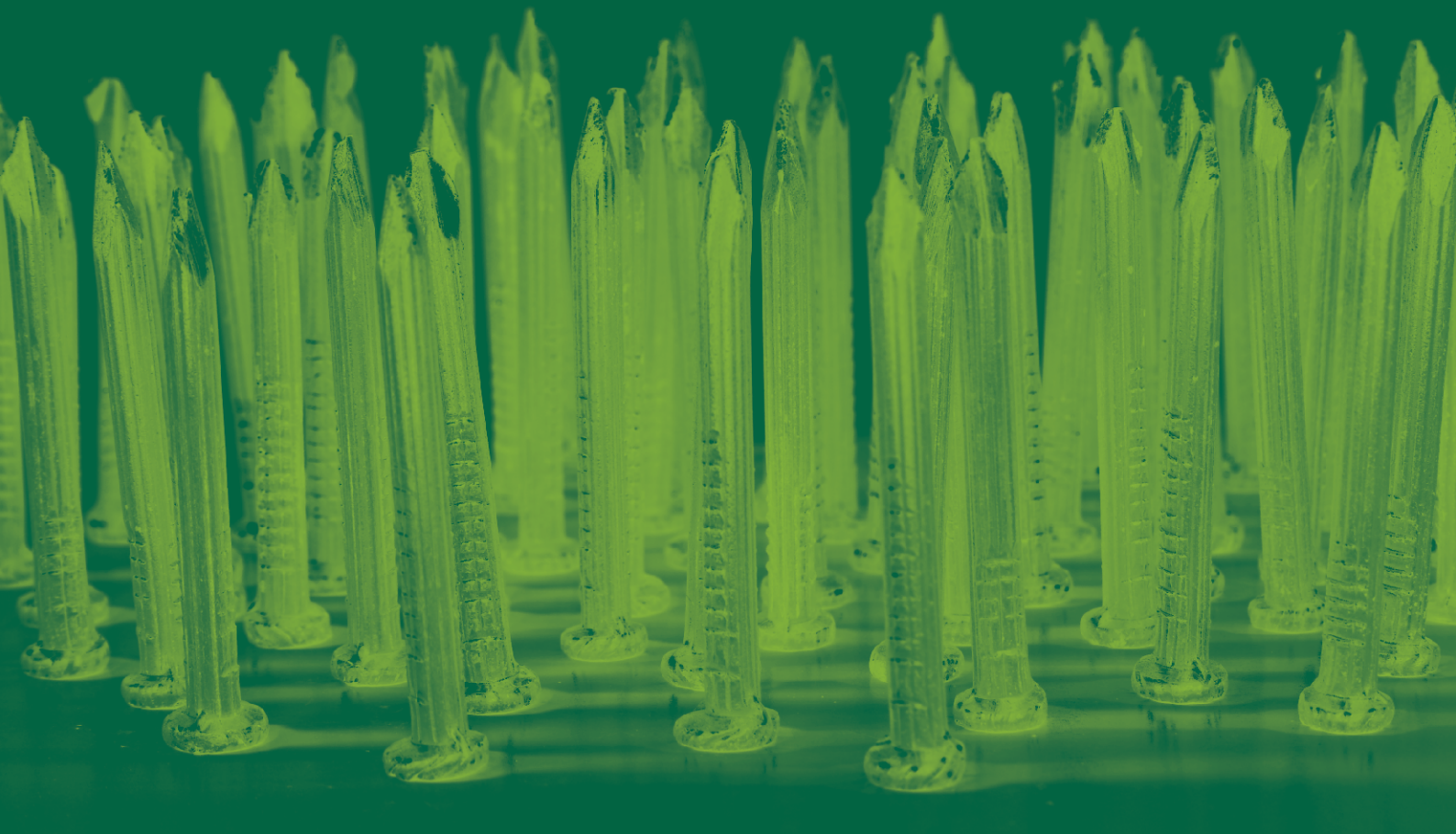
DESIGN GUIDELINES FOR IN-CIRCUIT TESTABILITY

MANUFACTURING

An ESCATEC Company

DESIGN GUIDELINES FOR IN-CIRCUIT TESTABILITY

IN-CIRCUIT TEST (ICT) HAS REMAINED ONE OF THE MOST POPULAR AND COST-EFFECTIVE TEST METHODS FOR MEDIUM AND HIGH VOLUME PRINTED CIRCUIT BOARD ASSEMBLY (PCBA) FOR MANY YEARS. THIS IS DUE TO ITS COMPONENT-LEVEL FAULT DIAGNOSIS CAPABILITY- AND ITS SPEED.



ICT checks each component on a PCB individually, delivering highly reliable results. It detects defects such as wrong or missing components, solder bridges and short circuits. While investing in this solution requires a larger initial upfront cost when compared to flying probe, the cost per unit is negligible - often less than £1 - due to the swift test time (less than one minute).

The ICT method comprises a test fixture and program dedicated to the target test platform and unit under test (UUT). In order to optimise the effectiveness of the test, the circuit design and layout of the PCBA itself must be suitable for ICT. Therefore, design for test (DFT) is an integral stage of PCB realisation; without taking this phase into account, you will not be able to get the most from your test strategy.

This technical paper describes what should be taken into consideration, to help maximise the achievable test coverage - and deliver the highest quality PCBAs to your customers.

TEST METHODS AND PRACTICE

Firstly, let's look at the basics of ICT, as these provide a background to the design requirements detailed later.

Computer-aided design (CAD) data, usually the ASCII file for the PCBA, is processed through an appropriate software package to produce the test fixture design files. It is also used, along with the bill of materials (BOM) and circuit diagrams, to create an automatic test equipment (ATE) input, which is used to generate and optimise the ICT program.

The test program is firstly set to detect short circuits wherever test access is available; it then features routines to measure the value of all testable discrete components, ensuring their correct measurement and isolated performance.

Digital "vector" tests are used for all ICs where templates exist - for example, standard parts such as logic gates. Wherever possible, presence and orientation tests will be applied to all ICs. "Vectorless testing", such as Framescan™ or TestJet™, can be used to detect dry joints on integrated circuits and connectors.

Function tests can be set for powered or unpowered analogue devices. Crystal frequencies can also be measured where test access and type makes this possible.

The fixture will comprise a "bed of nails" to probe the UUT, and usually feature a "hold down" gate on the top, to ensure that PCBs with open vias or irregular profiles are not susceptible to vacuum fixture sealing problems.

When ICT development is completed, it is standard to produce a documentation package detailing:

- Coverage report listing tested, partially tested and untested components;
- Details of fixture wiring;
- Details of probe types used;
- Software.

CIRCUIT DESIGN CONSIDERATIONS

The aim of ICT is to individually test components in isolation from the rest of the circuitry. A “bed-of-nails” fixture is created, ideally having access to each electrical node/net on the UUT via a test pad, providing access to all signals to an individual component. If this is not possible then “cluster” testing groups of components can be performed. However, this increases programming and test time, as well as cost, as faults will be traced to a cluster of parts instead of the individual component fault.

To maximise test coverage, the following points should be considered:

- Test pads should appear as components in the CAD file, with unique identifiers and XY co-ordinates.
- All digital devices that are controlled by a chip enable/select should have this pin connected to the power supply rail through a pull up/down resistor, not directly tied. Any resistor value from 100R to 100K is acceptable.
- Batteries should not be fitted at in-circuit test. If they are fitted, a removable link must be provided to isolate the battery from the rest of the circuit.
- All chips that have a RESET pin should also have this pin available for individual test control via a pull-up/down resistor. Try to avoid directly connecting the reset line of the microprocessor/microcontroller to another bussed integrated circuit. Use a low value resistor (approximately 100 ohms). This will allow the micro to be kept in reset while testing the other device.
- Where a device is driven by an external clock circuit, this should be driven via a tri-state buffer (i.e. not directly) or an AND gate with its other signal controlled by a pull-up resistor. The oscillator can then be stopped from affecting the stability of other tests.
- Any unused inputs or outputs of devices should have their signals tied individually, preferably via a resistor, rather than directly to supply rails. This enables the use of standard library tests where available, making programming quicker and therefore less expensive.
- Show the spare gates and unused pins of ICs on circuit diagrams. On surface mount (SMT) designs a test pad should ideally be provided for unused pins of ICs, as otherwise short circuits to pins with no test points will not be detected.
- To keep test times as short as possible try to use low capacitance values on control lines - e.g. power on reset. This enables all digital tests to be carried out at higher speeds.
- To help avoid unstable test results due to “back-driving”, where programmable devices are to be used:
    - Do not tie chip enable pins to supply rails, use pull-ups;
    - Attempt to include a test vector that will either cause the output pins to become tri-state or active high;
    - Program a combination of input stimuli that will drive all output signals high.

FIXTURING AND PCB LAYOUT CONSIDERATIONS

The minimum centre-to-centre spacing between test points is governed by the pitch limitations of ICT probes. The following chart shows the pitch between test point centres that are achievable using the three standard sizes of test probes:

Probe 1	Probe 2	Min. Spacing
100mil	100mil	0.0824"
100mil	75mil	0.0754"
100mil	50mil	0.0674"
75mil	75mil	0.0685"
75mil	50mil	0.0605"
50mil	50mil	0.0500"

Where possible, try to keep the distance between test points/pads to a minimum of 0.100”, so standard 100mil probes can be used. When this cannot be achieved there are smaller probes that can be used down to 0.050” and specialist probes that will afford contact on even closer pitch - but experience has shown that the smaller the probe, the larger the probability of contact problems and reduced long-term reliability. However, it is possible to mix the various sizes on a single fixture. Another point to remember is that smaller probes tend to cost considerably more.

PCB test pads must be at least 0.125” away from the edge of the PCB. If the PCB is mounted in a frame, the targets need to be within the inside edge of the frame by this amount.

Test pads should preferably be 0.05” in diameter, but can be reduced if absolutely necessary by using alternative methods of tooling and fixture design. Square test pads are preferred as they have 27 per cent more target area over the round shape.

Test pads can be placed over the top of vias, though the hole must not exceed 0.02” diameter and the wall thickness must be sufficient to withstand the probe pressure.

Multiple test pads should be included for ground and power supply rails, and should be distributed across the PCB.

Test targets should be at least 0.100” away from any components on the probing side of the PCB.

Test pads should be distributed evenly over the surface of the PCB. Areas of high probing density should be avoided as this may cause flexing of the PCB. This in turn may cause flexing damage to components. If high-density areas do exist then the board should be stress analysed and/or redesigned.

Space must be left on the component side of the board to allow “pusher rods” to press the board down. This is particularly important in areas of high probe density. Pusher rods are typically 2mm diameter, and one is required for approximately every 2in^2 of PCB.

Note fixtures for ICT are normally actuated by vacuum, but options for mechanical and pneumatically actuated fixtures are also available.

Test pads must be provided on each net where tracks interconnect SMT devices. However, on mixed technology boards connection can often be made on conventional through-hole components. Although probing the legs of through-hole components is acceptable, more reliable results can be obtained with the use of dedicated test pads.

Through-hole components should have controlled lead length, ideally no greater than 0.062”. Keeping the lead lengths the same will assist with an even compression of all test probes, resulting in consistent compression forces.

Ensure that the solder resist does not cover any test pads or vias. Also ensure soldered test pads and particularly vias are domed with solder above the height of the solder resist mask.

To ensure accurate positioning of the board in the fixture, the tooling holes in the PCB should be at least 3 or 4mm diameter (0.125”) - though 2mm is possible if essential. Tolerances should be +0.05mm, -0.0mm. The tooling holes must not be plated. Fit two tooling holes per PCB, ideally located in diagonally opposed corners (pitch tolerance ±0.125mm), keeping the distance between them as great as possible but located a minimum distance of 3mm from the edge of the PCB. Tooling holes should appear in the CAD data as unique components with XY coordinates.

There should be an area of at least 5mm diameter around the tooling hole, on the underside of the board, which is free of components and tracks. This allows good board support without the possibility of track shorts to the tooling pins.

The minimum PCB thickness should be 0.062” inches (1.58 mm).

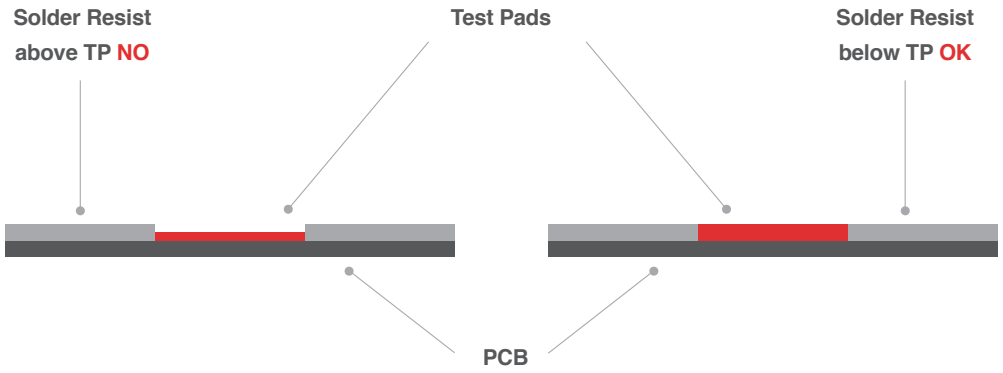
It is preferable not to perform “cut and strap” wiring modifications on the underside of the board, as the wiring could obscure the test pads.

Any components with a standoff height greater than 0.100” on the underside of the board will require milling of the fixture, which will add to the cost. Standard SMT devices are normally less than this and provide no problem.

It is mandatory to keep component bodies at least 0.050” away from adjacent test pad centres but try to achieve 0.100” wherever possible.

Probing on the component legs of SMT devices is highly undesirable as this could turn a potential dry joint into a good contact during test, as the probe tip in contact with the leg can compress the contact between the component leg and the solder pad, and thus a defective joint will pass undetected.

The best layout configuration is to have all the components on one side of the board and all test pads on the other. Fixtures are available that will allow probing to both sides of the board, but this will increase the fixture cost and program debug time. If the only way to incorporate test pads is to use both sides of the board, then the minimum size test pad target for topside probing is 0.040”.



Where functional testing is required as well as ICT on an in-circuit tester, it is essential to withdraw the probes that are used for ICT during the functional test cycle of the board. There are three options for dual stage contact within fixturing:

a) Standard vacuum fixture technology featuring a “shuttle plate” that controls the length of travel of the top plate during the ICT and functional test cycle. By using a mixture of standard and “long throw” probes, access can easily be modified to restrict in-circuit probe contact during functional testing.
b) Standard and long throw probes are used but fixture actuation is performed by pneumatic cylinders with two travel lengths. This proves to be a more robust, but more expensive solution.
c) Use discrete pneumatic probes for functional test point access.

Whichever solution is adopted it is advisable to take special care on the design of the test pads and their spacing. Long throw probes are readily available and reliable in 0.100” format. They are also available in 0.075” format but are perhaps not as reliable.

Another point to consider is that while functionally testing the board, it is generally running at higher speed than at in-circuit and is thus more susceptible to noise caused by the wiring contained in the fixture. In order to minimise this effect, it is desirable to design a board with two test pads per functional net, so only the wiring associated with functional testing is connected to the board during this part of the test cycle.

To summarise:

1. Minimum 0.035” diameter test pads on the bottom side of the PCB.
2. Minimum 0.040” diameter test pads on the top side of the PCB.
3. Test point pitch preferred at 0.100” as this is the most reliable and lowest cost.
4. At least 2x 0.125”, diagonally opposite non-plated through tooling holes in the PCB.
5. Test pads on one side of the board only.
6. All test pads/points a minimum of 0.125” away from the edge of the PCB.
7. No component more than 0.100” high on solder side of the PCB.
8. No wire links on the test access side of the PCB.
9. Two test points per functional test net.
10. Minimum 0.075” probes for functional testing.

MANUFACTURING TOLERANCES OF PCBS AND FIXTURES

In order to achieve consistent test results and contact accuracy, both fixture and PCB manufacturing tolerances need to be controlled. The chart below outlines typical tolerances that can be expected in fixturing, and the desired tolerances of PCBs:

Item	Tolerance
Test fixture drilling	± 0.002"
Receptacle and probe perpendicularity	± 0.003"
Test probe run out at the tip as it rotates	± 0.002"
Fixture tooling pin size and placement accuracy	± 0.003"
Variance of tooling hole diameter in PCB	+0.002" – 0.000"
Centre of test target to centre of tooling hole in PCB	± 0.002"
Test pad or via diameter on PCB	± 0.002"
Total Tolerance stack up	**0.032"**
Test pad size required	**0.035"**

The total tolerance stack up is double the sum of the individual tolerances, as the tolerances are ± (effectively doubling the size of tolerance error). It is most critical to control and monitor the PCB artwork tolerance, as in the above scenario there is only a margin of ± 0.0015” before the tolerance stack starts to exceed the theoretical limit of contact accuracy in a standard ICT fixture.

INFORMATION REQUIRED TO PRODUCE ICT FIXTURES AND PROGRAMS

- CAD data, usually in ASCII format, with identification of the version and format of the files.
- A bill of materials, preferably in electronic format, (e.g. Word/Excel).
- Circuit diagrams / schematics, ideally in electronic format (JPG, TIFF, or PDF).
- Populated and bare PCBs of the revision level required for the fixture and test program. If these are not available, it may be acceptable to use older issue boards provided acetates of the current revision are supplied with the changes clearly identified.
- Details of the target test system type and configuration.
- Datasheets on any non-standard components (e.g. ASICs).
- Test programming protocol specifications.
- Fixture default specifications.
- Details of any health and safety/compliance issues, especially relating to fixture handling or electrical test program operation.

CONCLUSION

In-circuit test is one of the most popular types of automated test equipment (ATE) used in medium to high volume electronic PCB assembly. And while it delivers highly reliable results, it is vital to ensure that your PCB is designed correctly, in order to achieve the optimum results.

You should ensure that you have the correct CAD data and schematics and test pads should be designed into the PCB up front. Manufacturing tolerances need to be controlled for both the fixture and the PCB.

ICT tests every component individually, identifying issues such as wrong or missing components, solder bridges and short circuits. And with a test time typically less than one minute and a cost per unit typically less than £1, it is a cost-effective method – which more than recompenses for the initial upfront cost.

Investing in an ICT solution can help your business to consistently deliver fully functional PCBs, on time and to specification. The time and money saved can be redirected back into other core aspects of your operation.

ABOUT

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