Single Floating – Isolated GaN FET Driver

FEATURES

- Floating 650V isolated driver for high-voltage GaN FET's
- No bootstrap components or isolated supply required.
- >100V/ns dv/dt immunity (CMTI)
- 35ns propagation delay with excellent device-to-device matching of <5ns
- Separate pull-up/ down drive output pins. Pull-down impedance ≤ 0.8Ω. Pull-up impedance ≤ 2.8Ω
- ≥ 100µm Distance through isolation (DTI)
- 5.5V < V_{DRIVE} < 15V.
- First pulse perfect – first drive pulse within specification
- Continuous ON time capability – no need to recycle drive
- Output drive pins OUTPU, OUTPD and OUTSS can swing ± 5kV with respect to GND
- Safety-Related and Regulatory Approvals (planned)
  - 5700VRMS Withstand isolation voltage per UL 1577
  - 8000VPK Maximum transient isolation voltage per VDE0884-10
  - 630VPK Maximum working isolation voltage

APPLICATIONS

- Totem Pole PFC, Half/ Full-Bridge, LLC, SR Drivers, Multi-level converters using stacked switches
- Secondary side control to primary drives
- Automotive

DESCRIPTION

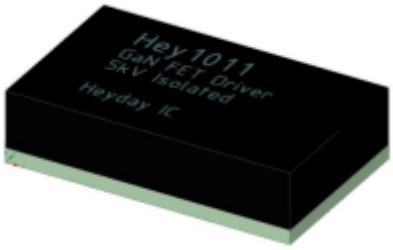


Figure 1: LGA: 10 x 7.66 x 2.64mm 12-pin integrated prototype package

BLOCK DIAGRAM

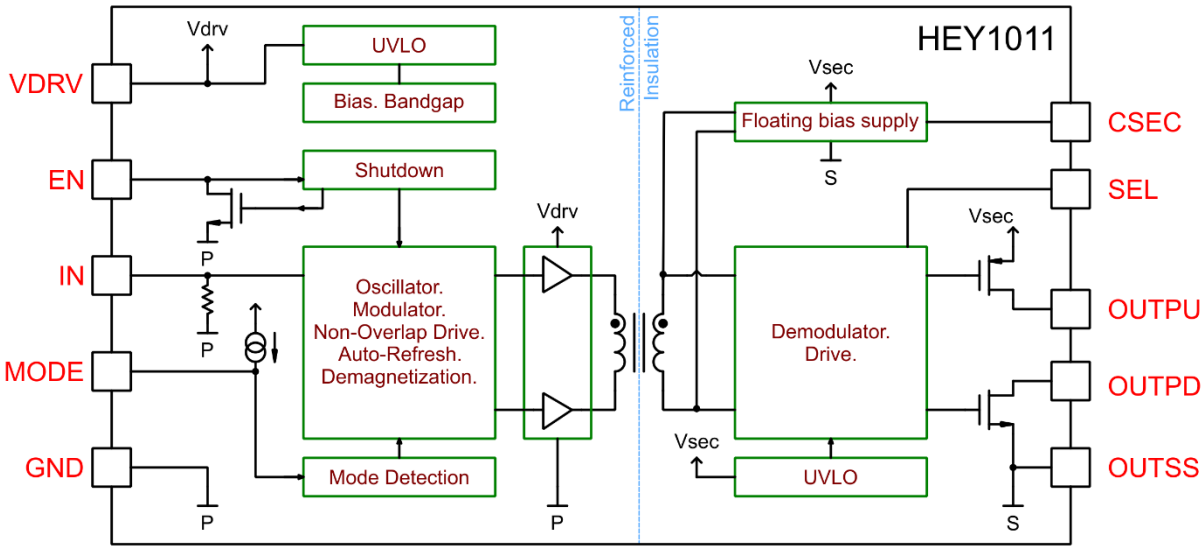


Figure 2: HEY1011 Block Diagram

Contents

TYPICAL APPLICATIONS

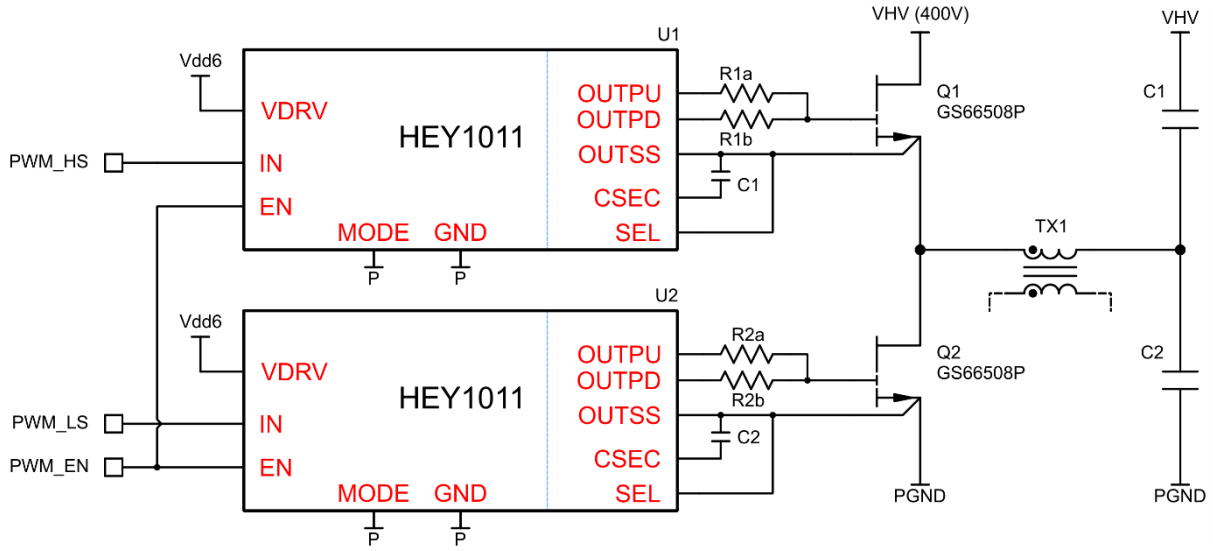


Figure 3: Half-Bridge with Hey1011 as high and low side drivers

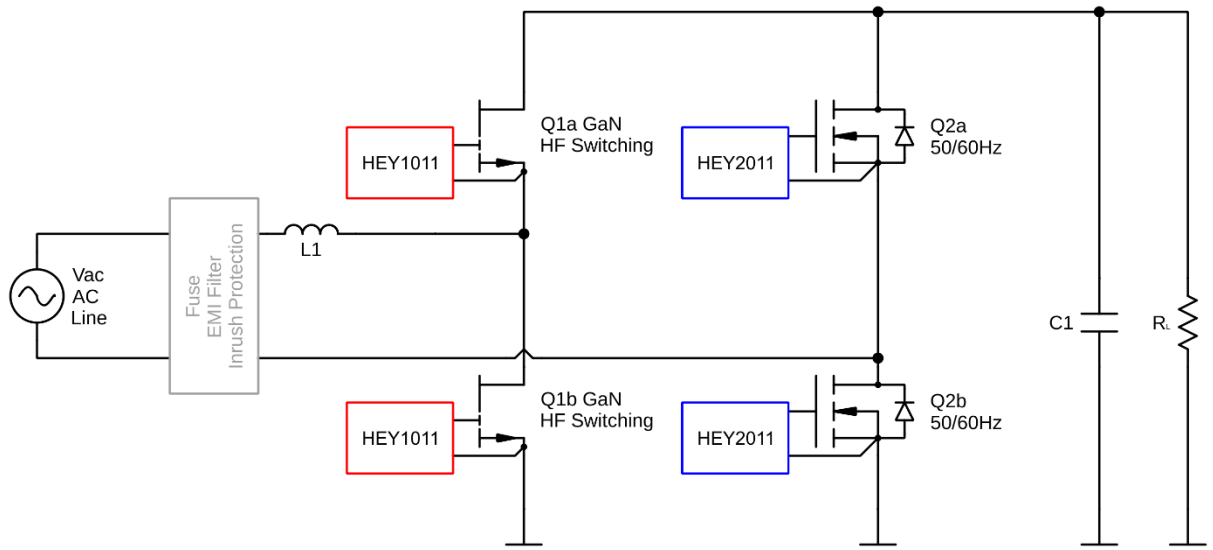


Figure 4: Totem pole PFC: Hey1011 and Hey1012 as high and low side drivers

Application Circuits (contd.)

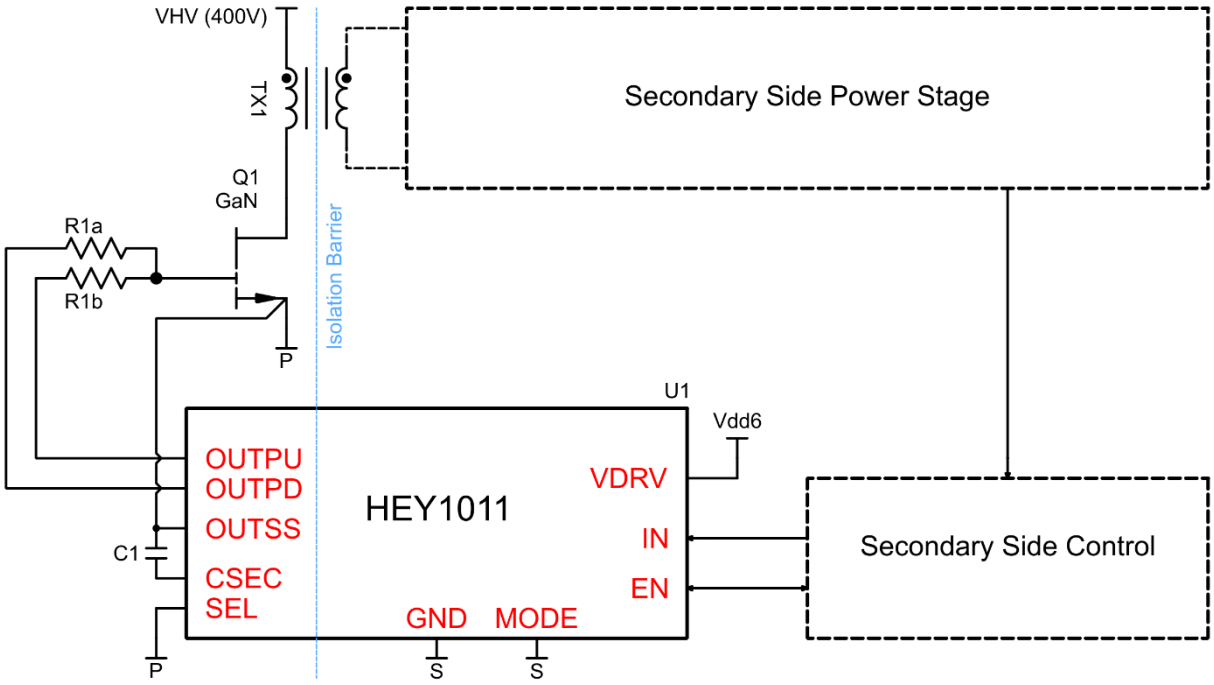


Figure 5: Secondary control to primary drive - Hey1011 single driver

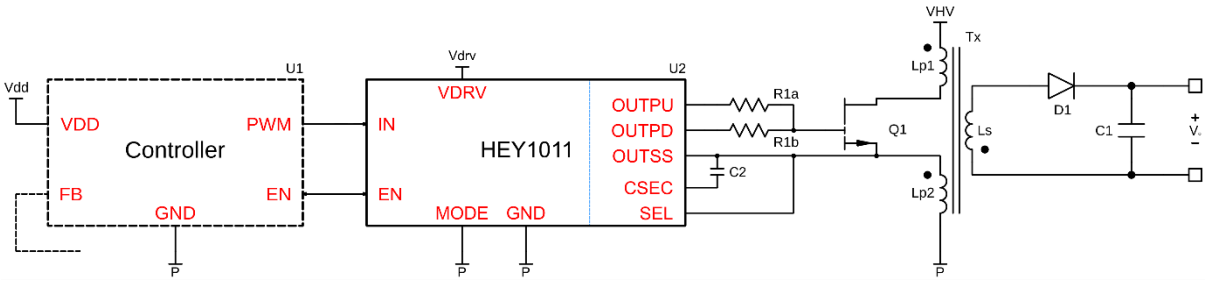


Figure 6: Centre switched Flyback – Hey1011 driving centre tapped switch (symmetrical bipolar voltage swings)

Application Circuits (contd.)

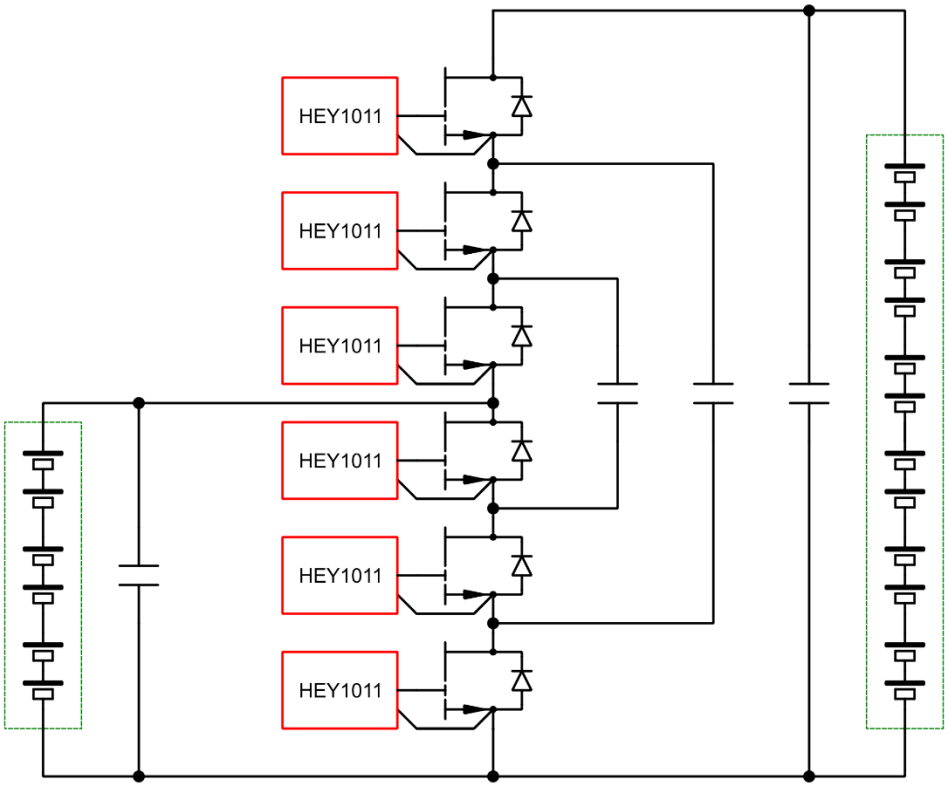


Figure 7: Multi-Level Converter – stacked low voltage switches results in higher efficiency. Hey1011 makes this drive easy.

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Function
1	N/C	Reserved
2	MODE	Sets one of the 16 modes of operation. External resistor referenced to GND. See MODE table.
3	EN	Bidirectional enable pin
4	IN	PWM input
5	VDRV	Ground referenced bias voltage supply. This bias voltage directly sets the output gate drive amplitude.
6	GND	Ground pin
7	SEL	Select pin. Connected either to OUTSS or CSEC pin.
8	CSEC	External capacitor referenced to OUTSS.
9	OUTSS	Floating output reference pin
10	OUTSS	Floating output reference pin
11	OUTPD	Floating output pull-down pin
12	OUTPU	Floating output pull-up pin

Table 1: HEY1011 Pin Descriptions

SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating Conditions						
VDRV	Drive supply voltage		GND - 0.5V		17	V
IN	Input data		GND - 0.5V		17	V
EN	Enable		GND - 0.5V		17	V
MODE	Mode setting		GND - 0.5V		3.6	V
OUTPU	Output pull up		OUTSS - 0.5V		17	V
OUTPD	Output pull down		OUTSS - 0.5V		17	V
CSEC	Floating supply		OUTSS - 0.5V		17	V
Tj	Junction Temperature		-40		150	°C

Table 2: Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ESD Ratings

		Value	Unit
ESD	Human body model (HBM)	2	kV
	Charge Device Model (CDM)	500	V

Table 3: ESD Ratings

Recommended Operating Conditions

-40°C <T_J< 125°C, 5.5V < V_{DRV} < 15V. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating Conditions						
VDRV	Drive supply voltage		5.5		15	V
Input Pins						
IN	Input Data		GND		V_{DRV}	V
EN	Enable Active High		GND		V_{DRV}	V
MODE	Mode setting pin		GND		3.3	V
Output Pins						
OUTPU	Output pull-up		0		15	V
OUTPD	Output pull-down		0		15	V
CSEC	Floating supply referenced to OUTSS		0		15	V
T_J	Junction Temperature		-40		125	°C

Table 4: Recommended Operating Conditions

Thermal Information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	tbd	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	tbd	°C/W

Table 5: Thermal Information

Electrical Characteristics

-40°C <T_J< 125°C, 5.5V < V_{DRV} < 15V. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Currents						
$I_{S\ DRV}$	V_{DRV} static current	IN=0, MODE=0, VDRV=7V		1000		µA
$I_{D\ DRV}$	V_{DRV} switching current	F_S = 100 kHz C_{LOAD} = 1nF (see plot), VDRV=7V		3		mA
Input Pins						
IN	Input Data	Logic low			1.0	V
		Logic High	2.0			
	Hysteresis		300			mV
EN	Enable Active High	Logic low			1.0	V
		Logic High	2.0			
	Hysteresis		400			mV
MODE	Mode Setting Pin		GND		3.6	V
R_{IN}	IN pin input pull down resistance on chip	Always present		300		kΩ
Output Pins						
R_{PU}	OUTPU pull up resistance			2.8		Ω
R_{PD}	OUTPD pull down resistance			0.8		Ω
I_{SOURCE}	High level source current	VSEC=10V, RPU=0Ω, C_{LOAD}=10nF, Note 3		2		A
I_{SINK}	Low level sink current	VSEC=10V, RPU=0Ω, C_{LOAD}=10nF, Note 3		4		A
Under Voltage Lock Out						
V_{UV}	V_{DRV} Threshold (voltage falling)	Note 1 Note 2	3.9 9.5	4.15 10.0	4.4 10.5	V
V_{UVH}	V_{DRV} Threshold Hysteresis	For 4.15V threshold For 10V threshold		0.3 0.7		V

Table 6: HEY1011 Electrical Characteristics

1. When Vdrv falls below the UVLO threshold the driver output is driven and held low.
2. The UVLO trip point is programmable using the MODE pin. See Table 9: HEY1011 Operating Modes.
3. See test circuit in Test Circuit section of datasheet.

CSEC Capacitor

-40°C <T_J< 125°C, 4.5V < V_{DRV} < 15V. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Capacitor CSEC						
C_{SEC}	External capacitance connected between CSEC and OUTSS pins	External switch C_{ISS} = 1nF	5 Note1	27	100 Note 2	nF

Table 7: Choosing CSEC capacitor value

1. Smaller CSEC values than the recommended typical value can be used but hold-up time on OUTPU and OUTPD will be reduced.
2. Larger CSEC values will mean longer start up times.

Switching Characteristics

-40°C <T_J< 125°C, 5.5V < V_{DRV} < 15V. Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Propagation Times						
T_{PHL}	Propagation delay, high to low (IN to TXPP,TXPN)	Resistive load of 1k between TXPP and TXPN		35		ns
T_{PLH}	Propagation delay, low to high (IN to TXPP,TXPN)	Resistive load of 1k between TXPP and TXPN		35		ns
T_{PM}	Propagation matching (IN to TXPP,TXPN)	Part to part		10		ns
Rise and Fall times						
t_r	Rise time	C_{LOAD} = 1nF R_{EXT} = 100mΩ 20-80%		8		ns
t_f	Fall time	C_{LOAD} = 1nF R_{EXT} = 100mΩ 20-80%		6		ns
t_{pw}	Minimum input pulse width that makes output change			50		ns
Start up time						
T_{START}	Wait time before first IN edge is delivered after V_{DRV} is within specification	100k <= RMODE <= open cct 10k <= RMODE <= 66.5k Short cct <= RMODE <= 6.65k			150 250 350	µs

Table 8: HEY1011 Switching Characteristics

MODES OF OPERATION

MODE	R_{MODE} (kΩ)	T_{REF_ON} (µs)	T_{REF_OFF} (µs)	$T_{PW\ ON,OFF}$ (ns)	UVLO (V)
0	Short circuit	4	8	96	4.15
1	1	6	12	96	4.15
2	1.6	16	32	96	4.15
3	2.7	4	8	96	10
4	4.3	6	12	96	10
5	6.65	16	32	96	10
6	10	4	8	144	4.15
7	16	6	12	144	4.15
8	27	16	32	144	4.15
9	43	4	8	144	10
10	66.5	6	12	144	10
11	100	16	32	144	10
12	160	6	12	128	4.15
13	270	6	12	112	4.15
14	430	4	8	96	4.15
15	Open Circuit	No Refresh	No Refresh	80	4.15

Table 9: HEY1011 Operating Modes

Refresh On

This is automatic on-chip refresh of a very 'long' ON pulse. It is timer based with an on-chip 10MHz oscillator which automatically refreshes the ON and OFF pulses. This is to account for leakage current into FET gates.

Enable/Disable bidirectional

When the enable pin is externally driven low this forces the driver into a low power mode. The output is pulled low in this mode. When the enable pin is driven high this forces the driver into normal operating mode. In the event of an internal fault condition, such as UVLO, this pin is actively pulled low by the driver. This information can be used by the controller, for example, as required. It is typically wired AND with the controller Enable pin as shown in Figure 8 below.

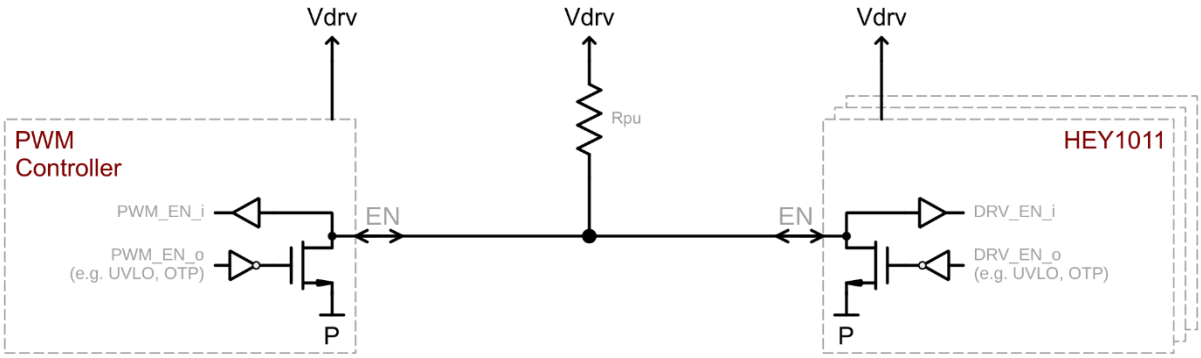


Figure 8: Example 'Wired AND' connection between driver and controller

TEST CIRCUITS

Test circuit for measuring Isink and Isrc is shown below. (To be added).

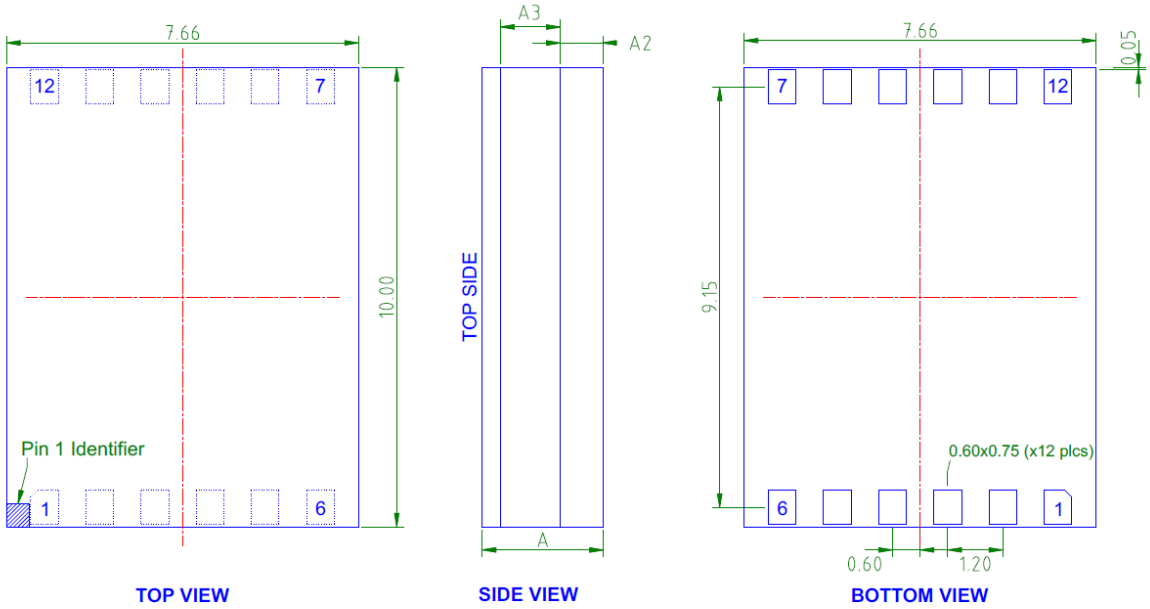
SEL PIN

Table 10 gives guidance for connecting SEL pin. The SEL pin should be tied to either OUTSS or CSEC depending on the MODE of operation chosen by the user.

MODE	SEL
0,1,2,3,4,5,14,15	OUTSS
6,7,8,9,10,11,12,13	CSEC

Table 10: HEY1011 Operating Modes

PACKAGE OUTLINE



Dimensional Ref.			
Ref	Min	Nom	Max
A	2.54	2.64	2.74
A2	0.89	0.94	0.99
A3	1.3 Basic		

Figure 9: HEY1011 Package Outline

RECOMMENDED PCB FOOTPRINT

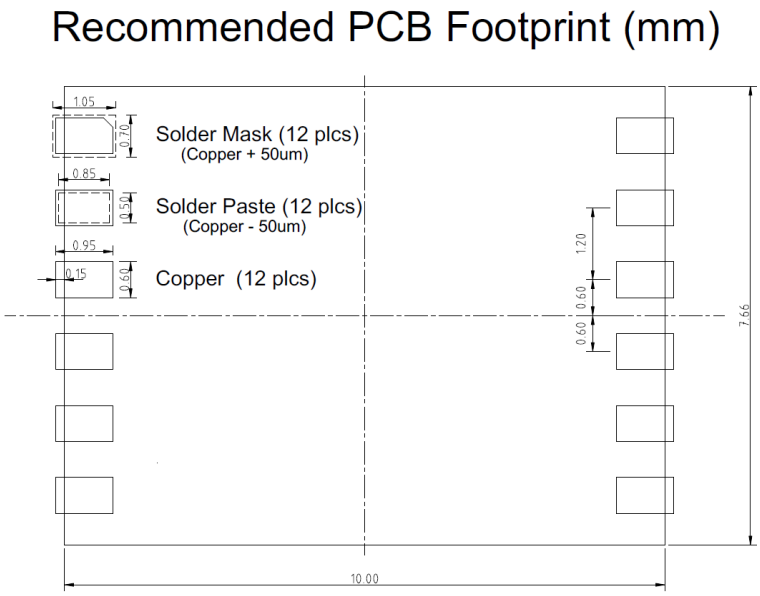


Figure 10: Recommended PCB footprint

REGULATORY INFORMATION (PENDING)

Safety Certification Standards

- UL1577 Component safety (optical and digital isolators)
- VDE0884-10 Component safety (digital isolators)

Specification Parameter	Target Specification	Specification detail and comments
V_{ISO}	5700 V_{RMS}	Withstand isolation voltage per UL 1577
V_{IOTM}	8000 V_{PK}	Maximum transient isolation voltage per VDEE0884-10
V_{IORM}	630 V_{PK}	Maximum working isolation voltage
C_{IO}	1pF	Barrier capacitance, two terminal device connection
R_{IO}	$>10^{12}\Omega$	Isolation resistance, two terminal device
DTI	>100µm	Distance through isolation (expandable)
Creepage	>8mm	External package creepage
Clearance	>8mm	External package clearance
Specification Parameter	Target Specification	Specification detail and comments

Table 11: Target Regulatory Specifications

ORDERING INFORMATION

Driver	Switch	#channels	Output	Isolation	package
HEY1011-NL12	GaN driver	1	Unipolar	Non-isolated	LGA 12 pin
HEY1011-AL12	GaN driver	1	Unipolar	Isolated	LGA 12 pin

REVISION HISTORY

Revision	Description	Date
1.00	Revision released	29/11/2018
1.01	Deleted pulse width column from table 8.	21/12/2018
1.02	Updated package to 12pin and associated drawings	18/01/2019
1.03	Updated: features, description fig1, general layout	22/01/2019
1.04	Updated: package drawing and PCB footprint	06/02/2019
1.05	Updated electrical specifications	17/05/2019
1.10	Updated electrical specifications	26/06/2019
1.11	Added Ordering Information, added SEL pin detail	01/08/2019

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