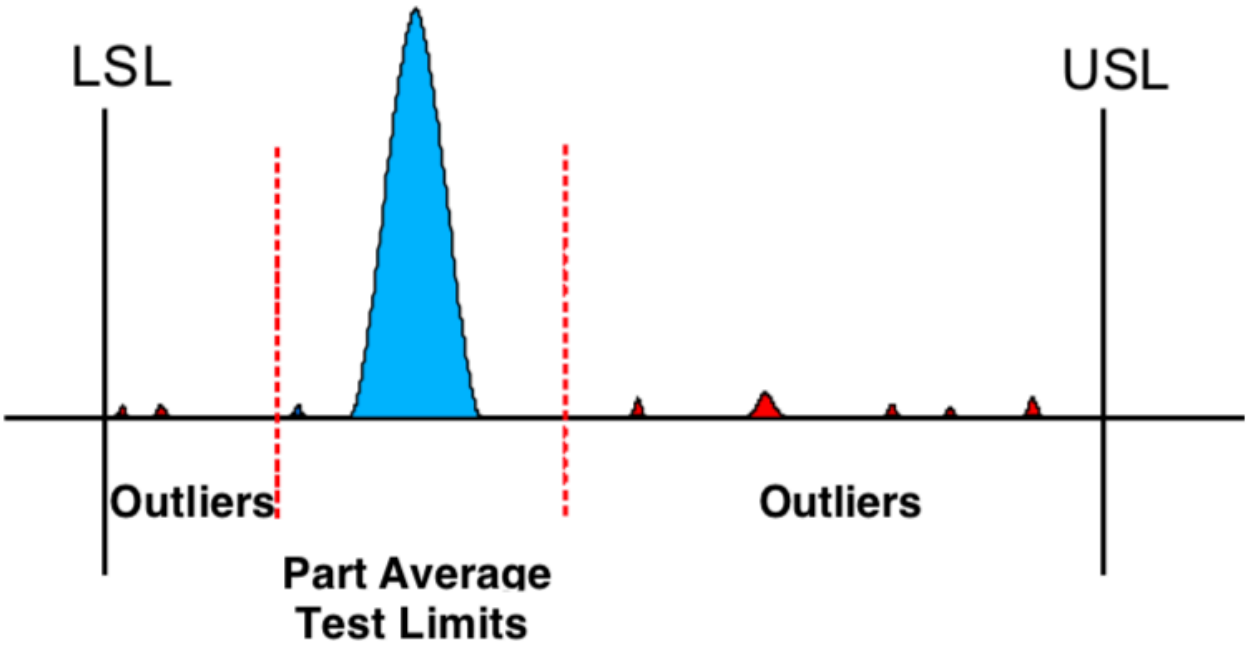
Part Average Testing (PAT)



What is Part Average Testing (PAT)?

With semiconductor manufacturers producing huge amounts of data, it can be hard to guarantee quality and reliability, even with internal tools.

Many companies outsource Part Average Testing (PAT) to a bespoke yield management provider. Provided they meet the standards set out by AEC, the tool will be invaluable in guaranteeing quality and reliability for your customers.

- Part Average Testing (PAT) screens each die to give typical limits across various parameters. Any die outside of the statistically determined norm is considered an “outlier”.
- The goal of PAT is to remove “outliers”, that is, otherwise good parts that exhibit characteristics that are vastly different from the norm. It

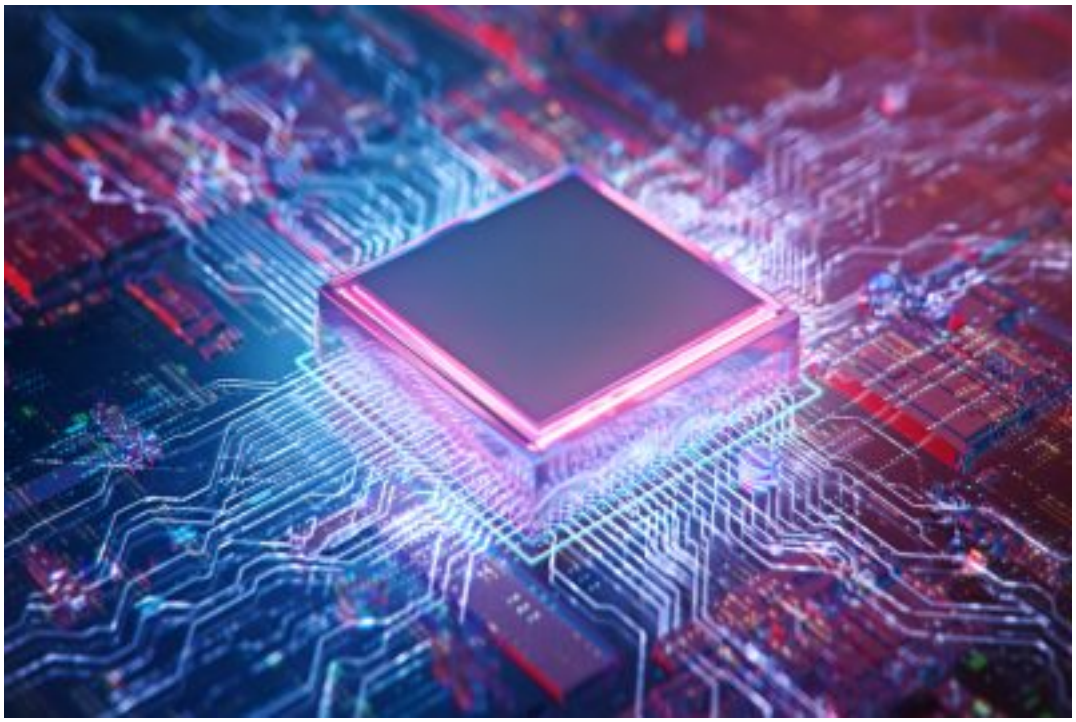
uses a recipe based on statistical analysis to find and fail these parts (outliers).

- In PAT, a wafer undergoes an additional test, after all standard tests are complete. Then, using a combination of hardware and PAT algorithms (recipe), the outliers or faulty dies that reside outside standard limits are detected. The outliers are then failed and removed.
- The AEC designed the statistical screening technique to improve the reliability and quality of automotive products. PAT is the standard for the automotive industry as outlined by AEC
- PAT is one way to apply Outlier Detection. Others include Out of family (OOF), Good Die Bad Neighbourhood (GDBN) Statistical Bin Limits (SBL) and Statistical Yield Limits (SYL).

Part Average Testing (PAT) allows you to find each die with parametric characteristics falling outside of a statistically calculated pass-fail limit. In the past, there was a certain tolerance for defects in semiconductors. However, these days the automotive industry has a zero-tolerance policy

By removing defective chips at manufacture, you increase the quality of your yield. This means less chance of customer returns. While it may affect your yield slightly during manufacture, it improves quality and reliability, and in turn, the overall reputation of your company.

This is why we're seeing more and more industries outside of the automotive sphere adopting outlier detection. Equally quality and reliability are becoming key criteria for everyone in the industry, not just manufacturers.



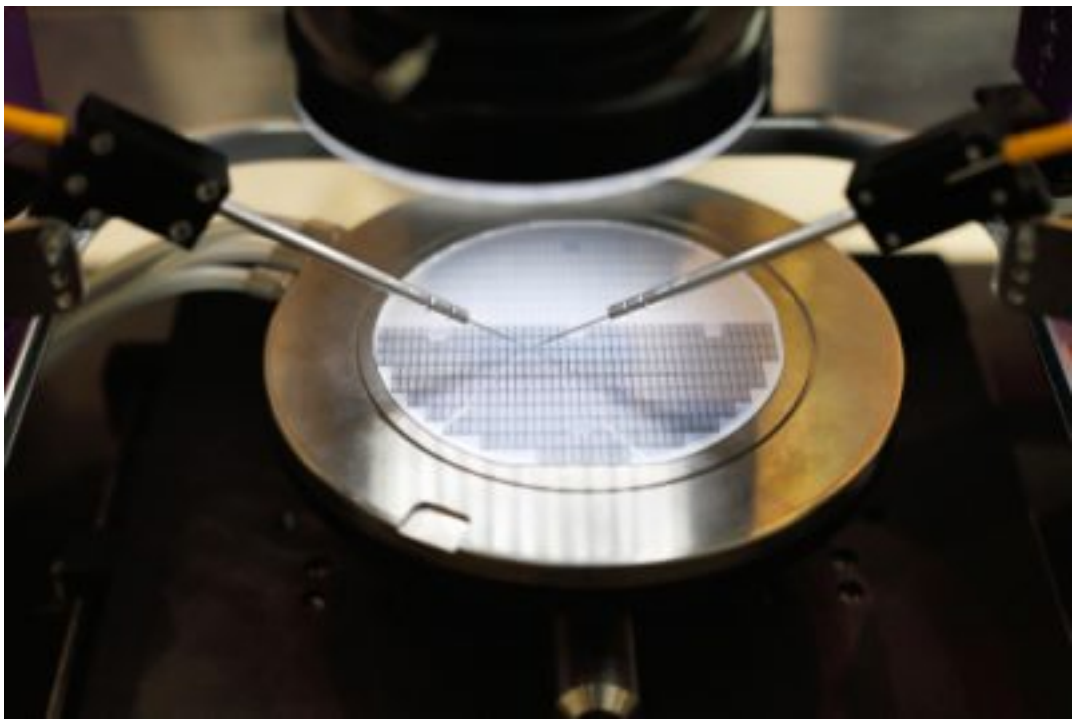
What are the benefits of yieldHUB's Part Average Test (PAT) Solution?

yieldHUB's Part Average Test (PAT) module is a stand-alone tool that is part of our Outlier Detection suite. The tool is fully compliant with AEC guidelines. It manages the entire outlier removal process from initial wafer lot characterization to final-test yield monitoring.

It is an existing service we offer. We're currently upgrading it to allow for scale, speed and added security.

FEATURES AND BENEFITS:

- The tool supports PAT, GDBN, Lots on Hold other outlier detection techniques.
- By using Our Part Average Testing tool, you will see a huge increase in the quality and reliability of semiconductors and ICs. Therefore the end product is less likely to stop working before it's predicted life-cycle.
- With more reliable products, you decrease customer returns and increase your reputation and repeatability.
- It enables fast communication across the team, through the tool itself
- The tool gives you an overall view of what's happening on the manufacturing floor.
- You can generate sophisticated reports at the touch of a button
- You can share reports with the team no matter where they are based. You can even give customers access to the data if required.
- yieldHUB's Part Average Test (PAT) solution lets you avoid program updates or updates to tester software.
- It is entirely cloud-based. No need to download anything to your computer. Each time you login, you're looking at the most up to date information possible.



What is the value of PAT?

“The intent of PAT is to increase the quality and reliability of AEC-Q100 and AWS-Q101 parts by removing abnormal parts as early in the manufacturing process as possible (preferably at wafer test). This should minimize costs related to customer support and failure analysis, and provide early feedback to prevent the occurrence of quality accidents.” **AEC**

More and more, we are seeing a need for improved quality, reliability and transparency across the industry. There used to be some-tolerance for defects in the semiconductor industry. But we’re seeing a zero tolerance approach in the automotive industry and in many other industries too.

For example, if a consumer buys an expensive smartphone and it stops working sooner than expected, they are more likely to lose trust and switch brands permanently. By investing in Outlier Detection and PAT, you increase

quality and reliability. Thereby maintaining your reputation and trust with your customers and their customers.

With so many companies investing in PAT and Outlier Detection, if you choose to ignore it you might get lost in the mix. If your customers or prospective customers are evaluating suppliers, they are more likely to choose a vendor who can guarantee quality, than one who can't. You should invest in PAT to win new business and avoid losing existing business.

Who should use Part Average Testing (PAT)?

Part Average Testing (PAT)is the required standard for the automotive industry. Companies supplying semiconductors/ICs to the automotive industry should provide PAT, as standard.

Additionally, semiconductors aiming for high quality and reliability invest in PAT or another form of Outlier Detection. With technology moving at such a fast pace, quality is everyone's responsibility.

How is the PAT algorithm calculated?

According to the AEC "Outlying data is considered to be data that is more than 6 standard deviations from the mean of the main distribution."

The quality standard describes two approaches, Static PAT Limits and Dynamic PAT Limits. Both are included in yieldHUB. PAT is part of our Outlier Detection module.

Test limits may be set in either a static or dynamic manner.

Static Test Limits

“The static limits are established based on an available amount of test data and used without modification for some period of time.” AEC

In this case, historical data is reviewed in order to set new test limits which are intended to remove (by failing) devices which are outside of the normal distribution but would have passed by being inside the specification limits. The algorithm for calculating these is given in the standard. We developed a software module which calculates static PAT limits in a few moments. These limits can then be implemented on the test floor.

Dynamic Test Limits

“The dynamic test limits are based on the static limits, but are established for each lot (Or wafer in a lot) and continuously modified as each lot (or wafer) is tested.” AEC

Using Dynamic PAT Limits is preferable as the limits are calculated on the actual material being tested. This means that lot-to-lot variation is not an issue. There are two places in the supply chain that Dynamic PAT can be implemented, at Chip Probe and at Final Test.

Dynamic PAT at Chip Probe is very efficient and implementation is quicker and easier than at final test. yieldHUB's solution for Dynamic PAT at probe is standard and can be included as an additional tool with any of our products. yieldHUB is a trouble-free/low maintenance solution for implementing the AEC – Q001 requirements at probe. There are no program updates, separate DPAT limits for each site are set-up automatically and there is a full record of all limits applied. A report is provided per lot and each lot can be signed-off by engineering before the assembly maps are sent on.

New PAT Limits

New PAT limits (Both static and dynamic) must be established when wafer level design changes, die shrinks or process changes have been made Dynamic PAT Limits are preferred over Static PAT Limits because the reference population is the same as the parts being tested. Dynamic PAT can provide tighter limits without causing rejection of good parts because it does not have to consider the lot-to-lot variation that is part of Static PAT Limits" AEC

The dynamic PAT limits for each selected test must be calculated and stored in memory for use on subsequent tests. The original LSL and USL are unchanged and used to detect test failures according to the original test program pass/fail binning. Calculations to identify outliers in the baseline for the selected tests are performed. At probe test, the X-Y coordinates are

saved for processing at end of wafer. At package test, the baseline devices are binned to a “baseline” bin. If outliers are detected in the baseline these devices can then be identified for re-test.

After the baseline is reached, each selected test is checked against the dynamic PAT limits and binned accordingly in real-time for each device. Devices that fail the PAT limits drop into a unique “outlier” software or hardware bin, which identifies them as PAT outlier devices post-test.

Thank you for reading our information about Part Average Testing (PAT).

If you’d like more information, visit our site: www.yieldhub.com

Contact us at any stage for a demo or more information about yield management.