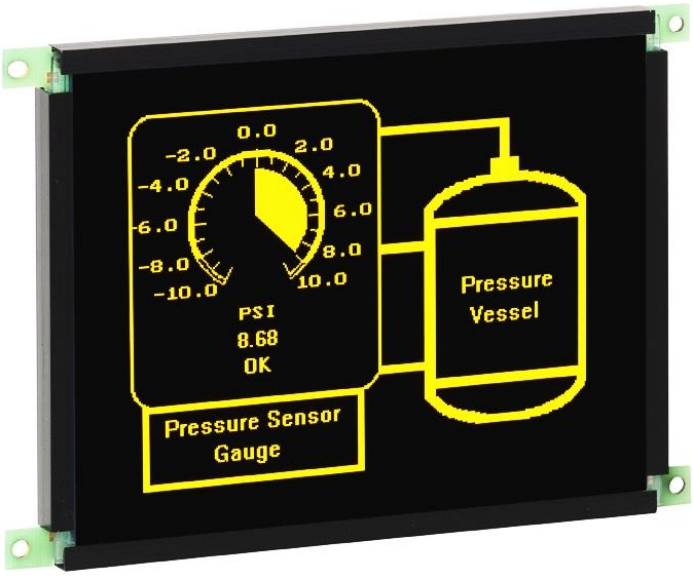


# EL320.240.36-HB SPI

## Operation Manual

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# 1 EL320.240.36-HB SPI Quarter-VGA display

The EL320.240.36-HB SPI thin film electroluminescent (TFEL) display is a high-performance alternative to quarter-VGA LCDs and the ideal solution in demanding applications where superior visual performance and environmental ruggedness are critical. The EL320.240.36-HB SPI utilizes Lumineq® Displays' proprietary Integral Contrast Enhancement (ICEBrite™) technology to achieve unparalleled image quality without the use of expensive filters. This small graphics display excels in a wide range of ambient lighting environments while effectively eliminating the blooming common to other high-bright displays.

The display consists of a TFEL glass panel and control electronics assembled into a space-saving, rugged package for easy mounting. The EL320.240.36-HB SPI is easily interfaced using the Serial Peripheral Interface (SPI) bus. Each of the 76,800 pixels is individually addressable to clearly display high information content graphics and text.

## 1.1 Features and benefits

- Excellent visual performance
  - High brightness and contrast
  - Wide viewing angle < 179°
- Rapid display response < 1 ms
- Frame buffer
- Space-efficient mechanical package
- Low EMI emissions
- Extremely rugged and durable
- Reliable, long operating life
- SPI interface

# 2 Installation and handling

Do not drop, bend, or flex the display. Do not allow objects to strike the surface of the display.

**CAUTION:** The display uses CMOS and power MOS-FET devices. These components are electrostatic-sensitive. Unpack, assemble, and examine this assembly in a static-controlled area only. When shipping the displays, use packing materials designed for protection of electrostatic-sensitive components.

## 2.1 Mounting TFEL displays

Properly mounted, TFEL displays can withstand high shock loads as well as severe vibration found in demanding applications. However, the glass panel used in a TFEL display will break if subjected to bending stresses, high impact, or excessive loads.

Avoid bending the display. Stresses are often introduced when a display is mounted into a product. Ideally, the mounting tabs of the display should be the only point of contact with the system. Use a spacer or boss for support; failure to do so will bend the display and cause the glass to break. The instrument enclosure or frame should not flex or distort in such a way that the bending loads might be transferred to the display during use. The EL320.240.36-HB SPI mounting tabs are designed for 3 mm screws. Mounting surfaces should be flat to within ±0.6 mm (±0.025"). Use all the mounting holes provided. Failure to do so will impair the shock and vibration resistance of the final installation.

**CAUTION:** To prevent injury in the event of a glass breakage, a protective overlay should be used on the viewer side of the display.

**WARNING:** These products generate voltages capable of causing personal injury (high voltage up to 235 $V_{AC}$). Do not touch the display electronics during operation.

## 2.2 Cable length

A maximum cable length of 0.6 m (24 in.) is recommended. Longer cables may cause data transfer problems between the data transmitted and the display input connector. Excessive cable lengths can pick up unwanted EMI.

## 2.3 Cleaning

As with any glass or coated surface, care should be taken to minimize scratching. Clean the display glass with mild, water-based detergents only. Apply the cleaner sparingly to a soft cloth, and then wipe the display. Disposable cleaning cloths are recommended to minimize the risk of inadvertently scratching the display with particles embedded in a re-used cloth. Particular care should be taken when cleaning displays with anti-glare and anti-reflective films.

## 2.4 Avoiding burn-in

As with other light-emitting displays, use a screensaver or image inversion to avoid causing burn-in on the display. Displaying fixed patterns on the screen can cause burn-in where luminance variations can be noticed.

# 3 Specifications

Performance characteristics are guaranteed when measured at 25 °C with rated input voltage unless otherwise specified.

## 3.1 Control basics

The TFEL panel is a matrix structure with column and row electrodes arranged in an X-Y formation. Light is emitted when an AC voltage of sufficient amplitude is applied at a row-column intersection. The display operation is based on the symmetric, line-at-a-time data addressing scheme.

## 3.2 Power

The supply voltages are shown in Table 1. All internal high voltages are generated from the display supply voltage ($V_H$). The logic supply voltage ($V_L$) should be present whenever video input signals or $V_H$ is applied. The minimum and maximum specifications in this manual should be met, without exception, to ensure the long-term reliability of the display. Beneq does not recommend operation of the display outside these specifications.

**Table 1. DC input voltage requirements**

| Parameter | Symbol | Min | Typ | Max | Absolute Max |
|---|---|---|---|---|---|
| Logic supply voltage | $V_L$ | 4.75 V | 5 V | 5.25 V | 6 V |
| Logic supply current at +5 V | $I_L$ | | | 0.10 A | |
| Display supply voltage | $V_H$ | 8 V | 12 V | 18 V | 19 V |
| Supply current at +12 V | $I_H$ | | 0.4A | 0.9 A | |
| Power consumption @ maximum frame rate | | | 5.5 W | 11 W | |
| Power consumption @ 120 Hz | | | 3.5 W | | |

**CAUTION:** Absolute maximum ratings are those values beyond which damage to the device may occur.

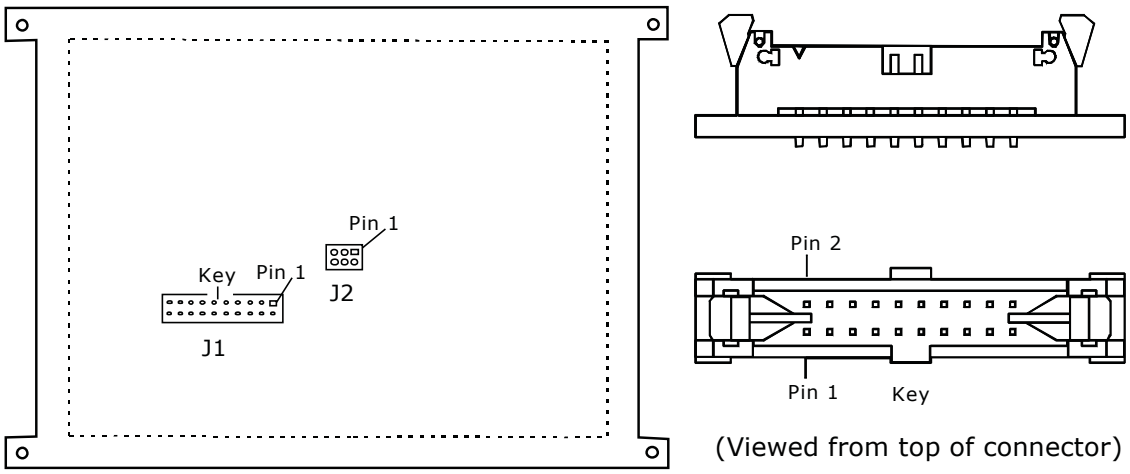
**Table 2. SPI input requirements**

| Description | Min | Max | Units | Notes |
|---|---|---|---|---|
| Absolute Input Voltage Range | -0.3 | 5.5 | V | $V_L$= 5.0 V |
| SPI Logic high voltage | 2.2 | 5.0 | V | All input thresholds are TTL |
| SPI Logic low voltage | 0 | 0.8 | V | |
| Input capacitance | – | 15 | pF | |

There is no overcurrent protection on either the $V_H$ or $V_L$ inputs to protect against catastrophic faults. Beneq recommends the use of a series fuse on the 12 volt supply ($V_H$). A general guideline is to rate the fuse at 1.8 to 2 times the display maximum current rating.

## 3.3 Connector

The display uses the Samtec EHT-110-01-S-D or equivalent locking connector. The mating connector is in the Samtec TCSD family of cable strips. The proper connector, user-specified cable length and connector configuration is supplied as a single unit. Consult your Samtec representative for the cable/connector options. Compatibility with non-Samtec equivalents should be verified before use.




(Viewed from back of display)

(Viewed from top of connector)

**Figure 1. Data/power connector**

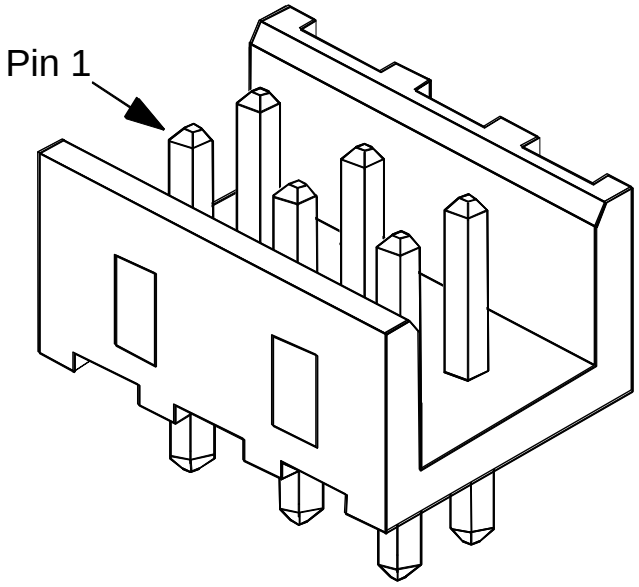
**Table 3. J1 Connector pinouts**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | $V_H$ | +12 VDC Power | 2 | $V_H$ | +12 VDC Power |
| 3 | Self-test | Self-test Input (1) | 4 | Reserved | Do not connect |
| 5 | $V_L$ | +5 VDC Power | 6 | GND | Ground |
| 7 | SS | Slave Select | 8 | GND | Ground |
| 9 | Reserved | Do not connect | 10 | GND | Ground |
| 11 | SCLK | Clock from master | 12 | GND | Ground |
| 13 | MOSI | Master Out Slave In | 14 | GND | Ground |
| 15 | Reserved | Do not connect | 16 | GND | Ground |
| 17 | Reserved | Do not connect | 18 | GND | Ground |
| 19 | Reserved | Do not connect | 20 | GND | Ground |

Note: 1) Connect pin 3 to ground for normal display operation.

### 3.3.1 Dimming connector J2

The J2 analog dimming connector is a Berg six-pin, dual in-line header, part number 98424-G52-06LF. The mating connector is the Berg 89947-106LF (IDC) or a combination of the Berg 77138-101LF (discrete crimp-to-wire) and the Berg 903111-006LF (housing). Refer to "Dimming" on page 9 for more information.




The pin assignments are:

| Pin | Symbol | Description |
|---|---|---|
| 1 | LUMA | Analog dimming |
| 2 | GND | Ground |
| 3 | Reserved | Reserved, do not connect |
| 4 | Reserved | Reserved, do not connect |
| 5 | GND | Ground |
| 6 | Reserved | Reserved, do not connect |

## 3.4 Interface information

Beneq EL320.240.36-HB SPI incorporates a common SPI interfaces. This interface is supported by a variety of off-the-shelf chip sets and embedded boards. Designers should select the chip set or embedded board that best suits their particular architecture.

### 3.4.1 Video input signals

The SPI is driven with the rising edge of SCLK. A falling edge on SS signal indicates the beginning of an access on the SPI, the rising edge of SS signal ends an access on SPI. An access must consist of exactly 16 bits for write operation.

The SPI interface Clock polarity (CPOL) and clock phase (CPHA) are 0.At CPOL=0 the base value of the clock is zero for CPHA=0 and data are captured on the clock's rising edge (low to high transition) and data is propagated on a falling edge (high to low clock transition).

The timing restrictions on SPI are defined in figure 2 and table 4:

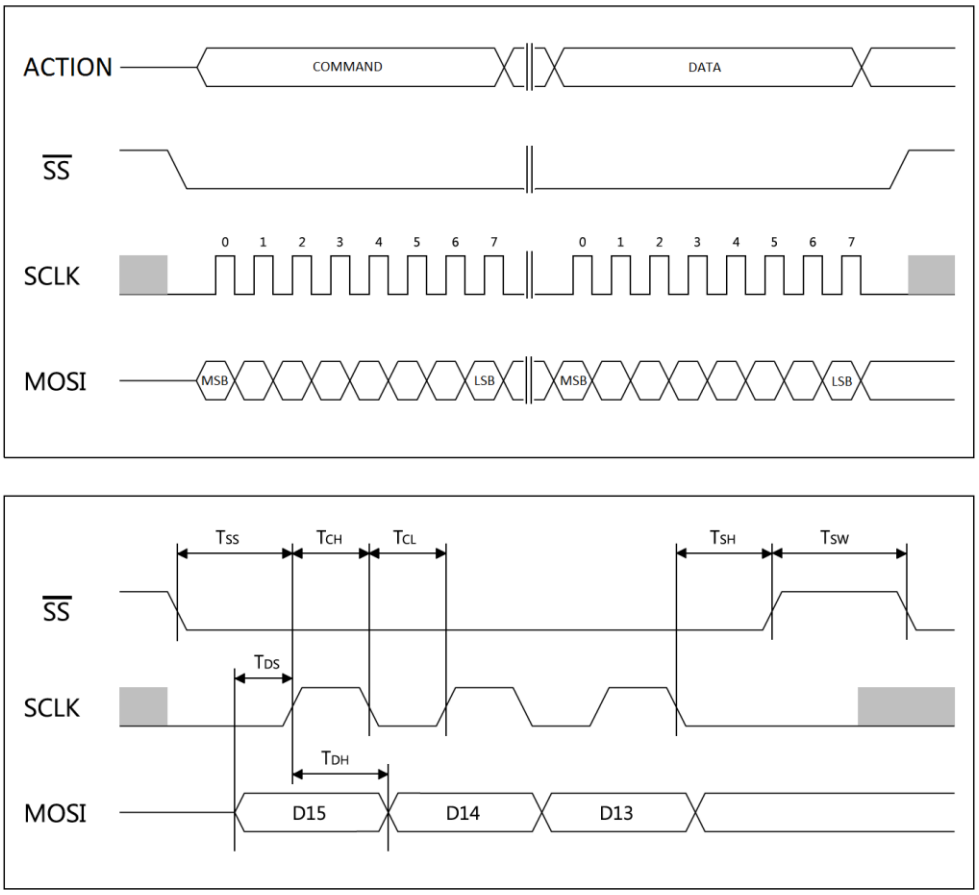



**Figure 2. Video input timing diagram**

**Table 4. Timing restrictions**

| Description | Symbol | Minimum value (ns) |
|---|---|---|
| SCLK high time | $T_{CH}$ | 100 |
| SCLK low time | $T_{CL}$ | 100 |
| SS -> SCLK setup time | $T_{SS}$ | 100 |
| SCLK -> SS hold time | $T_{SH}$ | 100 |
| SS disabled between cycles | $T_{SW}$ | 100 |
| Data setup time | $T_{DS}$ | 100 |
| Data hold time | $T_{DH}$ | 100 |

### 3.4.2 Initial power-up

On initial power-up, the display registers are reset to their default values and all pixels are blanked. At this time all registers must be programmed for normal operations.

## 3.5 SPI protocol

### 3.5.1 Commands

| **Command** | **Hex #** | **Binary** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Write complete display data | 01h | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Write display block (multiple rows) | 02h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Write one row | 03h | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Clear screen (full black) | 11h | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| All pixels ON (full yellow) | 12h | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Invert display image | 13h | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| Write 100 % luminance | 81h | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Write 75 % luminance | 82h | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Write 50 % luminance | 83h | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Write 30 % luminance | 84h | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

### 3.5.2 Write complete display data

| **Command** | **Data (1)** | **---** | **Data N (2)** |
|---|---|---|---|
| $80_h$ | 8 bits | 8 bits | 8 bits |

Notes: (1) First bits of first row
(2) Last bits of last row. N=( Number of rows/8) * Number of colums
(3) Pixels are going from left to right from top to bottom. A first pixel in a byte is the most significant one. See Figure 3. for reference

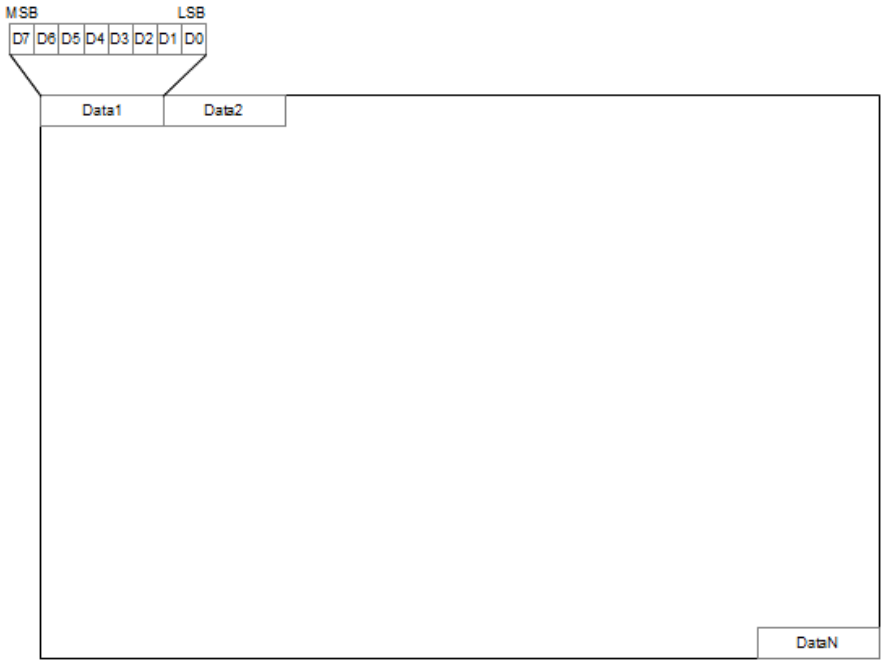



Figure 3. Display pixel locations on image data mapping.

### 3.5.3 Write display block (multiple rows)

| Command | First row number | Last row number | First bits of first row | ---- | Last bits of last row |
|---|---|---|---|---|---|
| $40_h$ | 8 bits | 8 bits | 8 bits | 8 bits | 8 bits |

### 3.5.4 Write one row

| Command | Row number | First bits of row | ---- | Last bits of row |
|---|---|---|---|---|
| $20_h$ | 8 bits | 8 bits | 8 bits | 8 bits |

### 3.5.5 Clear screen (full black)

| Command |
|---|
| $11_h$ |

### 3.5.6 All pixels ON (full yellow)

| Command |
|---|
| $12_h$ |

### 3.5.7 Invert display image

| Command |
|---|
| $13_h$ |

### 3.5.8 Write luminance

| Command | Relative Luminance |
|---|---|
| 81h | 100 % |
| 82h | 75 % |
| 83h | 50 % |
| 84h | 30 % |

## 3.6 Dimming

There are two standard methods for dimming the EL320.240.36-HB SPI display. Analog dimming using the J2 dimming connector described on page 7 of this manual allows for manual dimming from 100% to approximately 5% of the full brightness. To perform analog dimming, connect a 50 kΩ variable resistor between LUMA and GND.

Alternatively, the display can be dimmed by changing the display frame rate controller register value. See details 3.5 SPI protocol.

## 3.7 Self-test mode

The display incorporates a self-test mode composed of two patterns displayed at maximum frame rate for approximately 30 seconds each, and then repeated. The patterns are as follows: 50/50 Checkerboard and Full On. The self-test mode is entered by leaving pin 3 on J1 unconnected or pulled high. This pin has an internal pull-up. Connect pin 3 on J1 to ground for normal display operation.

## 3.8 Optical

**Table 4. Optical characteristics**

| | | |
|---|---|---|
| **Luminance** | | |
| $L_{on}$ (areal), min | 120 cd/m² | Screen center, maximum frame rate |
| $L_{on}$ (areal), typ | 150 cd/m² | Screen center, maximum frame rate |
| $L_{off}$ (areal), max | 0.3 cd/m² | 5 points: center plus four corners measured<br>1.0 ±0.25" from adjacent bezel edges, @ 120 Hz |
| **Non-uniformity** | | |
| All pixels fully lit | 35 % | Maximum difference two of five points, using the formula: BNU %=[1- (min_lum/max_lum)] x 100 % |
| **Luminance variation (temperature)** | | |
| Maximum | ±25 % | Across the operating temperature range |
| **Luminance variation (time)** | | |
| Maximum | < 20 % | 10,000 hours at 25 °C ambient |
| **Viewing angle** | | |
| Minimum | > 179° in all directions; no contrast or luminance change | |
| **Contrast ratio (typical)** | | |
| Typical | 90:1 | @ 500 lux ambient, maximum frame rate |
| | 8:1 | @ 10,000 lux ambient, maximum frame rate |

## 3.9 Environmental

**Table 5. Environmental characteristics**

| | |
|---|---|
| **Temperature** | |
| Operating | -40 °C to +85 °C |
| Operating Survival | -50 °C to +95 °C |
| Storage | -50 °C to +105 °C |
| **Humidity** | |
| Non-condensing, operating | 93% RH max at +40 °C, per IEC 60068-2-78 |
| Condensing, non-operating | 95% RH max at +55 °C, per IEC 60068-2-30 |
| **Altitude** | |
| Operating/non-operating | 0 to 18 km (58k ft), per IEC60068-2-13 |
| **Vibration** | |
| Random<br>Operating/non-operating | 0.02 $g^2$/Hz, ASD level, 5-500 Hz<br>per, IEC 60068-2-64 test Fh. |
| **Shock** | |
| Operating/non-operating | 100 g, 6 ms, half sine wave per<br>IEC 60068-2-27, test Ea. |

## 3.10 Reliability

The display MTBF is to be greater than 50,000 hours at 120 Hz with a 90 % confidence level at 25°C.

## 3.11 Safety and EMI performance

The display will not inhibit the end product from obtaining these certifications: IEC 950, IEC 601-1-1, UL2601, CSA 22.2 #601-M89, FCC Docket, Part 15, Subpart J, Class B; CISPR22, Class B; and VDE 871/VFG243 Class B.

## 3.12 Optional features

Conformal coating and anti-glare filters are available as an option.

## 3.13 Mechanical characteristics

**Table 6. Mechanical characteristics**

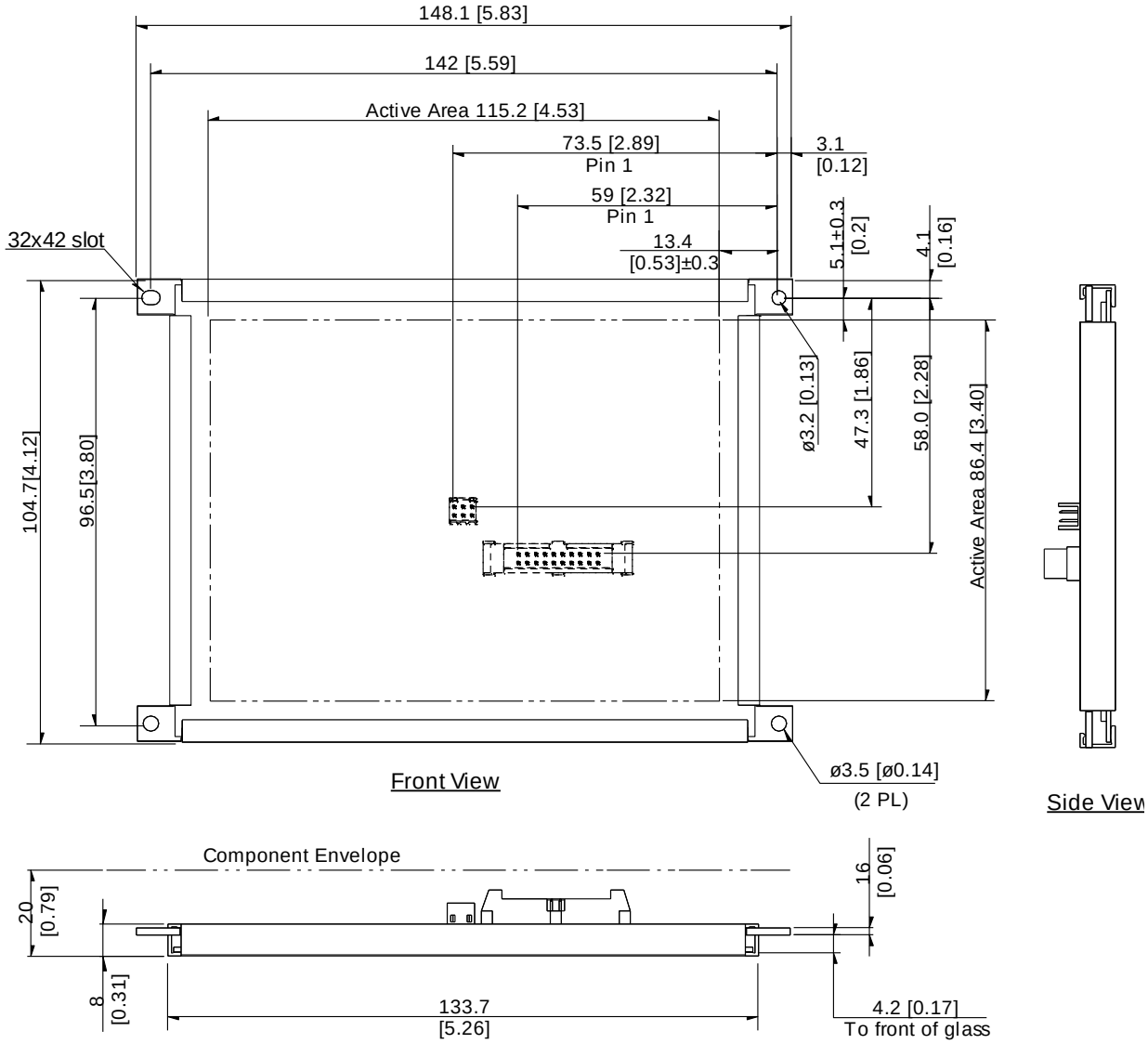
| | | |
|---|---|---|
| **Display external dimensions** | | |
| millimeters (inches) | width | 148.1 (5.83) |
| | height | 104.7 (4.12) |
| without locking connector | depth | 20 (0.8) |
| with locking connector | | |
| **Weight (typical)** | | 183 g (6.3 oz) |
| **Fill factor** | | 74 % |
| **Display active area** | | |
| millimeters (inches) | width | 115.1 (4.5) |
| | height | 86.3 (3.40) |
| **Pixel size** | | |
| | width | 0.31 (0.012) |
| | height | 0.31 (0.012) |
| **Pixel pitch** | | |
| millimeters (inches) | Width | 0.36 (0.014) |
| | Height | 0.36 (0.014) |

## 3.14 Component envelope

The component envelope shown in 4 illustrates the distance the components extend behind the display. Tall components do not necessarily fill this area. Beneq reserves the right to relocate components within the constraints of the component envelope without prior customer notification. For this reason, Beneq advises users to design enclosure components to be outside the component envelope.

Device designers will need to consider their specific system requirements to determine the spacing necessary to maintain the specified ambient temperature.

Air flow and surrounding component materials will affect the depth of the air gap.




Dimensions are in millimeters; inches in brackets.
Tolerances unless specified
.x ±0.50 [0.02]
.xx ±0.25 [0.01]

**Figure 4. Display dimensions**

# 4 Description of warranty

Seller warrants that the Goods will conform to published specifications and be free from defects in material during warranty time from delivery. To the extent that goods incorporate third-party-owned software, seller shall pass on seller's licensor's warranty to buyer subject to the terms and conditions of seller's license.

Warranty repairs shall be warranted for the remainder of the original warranty period. Buyer shall report defect claims in writing to seller immediately upon discovery, and in any event, within the warranty period. Buyer must return goods to seller within 30 days of seller's receipt of a warranty claim notice and only after receiving seller's return goods authorization. Seller shall, at its sole option, repair or replace the goods.

If goods were repaired, altered or modified by persons other than seller, this warranty is void. Conditions resulting from normal wear and tear and buyer's failure to properly store, install, operate, handle or maintain the goods are not within this warranty. Repair or replacement of goods is seller's sole obligation and buyer's exclusive remedy for all claims of defects. If that remedy is adjudicated insufficient, Seller shall refund buyer's paid price for the goods and have no other liability to buyer.

All warranty repairs must be performed at seller's authorized service center using parts approved by seller. Buyer shall pay costs of sending goods to seller on a warranty claim and seller shall pay costs of returning goods to buyer. The turnaround time on repairs will usually be 30 working days or less. Seller accepts no added liability for additional days for repair or replacement.

If seller offers technical support relating to the goods, such support shall neither modify the warranty nor create an obligation of seller. Buyer is not relying on seller's skill or judgment to select goods for buyer's purposes. Seller's software, if included with goods, is sold as is, and this warranty is inapplicable to such software.

SELLER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

# 5 Ordering information

| Product | Part Number | Description |
|---|---|---|
| EL320.240.36-HB SPI | 996-0292-12LF | 5.6" (142 mm) diagonal, quarter VGA (QVGA) high-bright display, -40°C to +85 °C operating temperature, SPI interface |
| EL320.240.36-HB SPI CC | 996-0292-14LF | Same as EL320.240.36-HB SPI, but with conformal coating added to the circuit board |

Design and specifications are subject to change without notice.

Beneq continues to provide optional, and in many cases custom, features to address the specific customer requirements. Consult Beneq Sales for pricing, lead time and minimum quantity requirements.

# 6 Support and service

Beneq is a Finnish company based in Espoo, Finland, with a world-wide sales distribution network. Full application engineering support and service are available to make the integration of Lumineq displays as simple and quick as possible for our customers.

**RMA Procedure:** For a Returned Material Authorization number, please contact Beneq Oy by email (rma.lumineq@beneq.com) with the model number(s), serial number(s) and brief description of the problem. When returning goods for repair, please include a brief description of the problem, and mark the outside of the shipping container with the RMA number.

# 7 RoHS II

Beneq Oy is committed to continuous improvement. As part of this process we are fully in support of EU directive 2011/65/EU, the Restriction of Hazardous Substances, commonly known as RoHS II or RoHS Recast, which, compared to RoHS, keeps the restrictions on the original six hazardous substances, including lead (Pb) in electronic equipment. It also expands these restrictions to previously exempted categories including medical devices and monitoring and control instruments.