ELT160.60.100-07NC
Transparent Matrix Display

Operations Manual

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1 ELT160.60.100-07NC display

The ELT160.60.100-07NC from Lumineq® Displays is a transparent thin film electroluminescent TASEL® display without cover glass (=NC) for transparent TFEL technology with a substrate thickness of 0.7 mm. The display is primarily for in-glass laminated applications.

The display consists of a TFEL glass panel and control electronics that are connected to TFEL glass with a flexible flat cable (aka. flexible printed circuit, FPC).

The display has 160 x 60 = 9,600 pixels. Each of the 9,600 pixels is individually addressable to clearly display high information content graphics and text. The display is equivalent to a 7 (rows) x 26 (columns) character display in text mode (assuming 5 (pixel width) x 7 (pixel height) characters with one pixel separation in row and col direction).

Product name:	ELT160.60.100-07NC
Product number:	EL00045100
Document number:	ED001129C

1.1 Features and benefits

- Wide viewing angle, ~180 deg from the two viewing sides
- Very good photopic transparency
- Rapid display response < 1 ms
- SPI ("serial peripheral interface") interface, protocol FPGA programmable at display controller electronics
- Dimming capability (for the whole display area, not for separate pixels)
- Dark Row Skipping feature enabling increased brightness
- MTBF: when properly laminated, 50,000 h based on historical references

1.2 Parts included

The display consists of a

- Transparent TFEL (TASEL) glass panel
- Control electronics connected to TFEL glass (PCB)
- Flexible flat cable(s) (flexible printed circuit, FPC) connecting the control electronics and display panel (connector at control electronics end, fixed to the glass panel end). There are four FPCs in the display, two for segment electrodes and two for row electrodes.

1.3 Note

All TBD items are to be specified later by Beneq Oy.

2 Installation and handling

Do not drop, bend, or flex the display. Do not allow objects to touch the surface of the display without cover glass. Additional handling instructions will be provided separately.

CAUTION: The display uses CMOS and power MOS-FET devices. These components are electrostatic sensitive. Unpack, assemble, and examine this assembly in an ESD controlled area only.

2.1 Mounting

Properly laminated into a larger glass and properly mounted, TFEL displays can withstand high shock loads as well as severe vibration found in demanding applications. However the glass panel used in a TFEL display will break if subjected to bending stresses, high impact, or excessive loads.

Avoid bending the display. Stresses are often introduced when a display is mounted into a product; improper mounting could cause the glass to break.

Avoid causing stress to the display flex cable connection. Extensive stress to the cable connection could damage the cable connection.

Avoid bending sharp edges to the display flex cable as this could break the FPC internally.

The display comes with no cover glass. This makes the top side (electrode side) of the glass very sensitive to any touch. Touch the display only by the sides and avoid any sharp contact to the top surface.

WARNING: These products generate voltages capable of causing personal injury (high voltage up to 235 V_{ac}). Do not touch the display electronics during operation.

2.2 Cleaning

As the display is delivered with no encapsulation (cover glass) and delivered clean, there should be no need for cleaning the display panel. Virtually any abrasive or wet wiping of the display area from the electrode side will damage the display.

Dust particles may be blown away with ionized dry air.

Installation in clean room environment is recommended.

2.3 Interface cable length

A maximum cable length of 600mm (24 in.) is recommended between the customer's electronics and display electronics. Longer cables may cause data transfer problems between the data transmitted and the display input connector. Excessive cable lengths can pick up unwanted EMI.

2.4 Glass Handling

For important safety information and tips in handling of the display glass, please consult www.beneq.com/glasshandling.

2.5 Avoiding latent image

As with all light emitting displays, displaying fixed patterns on the screen for extended periods of time can cause so-called latent image (aka. burn-in), where permanent luminance variations can be noticed in the display. If possible, turn the screen off from time to time, or use a screen saver or image inversion to avoid this.

3 Specifications

Performance characteristics are guaranteed when measured at 25 °C with rated input voltage unless otherwise specified.

3.1 Control basics

The TFEL panel is a matrix structure with column and row electrodes arranged in an X-Y formation. Light is emitted when an AC voltage of sufficient amplitude is applied at a row-column intersection. The display operation is based on the symmetric, line(row)-at-a-time data addressing scheme.

The display has no grayscale capability, but does have a dimming (overall brightness control) capability.

3.2 Power

The power consumption of the display (and display electronics) will depend on the overall brightness target. Estimated typical power consumption of the display device is 20 W.

The supply voltages are shown in Table 1. All internal high voltages are generated from the display supply voltage (V_H). The minimum and maximum specifications in this manual should be met, without exception, to ensure the long-term reliability of the display. Beneq does not recommend operation of the display outside these specifications.

Any combination or sequencing in the application or removal of V_L, V_H, or video signals will not result in abnormal display operation or display catastrophic failure.

Table 1. DC input voltage requirements

Description	Symbol	Min	Typ.	Max	Absolute Max	Units
Input voltage (nom=12.0 V)	V_H	8		18	19	V_{DC}
12 V input current (V_H =12.0 V)	I_H max			2		A_{DC}
Power consumption 12 V @ max. frame rate			20		36	W

CAUTION: Absolute maximum ratings are those values beyond which damage to the device may occur.

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Table 2. SPI input requirements

Description	Symbol	Min	Max	Units
SPI logic high voltage	VI_H	2	3.6	V
SPI logic low voltage	VI_L	0	0.8	V
SPI logic input current	II_L	-10	+10	µA

Data signal inputs are equipped with series resistors.

3.3 Connectors

3.3.1 Standard data and power connector

The EL160.60.100-07NC uses the 10 pin connector of type SAMTEC EHT-105-01-L-D-SM. The mating connector is the Samtec TCSD family of cable strips. Compatibility with non-Samtec equivalents should be verified before use.

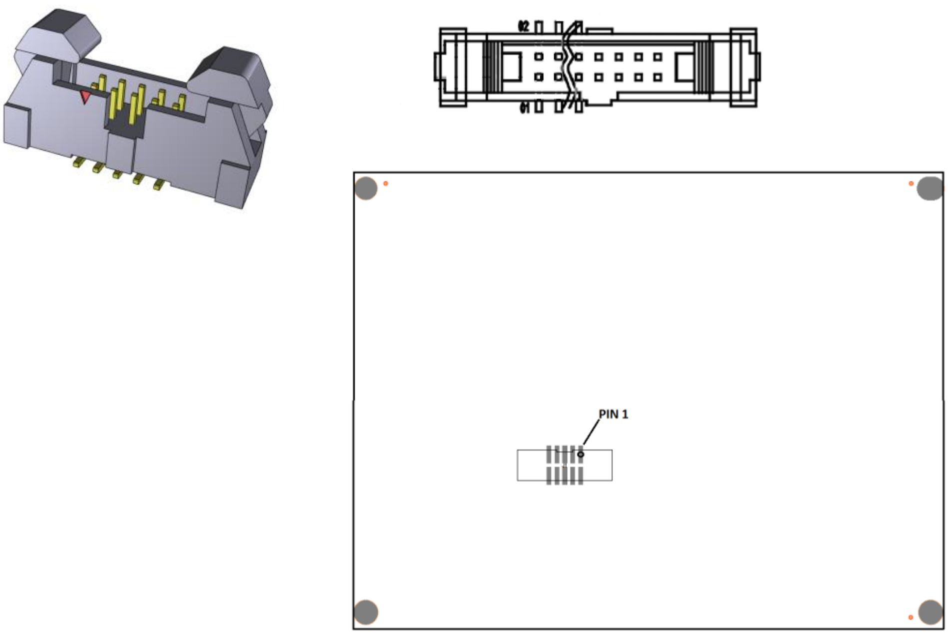

Figure 1. Data/power connector in different views

Table 3. J1 connector pinouts

PIN #	Symbol	Purpose
1	VH	+12V Power
2	VH	+12V Power
3	GND	Ground
4	GND	Ground
5	SCLK	SPI Clock from Master
6	MOSI	SPI Master Out Slave In
7	SS	SPI Slave Select
8	Reserved	Do not connect
9	SELFTEST	Self Test Input
10	LUMA	Analog dimming

3.4 Interface information and Protocol

Beneq EL160.60.100-07NC display incorporates an SPI interface that is similar to many LCD modules. This SPI video interface provides a low-cost, flexible method for controlling display brightness and power consumption. Designers should select the chip set or embedded board that best suits their particular architecture.

3.4.1 Video Input signals

The SPI is driven with the rising edge of SCLK. A falling edge on SS signal indicates the beginning of an access on the SPI, the rising edge of SS signal ends an access on SPI. An access must consist of exactly 8 bits for write operation.

The SPI interface Clock polarity (CPOL) and clock phase (CPHA) are 0. At CPOL=0 the base value of the clock is zero for CPHA=0 and data are captured on the clock's rising edge (low to high transition) and data is propagated on a falling edge (high to low clock transition).

The timing restrictions on SPI are defined in figure 2 and table 4:

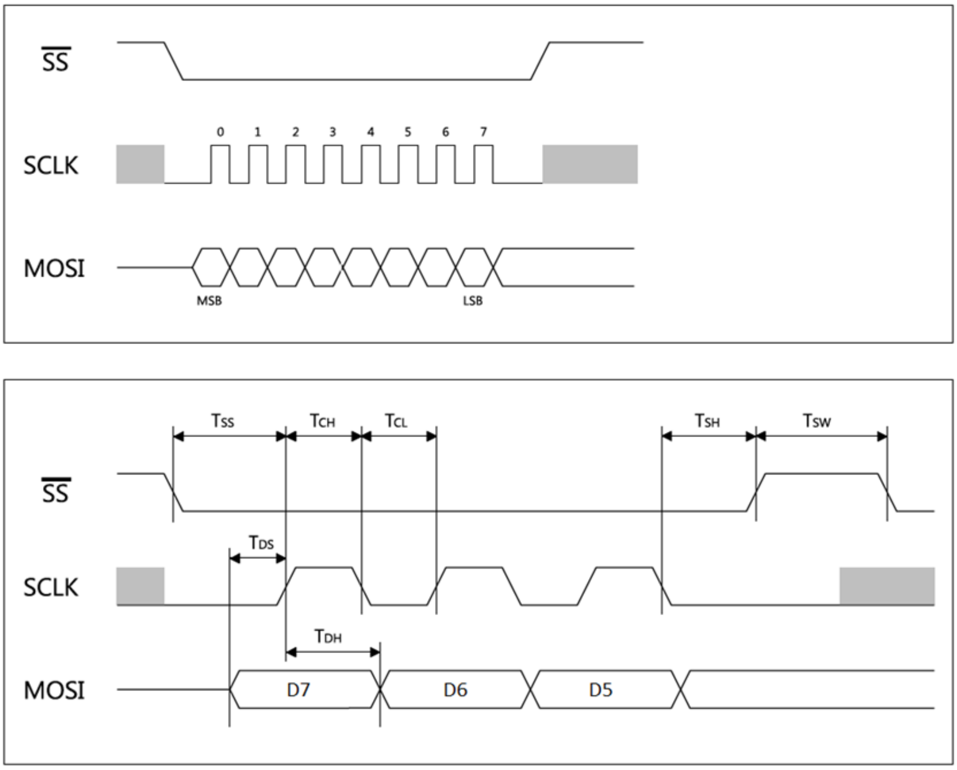

Figure 1. Video input timing diagram

Table 4. Timing restrictions

Description	Symbol	Minimum value (ns)
SCLK high time	T_{CH}	100
SCLK low time	T_{CL}	100
SS -> SCLK setup time	T_{SS}	100
SCLK -> SS hold time	T_{SH}	100
SS disabled between cycles	T_{SW}	100
Data setup time	T_{DS}	100
Data hold time	T_{DH}	100

3.4.2 Initial Power-up

The display enters a self-test mode when turned on, if the selftest pin is not grounded.

3.5 SPI protocol

3.5.1 Commands

Command	Hex #	Binary							
Write complete display data	01h	0	0	0	0	0	0	0	1
Write display block (multiple rows)	02h	0	0	0	0	0	0	1	0
Write one row	03h	0	0	0	0	0	0	1	1
Clear screen (full black)	11h	0	0	0	1	0	0	0	1
All pixels ON (full yellow)	12h	0	0	0	1	0	0	1	0
Invert display image	13h	0	0	0	1	0	0	1	1
Write frame frequency, 100 % luminance (1)	81h	1	0	0	0	0	0	0	1
Write frame frequency, 75 % luminance	82h	1	0	0	0	0	0	1	0
Write frame frequency, 50 % luminance	83h	1	0	0	0	0	0	1	1
Write frame frequency, 30 % luminance	84h	1	0	0	0	0	1	0	0

Note: (1) Default luminance

3.5.2 Write complete display data

Pixels are going from left to right from top to bottom. A first pixel in a byte is the most significant one. See Figure 3 for reference.

Command	Data1 (1)	---	Data N (2)
01h	8 bits	8 bits	8 bits

Notes: (1) First bits of first row
(2) Last bits of last row. N=(Number of rows/8) * Number of columns

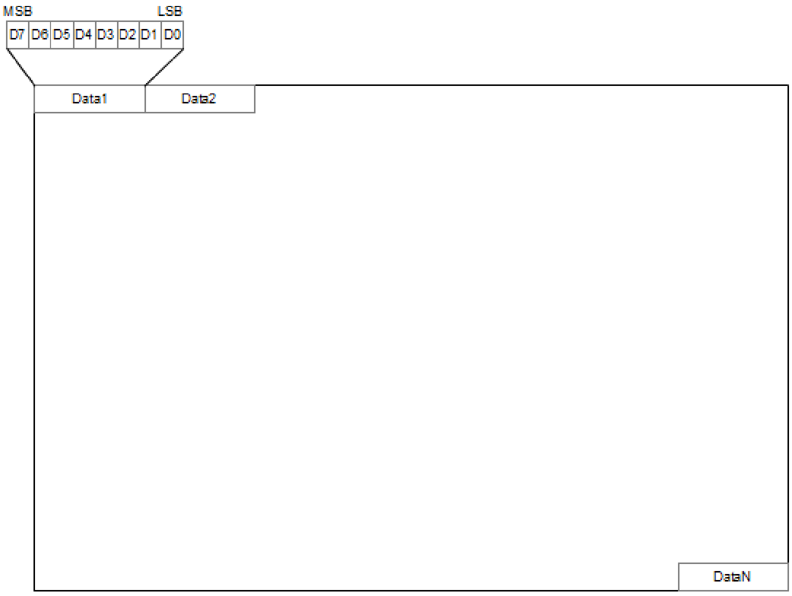

Figure 3. Display pixel locations on image data mapping.

3.5.3 Write display block (multiple rows)

Command	First row number	Last row number	First bits of first row	----	Last bits of last row
02_h	8 bits	8 bits	8 bits	8 bits	8 bits

3.5.4 Write one row

Command	Row number	First bits of row	----	Last bits of row
03_h	8 bits	8 bits	8 bits	8 bits

3.5.5 Clear screen (full black)

Command
11_h

Fill the display frame memory with '0'.

3.5.6 All pixels ON (full yellow)

Command
12_h

Fill the display frame memory with '1'.

3.5.7 Invert display image

Invert command only inverts visible display picture and does not manipulate picture data on display frame memory. Consecutive invert commands toggle displayed image between inverted and non-inverted mode.

Command
13_h

3.5.8 Write frame frequency

Command	Relative Luminance
81_h	100 %
82_h	75 %
83_h	50 %
84_h	30 %

3.6 Self-test mode

The display incorporates a self-test mode composed of two patterns displayed for approximately one minute each, and then repeated. The patterns are as follows: Full On and 1 x 1 Checkerboard.

The self-test mode is started at power-on until the first command to the display is detected. For no self-test at display startup, the SELFTEST pin must be connected to ground.

3.7 Material

Display material is soda lime glass with thin films of the display (DSD stack) and its electrical structure (ITO traces). ITO thickness is 600 nm.

3.8 Optical

The Display emits a yellow light with peak emission at approximately 582 nm. The luminance figures below relate to measurements in darkness (no ambient light).

Table 5. Optical characteristics

Luminance		
L_{on} (areal)	120 cd/m²	screen center, estimate, with a maximum frame rate
Non-uniformity		
All pixels fully lit	35 %	Maximum difference two of five points, using the formula: LNU%=[1- (min_lum/max_lum)] x 100%
Luminance variation (Temperature)		
Maximum	±20 %	Across operating temperature range
Luminance variation (Time)		
Maximum	<20 %	10,000 hours at 25 °C ambient
Viewing angle		
Both sides	179°	
Transparency (optically bonded to clear glass)		
Photopic Transparency	>70 %	
Pixels		
Pixel pitch	1 mm x 1 mm	
Pixel size	0.8 mm x 0.8 mm	leading to fill factor 64 %
Pixel amount	160 rows and 60 columns	

3.9 Dimming

Dimming of the display is handled through the communications protocol of the display ("digital dimming"), or through the LUMA pin (pin #10; analog dimming).

Analog dimming allows for manually adjustable dimming from 100% to approximately 5% of the full brightness. To perform analog dimming, connect a 50 kΩ variable resistor between LUMA and GND. Alternatively, an external voltage or current mode D/A converter may be used to facilitate dimming by sinking a maximum of 250 µA (for maximum dimming) from LUMA to GND on the input connector. Open circuit voltage of the LUMA pin is 4 V nominal.

3.10 Environmental

Table 6. Environmental characteristics

	Operating	**Non-operating**
Temperature		
Standard	-60 °C to +85 °C	-60 °C to 105 °C
Humidity	40C/93 % RH (complies with IEC60068-2-78 standard)	

In order to meet these values with the complete system design, including but not limited to lamination into a windscreen, all materials and processes need to be compliant with these requirements and values.

3.11 Mechanical characteristics

3.11.1 Display Panel

Table 7. Mechanical characteristics/dimensions of the display

Display external dimensions		
millimeters	width	for entire panel, 224 mm
	height	90 mm
	depth	0.7 mm glass with some 10 us of the display stack.
Weight (typical)		For glass panel with density 2.53 kg/dm3, approx. 30 g (without FPC and electronics)
Fill factor		64 % (0.8 mm pixel side with 1.0 mm pitch)

Display active area		
millimeters	width	159.8 mm
	height	59.8 mm
Contact area		
millimeters	height	4 mm
Misc		
32.1 mm wide row contact area at both sides of the active area needed for row electrode signal feed from the bottom of the display		

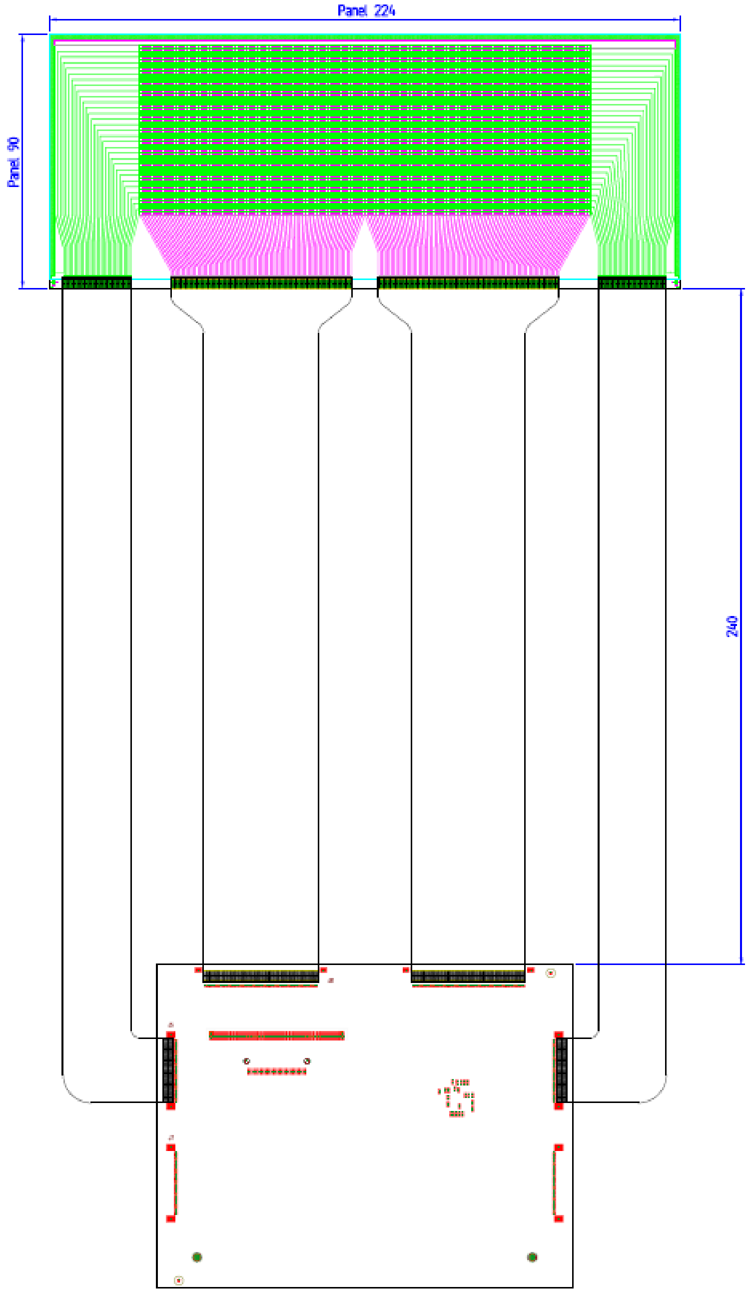

Figure 4. Overview figure of the 160.60.100-07NC

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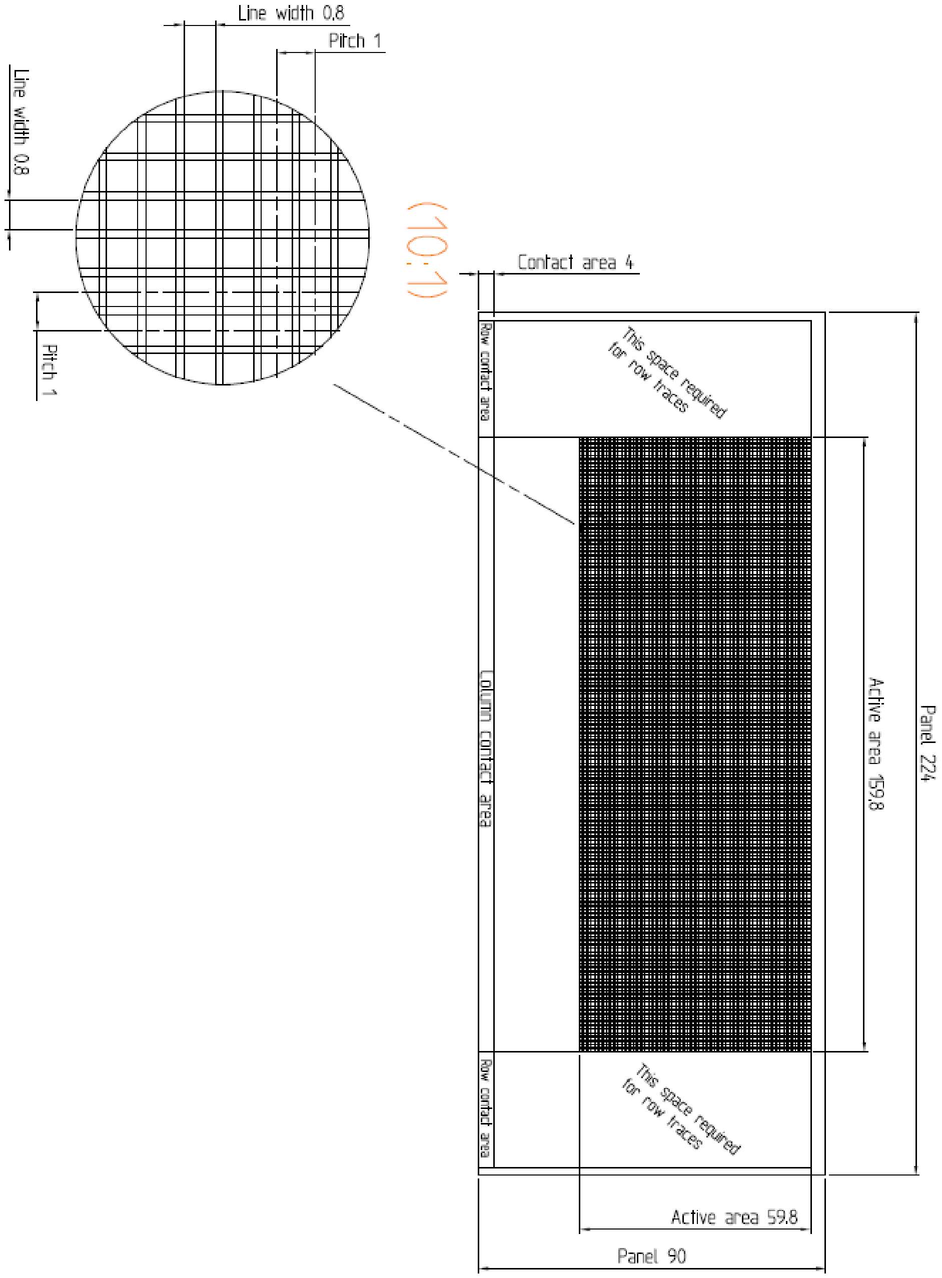

Figure 5a. Display Panel Sizes

Note that the display is viewed from the thin film side, as explained in Fig 5b.

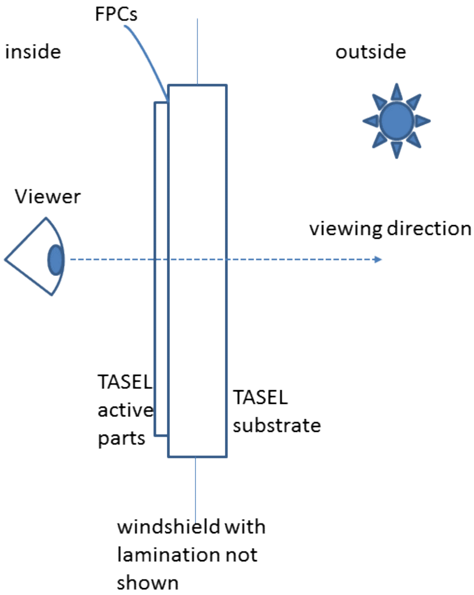

Figure 5b: The display is viewed from the thin film side.

3.11.2 Flexible Printed Circuit (FPC, Flex)

Driver FPCs look as in Figs 6a (row drivers) and 6b (column drivers). There are two column driver FPCs, and two row driver FPCs.

For row drivers, one is a mirror image of the other.

NOTE: All FPCs are bonded to the display glass in a fixed manner and they cannot be detached. Connectors are in the PCB end.

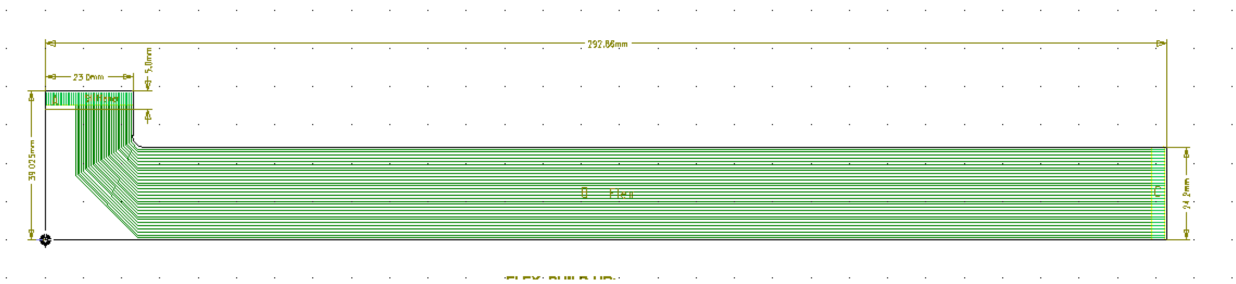

Figure 6a. Row Driver FPC

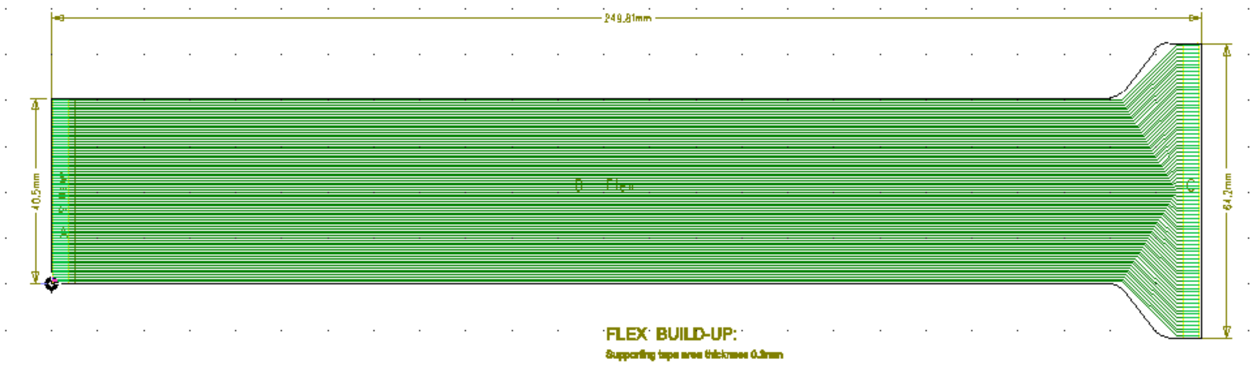

Figure 6b. Column Driver FPC

3.11.3 ECA Board (electronics board, PCB)

Dimensions of the ECA are 148.12mm x 114.72mm.

Max. height of the board is approximately 18mm (from the bottom of the lowest component on the backside to the top of the highest component on the topside)

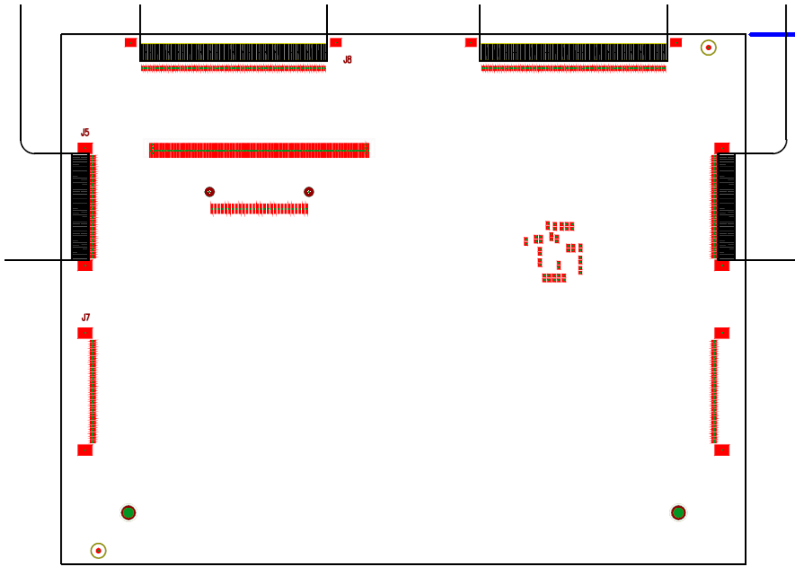

Figure 7. ECA layout

4 Quality

4.1 Defects

Testing method:

- Unaided eye unless otherwise specified.
- Ambient light 500 lux, paper white background and inspection distance 30 cm
- Display under direct light (not reflected) and display not tilted.

4.1.1 Defects in flex/glass (bonding) contact area

Narrow electrodes:

- Line width must exceed 50 % of the design nominal.
- Max. 3 pcs occurrences/pad.
- 90 % of the total designed free contact area must be present.

Scratches:

- Longitudinal scratches allowed
- For transversal scratches see criteria for narrow electrodes.

4.1.2 Glass surface defects

Following applies to all surfaces of the glass panel/s.

Scratches in glass surface depending on width:

- Width >100 μm not allowed
- Width 50-100 μm, max. scratch length 15 mm, 50 mm min. distance between scratches, 6 scratches max. per glass.
- Width < 50 μm allowed
- Glass fractures not allowed

Cavities in glass surface:

- Diameter < 0.5 mm allowed.
- Max. 1 per cm2 and max. 2 per glass.

4.1.3 Breaks in the glass panel/s edge

Breaks/fractures in the panel edge:

- May not exceed more than 0.5 mm from the edge of the glass panel.
- Max length of the breaks/fractures is 1 mm.
- Applies to all sides of the glass panel.

4.1.4 Dark areas in active area

Dark areas within visible segment of display when addressed to full ON luminance:

- 90 % of the nominal active segment area shall be intact.
- A dark area may not exceed more than 0.25 mm2
- Max. 1 per cm2 and max. 2 per glass.

- Dark area caused by thin film delamination is not allowed.

4.1.5 Bright spots in active area:

Bright spot in active area:

- Size of extra luminous area must be <15% of segment area when addressed to full ON.
- Max. 1 per cm2 and max. 2 per glass.

4.1.6 Thin film defects

Scratches in thin films not allowed in active area, allowed outside active area if remaining line width exceeds 1/3 of nominal.

Delamination not allowed in active area.

Thin films on outside side of TASEL glass not allowed (Thin film backside growth).

5 Description of warranty

Warranty of the in-glass laminated product is specified by Beneq in the sales agreement between Beneq and Customer.

SELLER DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

6 Ordering information

Product	Part number	Description
ELT160.60.100-07NC	EL00045100	Transparent TFEL display of matrix type, 160 x 60 pixels, no cover glass (intended for in-glass lamination), 4 FPCs and driving electronics

7 RoHS II

Beneq Oy is committed to continuous improvement. As part of this process we are fully in support of EU directive 2011/65/EU, the Restriction of Hazardous Substances, commonly known as RoHS II or RoHS Recast, which, compared to RoHS, keeps the restrictions on the original six hazardous substances, including lead (Pb) in electronic equipment. It also expands these restrictions to previously exempted categories including medical devices and monitoring and control instruments.

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