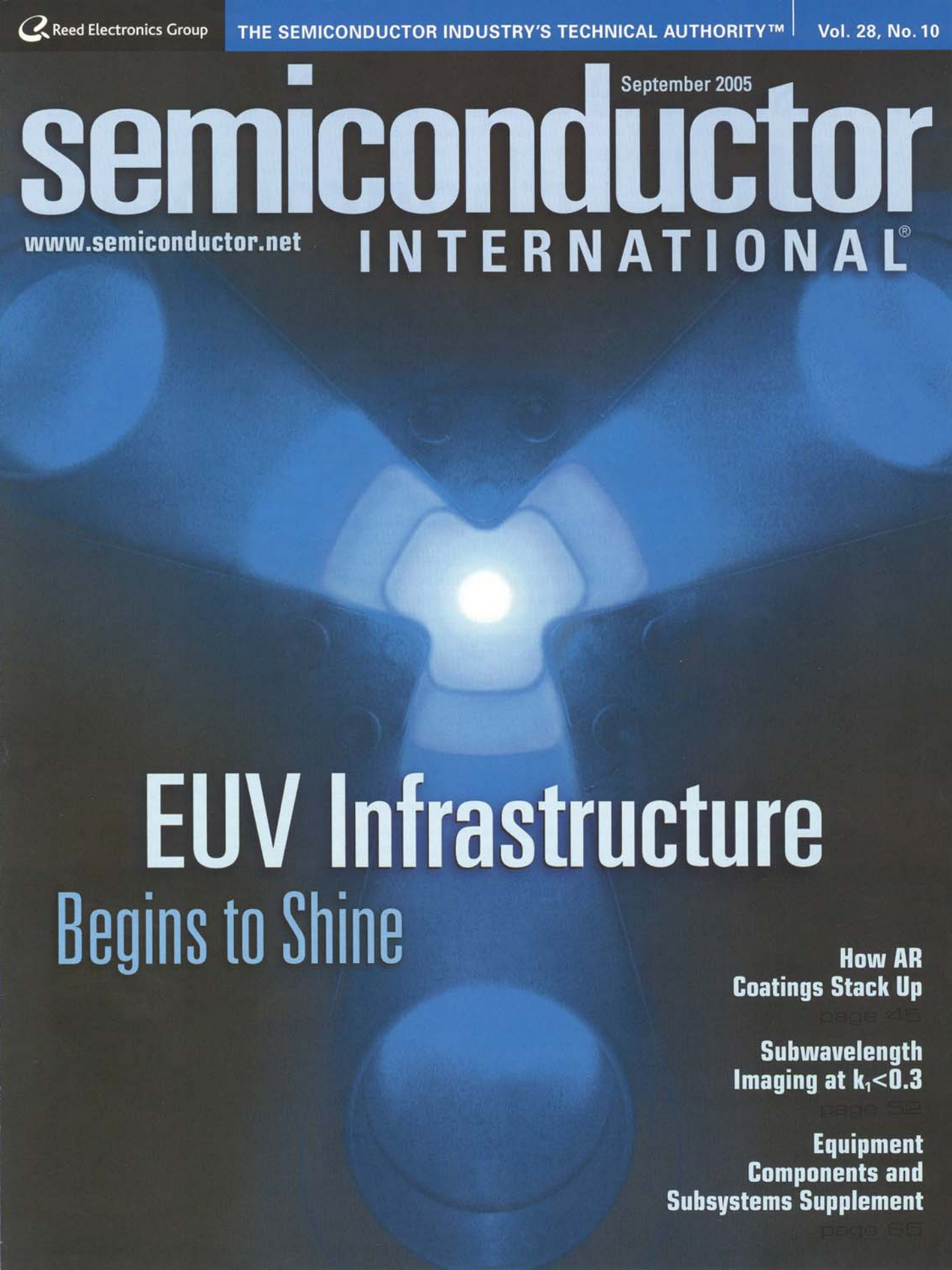
Reed Electronics Group
THE SEMICONDUCTOR INDUSTRY'S TECHNICAL AUTHORITY™
Vol. 28, No. 10
September 2005

semiconductor INTERNATIONAL®

www.semiconductor.net



EUV Infrastructure Begins to Shine

Infrastructure Steps Closer to EUV Lithography

Aaron Hand,
Managing Editor

The latest update of the International Technology Roadmap for Semiconductors (ITRS) lists several difficult challenges for lithography below the 45 nm node. The fact that several of those challenges are specific to extreme ultraviolet (EUV) lithography says two things: 1) There's a strong assumption that EUV lithography will be the exposure tool of choice for critical layers at the 32 nm node; and 2) it's not going to be easy to get it ready on time.

On the 2004 ITRS, listed among the difficult challenges for lithography below the 45 nm node are defect-free next-generation lithography (NGL) masks, especially EUVL mask blanks free of printable defects; protection of EUVL masks from defects without pellicles; NGL exposure tools capable of meeting ITRS requirements; and high-output, cost-effective EUV sources. According to ITRS timing for the 32 nm node, these difficulties need to be ironed out for high-volume production by 2013. Intel Corp., the semiconductor manufacturer making the strongest push for EUV development, aims to introduce its 32 nm node — and its use of EUV lithography — by 2009.

There are some who say there's no way EUV lithography can be ready that soon, and even a few who contend that it will never really be ready. But plenty are keeping the faith and continuing to make the push to completion.

All three major toolmakers — ASML, Nikon and Canon — have EUV development programs in place and plan to ship alpha tools next year. But no imaging capability from the exposure tools will be worth anything without an infrastructure that can support commercial viability.

As the most vocal proponent of EUV lithography, Intel has taken aim at building up the surrounding infrastructure, including masks, blanks, resists and sources. Intel announced last year that it had installed an integrated EUVL process line using a micro-exposure tool manufactured by Exitech Ltd. It can print at a resolution of 30 nm, and will be used to develop EUV technologies, including masks, resists, flare and defect printability. Intel also has established a pilot line for EUV masks.

Freescale Semiconductor, formerly part of Motorola, continues to support EUV development. "Motorola was one of the three charter members of EUV LLC.

At a Glance

Working exposure systems won't amount to a hill of photons if the masks, sources and resists aren't ready for EUV's introduction. Despite the technical challenges, economics promises to be the toughest test.

So we have been courting EUV, so to speak, for going on eight years. We continue to be strong supporters of EUV," said Joe Mogab, senior technical fellow and director of Freescale's Advanced Products Research and Development Laboratory. But many things have happened since 1997, he added, when there was initially a large infusion of funding for EUV. Not least of these were the long-lasting downturn that hit in late 2000; and the emergence of immersion lithography, which put a further damper on EUV.

How long the watery path?

Although immersion lithography was put on the table just a few short years ago, it has come on like gangbusters during that time.[1,2] Although 193 nm immersion lithography with water is generally accepted as being able to last through the 45 nm node (in a hyper-NA incarnation), even higher NAs (numerical apertures) could be achieved with a new immersion liquid with a higher refractive index than water. To be sure, immersion lithography is not without its own challenges, but an extension of its capabilities beyond water could give the industry the time it needs to further develop EUV lithography.

The lithography strategy at Texas Instruments is focused on the belief that 193 nm immersion lithography will be able to take the industry through the 45 and 32 nm nodes. The company is also involved in feasibility studies to take immersion beyond 32 nm.

"Research in areas such as EUV lithography and alternative low-cost lithography approaches is geared toward continued decreases in printed on-wafer dimensions and maximum throughput in wafers per hour," the company said in a statement.

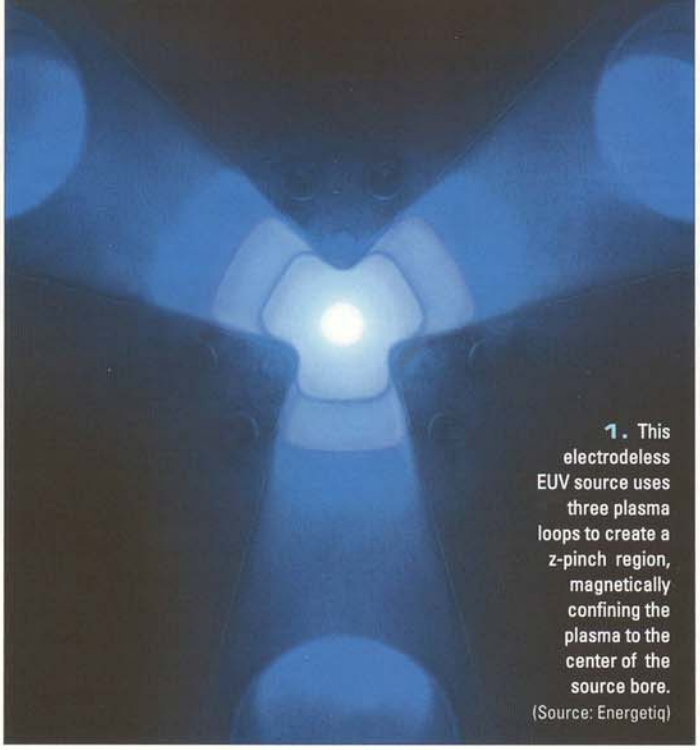
Like most of the industry, Freescale will push immersion as far as it can go, Mogab said. "But, pending any startling breakthroughs there, I don't see it going any further than 32 nm." Going beyond water will be very challenging, added Scott Hector, Freescale's advanced lithography manager, noting that, not only will a new fluid be needed, but also a new final lens element material. "Our prior experience with trying to bring in calcium fluoride (for 157 nm lithography) shows that that's not easy."

Phil Ware, senior lithography fellow at Canon USA, refers to this as "gonzo NA with Kool Aid immersion." But he seems skeptical about its success. Speaking at the Lithography Breakfast Forum during this year's SEMICON West, he pointed out the invention that would be required for "flavored water" immersion, including the continued work on a high-index fluid, as well as high-index lens elements. This is

the same kind of invention that was required for 157 nm lithography — a technology that has been tossed by the wayside because of continued difficulties. And the gonzo NAs would be no picnic either. "Even if you could build a 1.6 NA lens, it would be so huge, you couldn't handle it," Ware argued. "And it's a one-node solution, so why put all the effort into it?"

Not to say that he is any less skeptical about EUV lithography. Although EUV is scalable, can be done with a single exposure, and has a comfortable k_1 factor, there are considerable infrastructure, economic and timing challenges, he said.

Canon will continue with its EUV program, Ware said, but its strategy is to focus primarily on water immersion, putting lots of resources into a tool that can run really fast in water, and is extendable to the Kool Aid era.



1. This electrodeless EUV source uses three plasma loops to create a z-pinch region, magnetically confining the plasma to the center of the source bore. (Source: Energetiq)

Achievements at the source

Making EUV lithography a truly viable high-volume production technique will require that it achieve a throughput comparable to today's production standards. This correlates directly to the source power.

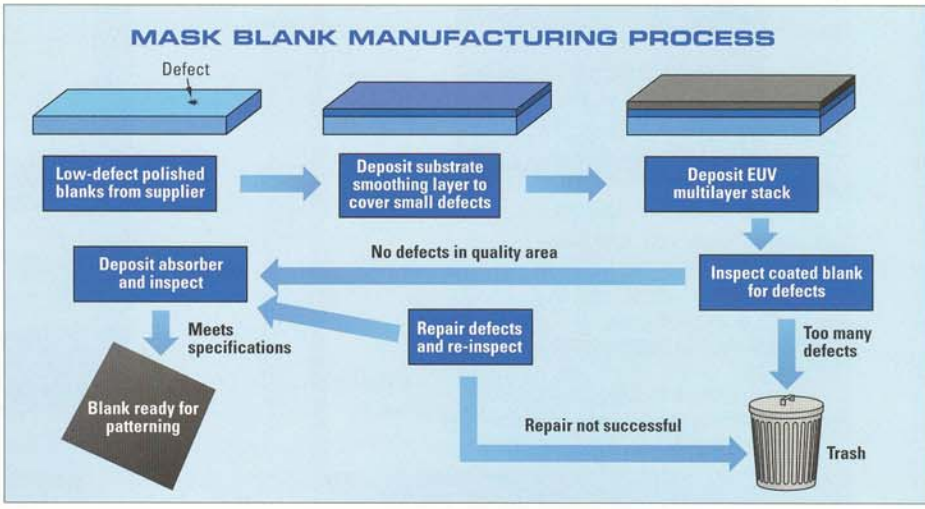
The general discussion for source power needs is targeted toward ~115 W at intermediate focus (IF) to achieve a throughput of >100 wph. Whether it's a laser-produced plasma source or a discharge source, the scaling that is needed is on the order of 4x from where people would like it to be for high-volume manufacturing. "I really think there's a path for that," said Noreen Harned, vice president for technology marketing and new business at ASML. "With that scaling there are other things you have to deal with, and thermal management is certainly one of them. But I think it can be managed. Not an invention, but engineering work needs to be done."

Leading source manufacturers include Cymer Inc., Xtreme technologies GmbH, Philips Extreme UV GmbH, and Gigaphoton Inc. Apparent from the results presented early this year at the SPIE Microlithography conference, power scaling is no longer the issue it was at the same time last year. "Power scaling is viable, but it comes with the challenge of debris mitigation," Harned said. "And that's as important because that will impact overall productivity." Most source developers are now talking about using tin rather than xenon as the "fuel" for the EUV source because of its superior conversion efficiency.

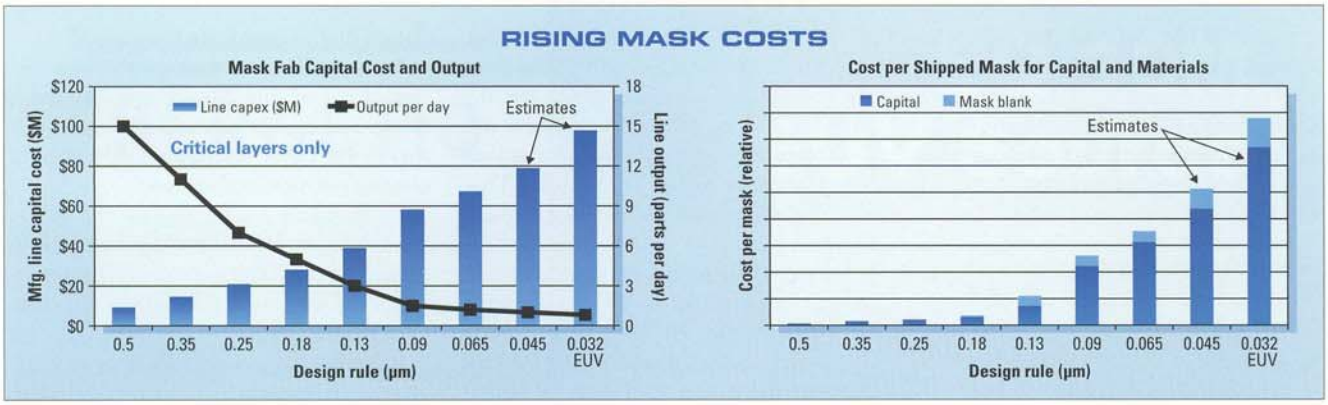
As announced late last year,[3] Cymer has settled on a laser-produced plasma source, largely because of its scalability. And one problem developers are facing with discharge sources is electrode erosion. On its current track, Cymer expects to reach an output power of 102.23 W IF by 2007.

Cymer also announced a switch to lithium as the source's target material. It has a conversion efficiency of >2.5%, as opposed to the <1% of xenon, which has been used extensively in research. More importantly, lithium has a positive impact on collector lifetime — a significant consideration in continued source development. Xenon and tin ions sputter more readily onto the collector. Also, the concept Cymer is using to evaporate any lithium sputtering from the collector does not work well for tin.

A new company on the playing field is Energetiq Technology Inc. Although its power scaling to date is not anywhere near the leading edge (~10 W at the source vs. ~25 W IF), the company's focus is more on availability of a cheap, workable source for infrastructure development. As CEO Paul Blackborow noted, researchers could use the relatively low-power but stable, small and bright source to get going on resist research, for example. "Nobody at the resist companies even has a source. This is nuts," he said. "How are they going to develop resists if they don't even have a



2. EUVL masks are patterned absorber layers on top of multilayer films of silicon and molybdenum deposited on low thermal expansion material substrates. A defect that appears on a mask blank could cause imaging problems. (Source: EUV LLC)



3. Mask manufacturing line capital costs are expected to rise 10x from the 0.5 µm to the 32 nm node (left), with a 190x increase in cost per shipped mask (right). Material costs alone per shipped 32 nm EUV mask will exceed the 130 nm mask line plus material costs. (Source: Toppan Photomasks)

lightbulb?" Albany NanoTech took delivery earlier this year of Energetiq's EQ-10M source, and plans to use it for metrology research.

Energetiq's is a discharge plasma source, but it is an electrode-free one. Discharge sources produce light by passing a current through a gas, heating the gas's atoms until they emit EUV light. Traditionally, these sources use a pair of electrodes through which the current is passed. Discharge sources are less expensive, Blackborow said, but debris is a problem. The electrodes are a major source of the debris, caused when the electrodes overheat.

In Energetiq's source, z-pinch occurs where three inductively coupled plasma loops (or six loops in a higher-power version) merge to create a magnetically confined pinch region (Fig. 1). In this way, there is less interaction between the plasma and walls, creating less debris and more light, Blackborow said.

Particle protection

Sources are not the only stumbling block in EUV development. Because photons at 13.5 nm are absorbed by most materials, including the glass that traditional lenses and masks are made of, EUVL relies on all-reflective optics instead of transmissive. Air will also absorb EUV light, so a vacuum environment is required.

In current photolithography setups, a pellicle is used to protect the reticle from defects or particles throughout the lithography process. But because there are so few materials that transmit in the EUV range, the industry has not been able to come up with a pellicle material that will work. So the expectation that has been reached is that no pellicle will be used for EUV lithography. Proposals tend to center on some sort of removable, temporary pellicle — one that will be used to protect the mask only during transport and storage.

ASML, for one, has proposed a frame with a removable cover that would stay with the reticle except during exposure and would be the only surface contacted by robotic handlers and the storage pod. "What it means is that you never directly handle the mask, so you remove that act of particle generation," Harned said.

This is not such an inconceivable notion, since exposure tools have historically not been big particle adders, noted Chris Progler, CTO at maskmaker Photronics Inc. "I think it's doable with the right enclosures."

Frankin Kalk, CTO of Toppan Photomasks Inc., said he is not too worried about not having a pellicle in the printing process. "We write these plates on e-beams for 15-20 hours without a pellicle," he said. "And it's held face up in the e-beam writer, which is the worst case for them."

The 'blankety-blank' blanks

Looking at the high-end, leading-edge 193 nm photomasks that require a considerable amount of resolution enhancement techniques (RETs), the writing part of the mask is a huge challenge. "The write times have gone up quite a bit over the past three to four generations," Kalk noted. "That's driven by OPC."

EUV lithography, on the other hand — because of its drastically reduced wavelength — brings with it a significantly relaxed k_1 factor (it will start near 1.0). This means less optical proximity correction (OPC) and therefore simplified mask writing. "For EUV, the challenge is in a whole different regime — it's getting the blank ready to be patterned, not the patterning," ASML's Harned said. "You'll be able to use binary masks with very simplistic RETs."

EUVL masks are patterned absorber layers on top of multilayer films of silicon and molybdenum deposited on low thermal expansion material substrates (Fig. 2). With today's high-end blanks for photolithography — with just one or two film layers on quartz — the industry already struggles with defects, Progler noted. EUV mask blanks have upwards of 80 layers of film. Every time a layer is deposited, the probability of adding enough defects to blow away the yield increases. And because it is such a thick film stack, if a defect is deposited on a lower layer, it cannot be repaired easily.

"So EUV mask blank defects are still a big concern," Progler said. "But the progress has been fairly positive." Blanks have gone from needing many orders of magnitude improvement to a point where their readiness becomes more conceivable. "It's been a great improvement, but squeezing that last 20% or more of capability will still be a big challenge that shouldn't be underestimated."

Last December, Sematech North announced that it had reduced deposition tool-generated defects in EUV mask blanks down to as few as one defect per mask at 80 nm resolution, which translates into 0.005 defects per square centimeter. The ultimate goal is for defect-free mask blanks, measured at 25 nm resolution.

"They were able to isolate and show that the defects that were a concern were really not in the multilayer coating, but more on the substrate itself, which comes down to a cleanliness issue," Harned said. "Still, you can't have the defects, but that's also an issue that's becoming more critical for 193."

Sematech has made a lot of significant progress, exceeding EUV LLC capabilities, noted Freescale's Hector, who recently completed an assignment at Sematech as mask strategy program manager. "The progress has been very good, but there's still a long way to go."

Seeing is believing

The defect size listed on the ITRS for the 32 nm node is 23 nm. That is a challenging goal, since current metrology tools cannot reliably detect particles below 80 nm, noted David Krick, program manager for Sematech North's Mask Blank Development Center.

Kalk said he is optimistic about mask metrology. "SEM-based CD metrology for masks has come a long way in the past seven to eight years," he said. Masks present a fairly different challenge for CD-SEM tools than wafers do, he added, because they don't have a conductive substrate. "But the newest tools are really good."

Mask inspection will need to be reflective rather than transmissive, which will be something new, Kalk noted. "It remains to be seen whether we'll be able to use just an extension of today's conventional mask inspection, or whether we're going to need something that's actinic and operates somewhere around 13 nm. Defect review will most likely have to be actinic."

Metrology causes somewhat of a timing concern, Progler noted, since really understanding the impact of ever-smaller defects rests on the ability to see them. "Usually, metrology is what drives improvement," he said. "When you have a technology that lets you see really well, you then see what needs to be improved."

Economic roadblocks

The complexity behind all of the technologies surrounding EUV lithography is part of what will make the technique an expensive one. And it is economics that is likely to be EUV's biggest downfall. "I think economics is really the driving factor. It's not a technical issue," Kalk said. "The industry has shown that time and again."

For masks, EUV costs are just a continuation of a long line of skyrocketing mask costs, according to Kalk. He noted that there are two main drivers for cost: device complexity, which drives the number of masks per set, and also drives the pattern complexity on the masks; and mask complexity, which is driven by the k_1 factor. The price growth for masks over the years has been considerable. Between the 0.5 µm node and the 130 nm node, there was a ~10x growth in cost. "The real reason was just complexity," Kalk said. "That trend is going to continue right on through 32 nm."

According to Kalk, per mask shipped, the cost of the mask line will be 2x that of a 90 nm line (Fig. 3). "For a yielded mask out — 32 nm EUV mask — just the cost of material for that mask will be higher than the cost of material plus capital equipment cost for 130 nm. Who can afford to purchase these things?"

The answer is the microprocessor manufacturers, for one, which is why Intel is so determined to make EUV lithography work. EUV should lend itself well to high-volume manufacturing, but not so much for specialized devices, Kalk said. "The mask cost is effectively part of the NRE," he said. "So if you're making a very large wafer run, you can afford a pretty large mask cost. But if you're building hundreds of wafers, you're going to be pretty worried."

EUV lithography will happen if it makes economic sense. "It will come in if it's cost-effective for a significant portion of the market," Kalk said. "If you're running a fairly low wafer volume per device, it might make sense to do X and Y exposure instead of having to spring for the EUV part of the equation."

A little skepticism

Although some critics are talking about EUV *never* coming to fruition, others figure it may be more a question of timing. Although Intel's push for 2009 may be a bit unrealistic, they realize how heroic this industry can be when it needs to be.

The big question is what alternatives exist. There is multiple-exposure 193 nm lithography with very high NA. Nanoimprint lithography is also considered by some to be a possibility.[4] But much of the support for EUV lithography comes with the belief that there really isn't anything else with anything close to the viability and momentum that EUV has.

"You can argue that there's a good technical path to get the technical requirements in all the different areas," Hector said. "They're probably not so much physics challenges, but engineering challenges that are not to be trivialized."

It comes down to how much time and money is available, Mogab said. "All these things can be solved and will be solved if there's no other alternative. It's really a question of time and dollars."

Chipmakers are saying that this is the economic model that will work for them, according to Blackborow. "It'll happen when the timing's right; when the costs match the need."

Just what that timing will be is an ever-changing target. On the ITRS, the insertion target for NGL has slipped from the 180 nm node on the 1992 version to the 32 nm node on today's iteration. Intel is targeting 2009 for high-volume EUV production, but that hasn't always been the case. It stated in 2001 that it expected to start using EUV technology in 2005, with the technology extendable beyond the end of the decade. Two years ago at Photomask Japan, Intel was saying, "EUVL is the only viable solution for 45 nm." A lot has changed in two years, and it has become generally accepted that 193 nm immersion lithography will take care of the 45 nm node. What will change in the next two years? •

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Energetiq Technology, Inc.,
7 Constitution Way,
Woburn, MA 01801, USA

Tel: +1 781 939 0763
Email: info@energetiq.com
Web: www.energetiq.com