Advances in Planar Coil Processing for Improved Microinductor Performance

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This paper examines the process challenges in developing high aspect-ratio copper structures for improving microinductor performance. With increased miniaturization, increasing windings losses become a major challenge limiting the microinductor efficiency. It was also identified that within constraint footprints coil thickness to spacing ratio increase can reduce dc resistance significantly. In this paper, we present a reliable process for developing high aspect ratio (∼5.8) resist moulds for copper electrodeposition. This resist provided coil spacings 10 μm for 58 μm resist thickness; this in turn reduces the dc resistance of a typical microinductor by more than 17% when compared with a similar device reported previously.

Index Terms— **High aspect-ratio resist mould, integrated magnetics, low winding losses, thin-film inductors.**

I. Introduction

THE miniaturization of inductors enabled by higher dc–dc converter switching frequency (>10 MHz) in switched mode power supplies has increasingly become an efficient replacement for linear regulators for hand-held portable devices. Such miniaturized inductors can be well integrated in a package along with active converter. Furthermore, silicon based monolithic microinductors compatible with existing CMOS technology can be fabricated with the ICs to achieve complete integration, also termed as power-supply-on-chip (PwrSoC) [1], [2]. This is further facilitated with the advancements in back-end-of-line MEMS based processes. This includes thick photoresist processing to achieve high aspect-ratio coil structures for realizing inductor windings [3]. In addition, the inclusion of magnetic film deposited by sputtering, electroplating, or screen printing techniques as core material enhances the inductance and Q-value of these inductors [4]–[7]. For PwrSOC applications, the size of the magnetic components has to be small enough to make it compatible with the rest of the converter circuitry. However, the efficiencies of these highly miniaturized devices are curtailed by core losses (hysteresis and eddy-current losses) and more importantly the winding losses.

Winding losses can be reduced by implementing wider conductor track, which will result in a larger footprint area, which is typically constrained. The ideal footprint area of these integrated inductors cannot be more than 2 mm^2 for low power applications, e.g., currents <1 A. In the previously demonstrated inductors and buck converters, it was reported that the winding conduction loss can be up to 80% of the total inductor loss [8]. This conduction loss issue will become significantly higher if the footprint area for inductors becomes smaller [9]. A high aspect-ratio winding structure (winding thickness/winding width) is the key in reducing the conduction loss and in turn increasing the efficiency [3].

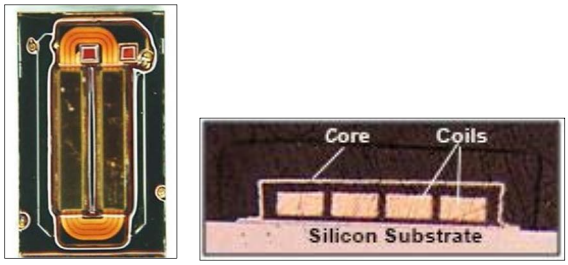

Fig. 1. (a) Top-view of a typical racetrack microinductor. (b) Cross section of a closed core racetrack inductor with four turns.

In this paper, we have developed a new single-spin process for deposition of high aspect-ratio resist moulds using THB-151N from JSR Micro to improve the device performance in constrained footprint area with a reduced ratio of winding thickness to spacing. A single spin-coating process is found to be highly desirable to simplify the photolithography process steps and shorten the overall process time [3]. The top view of a typical racetrack inductor is shown in Fig. 1(a) and its cross section is shown in Fig. 1(b). The impact of coil thickness to spacing ratio on conduction loss will be studied using a validated inductor model in Section II. The development of microfabrication process for winding deposition will be presented in Section III. The process results and conclusion will be presented in Sections IV and V, respectively.

II. Ratio of Winding Thickness to Spacing

A validated in-house developed analytical model [10], [11] is applied here to specifically investigate the influence of winding thickness to spacing ratio on the loss performance. The efficiency (η) of the inductor is calculated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{ind}}} \tag{1}$$

where P_{out} and P_{ind} represents the output power of the converter and net inductor loss. The inductor loss is contributed

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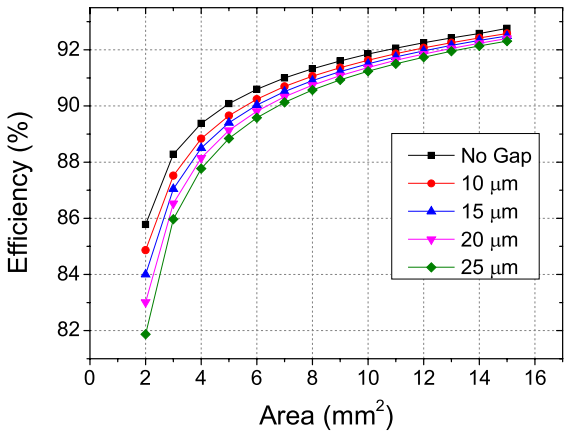

Fig. 2. Efficiency dependence on inductor footprint for varying coil spacings.

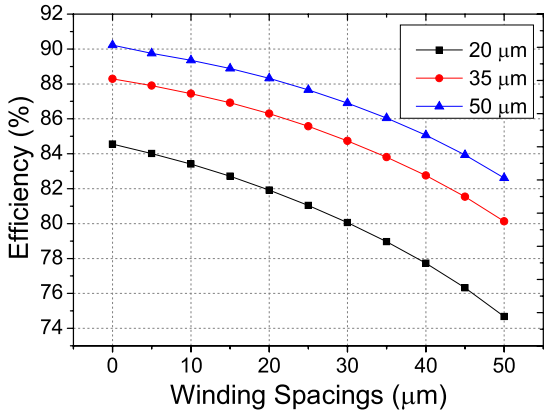

Fig. 3. Efficiency dependence on inductor coil thickness and spacings.

by core loss and winding loss. The model is incorporated in optimization tool [8]. It is then optimized to attain maximized inductor efficiency and minimized dc resistance at fixed process and material constraints at different winding spacings and thickness.

The winding spacing is varied from 5 to 25 μm for 35 and 50 μm winding thicknesses. While the winding width was varied from 15 to 50 μm for same thicknesses. An ideal inductor with negligible winding spacing (no gap) was considered for reference purpose.

Fig. 2 shows the highest efficiency achievable in a 120 nH racetrack inductor operating at 20 MHz switching frequency at different footprint areas (2 to 15 mm^2) for 35 μm-thick coils, from the analytical model. For smaller footprint areas, there is 4% efficiency fall from the ideal case, because of $\sim$26% rise in dc resistance. This effect is not very prominent for larger inductors (as observed from Fig. 2). It is apparent the percentage of device footprint occupied by the spacing becomes less significant for larger footprint area, which in turn make the device performance less sensitive to the spacing.

Fig. 3 shows the dependence of efficiency on windings thickness to spacing ratio for 120 nH inductors designs with 2 mm^2 footprint area. The winding thickness is varied from 20 to 50 μm, while the winding spacing is varied from 0 to 50 μm. It is evident that increase in winding thickness will lead to higher efficiency for the same spacing. In addition to that, the spacing also plays a very important role in influencing device performance. The inductor design using 50 μm winding thickness and 50 μm spacing is less efficient than the one using 20 μm winding thickness and 10 μm spacing.

A key figure of merit for inductor performance is the inductance per unit dc resistance. It is always beneficial to increase winding thickness to reduce the dc conduction loss. However, the thickness of winding is constrained by the maximum thickness of electroplating moulding using microfabrication lithography process. A thickness of 46 μm winding has been achieved using multiple sin-coating of photoresist [12]. This, however, comes at the cost of process complexity from multiple spins and resists resolution. To further improve the device performance and considering the difficulties in realizing thicker electroplating moulding using microfabrication lithography process, we choose to minimize the spacing while maintaining similar thickness of windings. The process constraints limit the design specifications on selecting a reasonable size of spacings for real fabrication.

III. High Aspect-Ratio Resist Mould Process for Copper Coil Deposition

A. Resist Mould Coating and Process Optimization

As aforementioned, to simplify the resist moulding process and reduce the winding gaps, one of the objectives of this paper is to develop a single-spin coating process to produce thick electroplating mould for windings. A detail review of all the thick photoresists was done and based on the process requirements, THB 151N was selected. THB 151N from JSR Micro is a negative tone acrylic chemistry based resist. With high achievable thickness with single spin-coating, excellent adhesion to copper surface, high resolution, clean development, easy stripping, and good overall throughput [13], [14]. Two different processes were developed for 35 and 50 μm resist thicknesses. The wafers were sputtered in Nordiko dc magnetron with 20 nm titanium (Ti) followed by 200 nm copper (Cu) that acts as seed for copper electrodeposition. The resist was allowed to settle down at room temperature before dispensing for eliminating bubbles during spin coating.

The resist was then dispensed covering over 50% of the wafer. It was then allowed to settle for 120 s and then spin coated in Laurell spinner for 2000 r/min/30 s (main spin) for 35 process. For 50 μm process the resist this spin was for 1300 r/min/30 s. This resist showed no bubbles on baking. Thick resists require longer soft bake times for reducing the solvent content. It was found that with THB 151N, optimized times between 300 and 900 s was ideal, keeping the solvent content 20%–40% essential for proper development without resist loss and overall thickness variation of less than 2 μm.

B. Lithography Process Optimization

The wafer was then exposed in hard contact mode for an exposure dose of 700 mJ/cm^2, in broadband (i, h, and g-line) Canon PLA-501FA optical mask aligner. The optimized exposure dose was found to be 500–900 mJ/cm^2. Increasing the exposure dose beyond 900 mJ/cm^2 would result in smaller gaps being overexposed. The wafer was puddle developed in

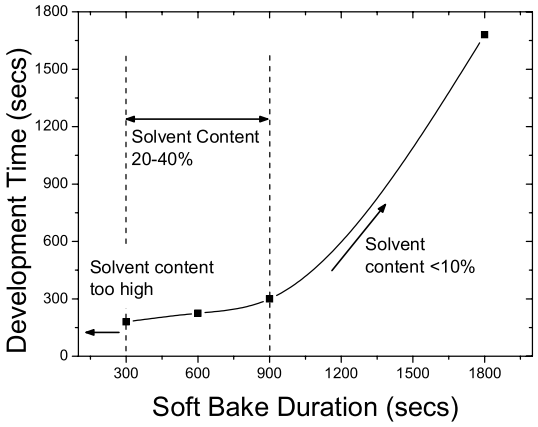

Fig. 4. Increase in development time with soft-bake duration for THB 151N.

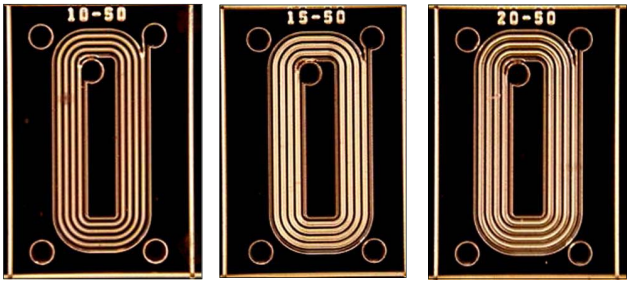

Fig. 5. Resist patterns with different coil widths and spacings.

TMA 238WA from JSR Micro, which is a TMAH (2%–3%) based metal-ion free (MIF) developer at room temperature. A thickness of 38 and 58 μm was measured with Tencor α-step profilometer. This thickness is higher than the reported work with a smaller spacing. As expected the development time increases with the postexposure bake (PEB). This is because on increasing the PEB, the developer soluble solvent content evaporates, decreasing the solubility during development phase (Fig. 4). The total process time was ~90 min, which is significantly shorter and simpler than previously reported in [3]. The developed resist patterns are shown in Fig. 5.

C. Copper Coil Deposition Process

The wafer was allowed to undergo an oxygen plasma treatment (March Plasmod) for 2 min to make the copper surface more hydrophilic. It was then direct current plated for 40 min copper (~35 μm obtained) and 55 min (~45 μm obtained) in SA/1b Digital Matrix system in Schlötter copper plating bath. 35 and 45 μm copper coils were deposited at direct current of 0.15 and 0.20 A. The resist was then removed using THB-S17 from JSR Micro at room temperature followed by Ti/Cu wet etch using metal etchant solution.

IV. Results and Discussion

The plated copper tracks showed an excellent side wall profile (~90.6°), as shown in Fig. 6(a) and (b). It was also found that wider tracks widths develop quickly compared with smaller tracks, as they are more accessible to the developer solution. A yield study showed that 87.5% of the coils

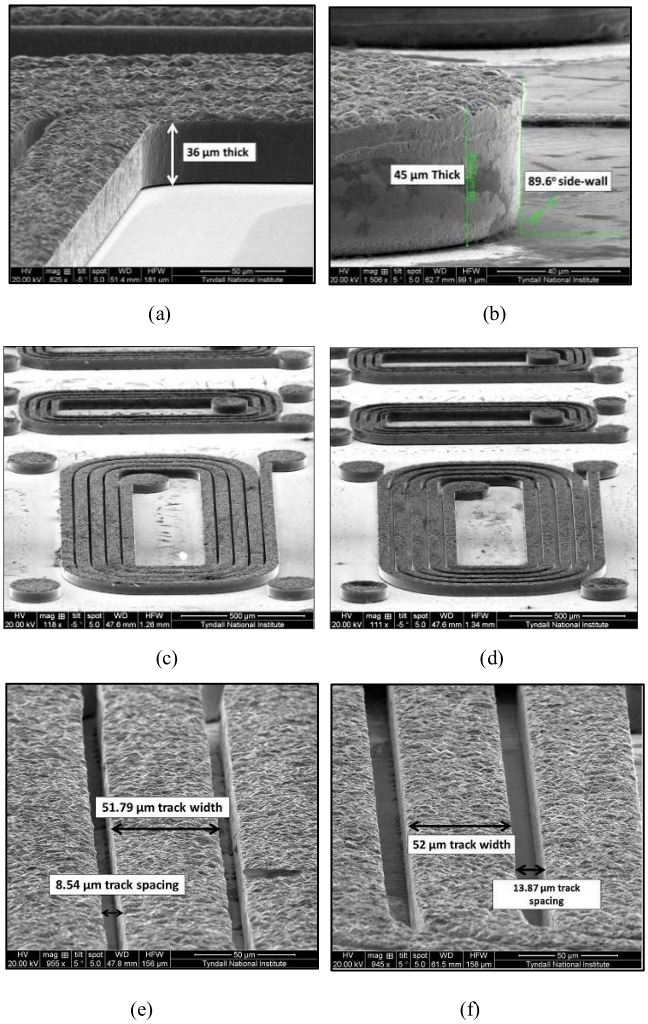

Fig. 6. SEM images of the copper tracks electroplated. (a) and (b) Side-wall profile of the 50 and 35 μm thick tracks. (c) and (d) Copper coils with 10 and 20 μm spacing. (e) and (f) Top view of the tracks with 10 and 15 μm spacings.

were realized for 10 μm spacings and 25 μm coil width for 35 μm coil thickness. This yield reaches almost 100% for wider track widths. Yield studies for 45 μm coil thickness suggested 100% yield for 10 μm resist widths with 50 μm coil widths. This process gives a considerable improvement over the previous report in [12]. Fig. 6(c) and (d) shows the copper tracks with 10 and 20 μm spacing. Scanning electron microscopy images [Fig. 6(e) and (f)] shows the coil spacings and widths.

The analytical calculations for the dc resistance variation (shown in Fig. 7) for 10 μm spacing showed an improvement of almost 32.64% and 25.28% for 35 and 50 μm coil thickness compared to 25 μm spacing. There is an improvement of 14.68% and 17.36% improvement for 50 and 35 μm coils, respectively, from its 20 μm spacing process previously reported [12]. In addition, this process has been able to provide winding thickness to spacing ratio of 4.5, which is higher than previously reported (~3.2 and 4) [15], [16]. In our opinion, the photolithography process also plays an important role in limiting the process.

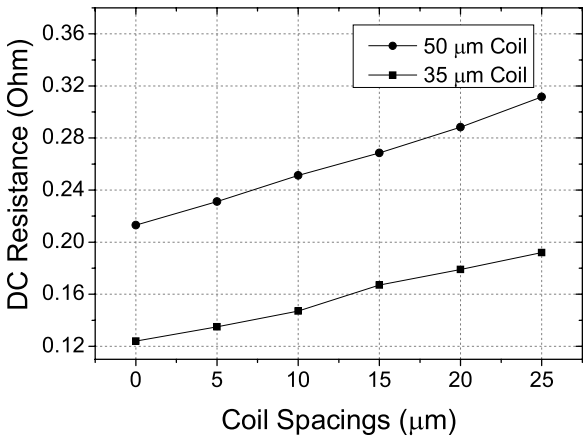

Fig. 7. DC resistance variation with various coil spacings for 35 and 50 μm-thick copper coils.

V. Conclusion

The influence on winding spacing and coil thickness on microinductor have been studied. It was found that coil thickness to coil spacing ratio has significant impact on dc resistance per unit footprint. We developed a new high aspect-ratio resist process of minimizing the coil spacings. It was found that 10 μm coil spacing could be achieved with THB 151N for thicknesses $\sim$50 μm. The developed process gave a resist aspect ratio of $\sim$3.8 (10 μm coil spacing and 38 μm resist thickness) and $\sim$5.8 (10 μm coil spacing and 50 μm resist thickness) with 100% yield. This showed a dc resistance reduction of 32.7% and 25.3% for 35 and 50 μm-thick tracks, respectively, for 2 mm^2 racetrack inductors. It was also found that 10 μm spacings reduced the winding losses by 14.7% and 17.4% compared with 20 μm spacing in a previously reported work. This process successfully provided winding thickness to spacing ratio of 4.5, which is also higher than previously reported work.

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