
CORIAL
A Plasma-Therm Company

CORIAL D500

Large capacity batch system for 24/7 production environment

High-quality films for a wide range of materials, incl. SiO2, Si3N4, SiOCH, SiOF, SiC and aSi-H films

Film deposition from 120°C up to 325°C. Optional low-temperature chamber for film deposition at 20°C

Large batch loading capacity (104 X 2”, 25 X 4”, 9 X 6”, 4 X 8” wafers, or large format substrates

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SYSTEM DESCRIPTION
CORIAL D500

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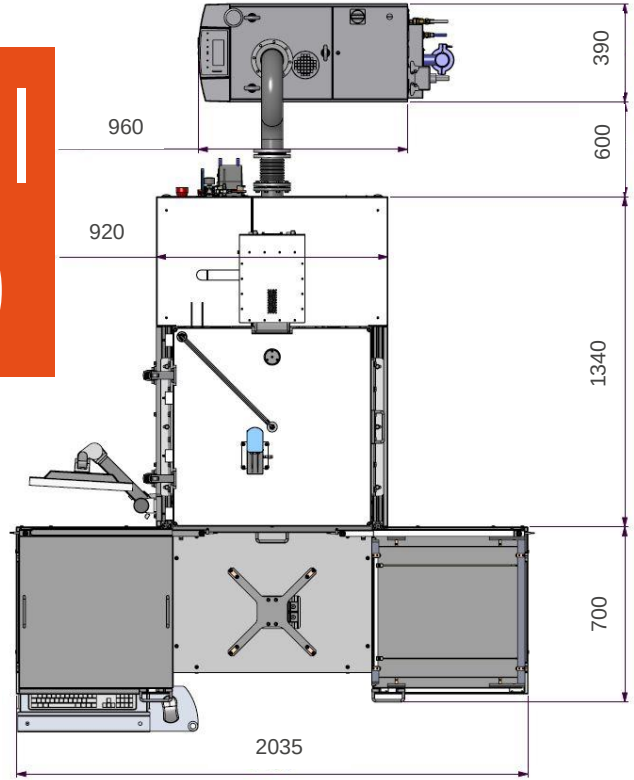
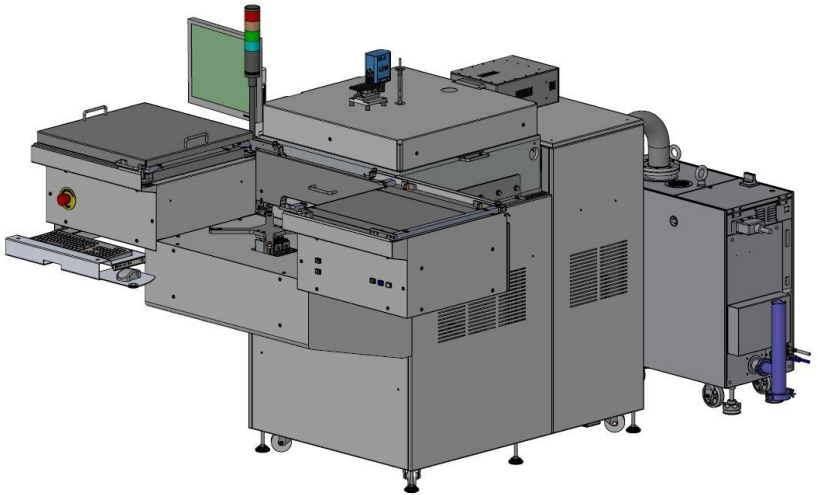
SYSTEM DESCRIPTION

General View

Corial D500

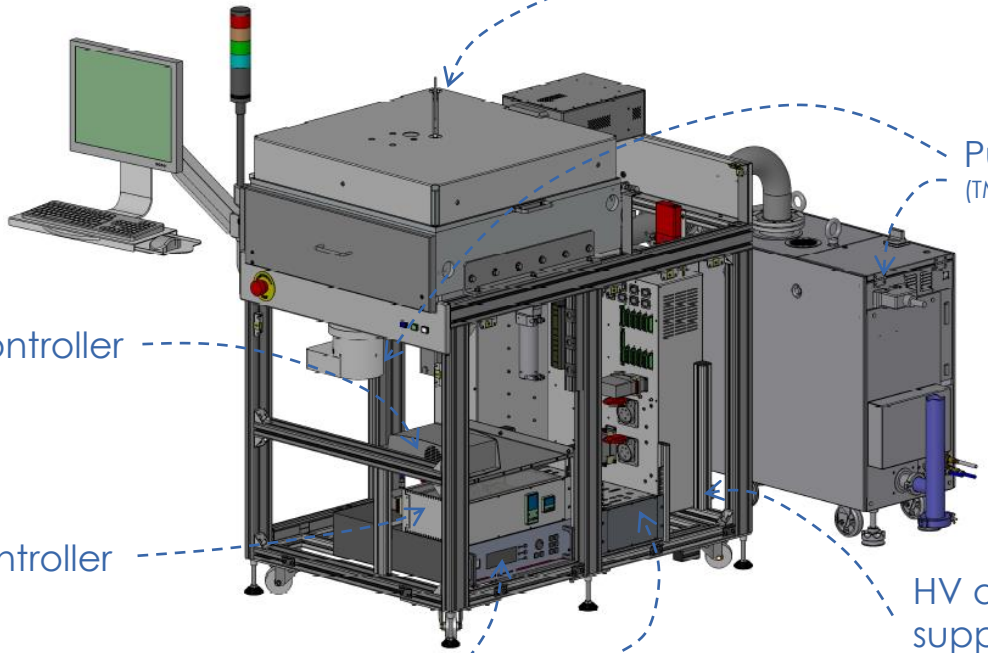


COMPACT FOOTPRINT



SYSTEM DESCRIPTION

Detailed View



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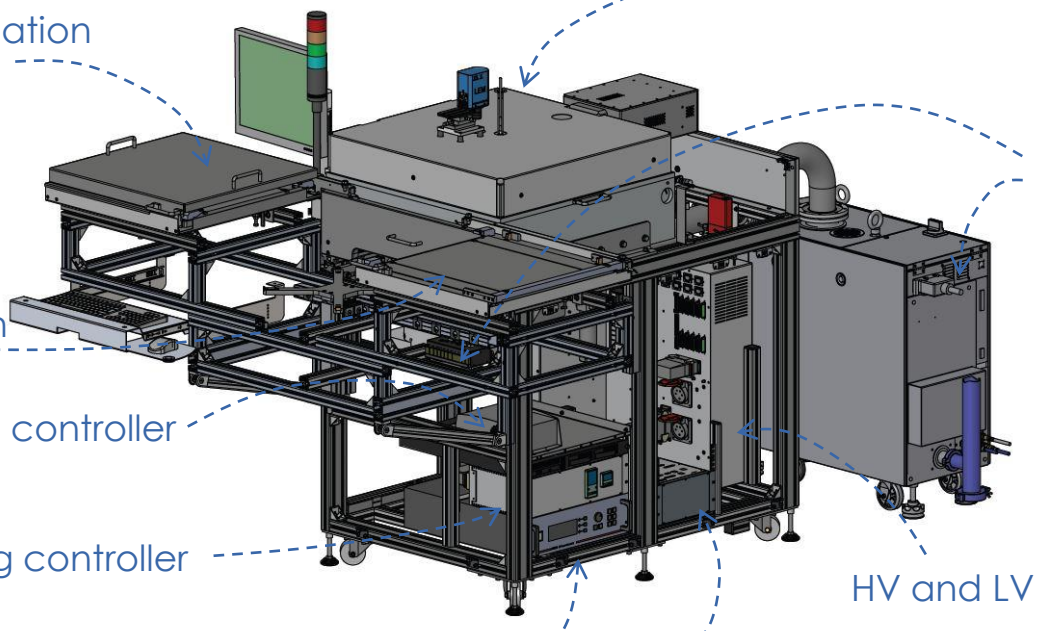
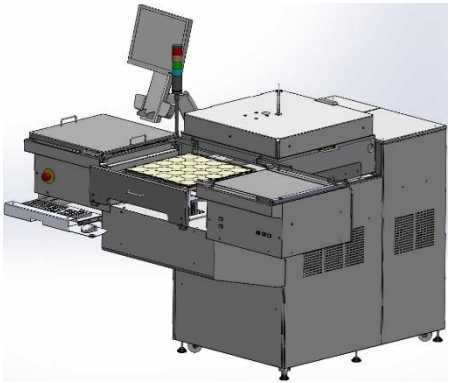


SYSTEM DESCRIPTION

Mechanically Assisted Loading



6 MIN

PRE-HEATING TIME IN DEDICATED STATION FOR FASTER SHUTTLE HEATING IN REACTOR

5 MIN

HEATING TIME IN REACTOR TO REACH 280°C

5 MIN

COOLING TIME IN DEDICATED STATION AFTER PROCESSING TO REACH <70°C SUBSTRATE TEMPERATURE

SAFE OPERATION

AVOID HANDLING DAMAGE TO THE WAFERS

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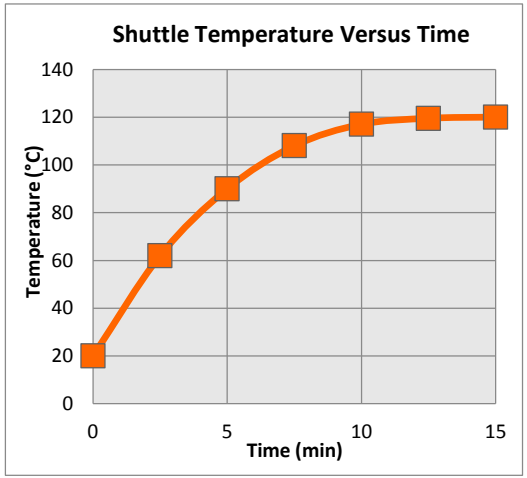
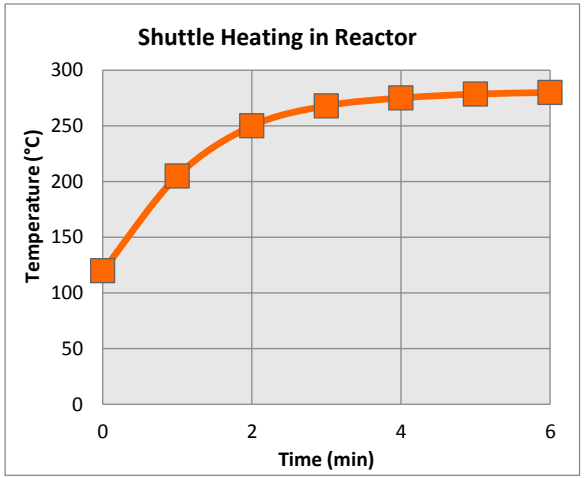
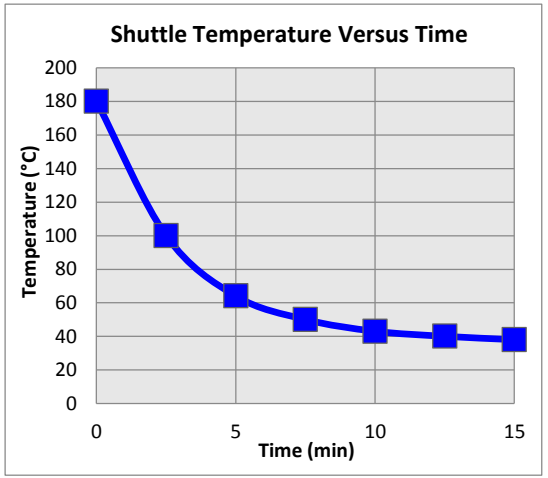
SYSTEM DESCRIPTION

Mechanically Assisted Loading







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PECVD REACTOR
CORIAL D500

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PECVD REACTOR

RAPID AND UNIFORM DEPOSITION

1. Precise and uniform temperature control of the substrate and reactor walls delivers excellent deposition repeatability and uniformity
2. Pressurized reactor ensures high-quality films free of pinholes
3. Optimized gas showerhead and symmetrical pumping deliver excellent deposition uniformity
4. High temperature, dual pumped configuration enables efficient plasma cleaning at operating temperature, with no corrosion of mechanical parts
5. Optimizing film stress control is simple to accomplish thanks to the reactor's symmetrical design
6. System can operate for years without the need for manual cleaning

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PECVD REACTOR

Flexibility

20 TO 150°C
TEMPERATURE RANGE

120 TO 325°C
TEMPERATURE RANGE

0.2 TO 2 T
PRESSURE RANGE

≤ 65°C
VACCUM VESSEL WALLS

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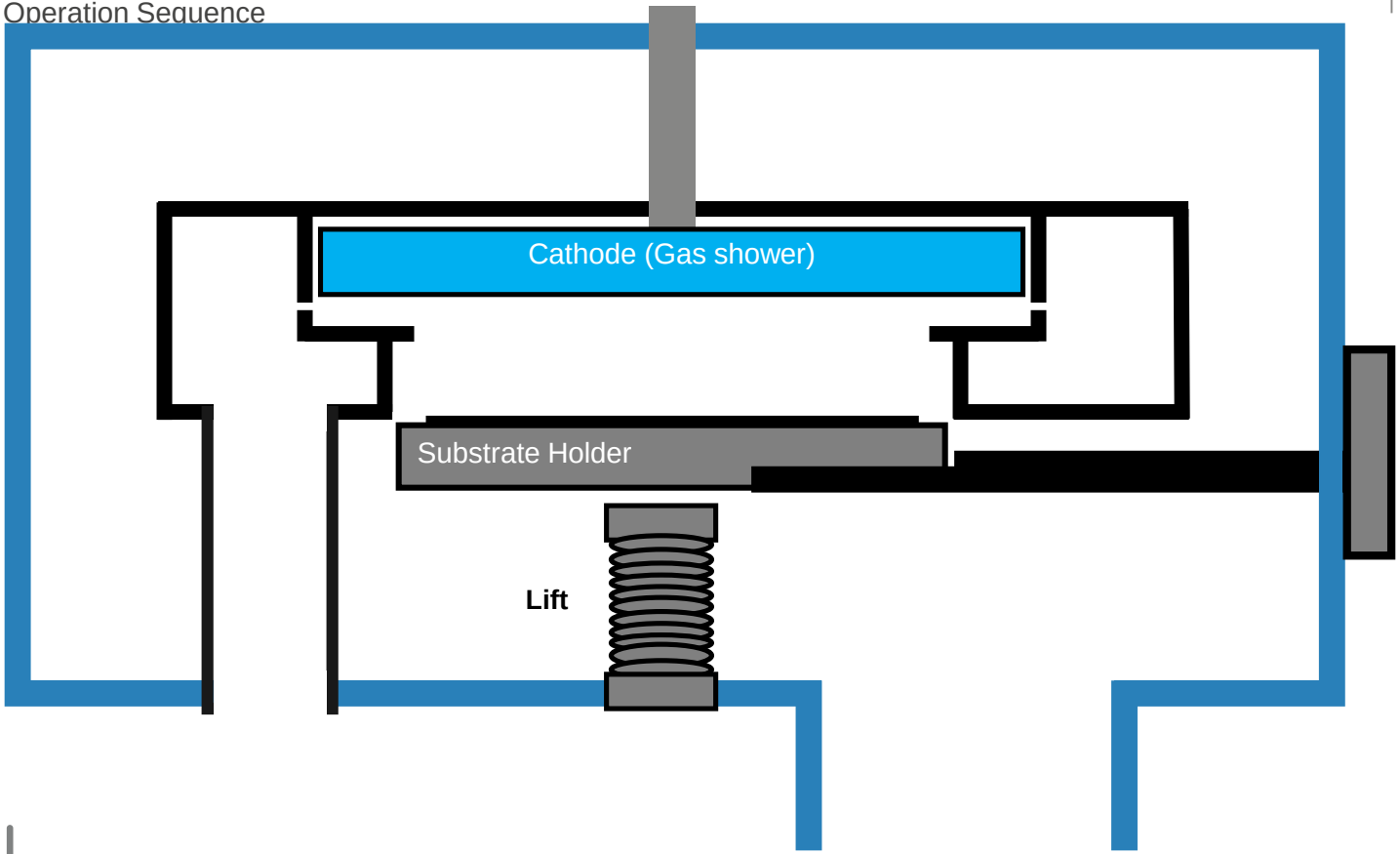
PECVD REACTOR

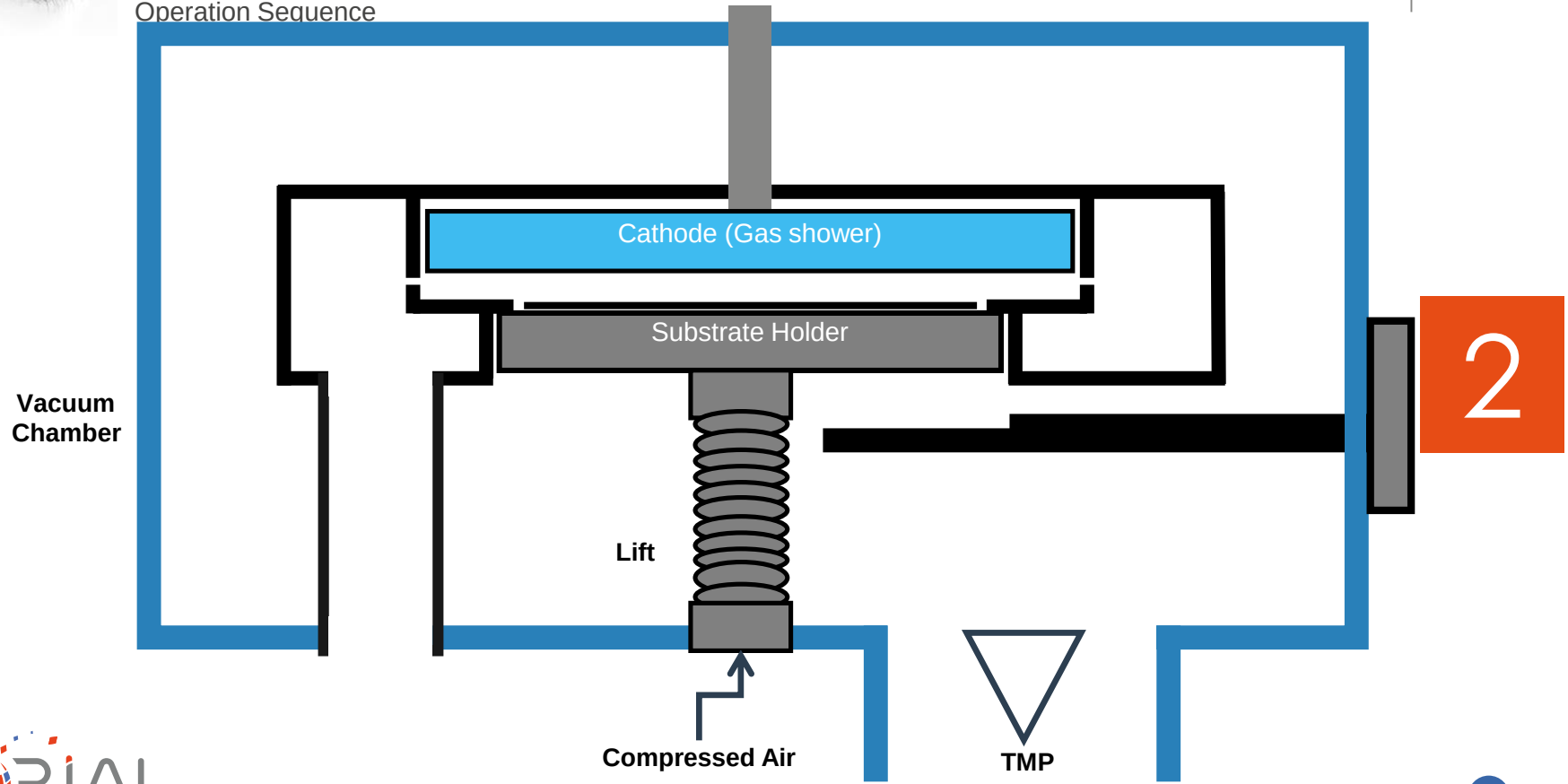
Operation Sequence

1



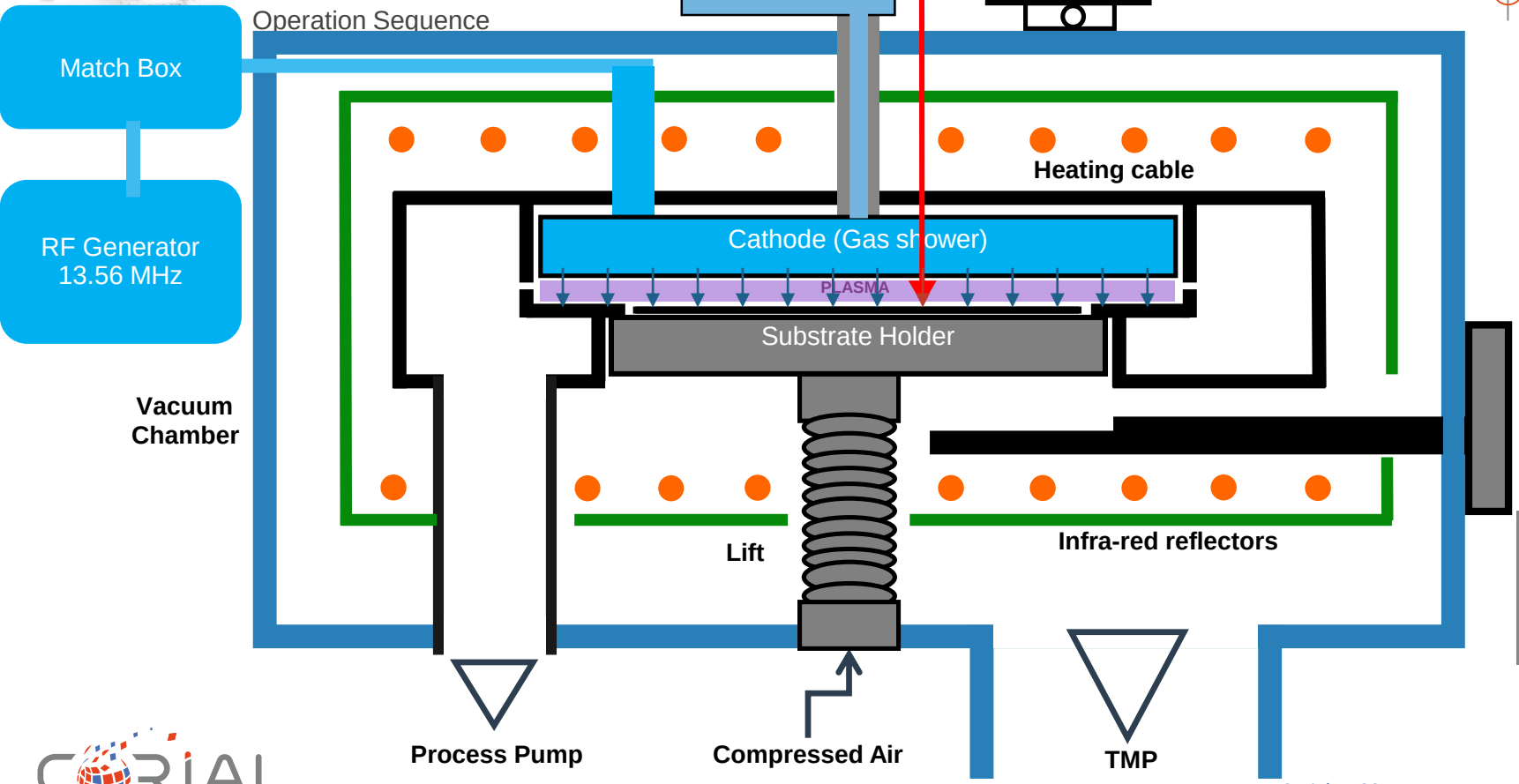
PECVD REACTOR

Operation Sequence



PECVD REACTOR

Operation Sequence



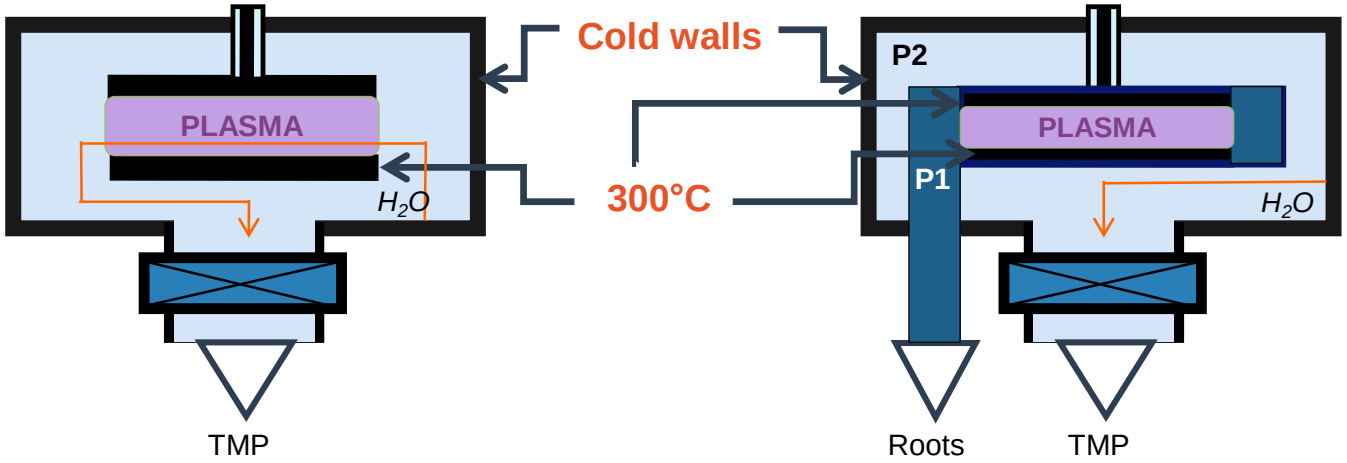
3

PECVD REACTOR

Standard vs. Pressurized Reactor

Standard PECVD

CORIAL Pressurized Reactor



Outgasing from the cold walls leads to **film contamination**

P1 >> P2 leads to **NO film contamination** (*H_2O is pumped away by TMP*)

PECVD REACTOR

Improved Film Quality

Very low concentration of O and C atoms in aSi-H films deposited in Pressurized Plasma Reactor

OXYGEN CONTAMINATION

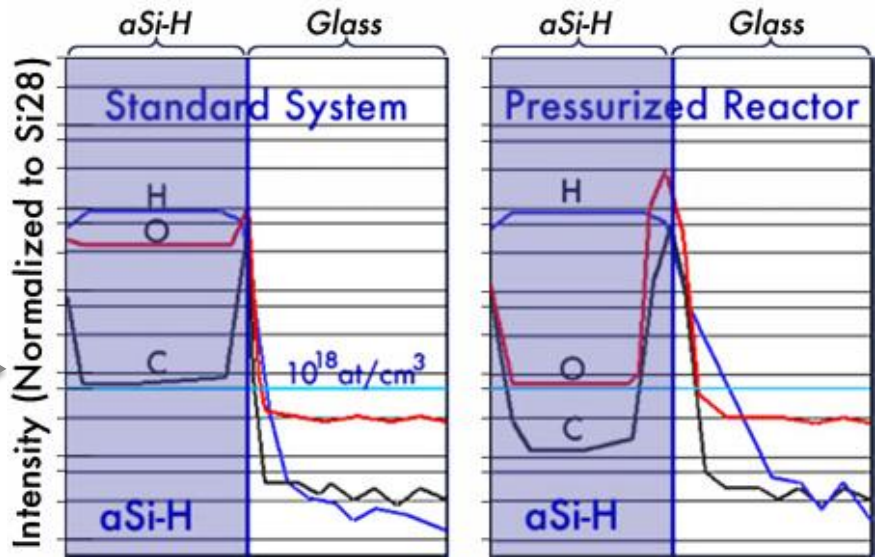
REDUCED BY 50

IN aSi-H FILM

CARBON CONTAMINATION

REDUCED BY 5

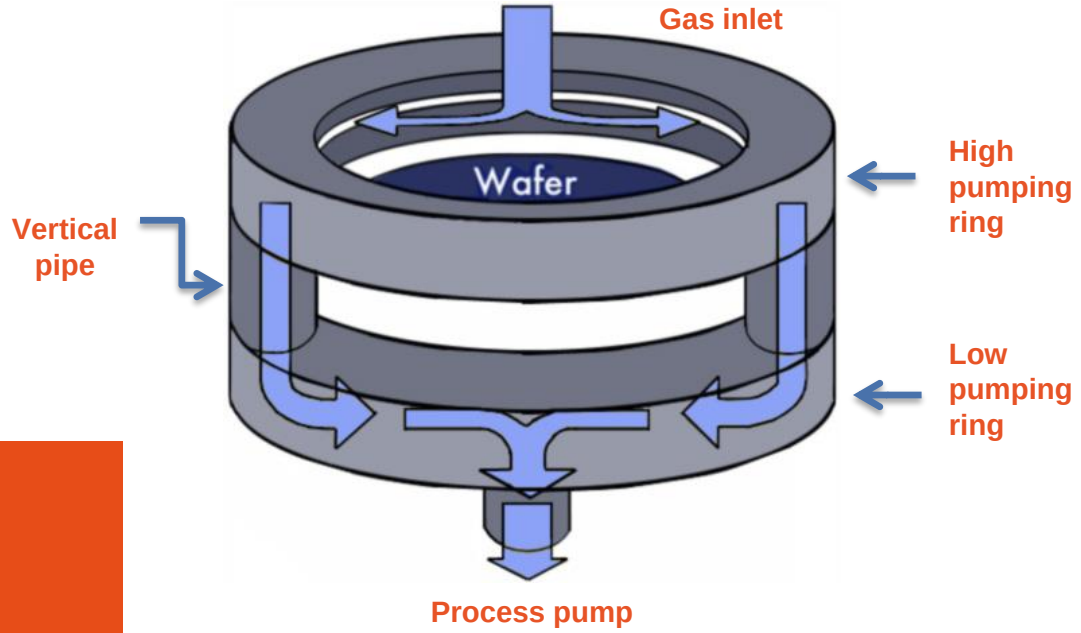
IN aSi-H FILM



PECVD REACTOR

Symmetrical Pumping

EXCELLENT DEPOSITION **UNIFORMITY**



SiO2 uniformity

< ±2 %

On 8'' wafer

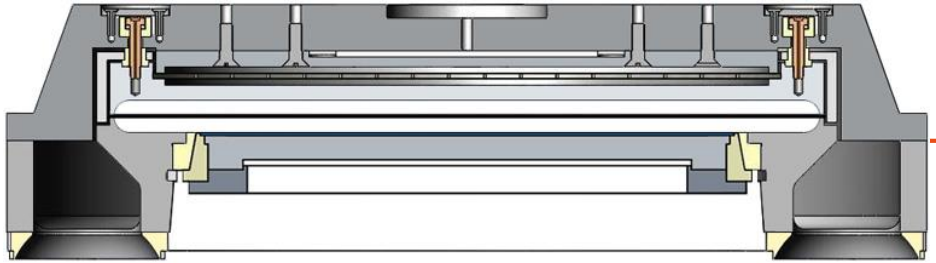
PECVD REACTOR

Symmetrical Design

Cathode area

=

Anode area

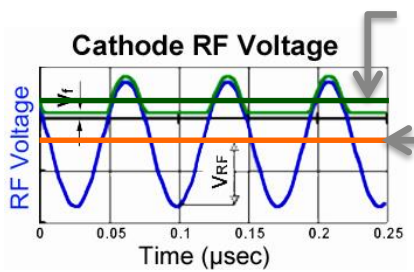


When an RF electric field is applied, the plasma potential adjusts itself until it is clamped on the positive portion of RF voltage (At the nearest floating potential (Vf)). The plasma potential is always higher than the highest potential of any surface in contact with the plasma

The mean plasma potential (Vp) and the self bias voltage (VDC) accelerate the positive ions and give them a high kinetic energy. In case of pressurized reactor the VDC is zero.

Ion energy is equal to

e·Vp + Initial energy of positive ions



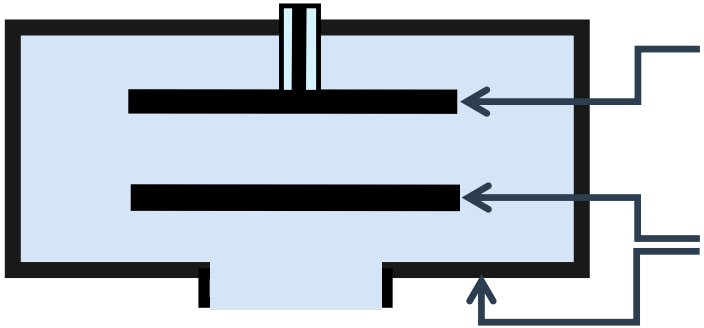
Mean plasma potential (V_p)

Self bias voltage ($-V_{DC}$). Zero bias in case of CORIAL reactor

PECVD REACTOR

Symmetrical Design

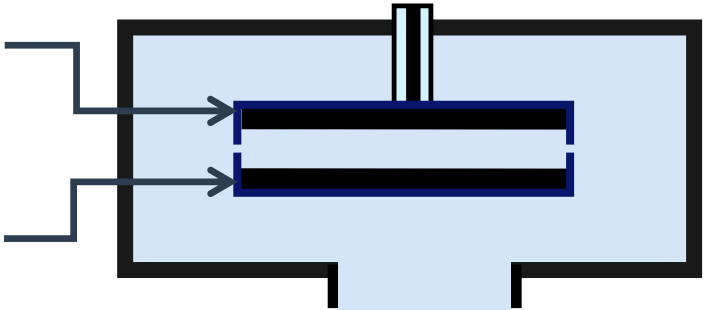
Standard PECVD



Anode area >> Cathode area

- Self bias voltage on cathode (V_{DC}) >> 100 V
- Mean plasma potential = (V_{RF} – V_{DC})/2 (≈ few Volts)
- Low energy ion bombardment on wafers sitting on the anode (ground)

CORIAL Pressurized Reactor



Anode area = Cathode area

- Self bias voltage on cathode (V_{DC}) = 0V
- Mean plasma potential = V_{RF} / 2 (Few hundred volts)
- High energy ion bombardment on wafers sitting on anode

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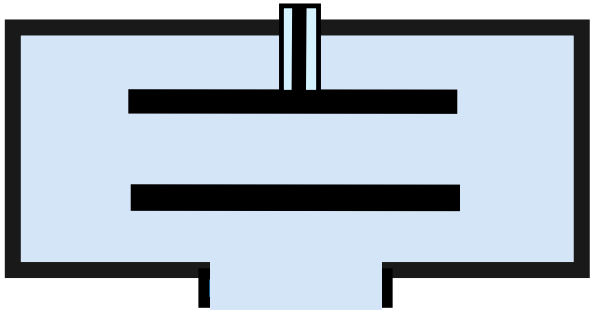
PECVD REACTOR

Stress Control

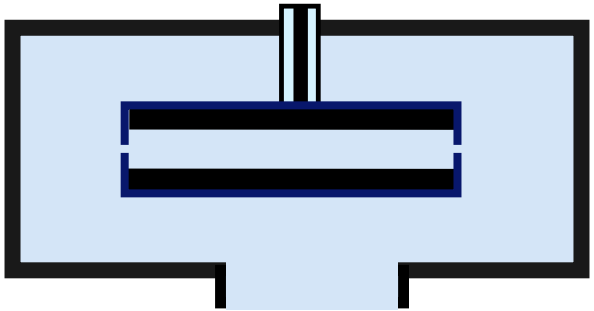
Standard PECVD



Double frequency system required for stress control

13.56 MHz for compressive stress
100 to 400 KHz for stress control

CORIAL Pressurized Reactor



Single frequency convenient for stress control

13.56 MHz for compressive & tensile stress

PRECISE AND SIMPLE STRESS CONTROL

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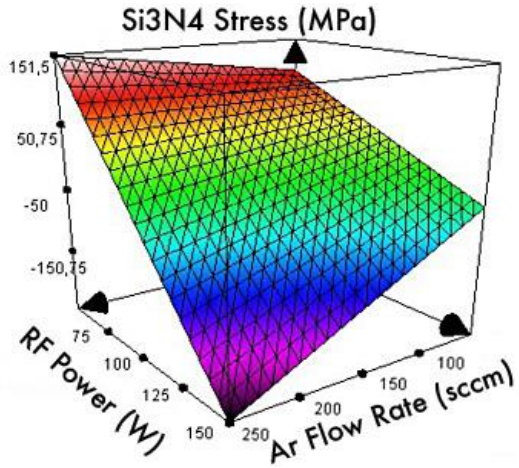
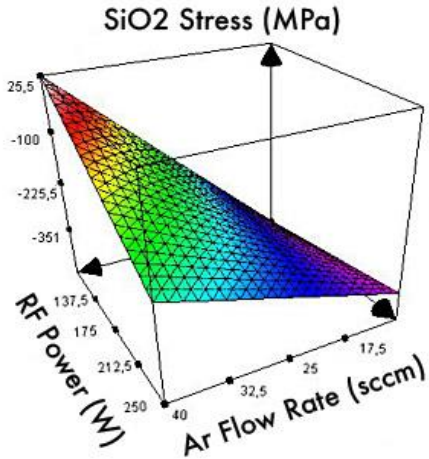
PECVD REACTOR

Stress Control

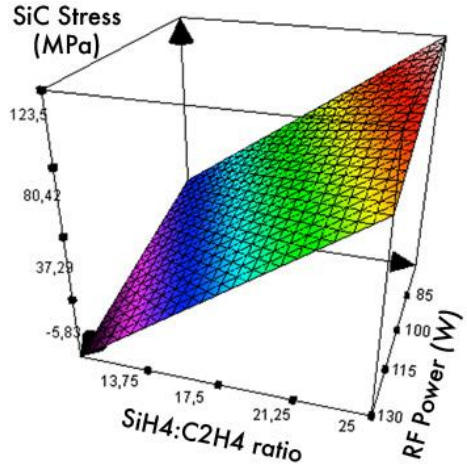
Stress controlled by RF power, Ar flow rate and gas mixture



Si_xN_y with tunable stress



SiO_2 with tunable stress



SiC with tunable stress

PERFORMANCES PECVD PROCESSES
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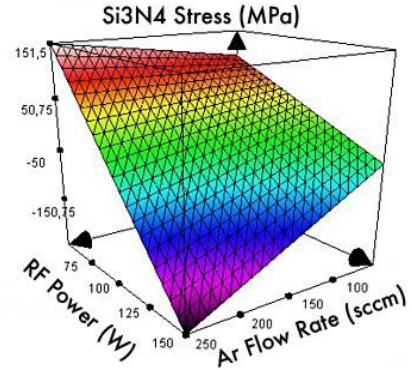
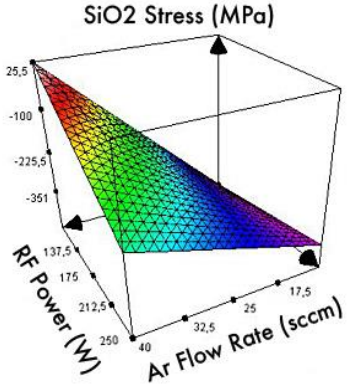
LAYER SPECIFICATIONS

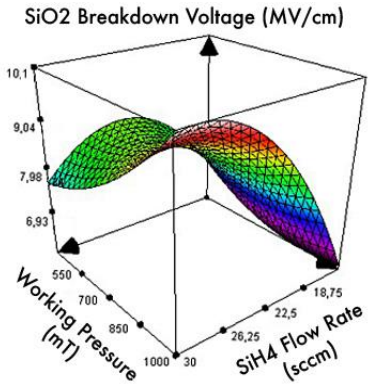
MEMS



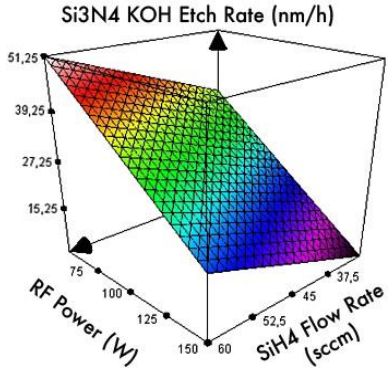
Si_xN_y with tunable stress



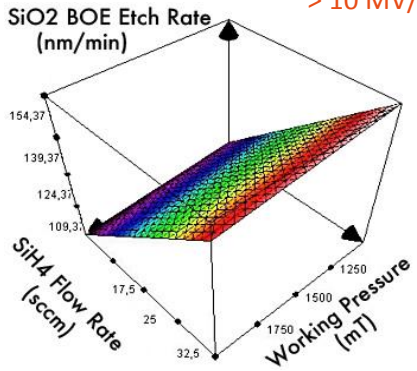
SiO_2 with tunable stress



SiO_2 with breakdown voltage > 10 MV/cm



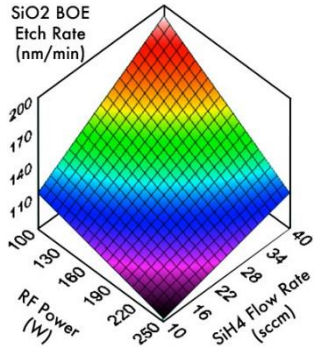
Si_3N_4 with low KOH etch rate



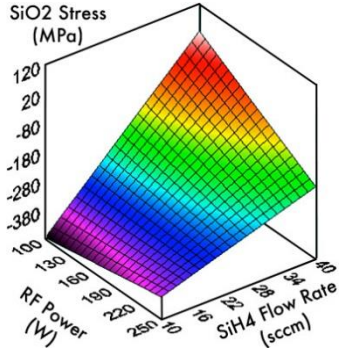
SiO_2 with low BOE etch rate

LAYER SPECIFICATIONS

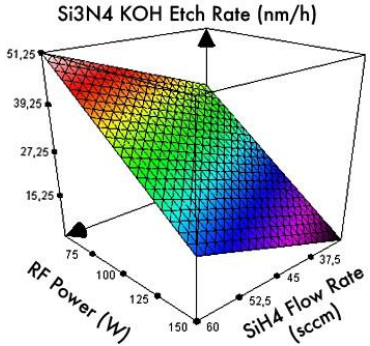
III-V Compounds, Optoelectronics



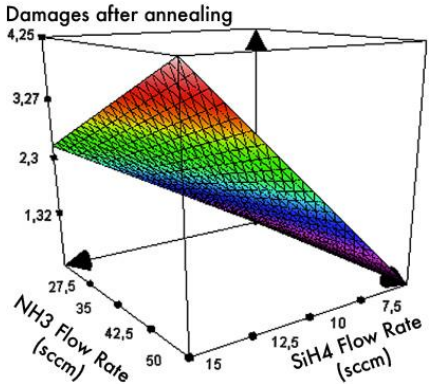
Low SiO_2 BOE etch rate



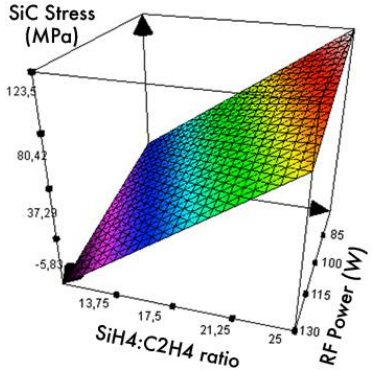
SiO_2 with tunable stress



Si_3N_4 with low KOH etch rate

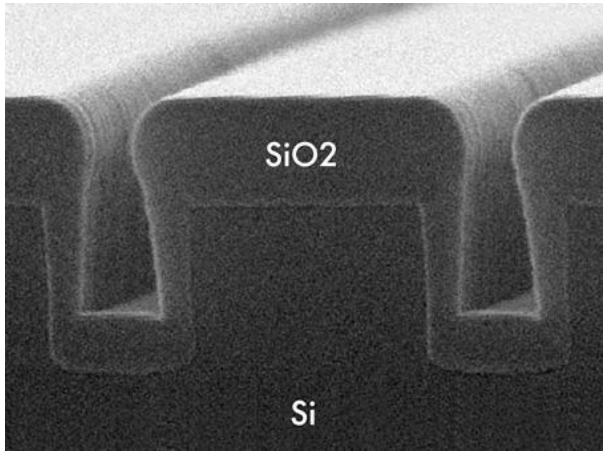


Low damaged after annealing

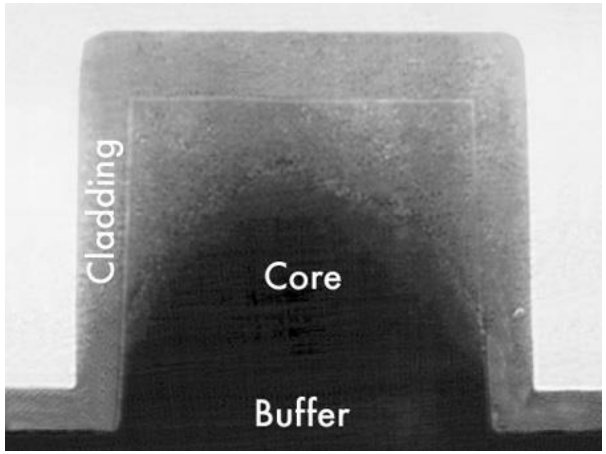


SiC tunable stress

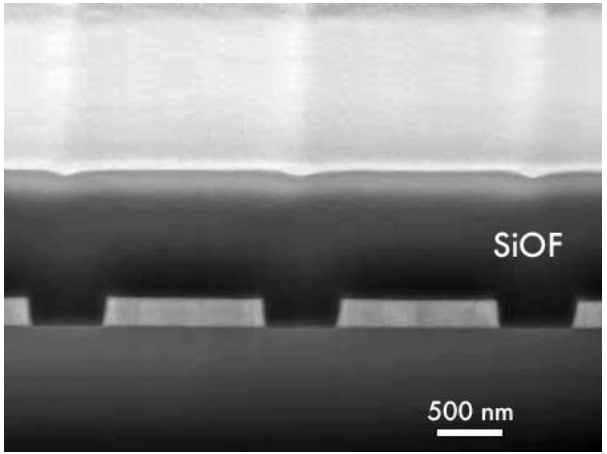
LAYER SPECIFICATIONS



Step coverage by
$SiH_4 + N_2O$ deposition



Step coverage by
HMDSO + O_2 deposition



Self-planarized
Deposition of SiOF

HIGH DEPOSITION RATES

Excellent Uniformities

Process	Deposition Rate (nm/min)	Refractive Index	Stress (MPa)	Uniformity on 8” Wafers
SiO_x	20 to 500 *	1.458 to 1.478	-300 to +50	< ± 3%
Si_xN_y	20 to 250 *	1.8 to 2.1	-300 to +150	< ± 3%
SiOF	> 50	1.41 ± 0.02	-100 to -0	< ± 3%
SiOCH	50 to 200	1.45 ± 0.02	-100 to -20	< ± 3%
Si_xC	20 to 150	2.6 to 2.9	-100 to +100	< ± 3%

* Configuration-dependent

Measurement performed with 5 mm edge exclusion

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HIGH THROUGHPUT

Large Capacity Batch System

Throughput calculations for 0,25 µm deposition of SiO2

Configuration	Deposition Time *(min)*	Loading Time *(min)*	Cleaning Time *(min)*	Throughput *(Wafer/month)*
104 x 2”	5	12	64	> 200,000
25 x 4”	5	12	64	> 50,000
9 x 6”	5	12	64	> 18,000
5 x 8”	5	12	64	> 10,000

Plasma cleaning when 5 µm of SiO2 are deposited

HIGH THROUGHPUT

Large Capacity Batch System

Throughput calculations for 2 µm deposition of SiO2

Configuration	Deposition Time *(min)*	Loading Time *(min)*	Cleaning Time *(min)*	Throughput *(Wafer/month)*
104 x 2”	18	12	74	> 78,000
25 x 4”	18	12	74	> 18,000
9 x 6”	18	12	74	> 6,700
5 x 8”	18	12	74	> 3,700

Plasma cleaning when 6 µm of SiO2 are deposited

CLEANING
CORIAL D500

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The 560x560 mm deposition system which never requires mechanical cleaning of reactor or vacuum vessel for many years of operation

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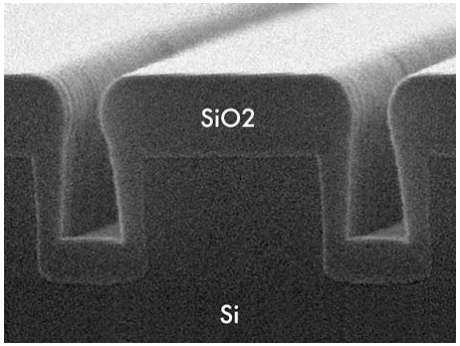
REACTOR PLASMA CLEANING

For Particle Free Processes



HIGH UPTIME

In situ
Reactor plasma cleaning

Pressurized
Reactor Design

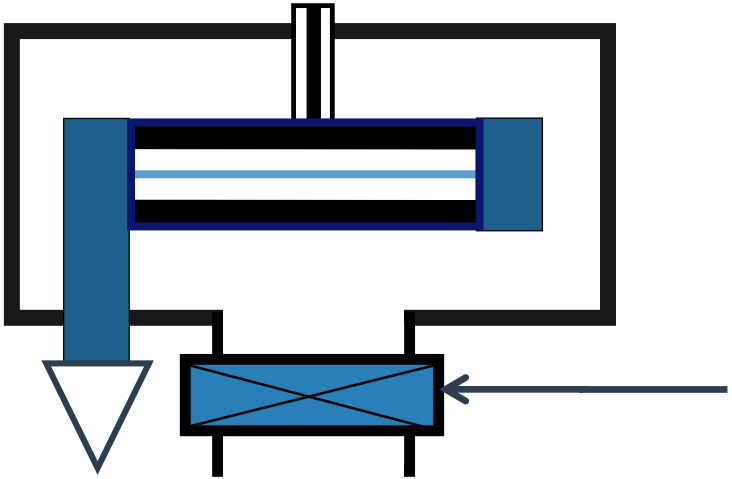
Automatic
EPD of reactor plasma cleaning process

NO MECHANICAL CLEANING

PECVD REACTOR

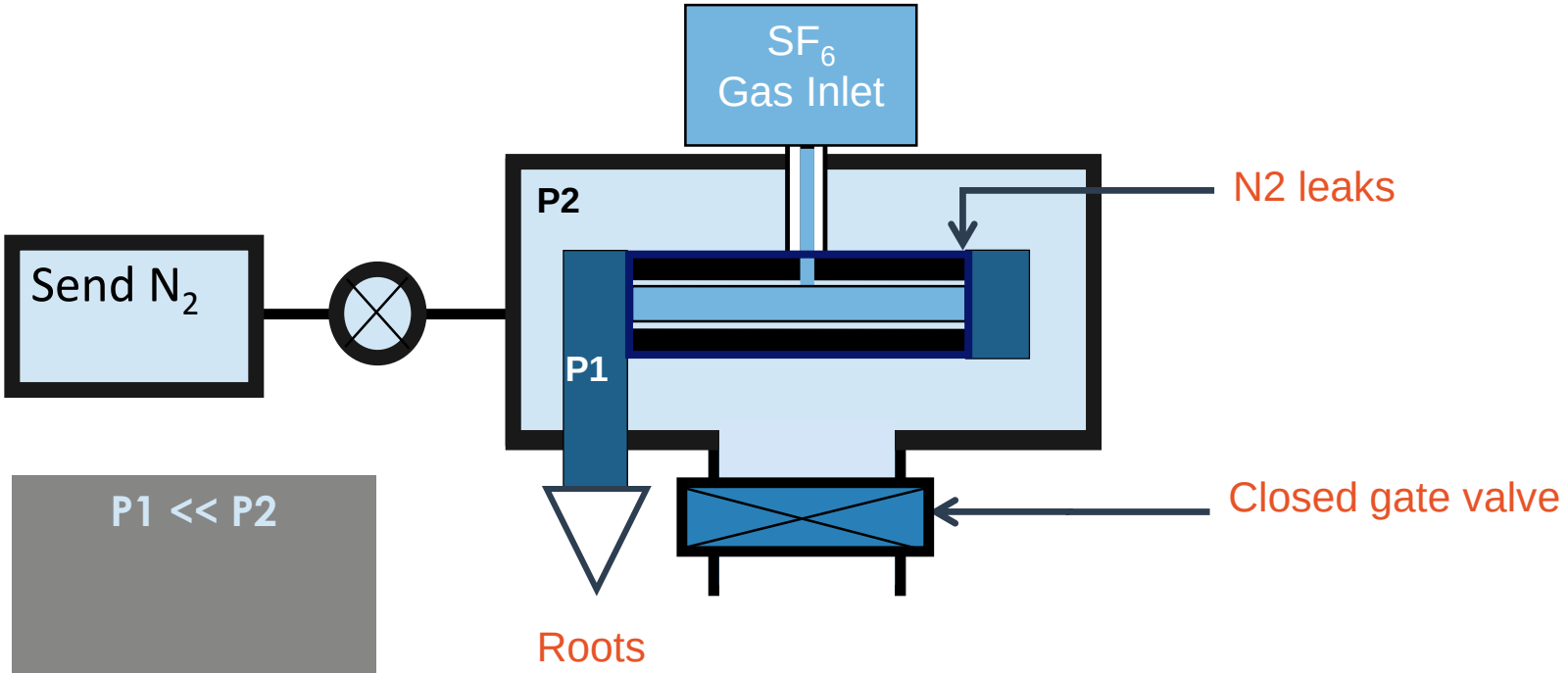
In Situ Cleaning Sequence

1



PECVD REACTOR

In Situ Cleaning Sequence

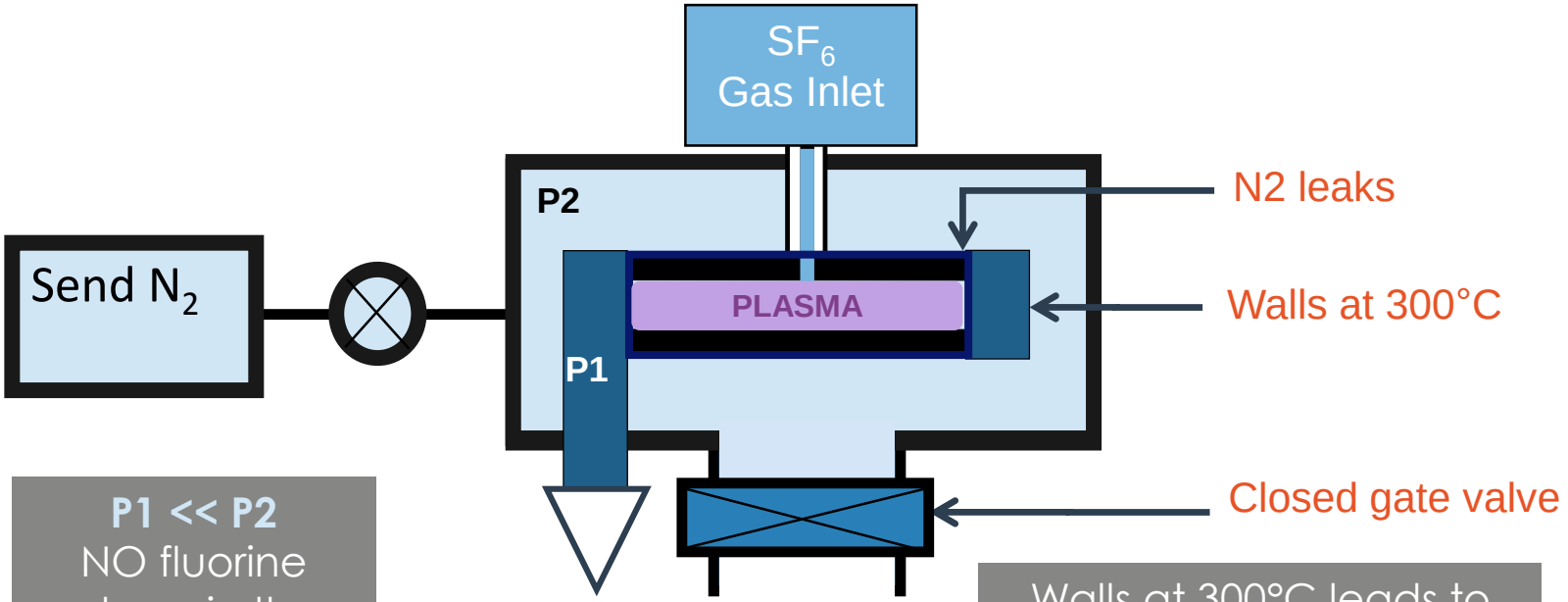


P1 << P2

2

PECVD REACTOR

In Situ Cleaning Sequence



P1 << P2
NO fluorine atoms in the vacuum vessel
NO corrosion

SiH_4 stopped while plasma still ON
NO pin holes

Walls at 300°C leads to efficient plasma cleaning and, thereby, **minimum particle contamination**

3

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USABILITY
CORIAL D500

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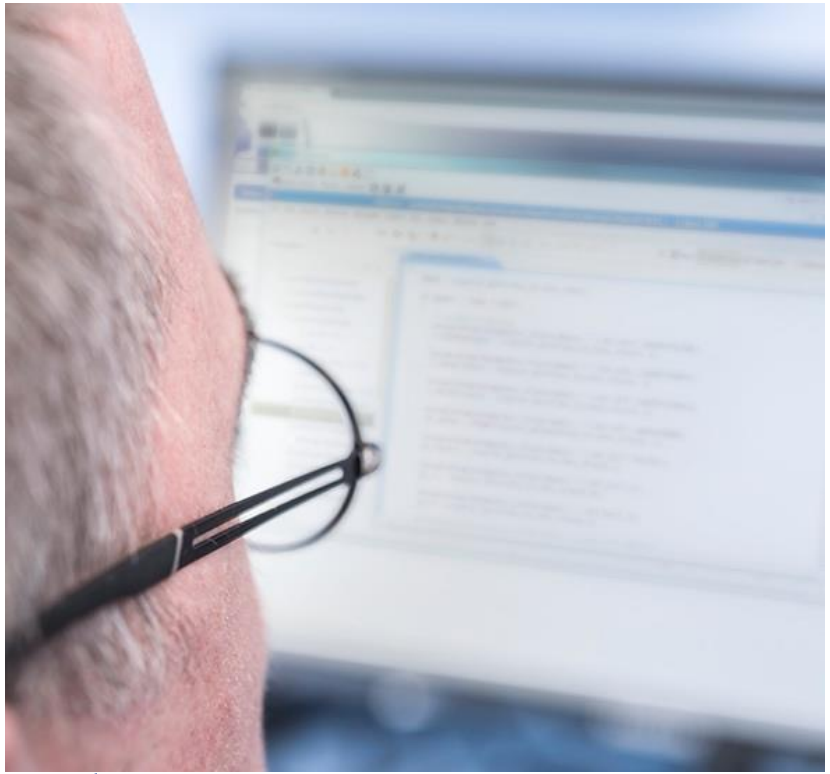
PROCESS CONTROL SOFTWARE

COSMA



COSMA

CORIAL **O**PERATING **S**YSTEM FOR **MA**CHINE

The simplest, most efficient software to develop processes, operate, and maintain CORIAL systems

DESKTOP APPLICATION

Process Editing I Process Adjustment I Process Operation I Process Tracability I System Maintenance

REMOTE CONTROL

CORIAL A Plasma-Therm Company

REPROCESSING SOFTWARE

COSMA RS

DISPLAY UP TO

4

PARAMETERS FROM A RUN

Simple and efficient software to analyze process runs and accelerate process development

REMOTE

ANALYSIS OF RUNS

DRAG AND DROP

CURVES TO CHECK PROCESS REPEATABILITY

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CORIAL D500

Large capacity batch system for 24/7 production environment

High-quality films for a wide range of materials, incl. SiO2, Si3N4, SiOCH, SiOF, SiC and aSi-H films

Film deposition from 120°C up to 325°C. Optional low-temperature chamber for film deposition at 20°C

Large batch loading capacity (104 X 2", 25 X 4", 9 X 6", 4 X 8" wafers, or large format substrates

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